National Semiconductor

March 1991

MM58248 High Voltage Display Driver

General Description

The MM58248 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P- and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58248 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 5 x 7 dot matrix display).

Applications

■ COPS™ or microprocessor-driven display
■ Instrumentation readouts
■ Industrial control indicator
■ Digital clock, thermostat, counter, voltmeter
■ Word processor text displays
■ Automotive dashboards

Features

■ Direct interface to high voltage display
■ Serial data input
■ No external resistors required
■ Wide display power supply operation
■ LSTTL compatible inputs
■ Software compatible with NS display driver family
■ Compatible with alphanumeric or dot matrix displays
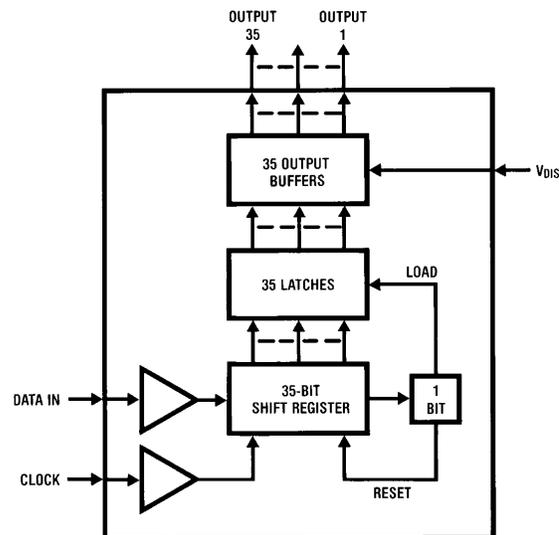■ No load signal required

Block Diagram

FIGURE 1

TL/F/5599-1

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	$V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD} - 62.5V$
$V_{DD} + |V_{DIS}|$	62.5V
Storage Temperature	$-65°C$ to $+150°C$

Power Dissipation at $+25°C$
  Molded DIP Package, Board Mount   2.28W*
  Molded DIP Package, Socket Mount   2.05W**

  *Molded DIP Package, Board Mount $\theta_{JA} = 46°C/W$,
   Derate 21.7 mW/°C above $+25°C$.

  **Molded DIP Package, Socket Mount, $\theta_{JA} = 51°C/W$,
   Derate 19.6 mW/°C above $+25°C$.

Junction Temperature	130°C
Lead Temperature	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD})			
$V_{SS} = 0V$	4.5	5.5	V
Display Voltage (V_{DIS})	-55	-25	V
Temperature Range	-40	$+85$	°C

DC Electrical Characteristics

$T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$, $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Currents	$V_{IN} = V_{SS}$ or V_{DD}, $V_{SS} = 0V$, V_{DIS} Disconnected			150	μA
I_{DIS}		$V_{DD} = 5.5V$, $V_{SS} = 0V$, $V_{DIS} = -55V$, All Outputs Low			10	mA
V_{IL}	Input Logic Levels DATA IN, CLOCK Logic '0'				0.8	V
V_{IH}	Input Logic Levels DATA IN, CLOCK Logic '1'	(Note 1)	2.4			V
I_{IN}	Input Currents, DATA IN, CLOCK	$V_{IN} = 0V$ or V_{DD}	-10		10	μA
C_{IN}	Input Capacitance, DATA IN, CLOCK				15	pF
R_{OFF}	Display Output Impedances Output Off *(Figure 3a)*	$V_{DD} = 5.5V$, $V_{SS} = 0V$ $V_{DIS} = -25V$ $V_{DIS} = -40V$ $V_{DIS} = -55V$	60 70 80		400 550 650	$k\Omega$ $k\Omega$ $k\Omega$
R_{ON}	Display Output Impedances Output on *(Figure 3b)*	$V_{DD} = 5.5V$, $V_{SS} = 0V$ $V_{DIS} = -25V$ $V_{DIS} = -40V$ $V_{DIS} = -55V$		3.0 2.6 2.3	4.0 3.7 3.4	$k\Omega$ $k\Omega$ $k\Omega$
V_{DOL}	Display Output Low Voltage	$V_{DD} = 5.5V$, $I_{OUT} =$ Open Circuit, $-55V \leq V_{DIS} \leq -25V$	V_{DIS}		$V_{DIS} + 4$	V

Note 1: 74LSTTL $V_{OH} = 2.7V$ @ $I_{OUT} = -400 \mu A$, TTL $V_{OH} = 2.4V$ @ $I_{OUT} = -400 \mu A$.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 2, 3)			1.0	MHz
t_H	Clock Input High Time		300			ns
t_L	Clock Input Low Time		300			ns
t_{DS}	Data Input Setup Time	$C_L = 50$ pF	100			ns
t_{DH}	Data Input Hold Time		100			ns

Note 2: AC input waveform specification for test purposes: t_r, $t_f \leq 20$ ns, f = 1 MHz, 50% $\pm 10\%$ duty cycle.

Note 3: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

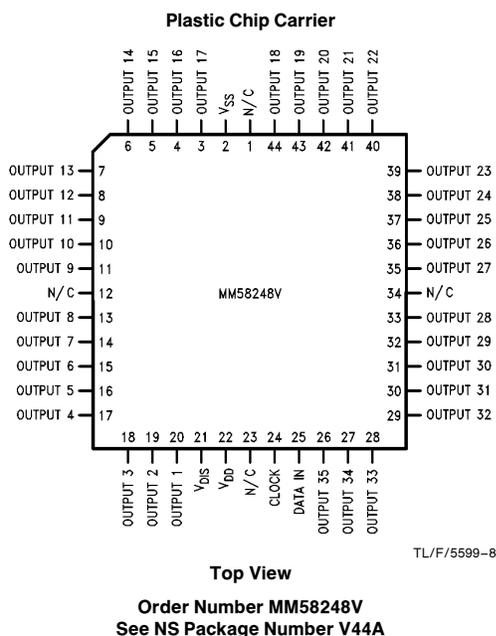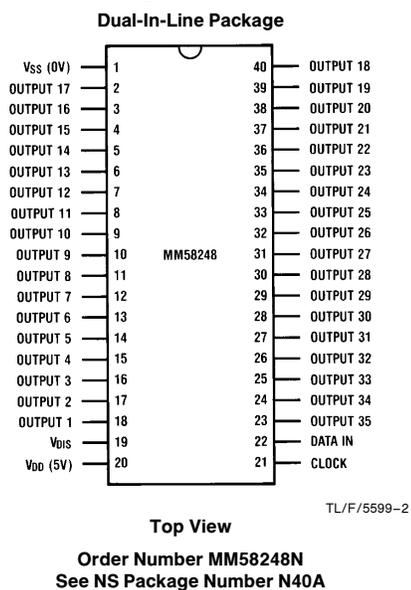**Dual-In-Line Package**

```
Vss (0V)      1        40   OUTPUT 18
OUTPUT 17     2        39   OUTPUT 19
OUTPUT 16     3        38   OUTPUT 20
OUTPUT 15     4        37   OUTPUT 21
OUTPUT 14     5        36   OUTPUT 22
OUTPUT 13     6        35   OUTPUT 23
OUTPUT 12     7        34   OUTPUT 24
OUTPUT 11     8        33   OUTPUT 25
OUTPUT 10     9        32   OUTPUT 26
OUTPUT 9     10  MM58248  31   OUTPUT 27
OUTPUT 8     11        30   OUTPUT 28
OUTPUT 7     12        29   OUTPUT 29
OUTPUT 6     13        28   OUTPUT 30
OUTPUT 5     14        27   OUTPUT 31
OUTPUT 4     15        26   OUTPUT 32
OUTPUT 3     16        25   OUTPUT 33
OUTPUT 2     17        24   OUTPUT 34
OUTPUT 1     18        23   OUTPUT 35
VDIS         19        22   DATA IN
VDD (5V)     20        21   CLOCK
```

TL/F/5599–2

Top View

Order Number MM58248N
See NS Package Number N40A

Plastic Chip Carrier

MM58248V

TL/F/5599–8

Top View

Order Number MM58248V
See NS Package Number V44A

FIGURE 2

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58248 uses two signals, DATA IN and CLOCK, with a format of a leading '1' followed by the 35 data bits, hence allowing data transfer without an additional signal. A block diagram of the MM58248 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58248 device, where output 1 (pin 18) is equivalent to bit 1, i.e., the first bit of data to be loaded into the shift register following the start bit. A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by the use of the MM58248, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58248.

In *Figure 5,* a start bit of logic '1' precedes the 35 bits of data, each bit being accepted on the rising edge of CLOCK, i.e., a '0'–'1' transition. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, thus loading the 35 bits of the shift register into the latches. At the low state of the clock, a RESET signal is generated, clearing all bits of the shift register for the next set of data. Hence, a complete set of 36 clock pulses is needed for the MM58248, or the shift register will not clear. To clear (reset) the display driver at 'power on' or any time, the following flushing routine may be used. Clock in 36 "zeroes", followed by a "one" (start bit), followed by 35 "zeroes". This procedure will completely blank the display. It is recommended to clear the driver at power on.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58248 is used to provide the anode drive for a 32-digit 5 x 7 dot matrix vacuum fluorescent (VF) display. The grid drive in this example is provided by another member of the high voltage display driver family, namely the MM58241, which has the additional features of a BLANKING CONTROL pin, a DATA OUT pin, and an ENABLE (external load signal) pin.
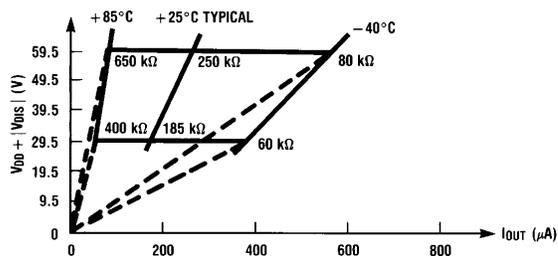
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Functional Description (Continued)
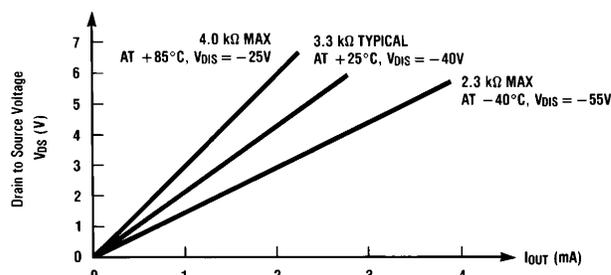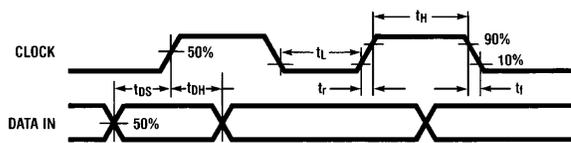

FIGURE 3a. Output Impedance Off

TL/F/5599–3

FIGURE 3b. Output Impedance On

TL/F/5599–4

Timing Diagrams

For the purposes of AC measurement, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$.

TL/F/5599–5
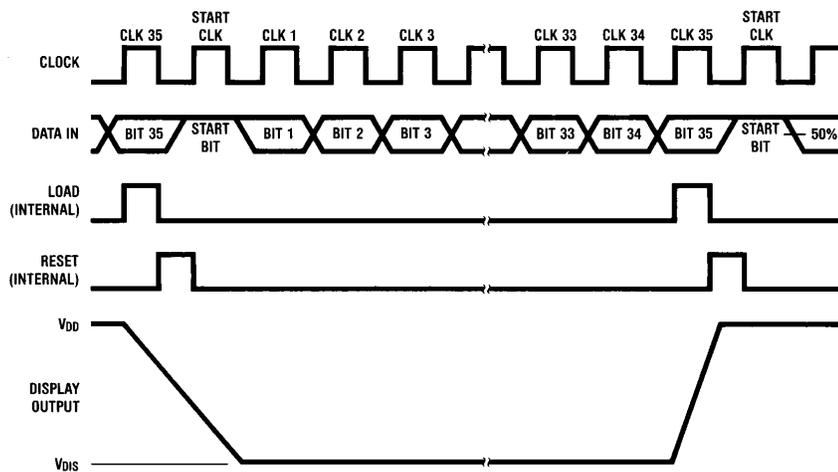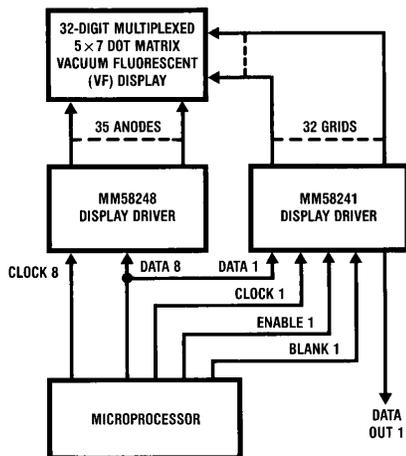
FIGURE 4. Clock and Data Timings

TL/F/5599–6

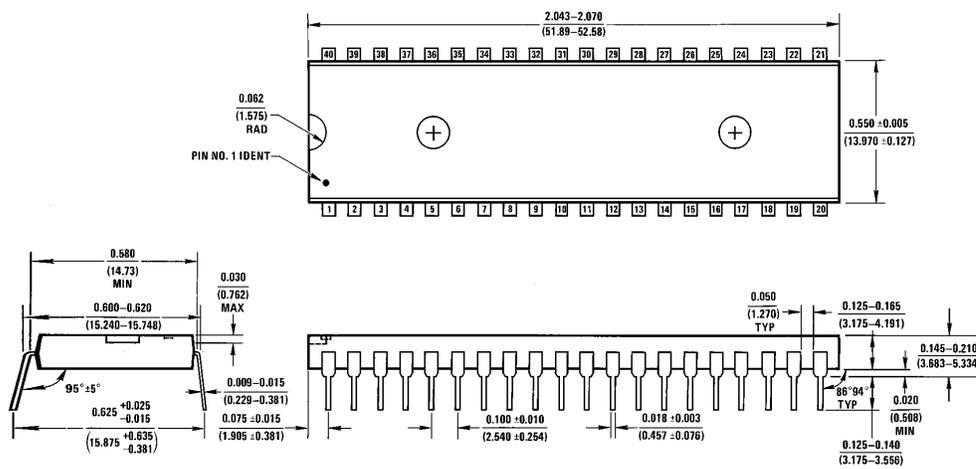FIGURE 5. MM58248 Timings (Data Format)

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Typical Applications

32-DIGIT MULTIPLEXED
5 × 7 DOT MATRIX
VACUUM FLUORESCENT
(VF) DISPLAY

35 ANODES   32 GRIDS

MM58248
DISPLAY DRIVER

MM58241
DISPLAY DRIVER

CLOCK 8   DATA 8   DATA 1
CLOCK 1
ENABLE 1
BLANK 1

MICROPROCESSOR

DATA
OUT 1

TL/F/5599–7

FIGURE 6. Microprocessor-Controlled Word Processor

Physical Dimensions inches (millimeters)

2.043–2.070
(51.89–52.58)

0.062
(1.575)
RAD

0.550 ±0.005
(13.970 ±0.127)

PIN NO. 1 IDENT

0.580
(14.73)
MIN

0.030
(0.762)
MAX

0.600–0.620
(15.240–15.748)

0.050
(1.270)
TYP

0.125–0.165
(3.175–4.191)

0.145–0.210
(3.683–5.334)

95° ±5°

0.009–0.015
(0.229–0.381)

0.625 +0.025
−0.015

0.075 ±0.015
(1.905 ±0.381)

0.100 ±0.010
(2.540 ±0.254)

0.018 ±0.003
(0.457 ±0.076)

86°94°
TYP

0.020
(0.508)
MIN

(15.875 +0.635
−0.381)

0.125–0.140
(3.175–3.556)

N40A (REV E)

Molded Dual-In-Line Package (N)
Order Number MM58248N
NS Package Number N40A

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MM58248 High Voltage Display Driver

Physical Dimensions inches (millimeters) (Continued)

0.650 +0.006/-0.000
[16.51 +0.15/0]

PIN 1 IDENT

6   1 44   40

7   39

17   29

18   28

0.050 [1.27] TYP

0.500 [12.70] TYP

0.017±0.004 [0.43±0.10] TYP

45°X 0.045 [1.14]

0.029±0.003 [0.74±0.08] TYP

0.610±0.020 [15.49±0.51] TYP

SEATING PLANE

0.020 [0.51] MIN TYP

0.105±0.015 [2.67±0.38] TYP

0.165-0.180 [4.19-4.57] TYP

△ 0.004[0.10]

45°X 0.045 [1.14]

0.690-0.005 [17.53-0.13] TYP

V44A (REV K)
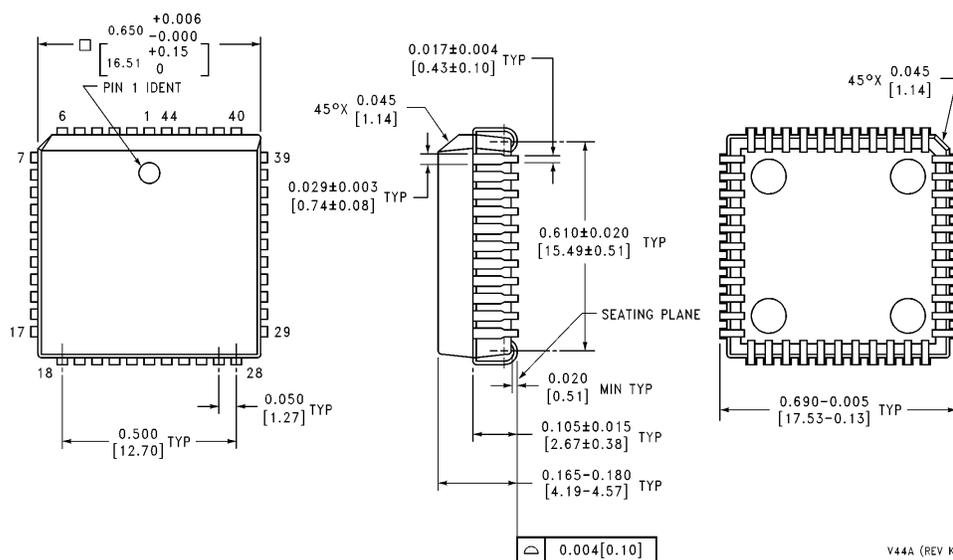
Plastic Chip Carrier (V)
Order Number MM58248V
NS Package Number V44A