MK1491-14
OPTi ACPI Firestar Clock Source

Description

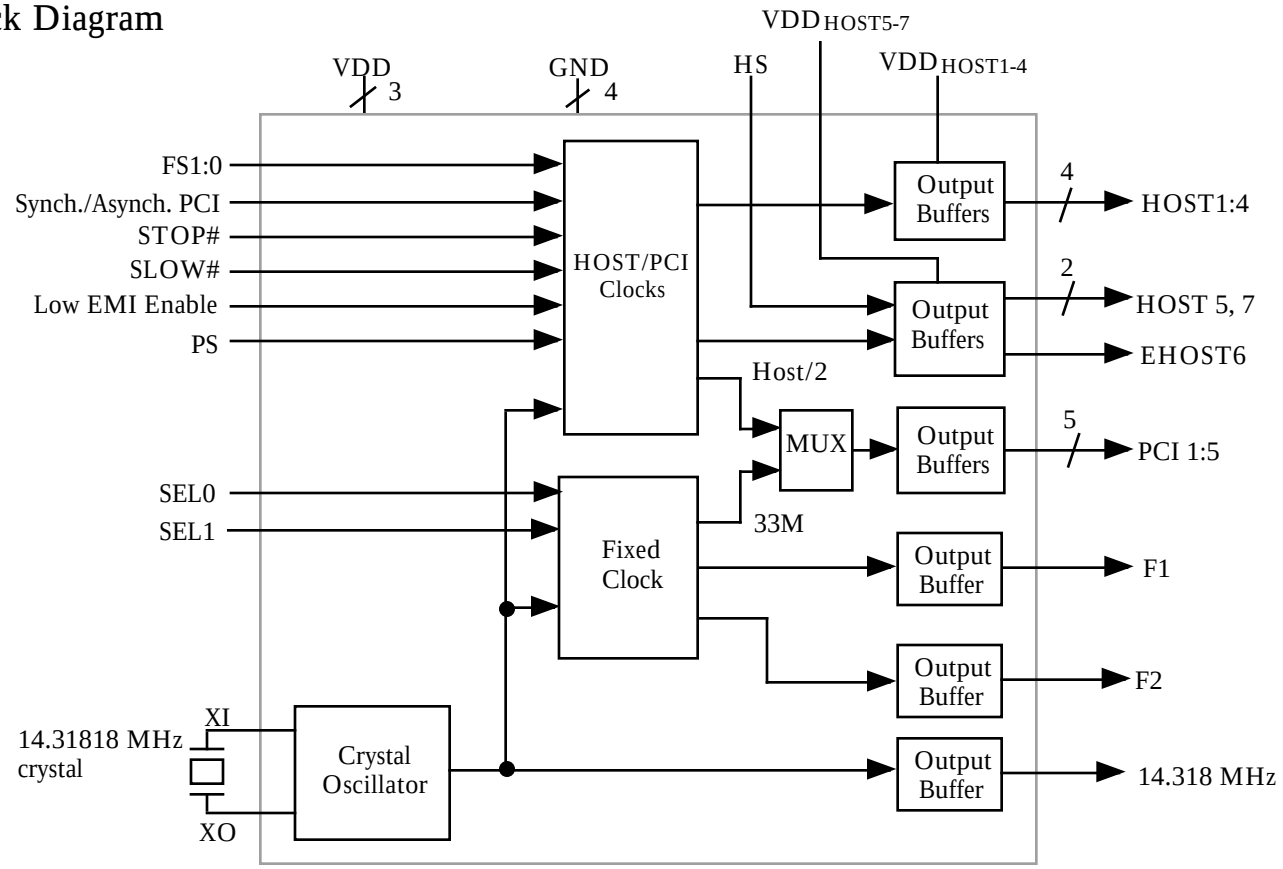
The MK1491-14 is a low cost, low jitter, high performance clock synthesizer for OPTi's Firestar and Firestar+ chipsets for Pentium™ Processor-based mobile computer applications. Using analog Phase-Locked Loop (PLL) techniques, the device uses a 14.318 MHz crystal input to produce multiple output clocks up to 75 MHz. It provides selectable Host and PCI local bus clocks as well as selectable clocks for Super I/O or Universal Serial Bus (USB). The device has up to seven Host output clocks.

The chip has three different power down modes that reduce power on various clocks.

Features

- Packaged in 28 pin, 150 mil wide SSOP
- Provides all critical timing for OPTi ACPI Firestar and Firestar+
- Early Host clock of 3.5ns
- Separate VDD and skew adjust for Host 5,6, and 7 supports field upgrade to Firestar+ and new 2.5V processors
- 48MHz USB, 24MHz SIO, and Audio clock support
- Single pin CPU(Host) slowdown to 33.3MHz
- Multiple power down modes
- Low EMI Enable pin reduces EMI radiation (patent pending)

Block Diagram



Integrated Circuit Systems, Inc. • 525 Race Street • San Jose •CA •95126 • (408)295-9800tel • www.icst.com

MK1491-14
OPTi ACPI Firestar Clock Source

Pin Assignment

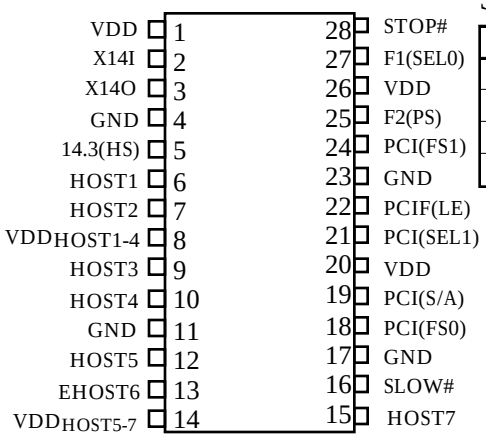


Table #1. F1, F2 Frequency Select (MHz)

SEL1	SEL0	F1	F2
0	0	14.318	14.318
0	1	14.318	48.000
1	0	24.000	14.318
1	1	16.934	24.576

Table #2. Host/PCI Frequency Select (MHz)

FS1	FS0	HOST	PCI (S/A=0)	PCI (S/A=1)
0	0	66.66	33.33*	HOST/2
0	1	60	33.33*	HOST/2
1	0	75	33.33*	HOST/2
1	1	50	33.33*	HOST/2

*2 MHz Accuracy

Table #3. Host 5-7 Skew Control

$VDD_{HOST5-7}$	HS
2.5V	0
3.3V	1

Low EMI for HOST & PCI

LE	Low EMI
0	OFF
1	ON

Table #4. Power Down Control (IDD measured at 3.3V)

STOP#	SLOW#	STATE	HOST	PCI	DESCRIPTION	IDD typ.
1	1	ON	ON	ON	All Clocks On.	50 mA
1	0	SLOW	33 MHz	ON	Host Clock smooth frequency transition to and from 33.33 MHz.	32 mA
0	0	CLK OFF	LOW	*	Asynchronously clamp HOST5, 7 to GND. HOST1-4,6, PCIF, F1, F2, 14.3M, continue to run.	44 mA
0	1	PLL/OSC OFF	LOW	LOW	All outputs asynchronously clamped low. PLLs and 14.3 MHz oscillators are off.	1 µA

*PCI Function Select (PS) set at Power Up. PS=0, PCI=LOW; PS=1, PCI=ON when clock is switched to "CLK OFF" mode.

Pin Descriptions

Pin #	Name	Type	Description
1, 20, 26	VDD	P	Connect to +3.3V. Must be same voltage on all pins.
2	X14I	I	Crystal connection. Connect to a 14.31818 MHz crystal or input clock.
3	X14O	O	Crystal connection. Connect to a 14.31818 MHz crystal, or leave unconnected for clock.
4, 11, 17, 23	GND	P	Connect to Ground.
5	14.3(HS)	I/O	14.318 MHz output. Amplitude matches VDD. Skew input control for Host 5-7.
6, 7, 9, 10	HOST 1, 2, 3, 4	O	Host Output clocks 1, 2, 3 and 4. Amplitude matches $VDD_{HOST1-4}$
8	$VDD_{HOST1-4}$	P	Connect to VDD supply.
12	HOST 5	O	Host Output clock 5. Amplitude matches $VDD_{HOST5-7}$.
13	EHOST 6	O	Early Host Output clock 6. Amplitude matches $VDD_{HOST5-7}$.
14	$VDD_{HOST5-7}$	P	Connect to 2.5 V or 3.3 V. Host 5-7 skew adjusted with HS input. See Table #3 above.
15	HOST7	O	Host Output clock 7. Amplitude matches $VDD_{HOST5-7}$.
16	SLOW#	I	Controls clock frequency and power downs, as defined in Table #4 above.
18	PCI(FS0)	I/O	PCI Output clock, CPU Frequency Select input, as per Table #2 above. Amplitude = VDD.
19	PCI(S/A)	I/O	PCI Output clock, and Asynchronous PCI Select input, as per Table #2 above.
21	PCI(SEL1)	I/O	PCI Output clock, and Frequency Select 1 input, as per Table #1 above.
22	PCIF(LE)	I/O	PCI Output clock that stays enabled when other PCI clocks are low. Low EMI enable input.
24	PCI(FS1)	I/O	PCI output and Frequency Select input. See Table #2 above.
25	F2(PS)	I/O	Fixed frequency output and PCI Function Select for "CLK OFF" mode.
27	F1(SEL0)	I/O	Fixed frequency output and frequency SEL0 input per Table #1 above.
28	STOP#	I	Controls clock frequency and power downs, as defined in Table #4 above.

Key: I = Input, O = Output, P = Power supply connection, I/O = Input on power up, becomes an Output after 10ms.
Internal pull-ups are on pins 5, 16, 18, 19, 21, 22, 24, 25, 27, 28.

Integrated Circuit Systems, Inc. • 525 Race Street • San Jose •CA •95126 • (408)295-9800tel • www.icst.com

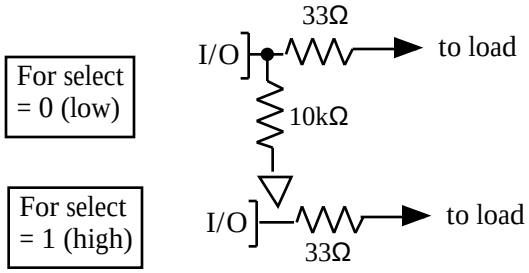
Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3V or 2.5V unless noted)					
Operating Voltage	VDD		3.3	3.6	V
Operating Voltage	$VDD_{HOST1-4, HOST5-7}$		2.5/3.3	VDD	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	IOH=-8mA	2.4			V
Output Low Voltage, VOL	IOL=8mA			0.4	V
Output High Voltage, VOH	IOH=-8mA	VDD-0.4			V
Operating Supply Current, IDD	No Load, 66.6MHz		48		mA
Power Down mode Supply Current			3		µA
Short Circuit Current	Each output		±50		mA
Short Circuit Current	VDD_{HOST} = 2.5V		±25		mA
Input Capacitance			7		pF
AC CHARACTERISTICS (VDD = 3.3V or 2.5V unless noted)					
Input Frequency			14.31818		MHz
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
HOST Output Clock Rise Time	VDD_{HOST} = 2.5V			2.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
HOST Output Clock Fall Time	VDD_{HOST} = 2.5V			2.5	ns
Output Clock Duty Cycle, all MHz clocks	At 1.5V	45	49 to 51	55	%
HOST1-4 Output to Output Skew	Rising edges at 1.5V			250	ps
Skew of HOST 5,7 with respect to HOST 1-4	With proper HSKEW setting			750	ps
PCI Output to Output Skew	Rising edges at 1.5V			500	ps
Lead of EHOST6 outputs with respect to PCI	Rising edges at 1.5V		1.9		ns
Lead of EHOST6 with respect to HOST1-5, 7	Rising edges at 1.5V		3.9		ns
Cycle to Cycle Jitter, CPU Clocks				1000	ps
Absolute Clock Period Jitter, Other MHz Clocks, except 14.318 MHz		-500		500	ps
EMI reduction, peaks of 5th - 19th odd harmonics	66.6 MHz clocks, LE=1		6	11	dB
Power up time, STOP# going high to all clocks stable			8	20	ms
Power on time, applied VDD to all clocks stable			12	25	ms

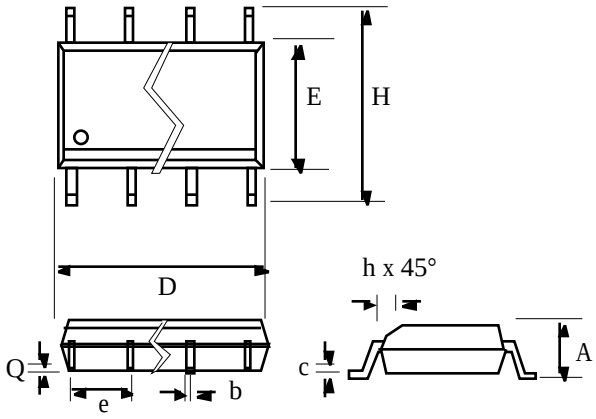
Note 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.

I/O Structure

The MK1491 provides more functionality in a 28 pin package by using a unique I/O technique. The device checks the status of all I/O pins during power-up. This status (pulled high or low) then determines the frequency selections and power down modes (see the tables on page 2). Within 10ms after power up, the inputs change to outputs and the clocks start up. In the diagrams to the right, the 33Ω resistors are the normal output termination resistors. The 10kΩ resistor pulls low to generate a logic zero. Internal pull-up resistors are present on all inputs to generate a logic one when an external pull-down resistor is not connected.



Package Outline and Package Dimensions



28 pin SSOP

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.061	0.068	1.55	1.73
b	0.008	0.012	0.203	0.305
c	0.007	0.010	0.190	0.254
D	0.385	0.400	9.780	10.160
E	0.150	0.160	3.810	4.064
H	0.230	0.245	5.840	6.223
e	.025 BSC		0.635 BSC	
h		0.016		0.410
Q	0.004	0.01	0.127	0.254

Ordering Information

Part/Order Number	Marking	Low EMI Feature	Package	Temperature
MK1491E-14R	MK1491E-14R	Yes	28 pin SSOP	0-70°C
MK1491E-14RTR	MK1491E-14R	Yes	Add Tape & Reel	-

External Components

The MK1491 requires some inexpensive external components for proper operation. Decoupling capacitors of 0.1µF should be connected on each VDD pin to ground, as close to the MK1491 as possible. A series termination resistor of 33Ω may be used for each clock output. See the discussion on page 4 for other external resistors required for proper I/O operation. The 14.318 MHz oscillator has internal caps that provide the proper load for a parallel resonant crystal with C_L=18pF. For tuning with other values of C_L, the formula 2•(C_L-18) gives the value of each capacitor that should be connected between X1 and ground and X2 and ground.