



STSJ50NH3LL

N-channel 30V - 0.008Ω - 12A - PowerSO-8™
Ultra low gate charge STripFET™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STSJ50NH3LL	30V	< 0.0105Ω	12A ⁽¹⁾

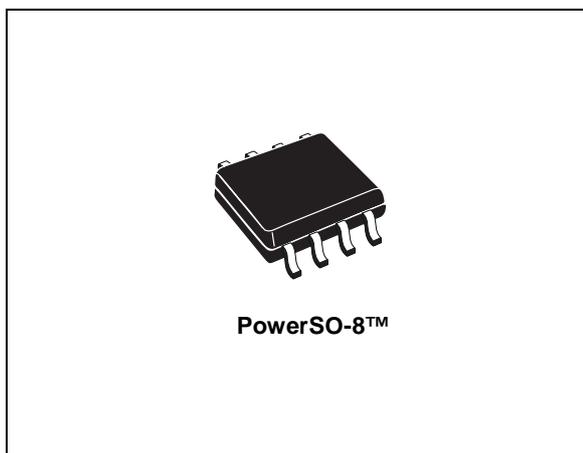
- Optimal R_{DS(on)} x Q_g trade-off @ 4.5V
- Reduced switching losses
- Reduced conduction losses
- Improved junction-case thermal resistance

Description

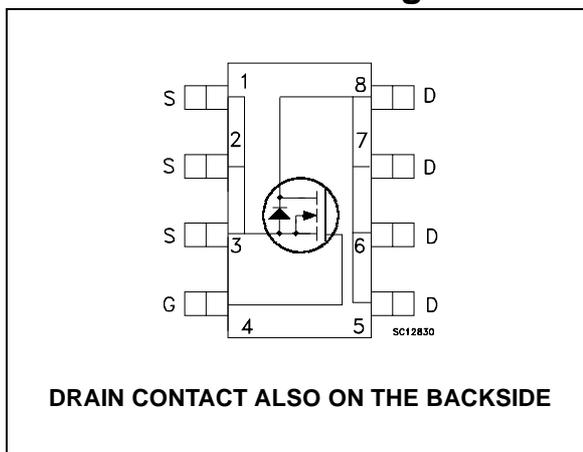
This series utilizes the latest advanced design rules of ST's proprietary STripFET™ technology, and a proprietary process for integrating a monolithic Scottky diode. The new Power MOSFET is optimized for the most demanding synchronous switch function in DC-DC converter for Computer and Telecom.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STSJ50NH3LL	50H3LL-	PowerSO-8	Tape & reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuit	9
4	Package mechanical data	10
5	Revision history	12

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
$V_{GS}^{(1)}$	Gate-source voltage	± 16	V
$V_{GS}^{(2)}$	Gate-source voltage	± 18	V
$I_D^{(4)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	50	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	12	A
$I_D^{(4)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	31.3	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	7.5	A
$I_{DM}^{(5)}$	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$ ⁽³⁾	3	W
	Total dissipation at $T_C = 25^\circ\text{C}$ ⁽⁴⁾	50	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Continuous mode
2. Guaranteed for test time $\leq 15\text{ms}$
3. This value is rated accordingly to $R_{thj-pcb}$
4. This value is rated accordingly to R_{thj-c}
5. Pulse width limited by safe operating area

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
R_{thj-c}	Thermal resistance junction-case Max	2.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb Max	42	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4 board, 2oz Cu ($t < 10\text{sec.}$)

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not repetitive avalanche current (pulse width limited by T_{jmax})	6	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 24\text{V}$)	800	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating } T_C=125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 6A$ $V_{GS} = 4.5V, I_D = 6A$		0.008 0.010	0.0105 0.013	Ω Ω
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 6A @ 125^{\circ}C$ $V_{GS} = 4.5V, I_D = 6A @ 125^{\circ}C$		0.012 0.016		Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10V, I_D = 12A$		38		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1MHz, V_{GS} = 0$		965 285 38		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 15V, I_D = 12A$ $V_{GS} = 4.5V, (\text{see Figure 15})$		9 3.7 3	12	nC nC nC
R_G	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level =20mv open drain	0.5	1.5	2.5	Ω

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=15V$, $I_D=6A$, $R_G=4.7\Omega$, $V_{GS}=4.5V$ (see Figure 14)		15 32		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=15V$, $I_D=6A$, $R_G=4.7\Omega$, $V_{GS}=4.5V$ (see Figure 14)		18 8.5		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				12 48	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=12A$, $V_{GS}=0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=12A$, $di/dt = 100A/\mu s$, $V_{DD}=20V$, $T_j=150^\circ C$ (see Figure 19)		24 17.4 1.45		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

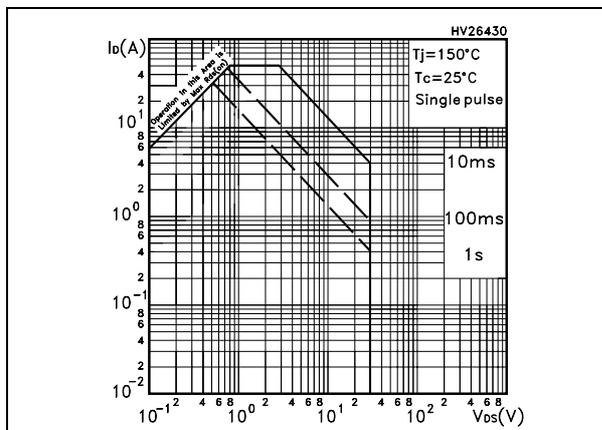


Figure 2. Thermal impedance

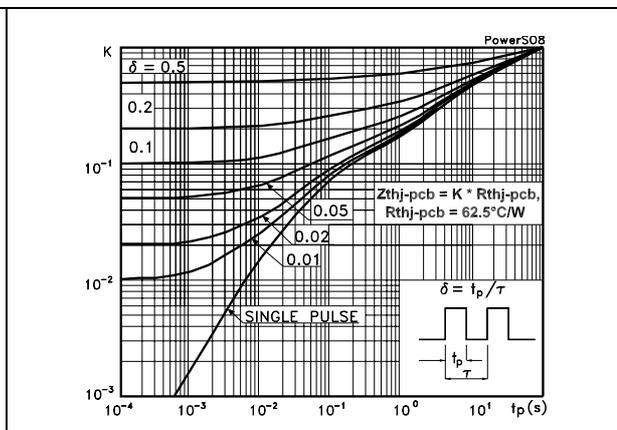


Figure 3. Output characteristics

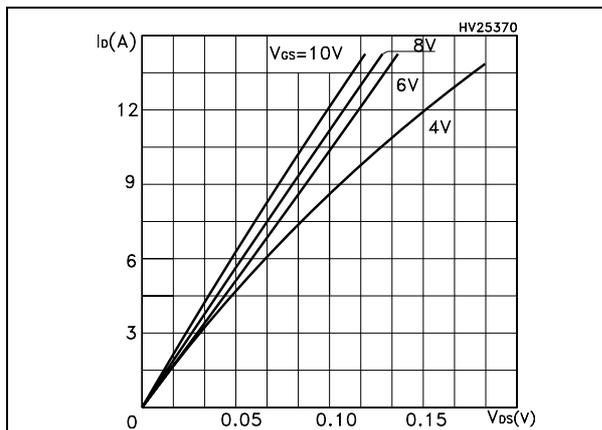


Figure 4. Transfer characteristics

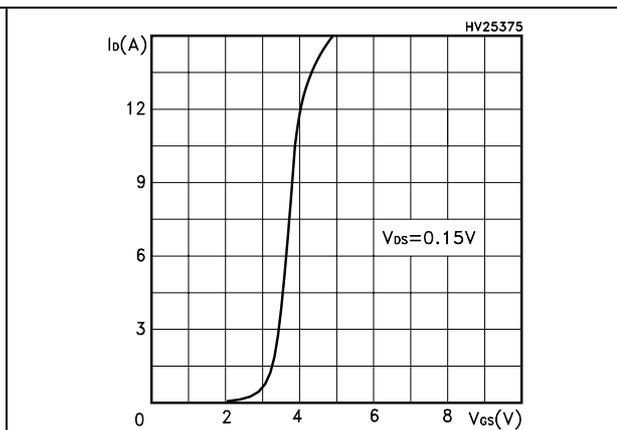


Figure 5. Transconductance

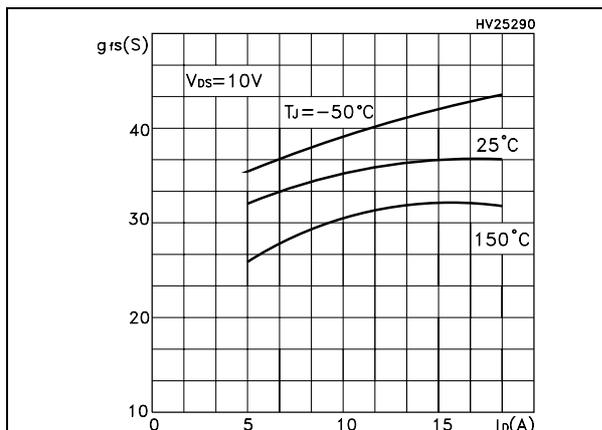


Figure 6. Static drain-source on resistance

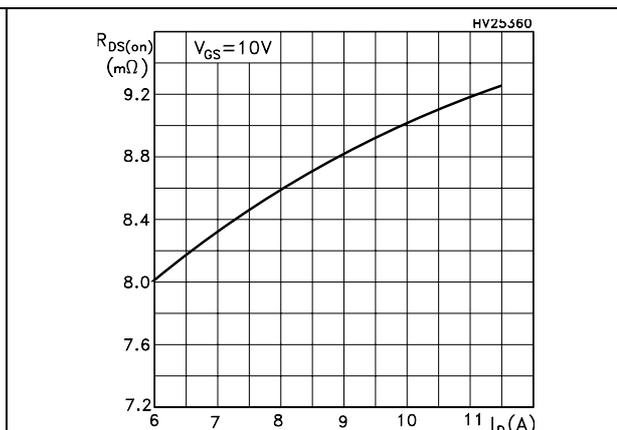


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

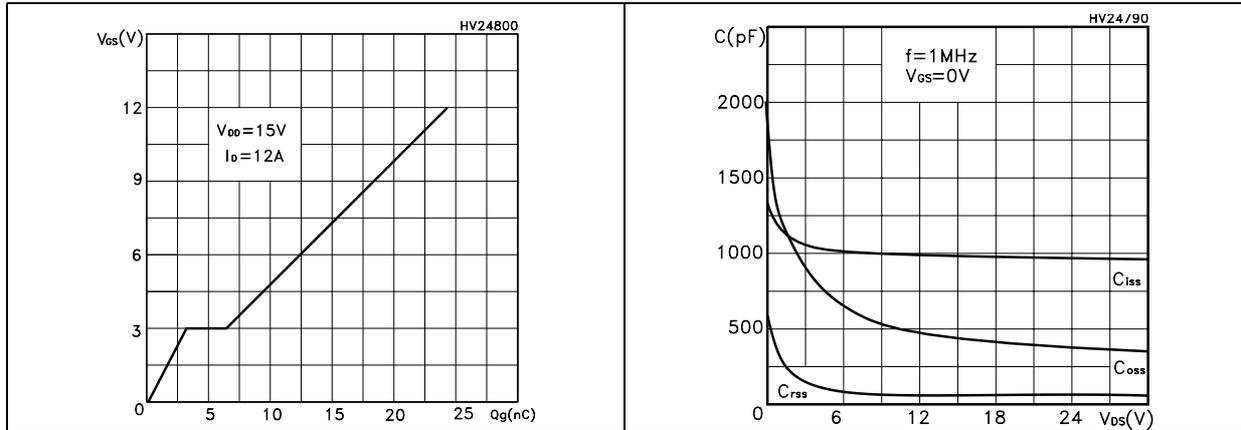


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

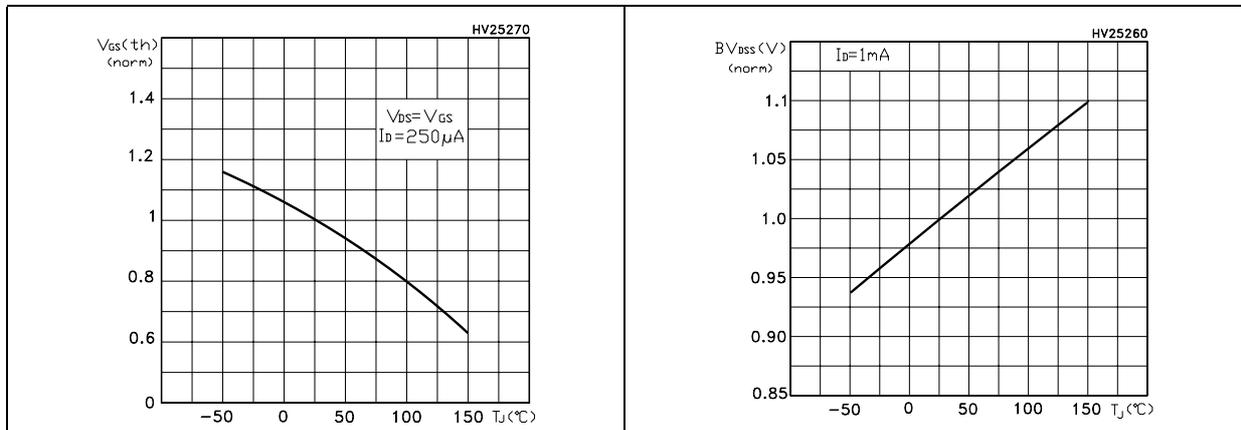


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized $B_{V_{DS}}$ vs temperature

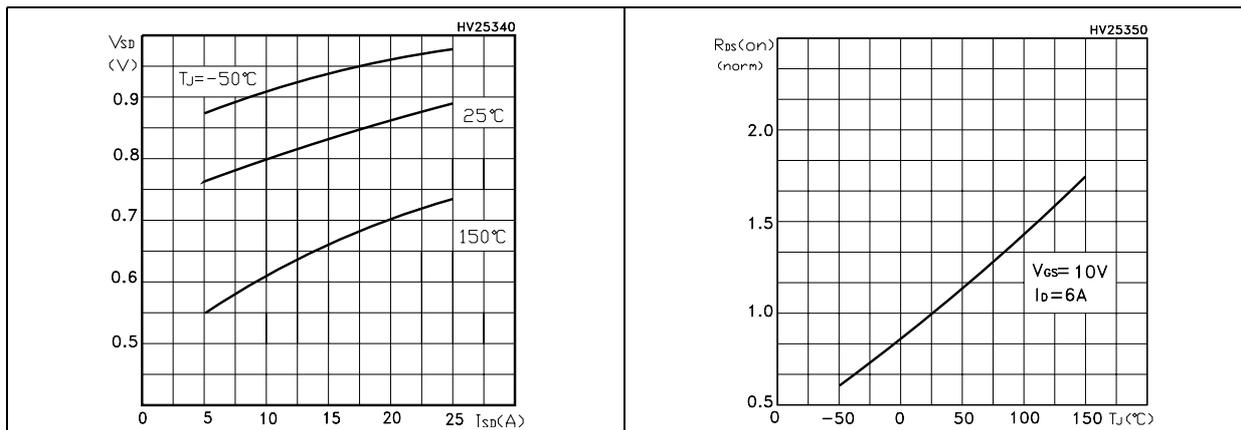
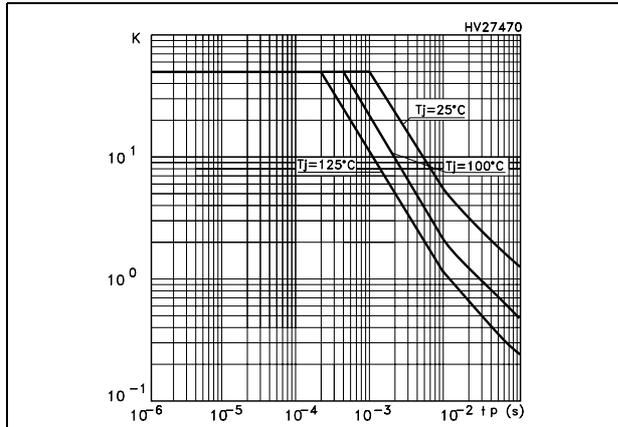


Figure 13. Allowable I_{AV} vs time in avalanche



The previous curve gives the single pulse safe operating area for unclamped inductive loads under the following conditions:

$$P_{D(AVE)} = 0.5 * (1.3 * BV_{DSS} * I_{AV})$$

$$EAS_{(AR)} = P_{D(AVE)} * t_{AV}$$

Where:

I_{AV} is the Allowable Current in Avalanche

P_{D(AVE)} is the Average Power Dissipation in Avalanche (Single Pulse)

t_{AV} is the Time in Avalanche

3 Test circuit

Figure 14. Switching times test circuit for resistive load

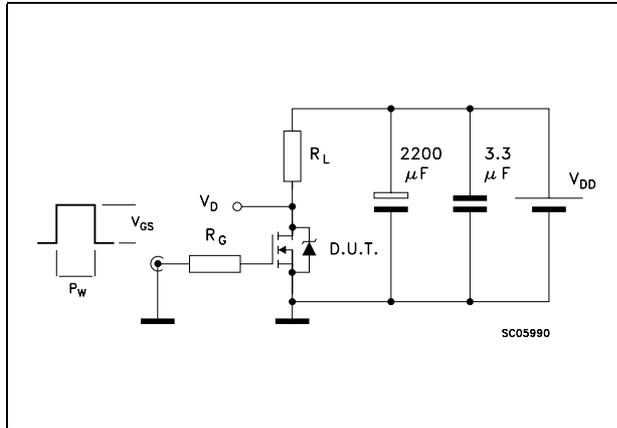


Figure 15. Gate charge test circuit

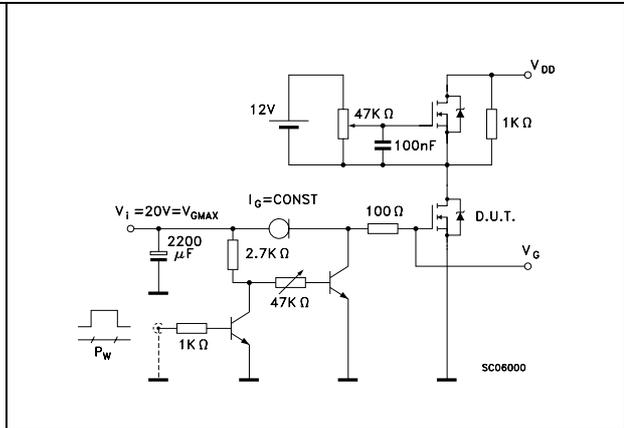


Figure 16. Test circuit for inductive load switching and diode recovery times

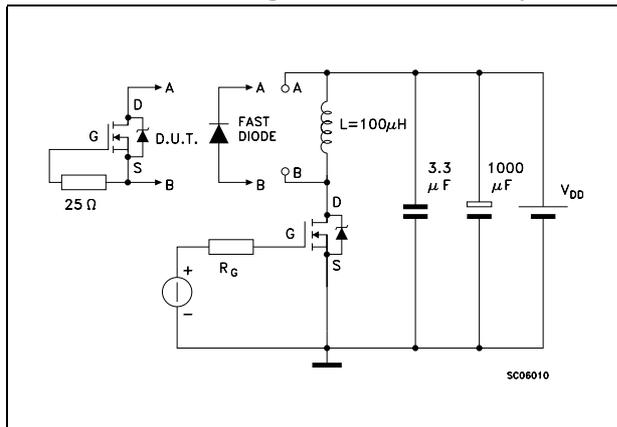


Figure 17. Unclamped inductive load test circuit

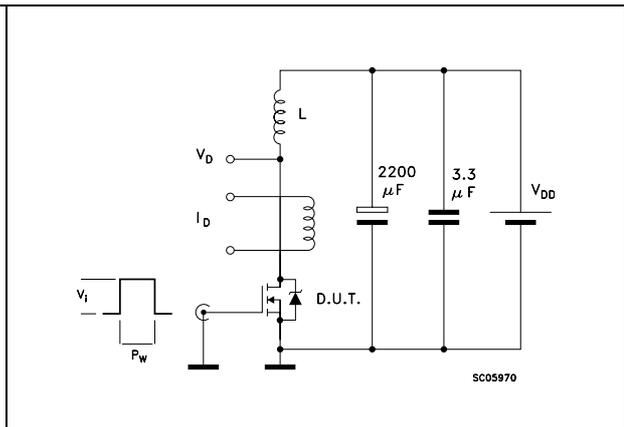


Figure 18. Unclamped inductive waveform

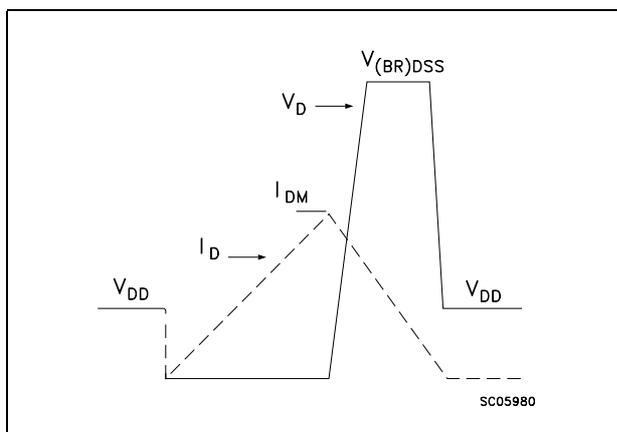
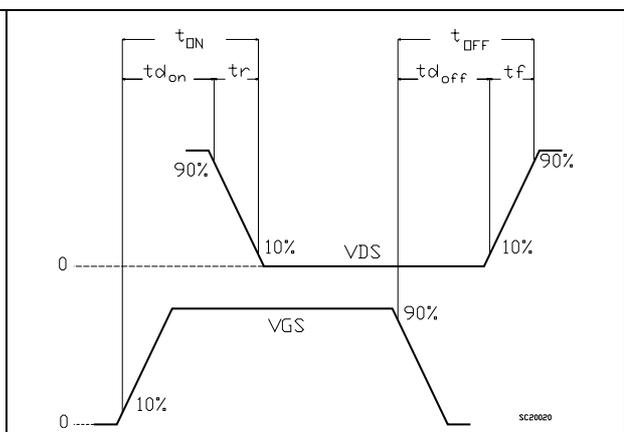


Figure 19. Switching time waveform

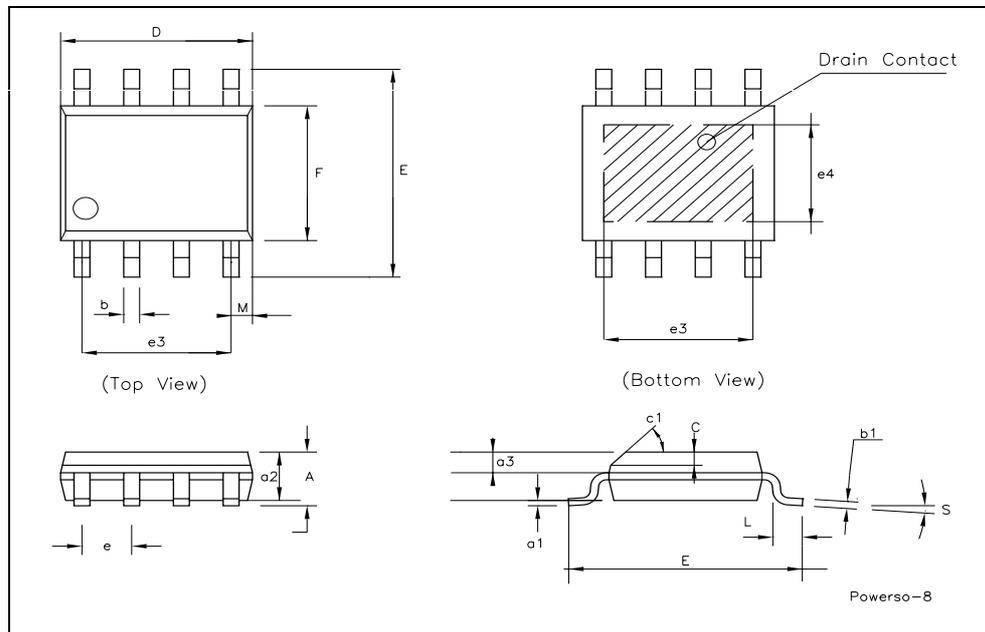


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

PowerSO-8™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45° (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
e4		2.79			0.110	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8° (max.)					



5 Revision history

Table 8. Revision history

Date	Revision	Changes
21-Jul-2004	1	Initial release.
24-May-2005	2	New value on Table 6
23-Jun-2005	3	New Rg value on Table 6
16-Nov-2005	4	Complete version
03-Apr-2006	5	New template

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED REPRESENTATIVE OF ST, ST PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS, WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2006 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

