

UTC MM1538 LINEAR INTEGRATED CIRCUIT

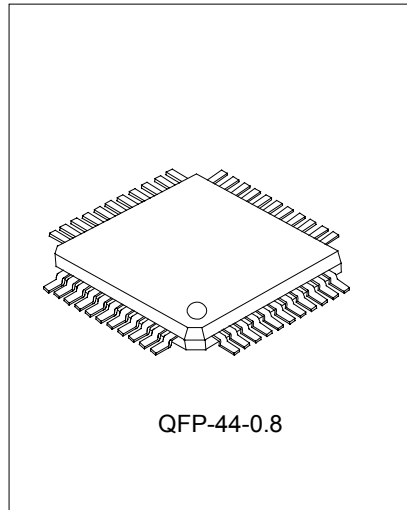
4-CH MOTOR DRIVER FOR PORTABLE CD PLAYERS

DESCRIPTION

The UTC MM1538 contains a 4ch H bridge driver and DC-DC converter control circuit on one chip, and was developed for use in portable CD players.

FEATURES

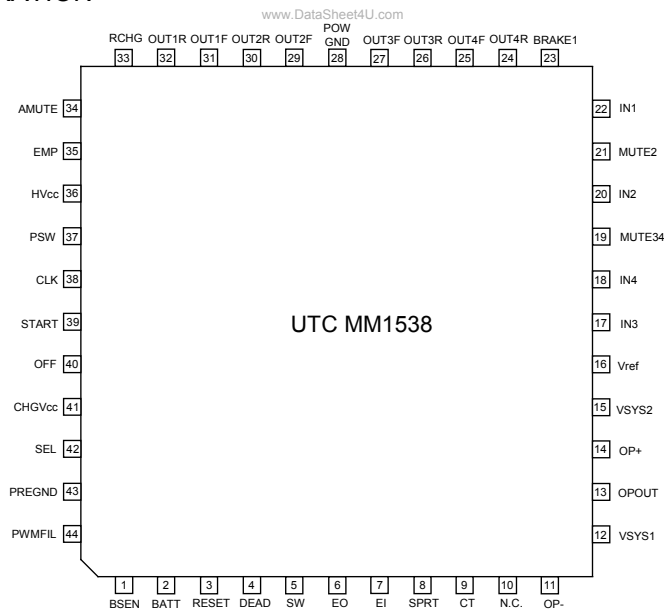
- *Built-in 4ch H bridge driver, and PWM control of load drive voltage is made possible by external components.
- *DC-DC converter control circuit on chip.
- *With reset output inversion output pin.
- *Empty detection level can be switched between rechargeable battery and dry battery.
- *Constant current charging; current value can be varied using external resistor.
- *Built-in power transistor for charging.
- *Built-in independent thermal shutdown circuit.



APPLICATIONS

- *Portable CD radio cassette recorders

PIN CONFIGURATION



UTCMM1538 LINEAR INTEGRATED CIRCUIT

PIN DESCRIPTION

PIN NO.	PIN NAME	INPUT/OUTPUT	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
1	BSEN	Input	Battery Voltage Monitor	
2	BATT	Input	Battery Power Supply Input	Power Supply
3	RESET	Output	Reset Detect Output	
4	DEAD	Input	DEAD Time Setting	
5	SW	Output	Transistor Drive For Voltage Multiplier	
6	EO	Output	Error Amplifier Output	
7	EI	Input	Error Amplifier Input	

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PIN NO.	PIN NAME	INPUT/OUTPUT	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
8	SPRT	Output	Short Circuit Protection Setting	
9	CT	Output	Triangular-Wave Output	
10	N.C.			
11 14	OP- OP+	Input	Op Amp Negative Input Op Amp Positive Input	
12	VSYS1	Input	Control Circuit Power Supply Input	Control Circuit Power Supply
13	OPOUT	Output	Op Amp Output	
15	VSYS2	Input	Driver Pre-step Power Supply	Pre-Drive Power Supply
16	Vref	Input	Reference Voltage Input	
17 18 20 22	IN3 IN4 IN2 IN1	Input	ch3 Control Signal Input ch4 Control Signal Input ch2 Control Signal Input ch1 Control Signal Input	

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PIN NO.	PIN NAME	INPUT/OUTPUT	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
19 21 23	MUTE34 MUTE2 BRAKE1	Input	Ch3 and 4 Mute Ch2 Mute Ch1 Brake	
24 25 26 27 29 30 31 32	OUT4R OUT4F OUT3R OUT3F OUT2F OUT2R OUT1F OUT1R	Output	Ch4 Negative Output Ch4 Positive Output Ch3 Negative Output Ch3 Positive Output Ch2 Positive Output Ch2 Negative Output Ch1 Positive Output Ch1 Negative Output	
28	POWGND		Power Block Power Supply Ground	
36	HVcc	Input	H-Bridge Power Supply Input	
33	RCHG	Input	Charge Current Setting	
34	AMUTE	Output	Reset Invert Output	
35	EMP	Output	Empty Detect Output	
37	PSW	Output	PWM Transistor Drive	
38	CLK	Input	External Clock Synchronizing Input	

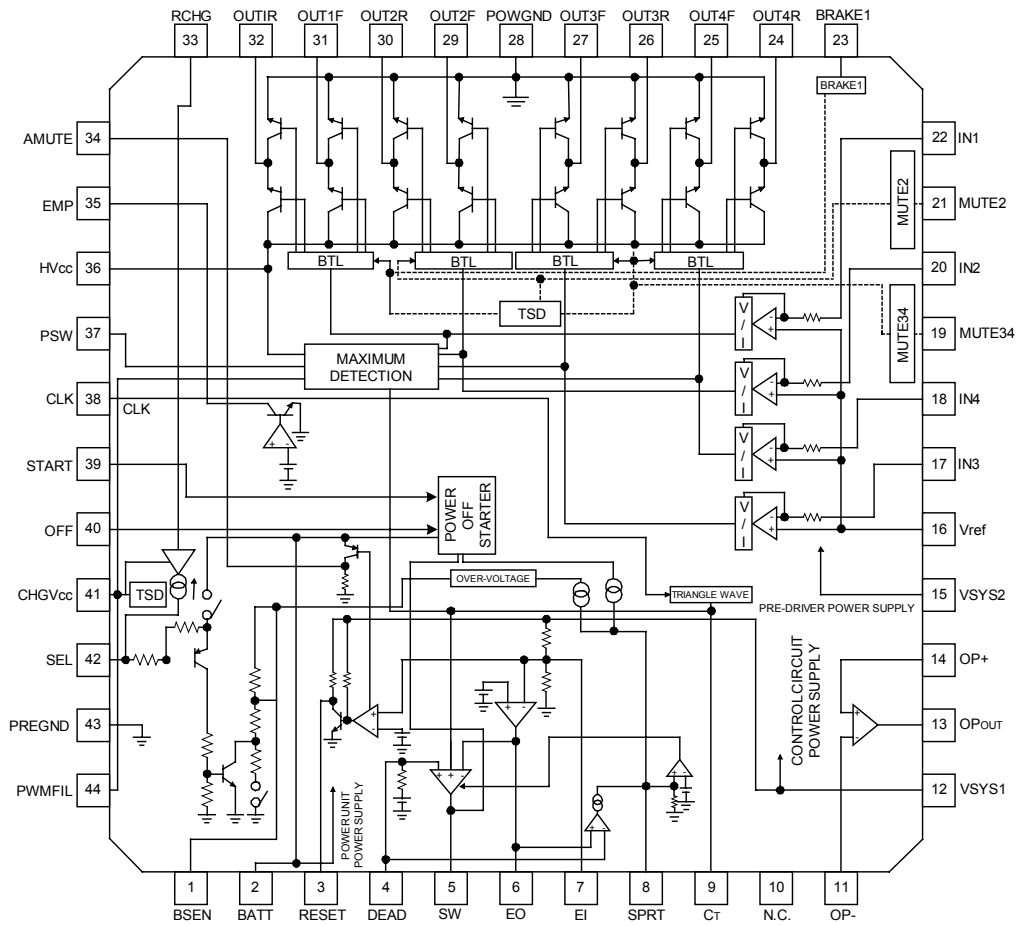
UTCMM1538 LINEAR INTEGRATED CIRCUIT

PIN NO.	PIN NAME	INPUT/OUTPUT	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
39	START	Input	Voltage Multiplier DC-DC Converter Start	
40	OFF	Input	Voltage Multiplier DC-DC Converter OFF	
41	CHGVcc	Input	Charging Circuit Power Supply Input	Charging Circuit Power Supply
42	SEL	Input/Output	Empty Detect Level Switch	
43	PREGND		Pre Section Power Supply Ground	Pre Section Power Supply Ground
44	PWMFIL	Input	PWM Phase Compensation	

*The positive and negative outputs are the polarity with respect to the input

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BLOCK DIAGRAM



UTCMM1538 LINEAR INTEGRATED CIRCUIT

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	Vcc *1	13.5	V
Driver Output Current	Io	500	mA
Power Dissipation	Pd	625	mW
Operating Temperature	TOPR	-30~+85	°C
Storage Temperature	TSTG	-55~+150	°C

*1: Vcc shows input voltage of VSYS1, VSYS2, HVcc, BATT, and CHGVcc.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Control Circuit Power Supply Voltage	VSYS1	2.7	3.2	5.5	V
Pre-Driver Circuit Power Supply Voltage	VSYS2	2.7	3.2	5.5	V
H-Bridge Power Supply Voltage	HVcc		PWM	BATT	V
Power Supply Voltage	BATT	1.5	2.4	8.0	V
Charging circuit Power supply Voltage	CHGVcc	3.0	4.5	8.0	V
Operating Temperature	Ta	-10	25	70	°C

ELECTRICAL CHARACTERISTICS

(Ta=25°C, BATT=2.4V, VSYS1=VSYS2=3.2V, Vref=1.6V, CHGVcc=0V, fCLK=88.2kHz, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common Section						
BATT Stand-by Current	IST	BATT=9.0V, VSYS1=VSYS2=Vref=0V		0	3	μA
BATT Supply Current (No load)	IBAT	HVcc=0.45V, MUTE34=3.2V		2.5	4.0	mA
VSYS1 Supply Current (No load)	ISYS1	HVcc=0.45V, MUTE34=3.2V, EI=0V		4.7	6.4	mA
VSYS2 Supply Current (No load)	ISYS2	HVcc=0.45V, MUTE34=3.2V		4.1	5.5	mA
CHGVcc Supply Current (No load)	ICGVCC	CHGVcc=4.5V, ROUT=OPEN		0.65	2.00	mA
H-Bridge Driver Part						
Voltage Gain ch1, ch3, ch4	GVC134		12	14	16	dB
Voltage Gain ch2	GVC2		21.5	23.5	24.5	dB
Gain Error By Polarity	ΔGVC		-2	0	2	dB
Input pin resistance ch1, ch3, ch4	RIN134	IN=1.7V and 1.8V	9	11	13	kΩ
Input pin resistance ch2	RIN2	IN=1.7V and 1.8V	6	7.5	9	kΩ
Maximum Output Voltage	VOU	RL=8Ω, HVcc=BATT=4.0V, IN=0-3.2V	1.9	2.1		V
Saturation Voltage (Lower)	VsatL	Io=-300mA, IN=0 and 3.2V		240	400	mV
Saturation Voltage (Upper)	VsatU	Io=-300mA, IN=0 and 3.2V		240	400	mV
Input Offset Voltage	VOI		-8	0	8	mV
Output Offset Voltage ch1, ch3, ch4	VOO134	Vref=IN=1.6V	-50	0	50	mV
Output Offset Voltage ch2	VOO2	Vref=IN=1.6V	-130	0	130	mV
Dead Zone	VDB		-10	0	10	mV
BRAKE1ON Threshold Voltage	VBRON	IN1=1.8V	2.0			V
BRAKE1OFF Threshold Voltage	VBR OFF	IN1=1.8V			0.8	V
MUTE2 ON Threshold Voltage	VM2ON	IN2=1.8V	2.0			V
H-Bridge Driver Part						
MUTE2 OFF Threshold Voltage	VM2OFF	IN2=1.8V			0.8	V
MUTE34 ON Threshold Voltage	VM34ON	IN3=IN4=1.8V			0.8	V
MUTE34 OFF Threshold Voltage	VM34OFF	IN3=IN4=1.8V	2.0			V
Vref ON Threshold Voltage	VrefON	IN1=IN2=IN3=IN4=1.8V	1.2			V
Vref OFF Threshold Voltage	VrefOFF	IN1=IN2=IN3=IN4=1.8V			0.8	V

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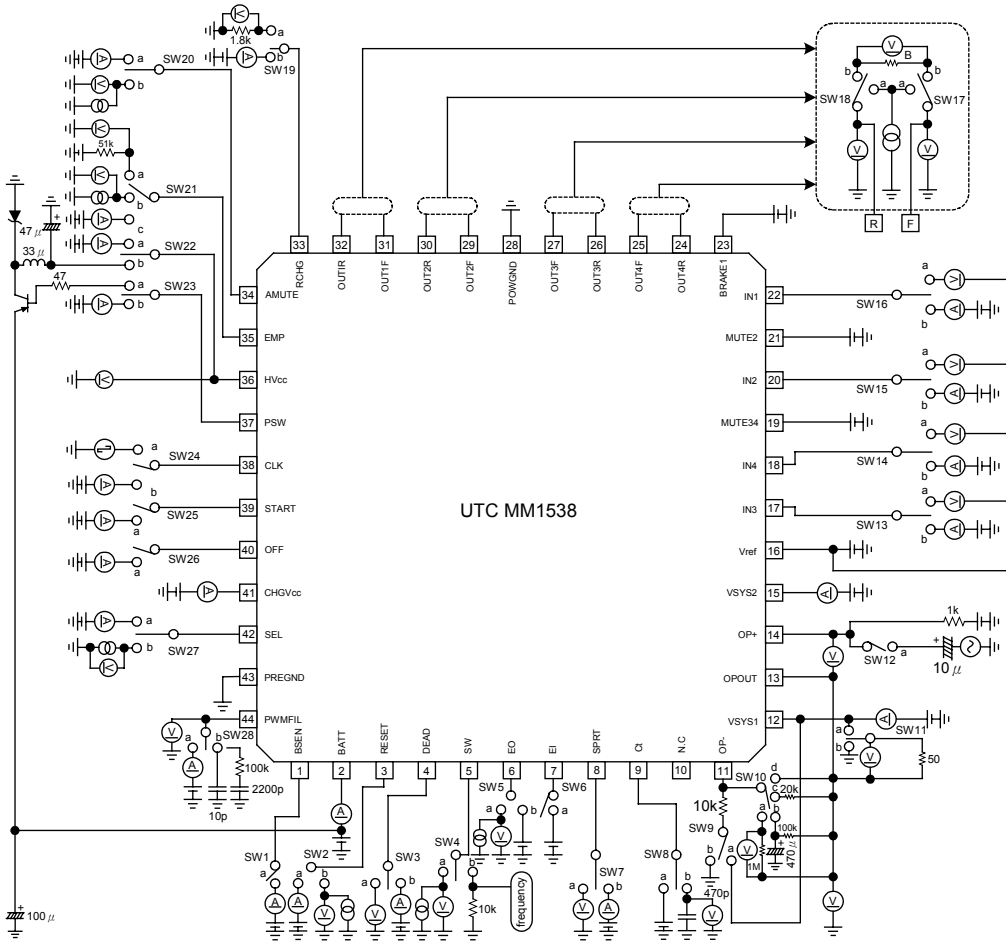
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BRAKE1 Brake Current	I _{BRAKE1}	Current difference between BRAKE pin "H" time and "L" time.	4	7	10	mA
PWM Power Supply Driving						
PSW Sink Current	I _{PSW}	IN1=2.1V	10	13	17	mA
HVcc Level Shift Voltage	V _{SHIF}	IN1=1.8V, HVcc=OUT1F	0.35	0.45	0.55	V
HVcc Leak Current	I _{HVK}	HVcc=9.0V, VSYS1=VSYS2=BATT=0V		0	5	μA
PWM Amp Transfer Gain	G _{PWM}	IN1=1.8V, HVcc=1.2 ~ 1.4V	1/60	1/50	1/40	1/kΩ
DC-DC Converter						
Error Amp						
VSYS1 Threshold Voltage	V _{S1TH}		3.05	3.20	3.35	V
EO Pin Output Voltage "H"	V _{EOH}	EI=0.7V, I _o =-100μA	1.4	1.6		V
EO Pin Output Voltage "L"	V _{EOH}	EI=1.3V, I _o =100μA			0.3	V
Short Circuit Protection						
SPRT Pin Voltage	V _{SPR}	EI=1.3V		0	0.1	V
EO=H SPRT Pin Current1	I _{SPR1}	EI=0.7V	6	10	16	μA
OFF=L SPRT Pin Current2	I _{SPR2}	EI=1.3V, OFF=0V	12	20	32	μA
SPRT Pin Current3 Over-Voltage	I _{SPR3}	EI=1.3V, BATT=9.5V	12	20	32	μA
SPRT Pin Impedance	R _{SPR}		175	220	265	kΩ
SPRT Pin Threshold Voltage	V _{SPTH}	EI=0.7V, C _T =0V	1.10	1.20	1.30	V
Over-Voltage Protection Detect	V _{HVPR}	BSEN Pin Voltage	8.0	8.4	9.0	V
Transistor Driving						
SW Pin Output Voltage1 "H"	V _{SW1H}	BATT=C _T =1.5V, VSYS1=VSYS2=0V, I _o =-2mA Starting Time	0.78	0.98	1.13	V
SW Pin Output Voltage2 "H"	V _{SW2H}	C _T =0V, I _o =-10mA, EI=0.7V, SPRT=0V	1.00	1.50		V
SW Pin Output Voltage2 "L"	V _{SW2L}	C _T =2.0V, I _o =10mA		0.30	0.45	V
SW Pin Oscillating Frequency1	f _{SW1}	C _T =470pF, VSYS1=VSYS2=0V Starting Time	65	80	95	kHz
SW Pin Oscillating Frequency2	f _{SW2}	C _T =470pF, CLK=0V	60	70	82	kHz
SW Pin Oscillating Frequency3	f _{SW3}	C _T =470pF		88.2		kHz
SW Pin Minimum Pulse Width	T _{SWmin}	C _T =470pF, EO=0.5V→0.7V Sweep	0.01		0.60	μs
Pulse Duty Start	D _{SW1}	C _T =470pF, VSYS1=VSYS2=0V	40	50	60	%
Max. Pulse Duty At Self-Running	D _{SW2}	C _T =470pF, EI=0.7V, CLK=0V	70	80	90	%
Max. Pulse Duty At CLK Synchronization	D _{SW3}	C _T =470pF, EI=0.7V	65	75	85	%
Interface						
OFF Pin Threshold Voltage	V _{OFTH}	EI=1.3V			VSYS1-2.0	V
OFF Pin Bias Current	I _{OFF}	OFF=0V	75	95	115	μA
START Pin ON Threshold Voltage	V _{STATH1}	VSYS1=VSYS2=0V, C _T =2.0V			BATT-1.0	V
START Pin OFF Threshold Voltage	V _{STATH2}	VSYS1=VSYS2=0V, C _T =2.0V	BATT-0.3			V
START Pin Bias Current	I _{START}	START=0V	10 13	20 16	30 19	μA
CLK Pin Threshold Voltage "H"	V _{CLKTHH}		2.0			V
CLK Pin Threshold Voltage "L"	V _{CLKTHL}				0.8	V
CLK Pin Bias Current	I _{CLK}	CLK=3.2V			10	μA
Dead Time						
DEAD Pin Impedance	R _{DEAD}		52	65	78	kΩ
DEAD Pin Output Voltage	V _{DEAD}		0.78	0.88	0.98	V
Starter Circuit						

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Starter Switching Voltage	V _{STNM}	VSYS1=VSYS2=0→3.2V, START=0V	2.3	2.5	2.7	V
Starter Switching Hysteresis Width	V _{SNHS}	START=0V	130	200	300	mV
Discharge Release	V _{DIS}		1.63	1.83	2.03	V
Empty Detection						
EMP Detection Voltage 1	V _{EMPT1}	VSEL=0V	2.1	2.2	2.3	V
EMP Detection Voltage 2	V _{EMPT2}	ISEL=- 2μA	1.7	1.8	1.9	V
EMP Detection Hysteresis Voltage 1	V _{EMHS1}	VSEL=0V	25	50	100	mV
EMP Detection Hysteresis Voltage 2	V _{EMHS2}	ISEL=- 2μA	25	50	100	mV
EMP Pin Output Voltage	V _{EMP}	I _o =1mA, BSEN=1V			0.5	V
EMP Pin Output Leak Current	I _{EMPL}	BSEN=2.4V			1.0	μA
BSEN Pin Input Resistance	R _{BSEN}	VSEL=0V	17	23	27	kΩ
BSEN Pin Leak Current	I _{BSENL}	VSYS1=VSYS2=0V, BSEN=4.5V			1.0	V
SEL Pin Detection Voltage	V _{SELTH}	VSELTH=BATT-SEL, BSEN=2.0V	1.5			V
SEL Pin Detection Current	I _{SELT}		-2			μA
Reset Circuit						
VSYS1 RESET Threshold Voltage Ratio	HSRT	Comparison with error amplifier threshold voltage	85	90	95	%
RESET Detection Hysteresis Width	VRSTHS		25	50	100	mV
RESET Pin Output Voltage	V _{RST}	I _o =1mA, VSYS1=VSYS2=2.8V			0.5	V
RESET Pin PULL UP Resistance	RRST		72	90	108	kΩ
AMUTE Pin Output Voltage 1	V _{AMT1}	I _o =-1mA, VSYS1=VSYS2=2.8V	BATT -0.4		BATT	V
AMUTE Pin Output Voltage 2	V _{AMT2}	I _o =-1mA, START=0V, VSYS1=VSYS2=0V	BATT -0.4		BATT	V
AMUTE Pin PULL DOWN Resistance	R _{AMT}		77	95	113	kΩ
Op Amp						
Input Bias Current	I _{BIAS}	OP+=1.6V			300	nA
Input Offset Voltage	V _{OIOP}		-5.5	0	5.5	mV
High Level Output Voltage	V _{OHOP}	RL=OPEN	2.8			V
Low level Output Voltage	V _{LOP}	RL=OPEN			0.2	V
Output Drive Current (Source)	I _{SOU}	50 Ω GND		-6.5	-3.0	mA
Output Drive Current (Sink)	I _{SIN}	50 Ω VSYS1	0.4	0.7		mA
Open Loop Voltage Gain	G _{VO}	V _{IN} =-75dBV, f=1kHz		70		dB
Slew Rate	SR			0.5		V/μs
Battery Charging Circuit						
RCHG Pin Bias Voltage	V _{RCHG}	CHGV _{cc} =4.5V, RCHG=1.8kΩ.	0.71	0.81	0.91	V
RCHG Pin Output Resistance	R _{RCHG}	CHGV _{cc} =4.5V, RCHG=0.5 and 0.6V	0.75	0.95	1.20	kΩ
SEL Pin Leak Current 1	I _{SELLK1}	CHGV _{cc} =4.5V, RCHG=OPEN, BATT=4.5V			1.0	μA
SEL Pin Leak Current 2	I _{SELLK2}	CHGV _{cc} =0.6V, RCHG=1.8kΩ, BATT=4.5V			1.0	μA
SEL Pin Saturation Voltage	V _{SELCG}	CHGV _{cc} =4.5V, I _o =300mA, RCHG=0Ω		0.45	1.00	V

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MEASURING CIRCUIT



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SWITCHING POSITION TABLE

ITEM	SW NO.									
	1	4	5	6	7	8	22	24	25	26
BATT Stand-by Current	-	-	-	-	-	-	-	-	-	-
BATT Supply Current (No load)	-	-	-	-	-	-	a	-	a	-
VSYS1 Supply Current (No load)	-	-	-	a	-	-	a	-	a	-
VSYS2 Supply Current (No load)	-	-	-	-	-	-	a	-	a	-
CHGVcc Supply Current (No load)	-	-	-	-	-	-	-	-	-	-
VSYS1 Threshold Voltage	-	-	a	-	-	-	-	-	-	-
EO Pin Output Voltage "H"	-	-	a	a	-	-	-	-	-	-
EO Pin Output Voltage "L"	-	-	a	a	-	-	-	-	-	-
SPRT Pin Voltage	-	-	-	a	a	-	-	-	-	-
SPRT Pin Current1 EO="H"	-	-	-	a	b	-	-	-	-	-
SPRT Pin Current2 OFF="L"	-	-	-	a	b	-	-	-	-	a
SPRT Pin Current3 Over-Voltage	a	-	-	a	b	-	-	-	-	-
SPRT Pin Impedance	-	-	-	-	b	-	-	-	-	-
SPRT Pin Threshold Voltage	-	-	-	a	a	a	-	-	-	-
Over-Voltage Protection Detect	a	-	-	-	a	-	-	-	-	-
SW Pin Output Voltage1"H"	-	a	-	-	-	a	-	-	a	-
SW Pin Output Voltage2"H"	-	a	-	a	b	a	-	-	-	-
SW Pin Output Voltage2"L"	-	a	-	-	-	a	-	-	-	-
SW Pin Oscillating Frequency 1	-	b	-	-	-	b	-	-	a	-
SW Pin Oscillating Frequency 2	-	b	-	-	-	b	-	b	-	-
SW Pin Oscillating Frequency 3	-	b	-	-	-	b	-	a	-	-
SW Pin Minimum Pulse Width	-	b	b	-	-	b	-	-	-	-
Pulse Duty Start	-	b	-	-	-	b	-	b	a	-
Max Pulse Duty At Self-Running	-	b	-	-	-	b	-	b	-	-
Max Pulse Duty At CLK Synchronization	-	b	-	a	-	b	-	a	-	-

-: Turn off switch

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ITEM	SW NO.									
	2	3	4	6	7	8	20	24	25	26
DEAD Pin Impedance	-	b	-	-	-	-	-	-	-	-
DEAD Pin Output Voltage	-	a	-	-	-	-	-	-	-	-
OFF Pin Threshold Voltage	-	-	-	a	a	-	-	-	-	a
OFF Pin Bias Current	-	-	-	-	-	-	-	-	-	a
START Pin ON Threshold Voltage	-	-	a	-	-	a	-	-	a	-
START Pin OFF Threshold Voltage	-	-	a	-	-	a	-	-	a	-
START Pin Bias Current	-	-	-	-	-	-	-	-	a	-
CLK Pin Threshold Voltage "H"	-	-	a	-	-	b	-	b	-	-
CLK Pin Threshold Voltage "L"	-	-	a	-	-	b	-	b	-	-
CLK Pin Bias Current	-	-	-	-	-	-	-	a	-	-
Starter Switching Voltage	-	-	a	-	-	-	-	-	a	-
Starter Switching Hysteresis Width	-	-	a	-	-	-	-	-	a	-
Discharge Release Voltage	-	-	-	-	a	-	-	-	-	-
VSYS1 Pin RESET Threshold Voltage Ratio	b	-	-	-	-	-	-	-	-	-
RESET Detection Hysteresis Width	b	-	-	-	-	-	-	-	-	-
RESET Pin Output Voltage	b	-	-	-	-	-	-	-	-	-
RESET Pin PULL UP Resistance	a	-	-	-	-	-	-	-	-	-
AMUTE Pin Output Voltage 1	-	-	-	-	-	-	b	-	--	-
AMUTE Pin Output Voltage 2	-	-	-	-	-	-	b	-	a	-
AMUTE Pin PULL DOWN Resistance	-	-	-	-	-	-	a	-	-	-

:- Turn off switch

ITEM	SW NO.						
	1	9	10	11	12	21	27
EMP Detection Voltage 1	a	-	-	-	-	a	a
EMP Detection Voltage 2	a	-	-	-	-	a	b
EMP Detection Hysteresis Voltage 1	a	a	-	-	-	a	a
EMP Detection Hysteresis Voltage 2	a	-	-	-	-	a	b
EMP Pin Output Voltage	a	-	-	-	-	b	-
EMP Pin Output Leak Current	a	-	-	-	-	c	-
BSEN Pin Input Resistance	a	-	-	-	-	-	a
BSEN Pin Leak Current	a	-	-	-	-	-	-
SEL Pin Detection Voltage	a	-	-	-	-	a	a
SEL Pin Detection Current	a	-	-	-	-	a	b
Input Bias Current	-	-	a	-	-	-	-
Input Offset Voltage	-	-	d	-	-	-	-
"H" Level Output Voltage	-	b	c	-	-	-	-
"L" Level Output Voltage	-	a	c	-	-	-	-
Output Drive Current (Source)	-	-	d	b	-	-	-
Output Drive Current (Sink)	-	-	d	a	-	-	-
Open Loop Voltage Gain	-	-	b	-	a	-	-
Slew Rate	-	-	d	-	a	-	-

:- Turn off switch

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ITEM		SW NO.						
		13	14	15	16	17	18	22
Voltage Gain	Ch1R	-	-	-	b	b	b	a
	Ch2R	-	-	b	-	b	b	a
	Ch3R	b	-	-	-	b	b	a
	Ch4R	-	b	-	-	b	b	a
Gain Error By Polarity	Ch1	-	-	-	b	b	b	a
	Ch2	-	-	b	-	b	b	a
	Ch3	b	-	-	-	b	b	a
	Ch4	-	b	-	-	b	b	a
Input Pin resistance	Ch1	-	-	-	b	b	b	a
	Ch2	-	-	b	-	b	b	a
	Ch3	b	-	-	-	b	b	a
	Ch4	-	b	-	-	b	b	a
Maximum Output Voltage	Ch1R	-	-	-	b	b	b	a
	Ch2R	-	-	b	-	b	b	a
	Ch3R	b	-	-	-	b	b	a
	Ch4R	-	b	-	-	b	b	a
Saturation Voltage (Lower)	Ch1F	-	-	-	b	a	-	a
	Ch1R	-	-	-	b	-	a	a
	Ch2F	-	-	b	-	a	-	a
	Ch2R	-	-	b	-	-	a	a
	Ch3F	b	-	-	-	a	-	a
	Ch3R	b	-	-	-	-	-	a
	Ch4F	-	b	-	-	a	-	a
	Ch4R	-	b	-	-	-	a	a
Saturation Voltage (Upper)	Ch1F	-	-	-	b	a	-	a
	Ch1R	-	-	-	b	-	a	a
	Ch2F	-	-	b	-	a	-	a
	Ch2R	-	-	b	-	-	a	a
	Ch3F	b	-	-	-	a	-	a
	Ch3R	b	-	-	-	-	a	a
	Ch4F	-	b	-	-	a	-	a
	Ch4R	-	b	-	-	-	a	a
Input Offset Voltage	Ch1	-	-	-	a	-	-	a
	Ch2	-	-	a	-	-	-	a
	Ch3	a	-	-	-	-	-	a
	Ch4	-	a	-	-	-	-	a
Output Offset Voltage	Ch1	-	-	-	b	b	b	a
	Ch2	-	-	b	-	b	b	a
	Ch3	b	-	-	-	b	b	a
	Ch4	-	b	-	-	b	b	a
Dead Zone	Ch1	-	-	-	b	b	b	a
	Ch2	-	-	b	-	b	b	a
	Ch3	b	-	-	-	b	b	a
	Ch4	-	b	-	-	b	b	a

-: Turn off switch

UTCMM1538 LINEAR INTEGRATED CIRCUIT

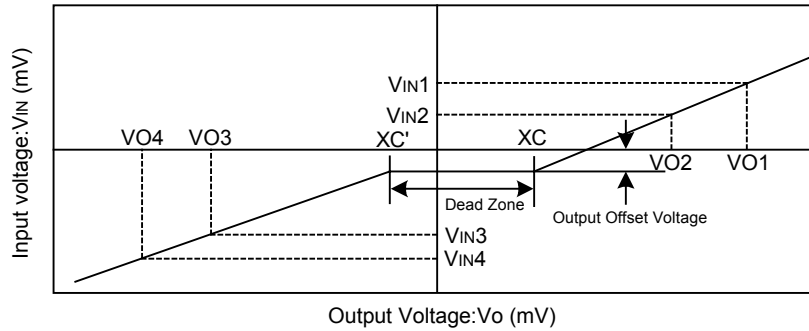
ITEM		SW NO.								
		13	14	15	16	17	18	22	23	28
BRAKE1 ON Voltage	Ch1	-	-	-	b	b	b	a	-	-
BRAKE1 OFF Voltage	Ch1	-	-	-	b	b	b	a	-	-
MUTE2 ON Voltage	Ch2	-	-	b	-	b	b	a	-	-
MUTE2 OFF Voltage	Ch2	-	-	b	-	b	b	a	-	-
MUTE34 ON Voltage	Ch3	b	-	-	-	b	b	a	-	-
	Ch4	-	b	-	-	b	b	a	-	-
MUTE34 OFF Voltage	Ch3	b	-	-	-	b	b	a	-	-
	Ch4	-	b	-	-	b	b	a	-	-
Vref ON Voltage	Ch1	-	-	-	b	b	b	a	-	-
	Ch2	-	-	b	-	b	b	a	-	-
	Ch3	b	-	-	-	b	b	a	-	-
	Ch4	-	b	-	-	b	b	a	-	-
Vref OFF Voltage	Ch1	-	-	-	b	b	b	a	-	-
	Ch2	-	-	b	-	b	b	a	-	-
	Ch3	b	-	-	-	b	b	a	-	-
	Ch4	-	b	-	-	b	b	a	-	-
BREAK1 Brake Current	Ch1	-	-	-	b	b	b	a	-	-
PWM Sink Current		-	-	-	b	-	-	a	b	a
HVcc Level Shift Voltage		-	-	-	b	b	b	b	a	b
HVcc Leak Current		-	-	-	-	b	b	a	-	-
PWM Amp Transfer Gain		-	-	-	b	b	b	a	-	-

ITEM	SW NO.	
	19	27
CHGSET Pin Bias Voltage	a	-
CHGSET Pin Output Resistance	b	-
SEL Pin Leak Current 1	-	a
SEL Pin Leak Current 2	a	a
SEL Pin Saturation Voltage	b	b

-: Turn off switch

UTCMM1538 LINEAR INTEGRATED CIRCUIT

SWITCHING POSITION TABLE



* Voltage Gain

$$G_{vc(+)} = 20 \log \frac{VO1 - VO2}{VIN1 - VIN2}$$

$$G_{vc(-)} = 20 \log \frac{VO3 - VO4}{VIN3 - VIN4}$$

* Gain Error By Polarity

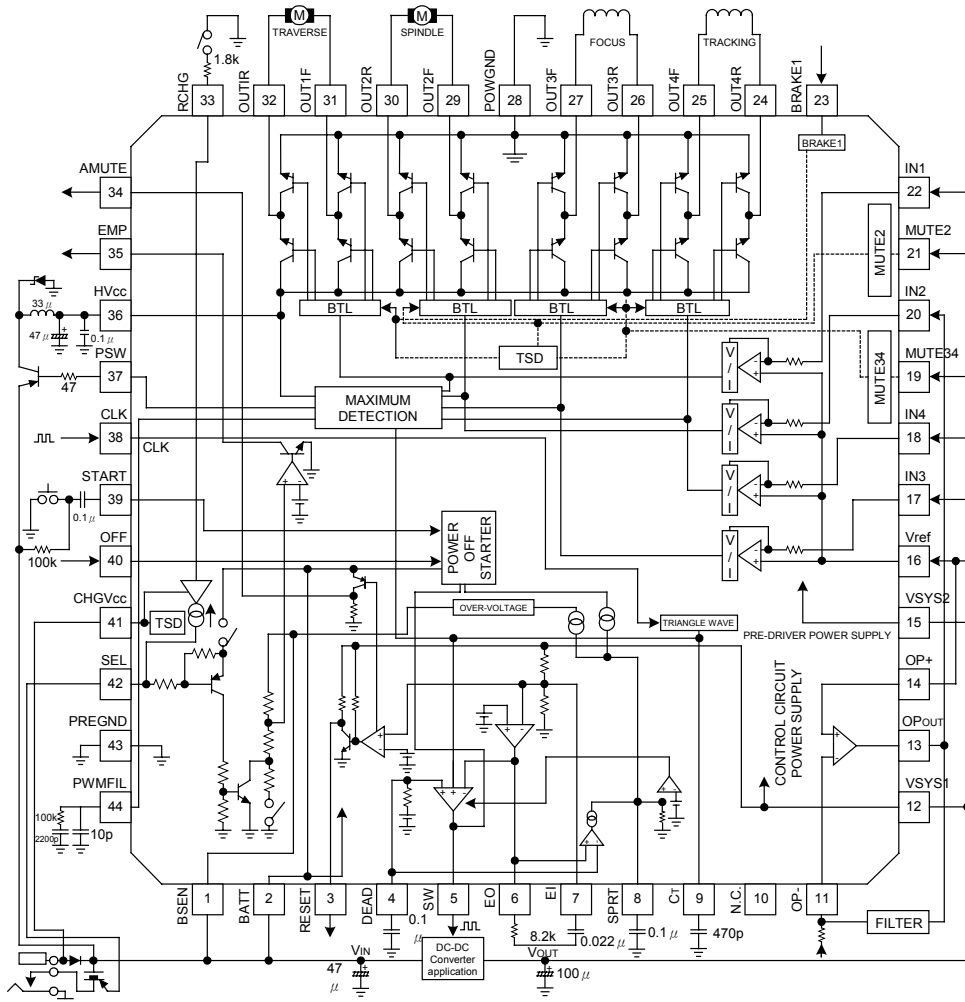
$$G_{vc} = G_{vc(+)} - G_{vc(-)}$$

* Dead Zone

$$XC - XC' = \frac{VIN2 \cdot VO1 - VIN1 \cdot VO2}{VO1 - VO2} - \frac{VIN3 \cdot VO4 - VIN4 \cdot VO3}{VO3 - VO4}$$

UTCMM1538 LINEAR INTEGRATED CIRCUIT

APPLICATION CIRCUIT



* We shall not be liable for any trouble or damage caused by using this circuit.
 * In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, Mitsumi Electric Co., Ltd. shall not be liable for any such problem, nor grant a license therefor.

UTCMM1538 LINEAR INTEGRATED CIRCUIT

CIRCUIT OPERATION

1 H-bridge driver block

(1) Gain setting

- The driver input resistance (ch 1,3 and 4) are $11k\Omega$ typ. ,ch2 is $7.5k\Omega$ typ. . Set the gain according to the following formula.

ch1 ch2 ch3	$GV=20 \log \left \frac{55k}{11k+R} \right $ (db)
ch2	$GV=20 \log \left \frac{110k}{7.5k+R} \right $ (db)

R:Externally-connected input

- The driver output stage power supply is HVcc (36PIN), and the bridge circuit power supply is VSYS2 (15PIN). Connect a bypass capacitor between these two power supplies (approximately $0.1\mu F$).

(2) Mute function

- Of the four drivers,ch1 has a brake function, and the other channels have a mute function.
- When BRAKE1(23PIN)is set to high level, both ch1 outputs go low level, and the circuit enters brake mode.
- When MUTE2(21PIN)is set to high level, the ch2 output is muted.
- When MUTE34(19PIN)is set to high level, the ch3 and 4 outputs are muted.

(3) Vref drop mute

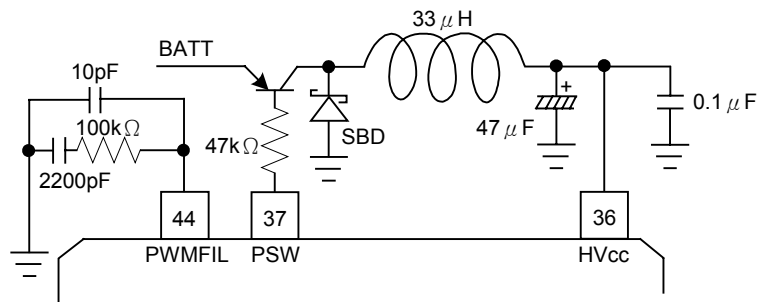
- When the voltage applied to Vref (16PIN)is $1.0V$ or less typ. , the driver outputs are set to high impedance.

(4) Thermal shutdown

- When the chip temperature reaches $150^{\circ}C$ typ. the output current is cut. The chip starts operating again at about $120^{\circ}C$ typ. .

2 PWM power supply drive block

- This detects the maximum output level from among the four channels, and supplies the load drive power supply (36PIN)for the PWM. The external components are a PNP transistor, coil, Schottky diode, and capacitor.



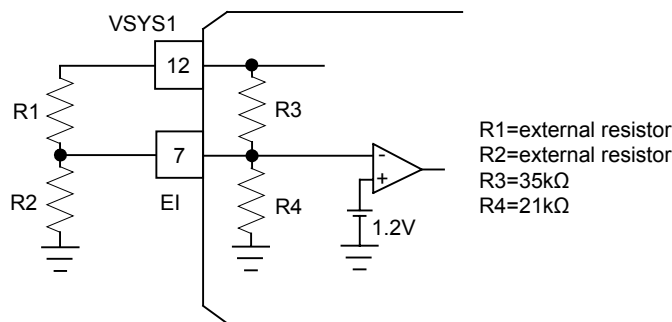
UTCMM1538 LINEAR INTEGRATED CIRCUIT

3 DC-DC converter block

(1) Output voltage

- 3.2V typ. voltage multiplier circuit can be constructed using external components. This voltage can be varied with the addition of an external resistor. The setting method is as follows.

$$V_{SYS1} = 1.2 \times \frac{\frac{R1 \cdot R3 + R2 \cdot R4}{R1 + R3} + \frac{R2 \cdot R4}{R2 + R4}}{\frac{R2 \cdot R4}{R2 + R4}} \text{ (V)}$$



(2) Short protect function

- When the error amplifier output (6PIN) has switched to the high-level state, SPRT (8PIN) is charged, and when the voltage reaches 1.2V typ., the SW (5PIN) switching stops. The time until switching stops is set by the capacitor connected to SPRT (8PIN) according to the following formula.

$$t = C_{SPRT} \times \frac{V_{TH}}{I_{SPRT}} \text{ (sec)} \quad (V_{TH}=1.2V, I_{SPRT}=10 \mu A)$$

(3) Soft start function

- The soft start function operates when a capacitor is connected between DEAD (4PIN) and GND. Also, the maximum duty can be varied by connecting a resistor to 4PIN.

$$t = C_{DEAD} \times R \text{ (sec)} \quad (R=65k\Omega)$$

(4) Power off function

- When low-level is applied to OFF (40PIN), SPRT (8PIN) is charged, and when the voltage reaches 1.2V typ., the SW (5PIN) switching stops. The time until switching stops is set by the capacitor connected to SPRT (8PIN) according to the following formula.

$$t = C_{SPRT} \times \frac{V_{TH}}{I_{OFF}} \text{ (sec)} \quad (V_{TH}=1.2V, I_{OFF}=20 \mu A)$$

(5) Over voltage protection circuit

- When the voltage applied to BSEN (1PIN) reaches 8.4V typ., SPRT (8PIN) is charged, and when the voltage reaches 1.2V typ., the SW (5PIN) switching stops. The time until switching stops is set by the capacitor connected to SPRT (8PIN) according to the following formula.

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$$t = \text{CSPRT} \times \frac{V_{\text{TH}}}{I_{\text{HV}}} \text{ (sec)} \quad (V_{\text{TH}}=1.2\text{V}, I_{\text{HV}}=20 \mu\text{A})$$

4 Empty detector block

(1) Output voltage

- When the voltage applied to the BSEN(1PIN) falls below the detector voltage, EMP(35PIN) goes from high level to low level (open-collector output). The detector voltage has 50mV typ. of hysteresis to prevent output chattering. Use SEL (42PIN) to switch the detection voltage as shown below.

SEL	Detect Voltage	Return Voltage
L	2.20V typ.	2.25V typ.
High-Z	1.80V typ.	1.85V typ.

5 Reset circuit block

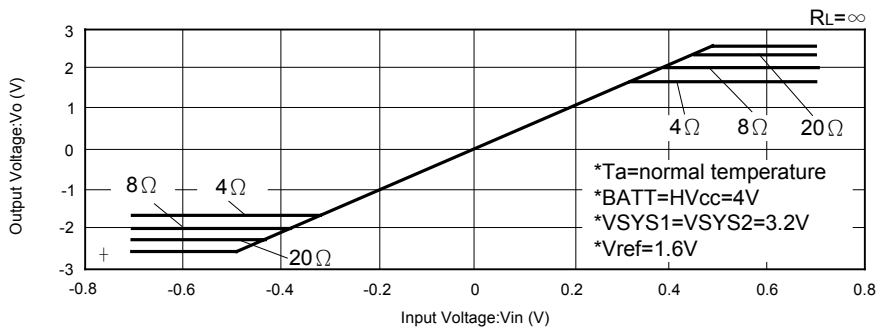
- At about 90% typ. of the DC-DC converter output voltage, RESET(3PIN) goes from low level to high level, and AMUTE(34PIN) goes from high level to low level. The reset voltage has 50mV typ. of hysteresis to prevent output chattering.

6 Charging circuit block

- The power supply for the charging circuit block is CHGVCC(41PIN), and is independent from the other circuits. The resistance between RCHG (33PIN) and GND sets the charging current. This current is drawn from SEL (42PIN).
- A thermal shutdown circuit is provided, and when the chip temperature reaches 150°C typ. the charging current is cut. The chip starts operating again at about 120°C typ. .

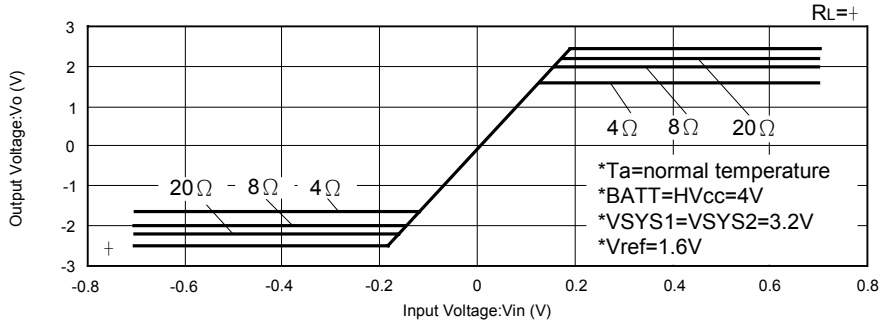
CHARACTERISTICS

Input Load Fluctuation

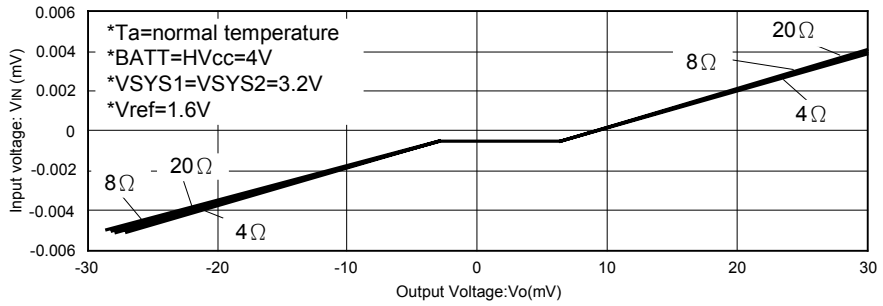


UTCMM1538 LINEAR INTEGRATED CIRCUIT

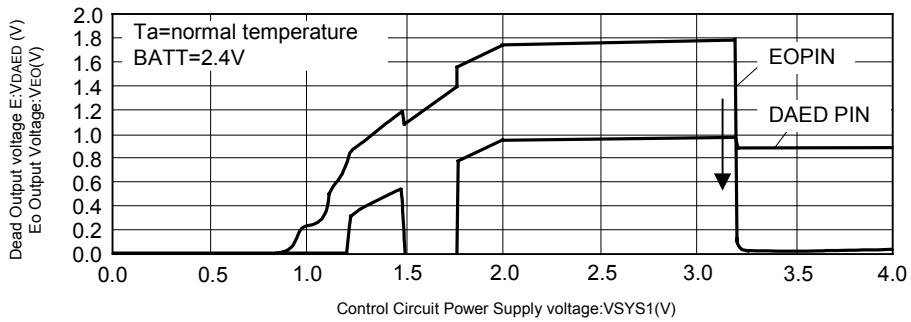
Input Load Fluctuation (ch2)



Dead Zone

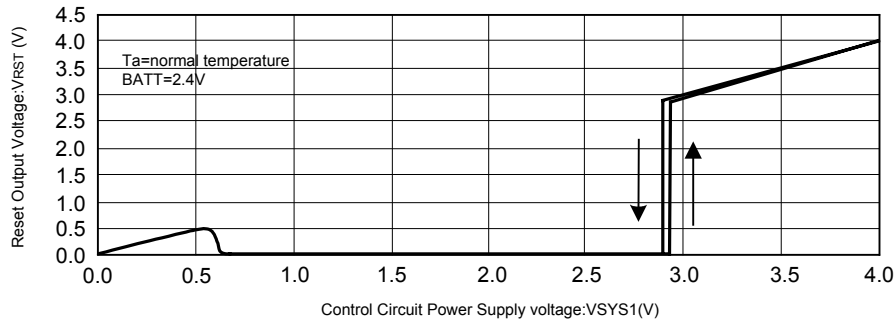


Error Amp Output Voltage



UTCMM1538 LINEAR INTEGRATED CIRCUIT

Resete Pin Voltage



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