# NTHD5903T1

# Power MOSFET
# Dual P-Channel ChipFET™

## 2.1 Amps, 20 Volts

**Features**

- Low $R_{DS(on)}$ for Higher Efficiency
- Logic Level Gate Drive
- Miniature ChipFET Surface Mount Package Saves Board Space

**Applications**

- Power Management in Portable and Battery–Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | 5 secs | Steady State | Unit |
|---|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | –20 | | V |
| Gate–Source Voltage | $V_{GS}$ | ±12 | | V |
| Continuous Drain Current ($T_J$ = 150°C) (Note 1)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $I_D$ | <br>±2.9<br>±2.1 | <br>±2.1<br>±1.5 | A |
| Pulsed Drain Current | $I_{DM}$ | ±10 | | A |
| Continuous Source Current (Diode Conduction) (Note 1) | $I_S$ | –1.8 | –0.9 | A |
| Maximum Power Dissipation (Note 1)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $P_D$ | <br>2.1<br>1.1 | <br>1.1<br>0.6 | W |
| Operating Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | | °C |

1. Surface Mounted on 1″ x 1″ FR4 Board.



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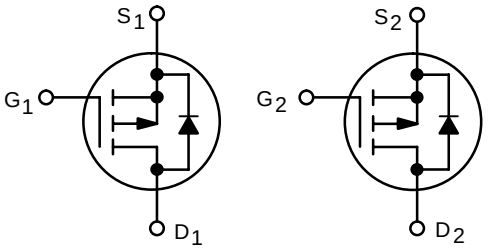
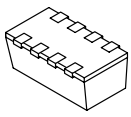
**DUAL P–CHANNEL**
**2.1 AMPS, 20 VOLTS**
**$R_{DS(on)}$ = 155 mΩ**

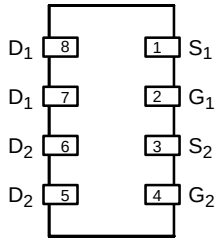



**P–Channel MOSFET** **P–Channel MOSFET**

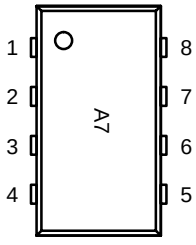


**ChipFET**
**CASE 1206A**
**STYLE 2**

**PIN CONNECTIONS**




**MARKING DIAGRAM**




A7 = Specific Device Code

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTHD5903T1 | ChipFET | 3000/Tape & Reel |

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Maximum Junction–to–Ambient (Note 2)<br>$t \leq 5$ sec<br>Steady State | $R_{thJA}$ | <br>50<br>90 | <br>60<br>110 | °C/W |
| Maximum Junction–to–Foot (Drain)<br>Steady State | $R_{thJF}$ | 30 | 40 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = -250$ μA | –0.6 | – | – | V |
| Gate–Body Leakage | $I_{GSS}$ | $V_{DS} = 0$ V, $V_{GS} = \pm 12$ V | – | – | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS} = -16$ V, $V_{GS} = 0$ V | – | – | –1.0 | μA |
| | | $V_{DS} = -16$ V, $V_{GS} = 0$ V, $T_J = 85$°C | – | – | –5.0 | |
| On–State Drain Current (Note 3) | $I_{D(on)}$ | $V_{DS} \leq -5.0$ V, $V_{GS} = -4.5$ V | –10 | – | – | A |
| Drain–Source On–State Resistance (Note 3) | $r_{DS(on)}$ | $V_{GS} = -4.5$ V, $I_D = -2.1$ A | – | 0.130 | 0.155 | Ω |
| | | $V_{GS} = -3.6$ V, $I_D = -2.0$ A | – | 0.150 | 0.180 | |
| | | $V_{GS} = -2.5$ V, $I_D = -1.7$ A | – | 0.215 | 0.260 | |
| Forward Transconductance (Note 3) | $g_{fs}$ | $V_{DS} = -10$ V, $I_D = -2.1$ A | – | 5.0 | – | S |
| Diode Forward Voltage (Note 3) | $V_{SD}$ | $I_S = -0.9$ A, $V_{GS} = 0$ V | – | –0.8 | –1.2 | V |
| **Dynamic** (Note 4) | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS} = -10$ V, $V_{GS} = -4.5$ V, $I_D = -2.1$ A | – | 3.0 | 6.0 | nC |
| Gate–Source Charge | $Q_{gs}$ | | – | 0.9 | – | |
| Gate–Drain Charge | $Q_{gd}$ | | – | 0.6 | – | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{DD} = -10$ V, $R_L = 10$ Ω, $I_D \cong -1.0$ A, $V_{GEN} = -4.5$ V, $R_G = 6$ Ω | – | 13 | 20 | ns |
| Rise Time | $t_r$ | | – | 35 | 55 | |
| Turn–Off Delay Time | $t_{d(off)}$ | | – | 25 | 40 | |
| Fall Time | $t_f$ | | – | 25 | 40 | |
| Source–Drain Reverse Recovery Time | $t_{rr}$ | $I_F = -0.9$ A, di/dt = 100 A/μs | – | 40 | 80 | |

2. Surface Mounted on 1″ x 1″ FR4 Board.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

## TYPICAL ELECTRICAL CHARACTERISTICS

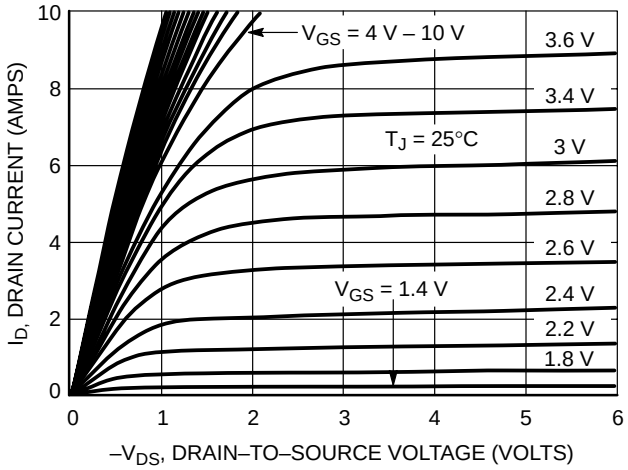



**Figure 1. On–Region Characteristics**

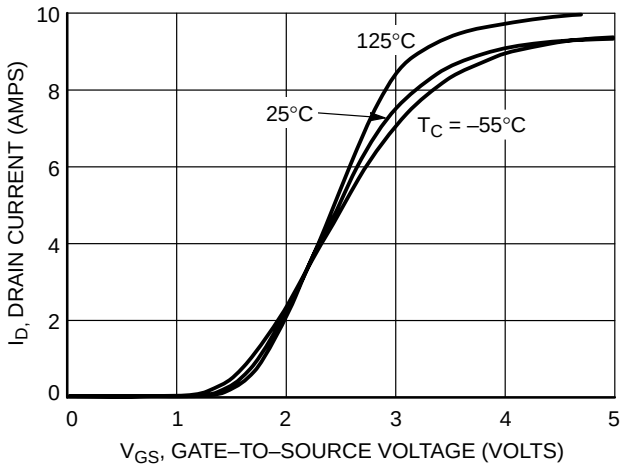



**Figure 2. Transfer Characteristics**

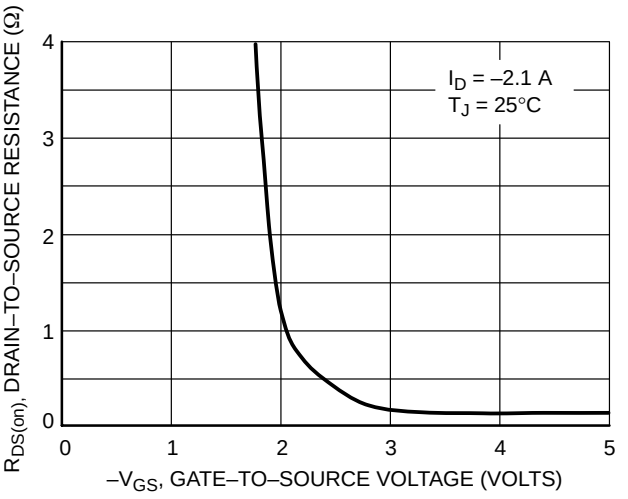



**Figure 3. On–Resistance vs. Gate–to–Source Voltage**

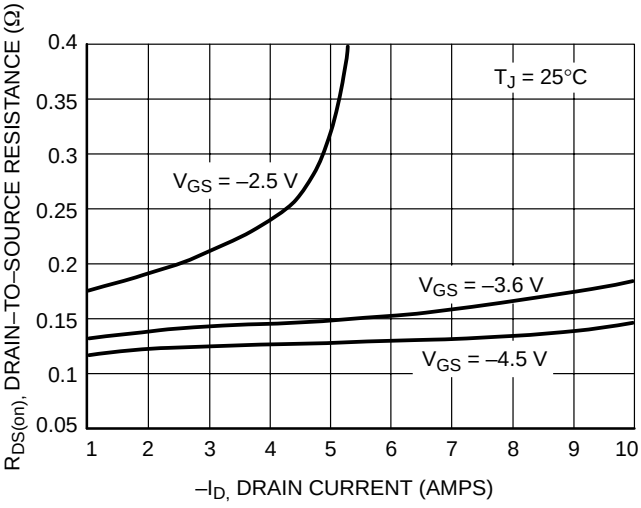



**Figure 4. On–Resistance vs. Drain Current and Gate Voltage**

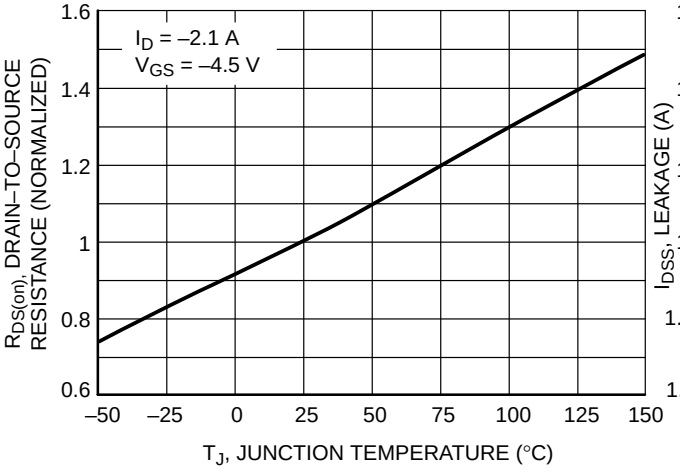



**Figure 5. On–Resistance Variation with Temperature**

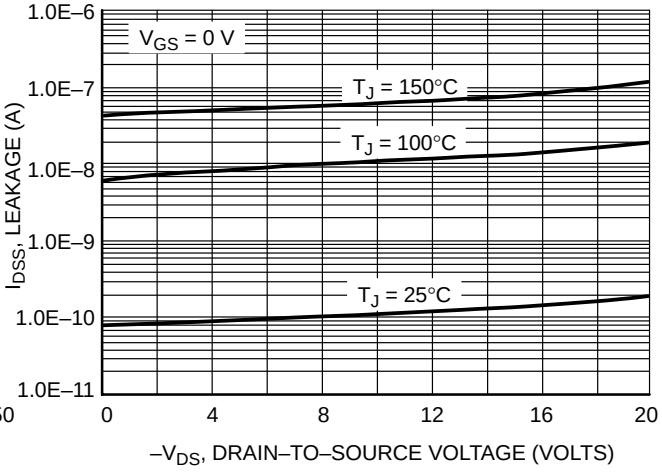



**Figure 6. Drain–to–Source Leakage Current vs. Voltage**

## TYPICAL ELECTRICAL CHARACTERISTICS

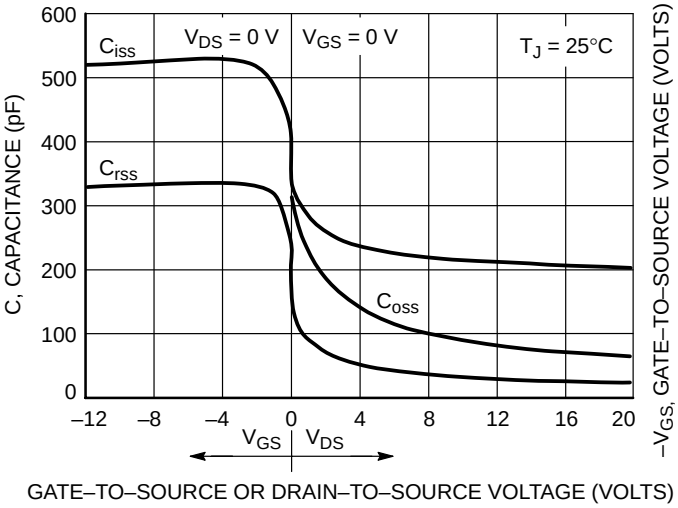



**Figure 7. Capacitance Variation**

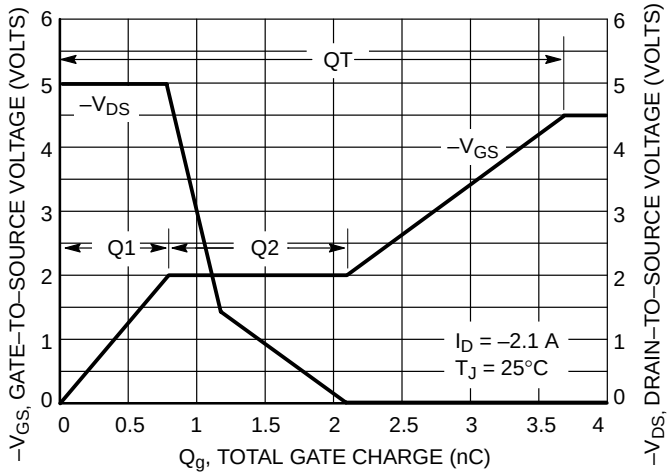



**Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

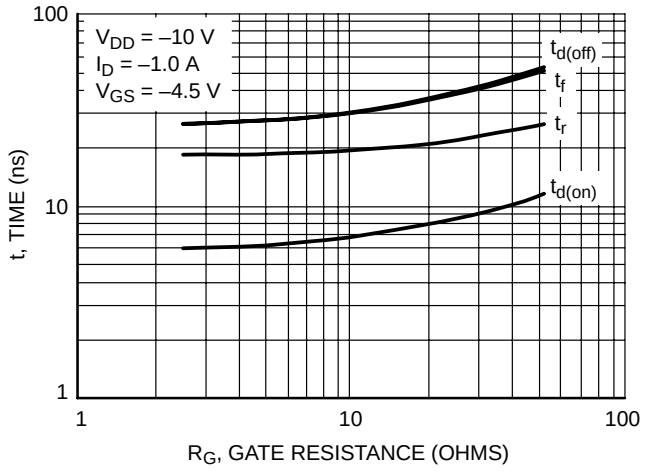



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

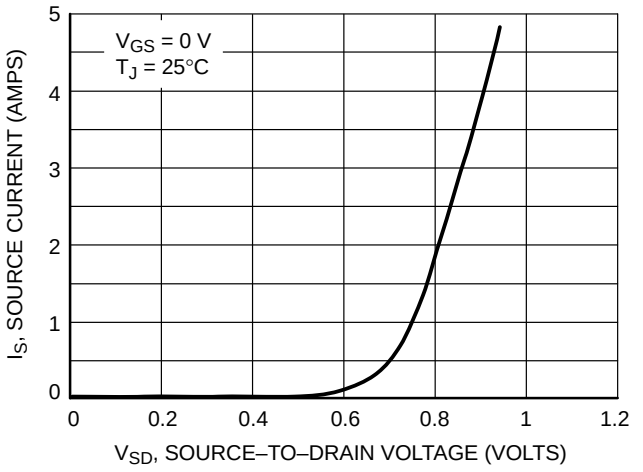



**Figure 10. Diode Forward Voltage vs. Current**

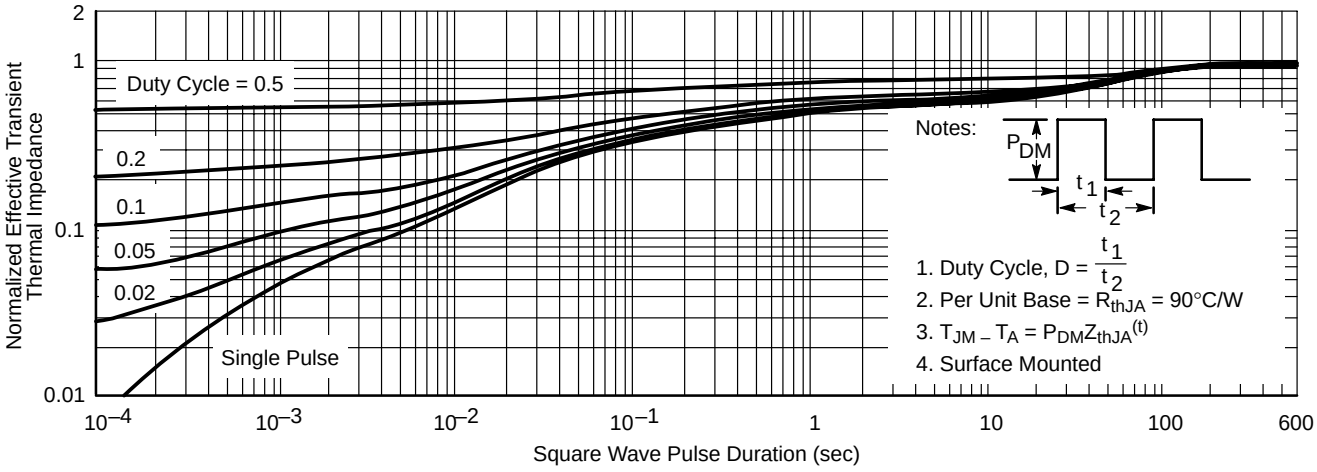


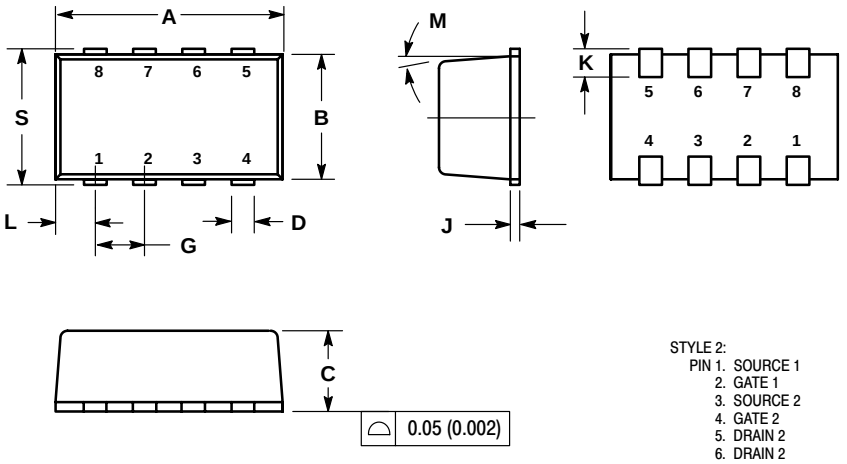

**Figure 11. Normalized Thermal Transient Impedance, Junction–to–Ambient**

# Notes

# Notes

## PACKAGE DIMENSIONS

**ChipFET**
CASE 1206A–03
ISSUE D




STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A–01 AND 1206A–02 OBSOLETE. NEW STANDARD IS 1206A–03.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.95 | 3.10 | 0.116 | 0.122 |
| B | 1.55 | 1.70 | 0.061 | 0.067 |
| C | 1.00 | 1.10 | 0.039 | 0.043 |
| D | 0.25 | 0.35 | 0.010 | 0.014 |
| G | 0.65 BSC | | 0.025 BSC | |
| J | 0.10 | 0.20 | 0.004 | 0.008 |
| K | 0.28 | 0.42 | 0.011 | 0.017 |
| L | 0.55 BSC | | 0.022 BSC | |
| M | 5 ° NOM | | 5 ° NOM | |
| S | 1.80 | 2.00 | 0.072 | 0.080 |

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