

# FAN5032

## 8-Bit Programmable 2 to 4 Phase Synchronous Buck Controller

### Features

- Selectable 2, 3, or 4 phase operation at up to 1MHz per phase
- $\pm 7.7\text{mV}$  worst-case differential sensing error over temperature
- Active current balancing between the output phases
- Power good and crowbar blanking supports on-the-fly VID code changes
- 0.5V to 1.6V output
- Fully compliant to Intel® VR10 and VR11 specifications
- Selectable VR10 extended (7 bit) and VR11 (8 bit) VID tables
- Programmable soft-start ramp
- Programmable short-circuit protection and latch-off delay

### Special Features

- 300mV OVP and crowbar threshold

### Applications

- Desktop PC/server processor power supplies for existing and next-generation Intel processors
- VRM modules

### Description

The FAN5032 is a controller for a multi-phase buck switching regulator optimized to convert a 12V input supply to the processor core voltage required by high-performance Intel processors. It has an internal 8-bit digital to analog converter (DAC) that converts a digital voltage identification (VID) code, sent from the processor to set the output voltage between 0.5V and 1.6V in 6.25mV steps. It outputs a pulse-width modulated (PWM) signal to external MOSFET drivers that, in turn, drive the switching power MOSFETs. The switching frequency of the design is programmable by a single resistor value and the number of phases can be programmed to support 2, 3, or 4 phase applications.

The FAN5032 also includes programmable no-load offset and droop functions to adjust the output voltage as a function of the load current, as required by the Intel specifications. The FAN5032 also provides an accurate and reliable short-circuit protection function with an adjustable over-current set point.

The FAN5032 is specified over the commercial temperature range of 0°C to 85°C and is available in a 40-lead MLP package.

[www.DataSheet4U.com](http://www.fairchildsemi.com)

### Ordering Information

Product Number	Package Type	Pb-Free	Operating Temperature Range	Packing Method	Quantity per Reel
FAN5032MPX	MLP-40	Yes	0°C to 85°C	Tape and Reel	3,000

### FAN5032 Block Diagram

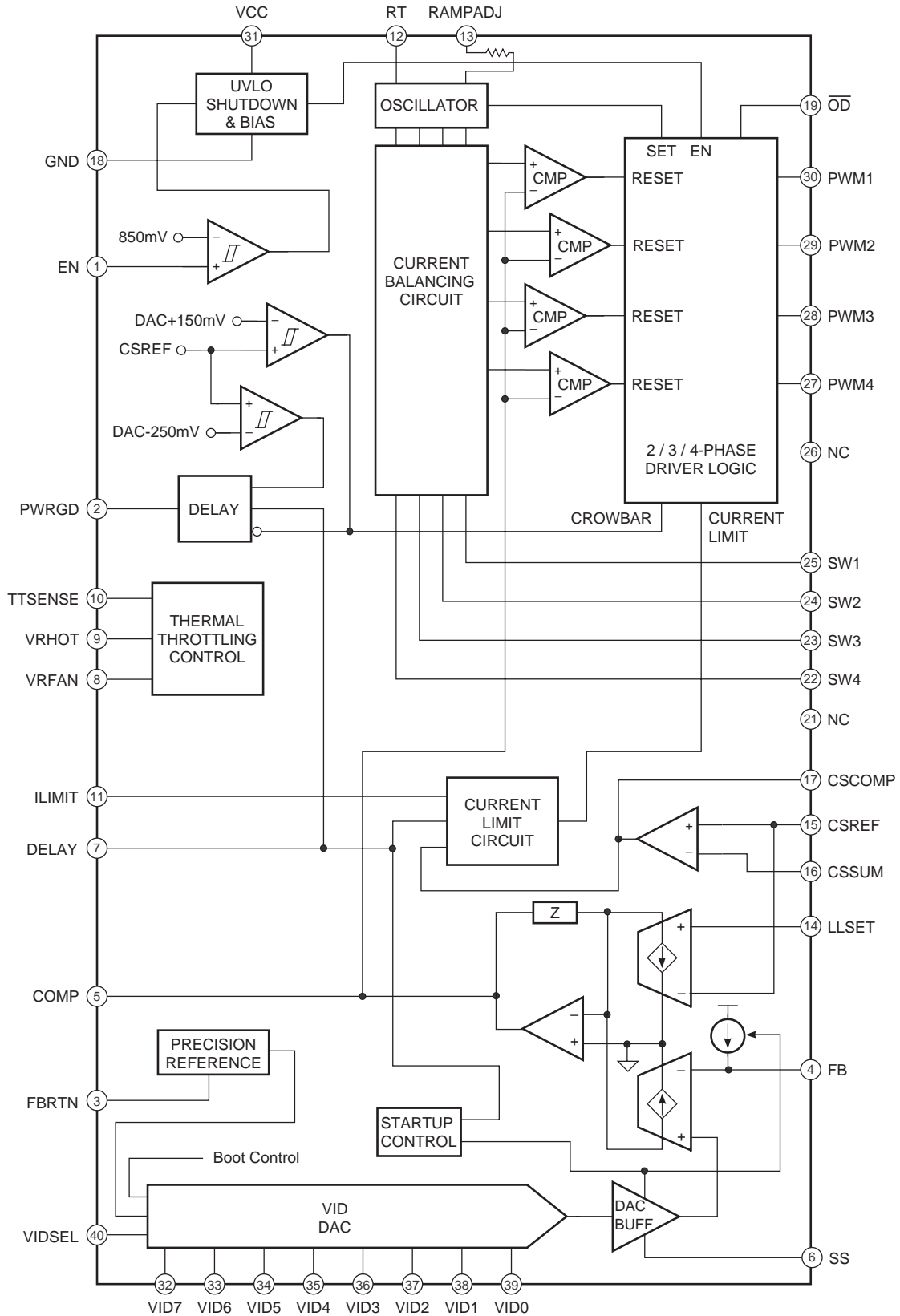


Figure 1. Block Diagram

## FAN5032 Pin Assignment

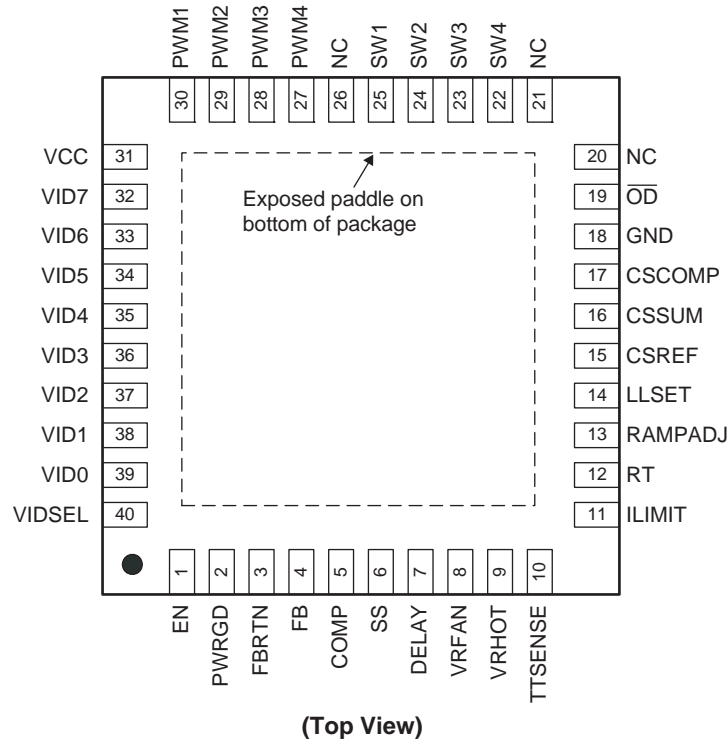


Figure 2. Pin Assignment

## Pin Assignments

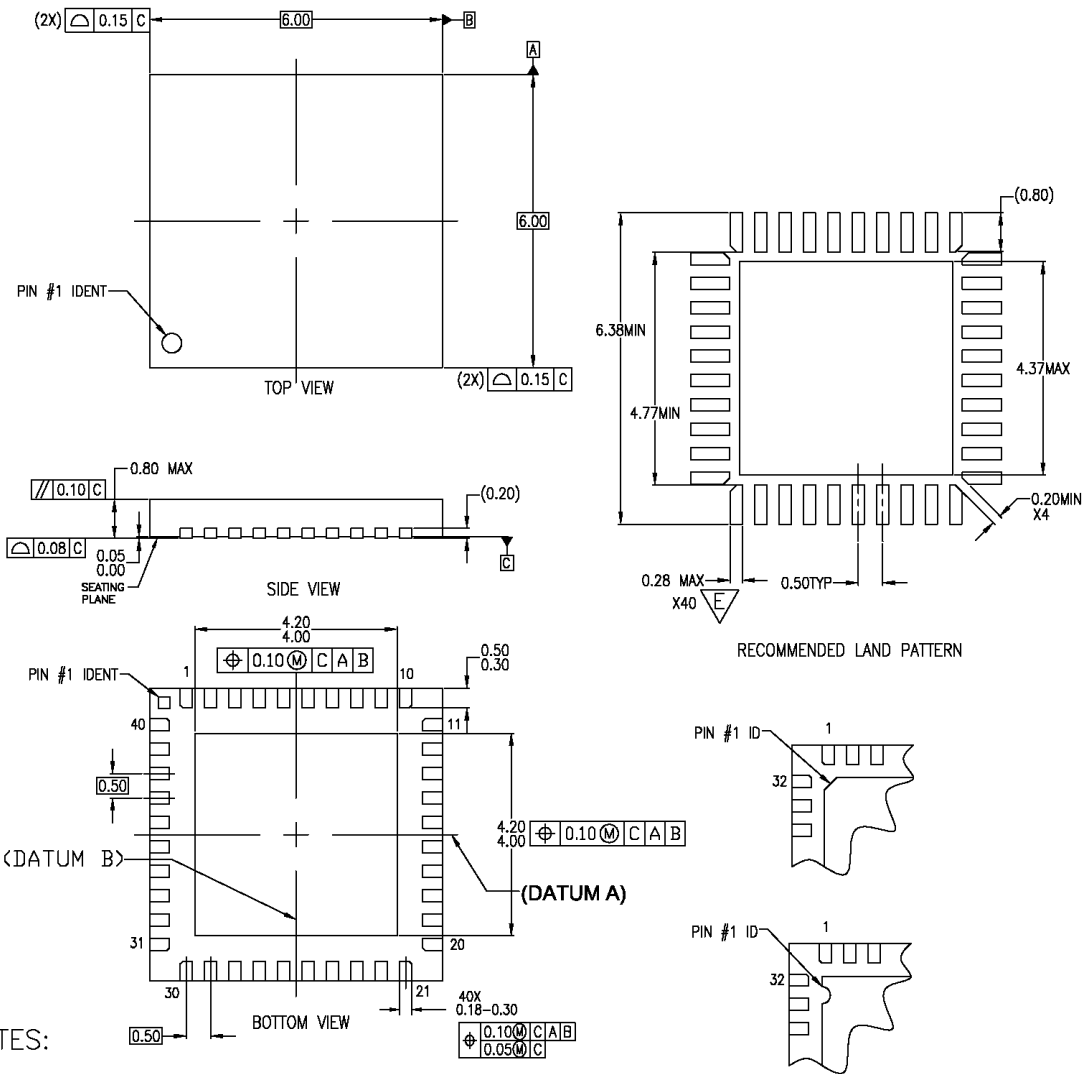
Pin #	Pin Name	Pin Description
1	EN	<b>Power Supply Enable Input.</b> Analog comparator input with hysteresis. If input voltage is higher than the internal threshold, the controller is enabled. If lower, the controller is disabled.
2	PWRGD	<b>Power Good Output.</b> Open drain output that pulls to GND when the output voltage is outside the proper operating range.
3	FBRTN	<b>Feedback Return.</b> VID DAC and error amplifier reference for remote sensing of output voltage.
4	FB	<b>Feedback Input.</b> Error amplifier input for remote sensing of output voltage. A positive internal current source is connected to this pin to allow the output voltage to be offset lower than the DAC voltage.
5	COMP	<b>Error Amplifier Output.</b> For loop compensation.
6	SS	<b>Soft-Start Input.</b> An external capacitor connected between this pin and GND sets the soft-start ramp time.
7	DELAY	<b>Delay Timer Input.</b> An external capacitor connected between this pin and GND sets the over-current latch-off delay time, BOOT voltage hold time, EN delay time, and PWRGD delay time.
8	VRFAN	<b>VR Fan Output.</b> Open drain output that goes high when the TTSENSE voltage goes below the internal VRFAN threshold.

## Pin Assignments (Continued)

Pin #	Pin Name	Pin Description
9	VRHOT	<b>VR Hot Output.</b> Open drain output that goes high when the TTSENSE voltage goes below the internal VRHOT threshold.
10	TTSENSE	<b>Thermal Sense Input.</b> A positive internal current source is connected to this pin. Connecting an external NTC thermistor between this pin and GND produces a positive input voltage that is proportional to temperature.
11	ILIMIT	<b>Current Limit Set.</b> An external resistor from this pin to GND sets the current limit threshold of the converter.
12	RT	<b>Frequency Set Input.</b> An external resistor connected between this pin and GND sets the oscillator frequency of the device.
13	RAMPADJ	<b>PWM Ramp Set Input.</b> An external resistor connected between this pin and the converter input voltage sets the internal PWM ramp.
14	LLSET	<b>Load Line Set Input.</b> This pin can be directly connected to CSCOMP or connected to the center point of a resistor divider between CSCOMP and CSREF. Connecting LLSET to CSREF disables positioning.
15	CSREF	<b>Current Sense Amplifier Positive Input.</b> The voltage on this pin is used as the reference for the current sense amplifier. The power good and crowbar functions are also internally connected to this pin.
16	CSSUM	<b>Current Sense Amplifier Negative Input</b>
17	CSCOMP	<b>Current Sense Amplifier Compensation Output</b>
18	GND	<b>Ground.</b> All internal biasing and logic output signals of the device are referenced to this ground.
19	$\overline{OD}$	<b>Output Disable.</b> This pin is actively pulled low when the EN input is low or when VCC is below its UVLO threshold, to disable the external MOSFET drivers.
20 to 21	NC	<b>No Connection</b>
22 to 25	SW4 to SW1	<b>Switching Node Current Balance Inputs.</b> Sense the switching side of the inductor and are used to measure the current level in each phase. The SW pins of unused phases should be left open.
26	NC	<b>No Connection</b>
27 to 30	PWM4 to PWM1	<b>PWM Outputs.</b> Each output is connected to the input of an external MOSFET driver, such as the FAN5109. Connecting the PWM3 and/or PWM4 outputs to VCC disables that phase, allowing the FAN5032 to operate as a 2, 3, or 4 phase controller.
31	VCC	<b>Supply Voltage for the Device</b>
32 to 39	VID7 to VID0	<b>Voltage Identification Code Inputs.</b> These digital inputs are connected to the internal DAC and are used to program the output voltage. These pins have 1 $\mu$ A internal pull-down; left open, the input state is decoded as logic low.
40	VIDSEL	<b>VID Table Select Input.</b> A logic low selects the extended VR10 DAC table and a logic high selects the VR11 DAC table. This pin has a 1 $\mu$ A internal pull-down; left open, the input state is decoded as logic low.
–	Exposed Paddle	<b>Internally connected to die ground.</b> May be connected to ground or left floating. Connect to ground for lowest package thermal resistance.

## Mechanical Dimensions

### 40-Lead MLP



#### NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WJJD-2 WITH EXCEPTION THIS IS A SAWN VERSION
  - DIMENSIONS ARE IN MILLIMETERS.
  - DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
  - LAND PATTERN PER IPC SM-782 FABRICATION AND ASSEMBLY TOLERANCES OF 0.1 MM APPLIED
- WIDTH REDUCED TO AVOID SOLDER BRIDGING.

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EcoSPARK™	I <sup>2</sup> C™	MSXPro™	RapidConnect™	UHC™
E <sup>2</sup> CMOS™	i-Lo™	OCX™	μSerDes™	UltraFET®
EnSigna™	ImpliedDisconnect™	OCXPro™	ScalarPump™	UniFET™
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## PRODUCT STATUS DEFINITIONS

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