IC for CMOS Regulator+Reset
Monolithic IC MM3018

Outline

This is a reset + regulator composite IC developed using the CMOS process.

The CMOS process is used to achieve ultra-low current consumption, aiming at use in memory cards and portable devices. Further, this exceptional IC can be used even when board mounting space is limited, due to the wafer level package, WLCSP-6.

Features

1. Built-in thermal shutdown circuit
2. Built-in current limit circuit
3. Low current consumption   15µA typ.
4. Series with reset detection voltage in 0.1V steps
5. Delay time from voltage detection to reset release can be set easily.
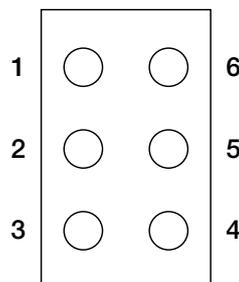
Package

WLCSP-6

Applications

1. Microcomputer, CPU and MPU reset circuit
2. Logic circuit reset circuit
3. Battery voltage check
4. Back-up circuit switching circuit
5. Level detection circuit
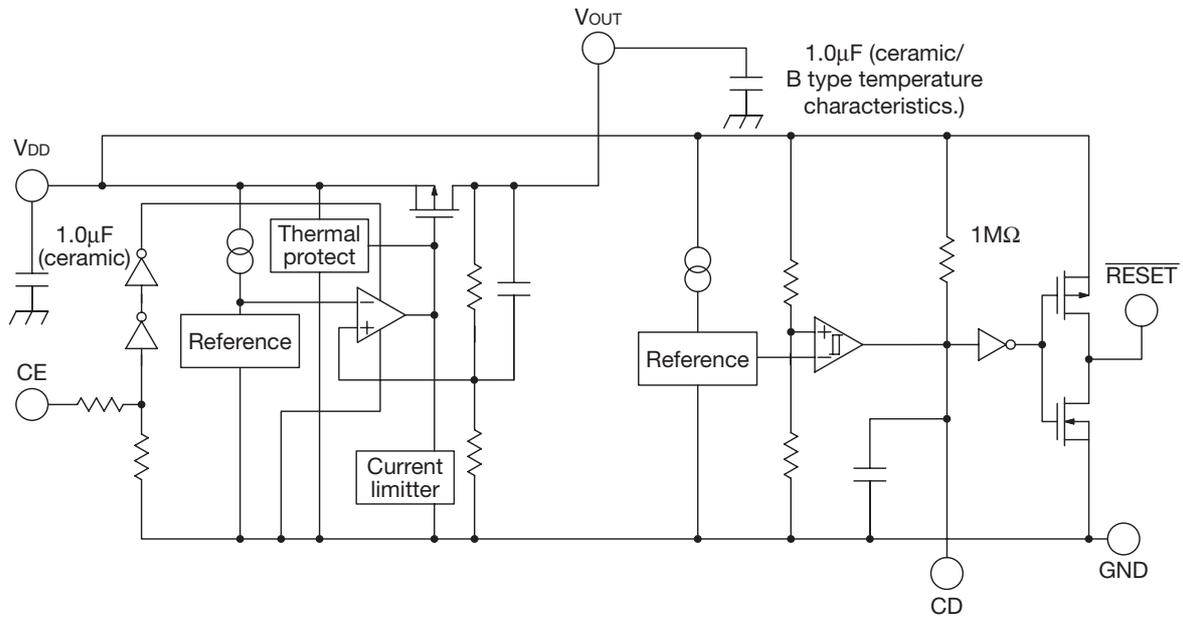6. Mechanical system reset circuit

Pin Assignment

WLCSP-6
(TOP VIEW)

1	V_{DD}
2	CE
3	$\overline{RESET}$
4	CD
5	GND
6	V_{OUT}

Block Diagram

Pin Description

Pin no.	Pin name	Functions
1	V_{DD}	Voltage-supply pin
2	CE	V_{OUT} ON/OFF control pin | CONT	V_{OUT}
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L	OFF
H	ON	 Connect CONT-TERMINAL with V_{DD},When it is not used.
3	$\overline{RESET}$	RESET-output pin $\overline{RESET}$ pin logic |	RESET
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V_{DD}<VS	L
V_{DD}>VS	H	
4	CD	Capacitor connect pin with delay
5	GND	GND pin
6	V_{OUT}	V_{OUT} pin (100mA)

Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	−55~+125	℃
Supply voltage for V_{DD}	V_{DD}	−0.3~+8	V
Supply voltage for CE	V_{CE}	−0.3~V_{DD}+0.3	V
Supply voltage for CD	V_{CD}	−0.3~V_{DD}+0.3	V
Allowable loss	Pd	600*	mW

Note: * With the double Bided PC Board of glass epoxy.
(Copper plane 80%   25✕25✕1.0^t mm)
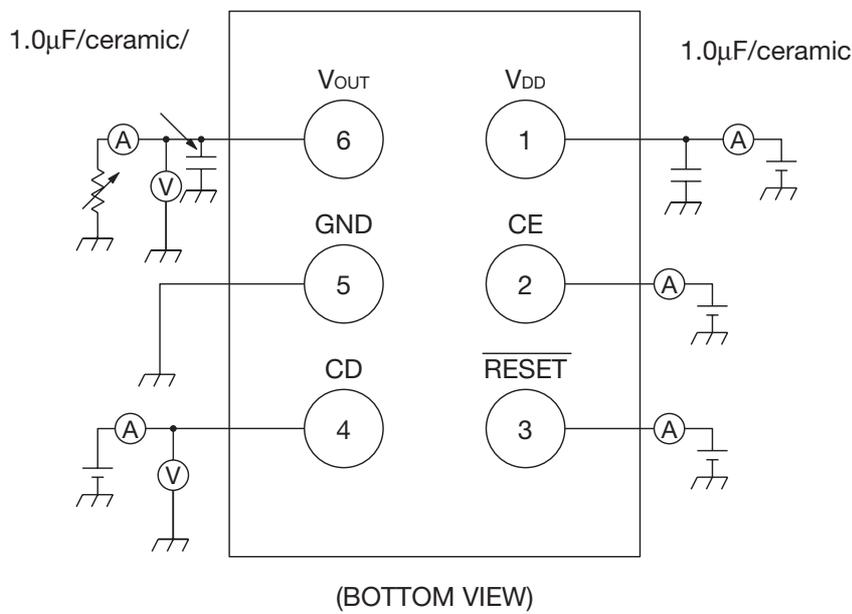
Recommended Operating Conditions (Ta=25℃)

Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}	−40~+85	℃
Operating supply voltage when regulator works	V_{OP-REG}	2.5~3.6	V
Operating supply voltage when reset works	V_{OP-RES}	0.7~3.6	V
Output current	I_{OUT}	100	mA

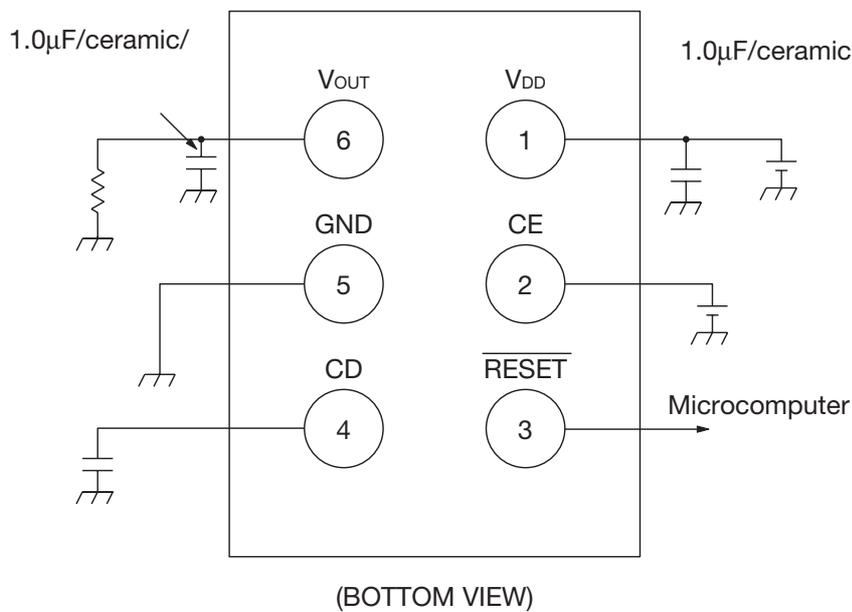# Electrical Characteristics (Except where noted otherwise, Ta=25℃, CE=3.6V) (Represent model MM3018A)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Current consumption						
V_{IN} input current 1	I_{ccq1}	V_{DD}=3.6V, I_{OUT}=0mA		15	30	μA
Input current when regulator is OFF	I_{ccq2}	V_{DD}=3.6V, I_{OUT}=0mA, CE=0.5V		2	5	μA
Input current when reset works	I_{ccq3}	V_{DD}=CE=2.2V, I_{OUT}=0mA		18	35	μA
Regulator						
Output Voltage 1	$V_{OUT}1$	V_{DD}=3.6V, I_{OUT}=50mA	1.764	1.8	1.836	V
Drop voltage	V_{IO}	V_{DD}=1.7V, I_{OUT}=50mA		120	250	mV
Line regulation	△V1	V_{DD}=2.5~3.6V, I_{OUT}=50mA		10	30	mV
Load regulation	△V2	V_{DD}=3.6V, I_{OUT}=0~100mA		30	90	mV
V_{OUT} temperature coefficient *	$△V_{OUT}/△T$	Tj=−40~+85℃		±100		ppm/℃
CE terminal current	I_{ON}	V_{DD}=3.6V		0.5	1.0	μA
High threshold voltage	H		V_{DD}-0.5		V_{DD}	V
Low threshold voltage	L	V_{DD}=2.7V			0.5	V
V_{DD} reset						
Detecting voltage	V_S	V_{DD}=H→L	2.254	2.3	2.346	V
Vs temperature coefficient *	$△V_S/△T$	Tj=−40~+85℃, V_{DD}=H→L		±100		ppm/℃
Hysteresis voltage	$△V_S$	V_{DD}=H→L→H	69	115	161	mV
Output current 1	$I_{OUT}1$	Nch V_{DS}=0.05V, V_{DD}=0.7V	0.01	0.05		mA
Output current 2	$I_{OUT}2$	Nch V_{DS}=0.5V, V_{DD}=1.5V	1	2		mA
Output current 3	$I_{OUT}3$	Pch V_{DS}=−2.1V, V_{DD}=3.6V	1	2		mA
CD pin threshold voltage	V_{TCD}	V_{DD}=2.53V	1.012	1.265	1.518	V
CD pin resistance	RD		0.7	1.0	1.3	MΩ
CD pin resistance temperature coefficient *	RD	Tj=−40~+85℃		−4500		ppm/℃
Threshold operating voltage	V_{OPL}	V_{DS} ≦ 0.1V			0.7	V

Note: * design guaranteed

Measuring Circuit

1.0μF/ceramic/

1.0μF/ceramic

V_{OUT}
6

V_{DD}
1

GND
5

CE
2

CD
4

$\overline{RESET}$
3

(BOTTOM VIEW)

Application Circuit

1.0μF/ceramic/

1.0μF/ceramic

V_{OUT}
6

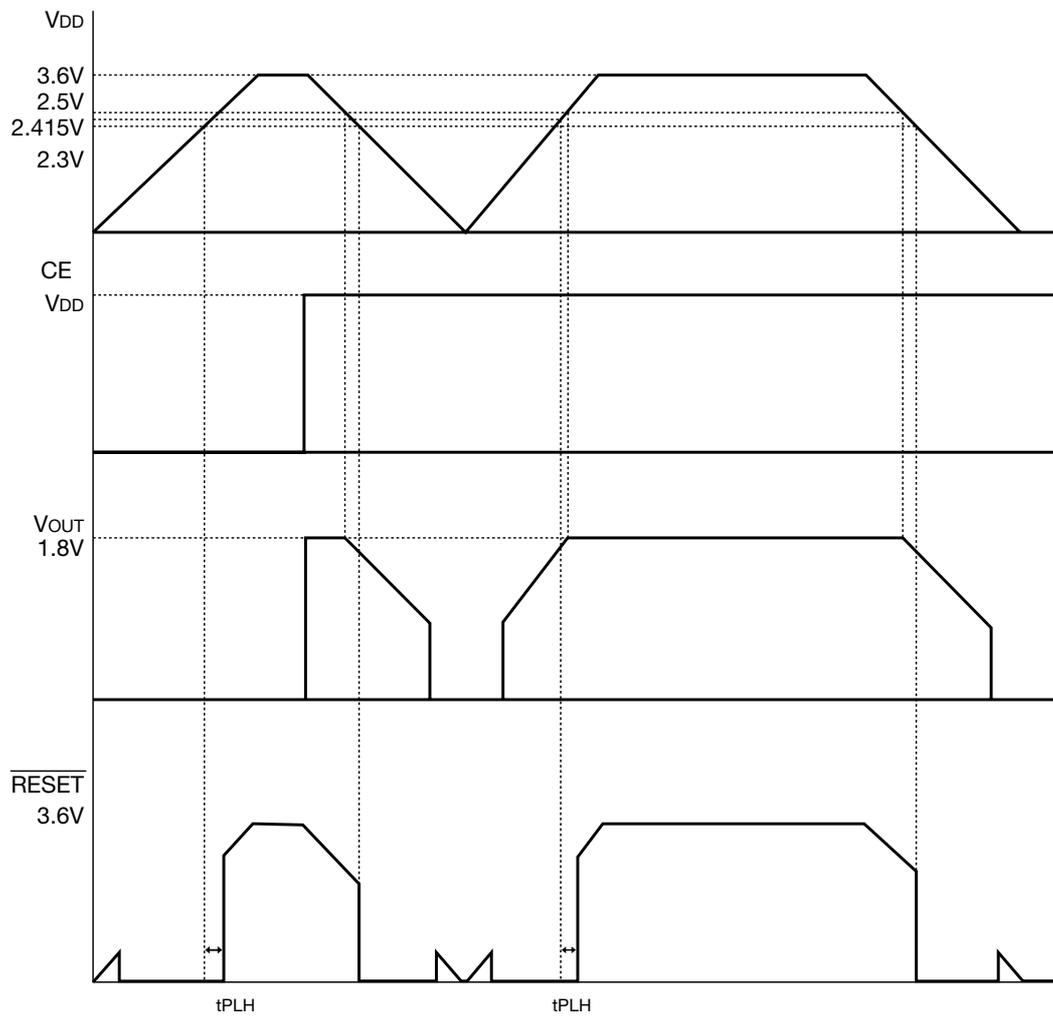V_{DD}
1

GND
5

CE
2

CD
4

$\overline{RESET}$
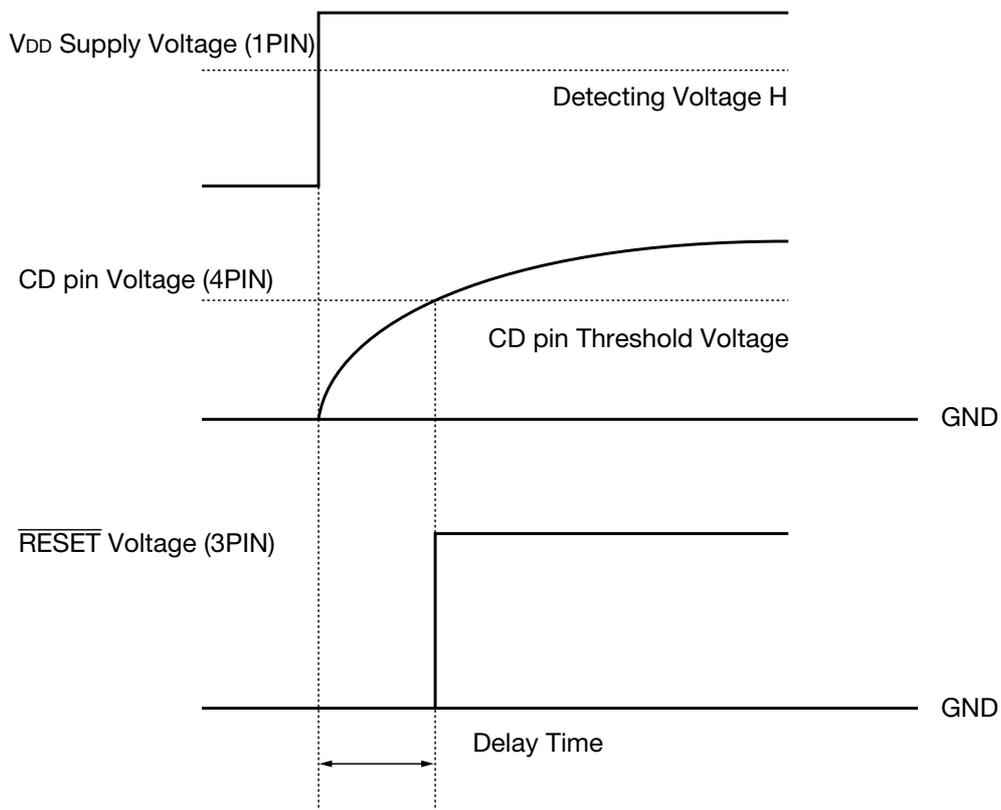3

Microcomputer

(BOTTOM VIEW)

Note

1. An output-capacitor recommended the capacitor with more than 1.0μF and B type temperature characteristics.
2. The wire of V_{DD} and GND is required to print full ground plane for noise and stability.
3. The input capacitor must be connected a distance of less than 1cm from input pin.
4. In case the output voltage is above the input voltage, the overcurrent flow by internal parasitic diode from output to input.

Timing Chart

Delay Time

VDD Supply Voltage (1PIN)

Detecting Voltage H

CD pin Voltage (4PIN)

CD pin Threshold Voltage

GND

$\overline{\text{RESET}}$ Voltage (3PIN)

GND

Delay Time

Delay Time (tPLH) $t_{PLH} \fallingdotseq 0.77 \times RD\ (\Omega) \times CD\ (F)$

RD: CD pin resistance
CD: Outer capacitor

■ Outer Capacitor Vs Delay Time

RD=920kΩ

Delay Time (ms) vs Outer Capacitor (pF)
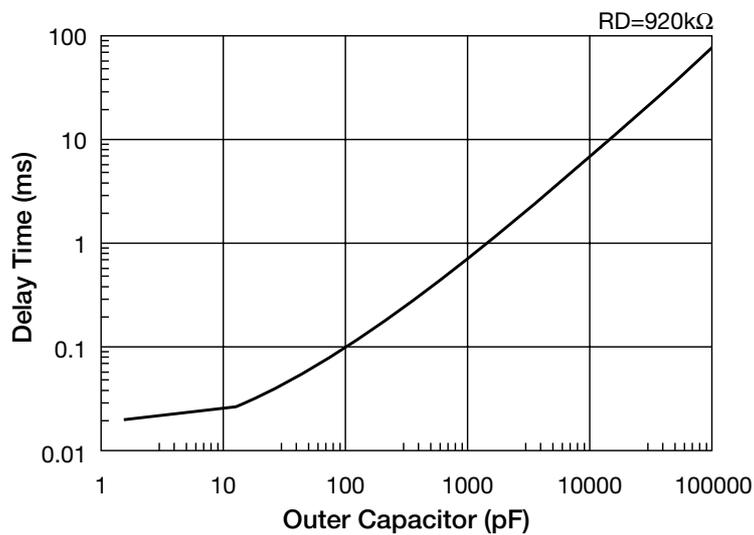
note: These are typical characteristics.

Characteristics (Except where noted otherwise, Ta=25°C, VDD=3.6V, VCE=VDD, CIN=1.0μF, CO=1.0μF) (Represent model MM3018A)

■ Output Voltage
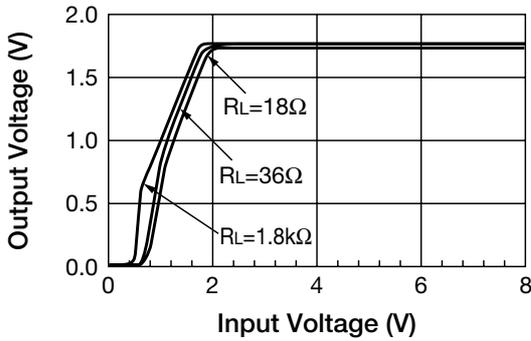
■ Detecting Voltage
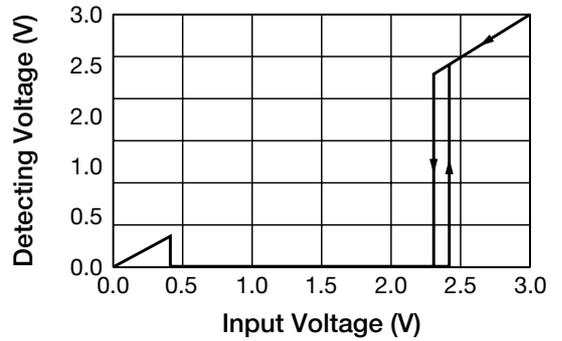
■ No-Load Input Current
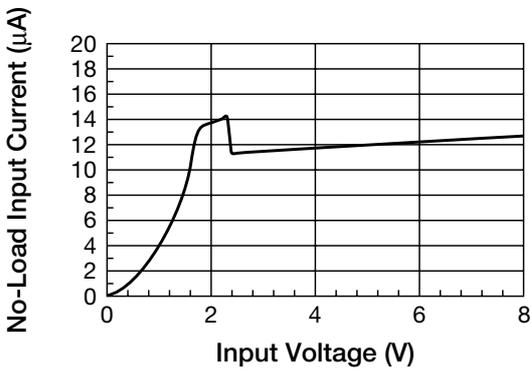
■ Dropout Voltage
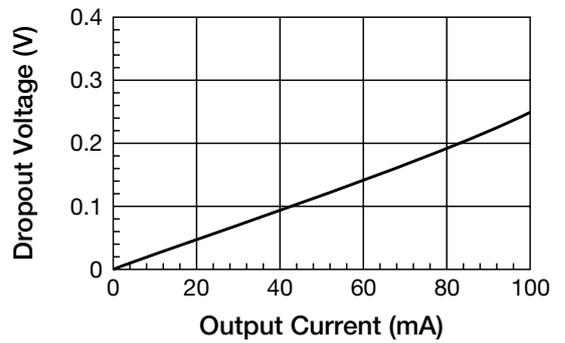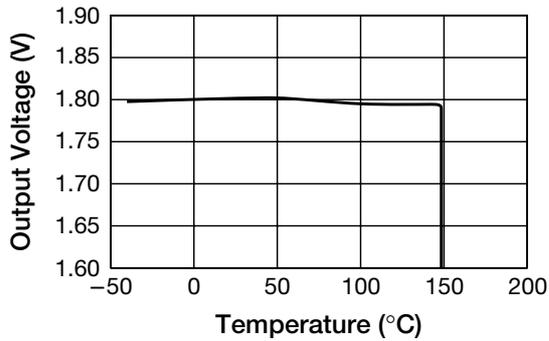
■ Load Regulation
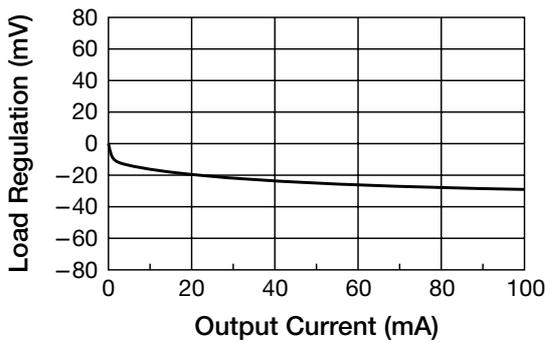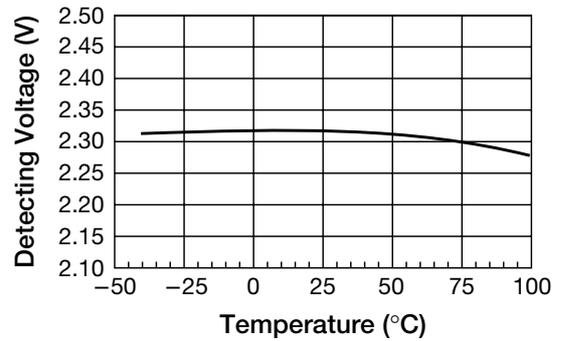
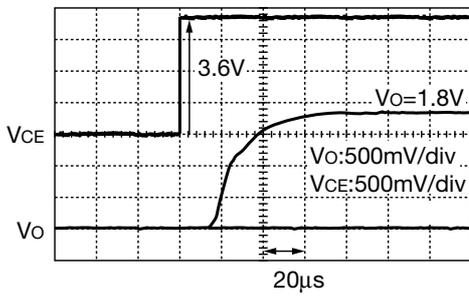### ■ Line Regulation
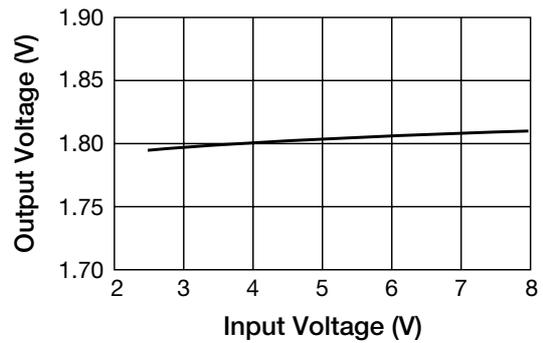
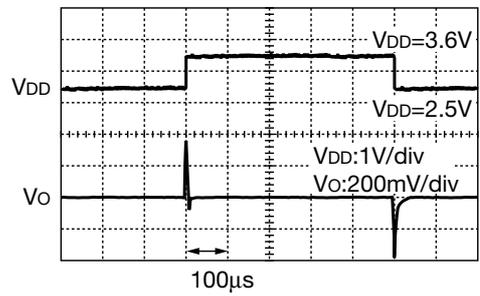### ■ Current Limit
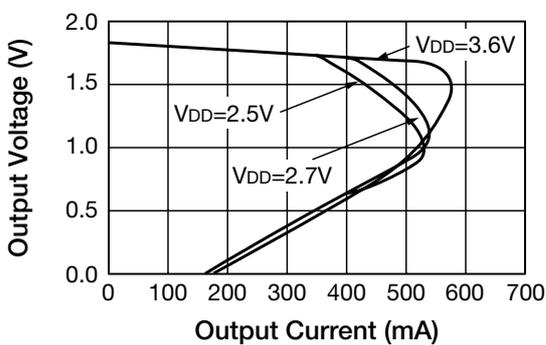
■ Ripple rejection
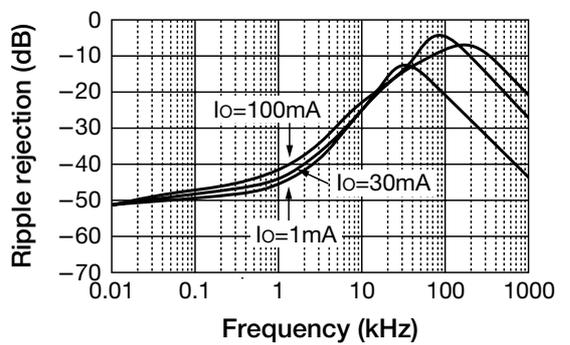
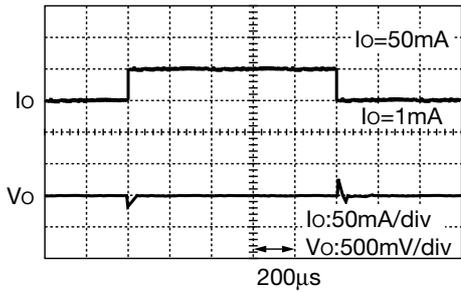■ Temperature - Output Voltage

■ Temperature - Detecting Voltage

■ Regulator rise (VDD=3.6V, VCE=0→2.0V, Io=50mA)
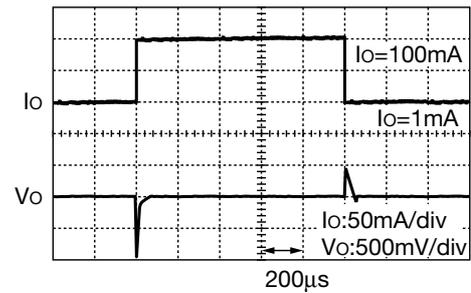

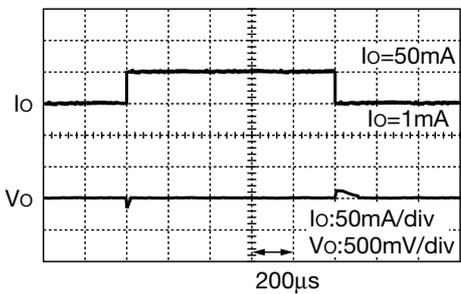■ Input transient response (VDD=2.5V→3.6V, Io=50mA, Co=0.1μF)

■ Load transient response (Io=1mA→50mA, Co=0.1μF)

■ Load transient response (Io=1mA→100mA, Co=0.1μF)

■ Load transient response (Io=1mA→50mA, Co=1.0μF)

■ Load transient response (Io=1mA→100mA, Co=1.0μF)