3-Input 2-Output 3-Circuit Video Switch
Monolithic IC MM1238

July 5, 1993

Outline

This IC is a video switch IC developed for high-end large/medium TVs incorporating three 3-input 2-output circuits. It is ideal for switching BS/JSB/CS or M-N converters (mute to NTSC conversion). The BS-CS decoder can be used as a W decoder.

Features

1. One of the two video signal outputs is used for external output, and has a 6dB amp, 75Ω, 1V_{P-P}
2. Input impedance
   - 1~3 video circuits 15kΩ
   - 1~3 audio circuits 68kΩ
3. Crosstalk
   - Video −60dB (at 4.43MHz)
   - Audio −80dB (at 1kHz)
   - Video : Audio −70dB (at 100kHz)
4. Frequency response 10MHz (6dB, 75Ω, amp only, 7MHz)
5. Supply voltage 8.0~13.0V

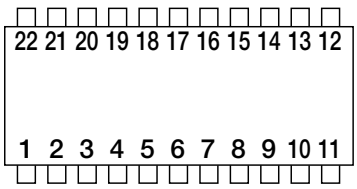
Package

SDIP-22A (MM1238XD)

Applications

1. TV
2. Free-standing VCR
3. Other video equipment

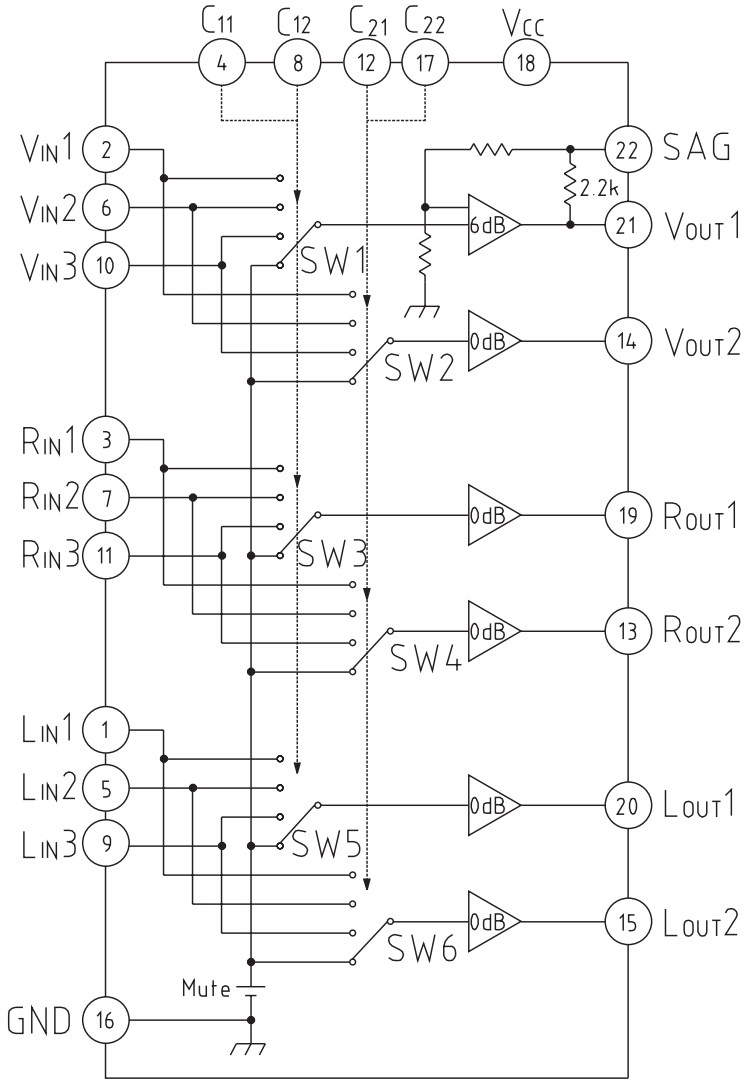
Pin Assignment



SDIP-22P

Pin no.	Pin name	Function	Pin no.	Pin name	Function
1	$L_{IN}1$	Audio $L_{IN}1$	12	C21	SW2 control
2	$V_{IN}1$	Video IN1	13	$R_{OUT}2$	Audio $R_{OUT}2$
3	$R_{IN}1$	Audio $R_{IN}1$	14	$V_{OUT}2$	Video OUT2
4	C11	SW1 control	15	$L_{OUT}2$	Audio $L_{OUT}2$
5	$L_{IN}2$	Audio $L_{IN}2$	16	GND	GND
6	$V_{IN}2$	Video IN2	17	C22	SW2 control
7	$R_{IN}2$	Audio $R_{IN}2$	18	V_{CC}	Power supply
8	C12	SW1 control	19	$R_{OUT}1$	Audio $R_{OUT}1$
9	$L_{IN}3$	Audio $L_{IN}3$	20	$L_{OUT}1$	Audio $L_{OUT}1$
10	$V_{IN}3$	Video IN3	21	$V_{OUT}1$	Video OUT1
11	$R_{IN}3$	Audio $R_{IN}3$	22	SAG	Sag pin

Block Diagram



SW Logic

Control input		Output signal		
C11	C12	VOUT1	ROUT1	LOUT1
L	L	Mute	Mute	Mute
L	H	VIn1	RIn1	LIn1
H	L	VIn2	RIn2	LIn2
H	H	VIn3	RIn3	LIn3

Control input		Output signal		
C21	C22	VOUT2	ROUT2	LOUT2
L	L	Mute	Mute	Mute
L	H	VIn1	RIn1	LIn1
H	L	VIn2	RIn2	LIn2
H	H	VIn3	RIn3	LIn3

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	TSTG	–40~+125	°C
Operating temperature	TOPR	–20~+75	°C
Power supply voltage	Vcc	15	V
Allowable loss	Pd	800	mW

Electrical Characteristics (Except where noted otherwise, Ta=25°C, V_{CC}= 8V~13V)

Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units
Operating power supply voltage	V_{CC}	V_{CC}		8.0		13.0	V
Consumption current	$I_{CC}1$		V_{CC}=9V		22.0	29.0	mA
	$I_{CC}2$		V_{CC}=12V		25.0	33.0	mA
$V_{OUT}1$ output							
Voltage gain	G_V1	TP7	SG2 : Sine wave 1V_{P-P}, 0.1MHz	5.7	6.2	6.7	dB
Frequency characteristic	F_V1	TP7	SG2 : Sweep signal 1V_{P-P} 7MHz/0.1MHz	−1.0	0	1.0	dB
Differential gain	DG1	TP8	SG2 : Staircase wave 1V_{P-P} APL=10, 50, 90%		0	3	%
Differential phase	DP1	TP8	SG2 : Staircase wave 1V_{P-P} APL=10, 50, 90%		0	3	deg
$R_{OUT}1$ output							
Voltage gain	G_R1	TP5	SG3 : Sine wave 2.5V_{P-P}, 1kHz	−0.5	0	0.5	dB
Total harmonic distortion	THD_R1	TP5	SG3 : Sine wave 2.5V_{P-P}, 1kHz		0.01	0.1	%
Mute noise	$V_{NM}1$	TP5	15kHz band during mute select		180		µVrms
Output noise voltage	$V_{NR}1$	TP5	15kHz band during pin select		3	50	µVrms
$L_{OUT}1$ output							
Voltage gain	G_L1	TP6	SG1 : Sine wave 2.5V_{P-P}, 1kHz	−0.5	0	0.5	dB
Total harmonic distortion	THD_L1	TP6	SG1 : Sine wave 2.5V_{P-P}, 1kHz		0.01	0.1	%
Mute noise	$V_{NM}2$	TP6	15kHz band during mute select		180		µVrms
Output noise voltage	$V_{NL}1$	TP6	15kHz band during pin select		3	50	µVrms
$V_{OUT}2$ output							
Voltage gain	Gv2	TP2	SG2 : Sine wave 1V_{P-P}, 0.1MHz	−0.5	0	0.5	dB
Frequency characteristic	Fv2	TP2	SG2 : Sweep signal 1V_{P-P} 10MHz/0.1MHz	−1.0	0	1.0	dB
Differential gain	DG2	TP3	SG2 : Staircase wave 1V_{P-P} APL=10, 50, 90%		0	3	%
Differential phase	DP2	TP3	SG2 : Staircase wave 1V_{P-P} APL=10, 50, 90%		0	3	deg
$R_{OUT}2$ output							
Voltage gain	G_R2	TP1	SG3 : Sine wave 2.5V_{P-P}, 1kHz	−0.5	0	0.5	dB
Total harmonic distortion	THD_R2	TP1	SG3 : Sine wave 2.5V_{P-P}, 1kHz		0.01	0.1	%
Mute noise	$V_{NM}3$	TP1	15kHz band during mute select		180		µVrms
Output noise voltage	$V_{NR}2$	TP1	15kHz band during pin select		3	50	µVrms
$L_{OUT}2$ output							
Voltage gain	G_L2	TP4	SG1 : Sine wave 2.5V_{P-P}, 1kHz	−0.5	0	0.5	dB
Total harmonic distortion	THD_L2	TP4	SG1 : Sine wave 2.5V_{P-P}, 1kHz		0.01	0.1	%
Mute noise	$V_{NM}4$	TP4	15kHz band during mute select		180		µVrms
Output noise voltage	$V_{NR}2$	TP4	15kHz band during pin select		3	50	µVrms
Output offset voltage							
$V_{OUT}1$	$V_{OFF}1$	TP7	$V_{OUT}1$ pin DC level difference during switching		0	±30	mV
$V_{OUT}2$	$V_{OFF}2$	TP2	$V_{OUT}2$ pin DC level difference during switching		0	±15	mV
$R_{OUT}1$	$V_{OFF}3$	TP5	$R_{OUT}1$ pin DC level difference during switching		0	±15	mV
$R_{OUT}2$	$V_{OFF}4$	TP1	$R_{OUT}2$ pin DC level difference during switching		0	±15	mV
$L_{OUT}1$	$V_{OFF}5$	TP6	$L_{OUT}1$ pin DC level difference during switching		0	±15	mV
$L_{OUT}2$	$V_{OFF}6$	TP4	$L_{OUT}2$ pin DC level difference during switching		0	±15	mV

Input impedance							
V_{IN}	R_{IV}		$V_{IN}1$~$V_{IN}3$		15		kΩ
R_{IN}	R_{IR}		$R_{IN}1$~$R_{IN}3$		68		kΩ
L_{IN}	R_{IL}		$L_{IN}1$~$L_{IN}3$		68		kΩ
Output impedance							
V_{OUT}	V_{OV}		$V_{OUT}2$		50		Ω
R_{OUT}	V_{OR}		$R_{OUT}1$ and $R_{OUT}2$		50		Ω
L_{OUT}	V_{OL}		$L_{OUT}1$ and $L_{OUT}2$		50		Ω
Crosstalk							
V_{IN}→V_{OUT}	CT_{VV}		SG2 : $1V_{P-P}$, 4.43MHz ∗1		–60	–50	dB
R_{IN}→R_{OUT}	CT_{RR}		SG3 : $2.5V_{P-P}$, 1kHz ∗2		–80	–70	dB
L_{IN}→L_{OUT}	CT_{LL}		SG1 : $2.5V_{P-P}$, 1kHz ∗3		–80	–70	dB
V_{IN}→R_{OUT}	CT_{RV}		SG2 : $1V_{P-P}$, 100kHz ∗4		–70	–60	dB
V_{IN}→L_{OUT}	CT_{LV}		SG2 : $1V_{P-P}$, 100kHz ∗5		–70	–60	dB
Switch input voltage							
SW input voltage H	V_{IH}		Switching H level for each IC SW	2.1			V
SW input voltage L	V_{IL}		Switching L level for each IC SW			0.7	V
Input dynamic range							
V_{IN}→V_{OUT}	D1		V_{CC}=12V, SG1 : sine wave, 1kHz	2.6			V_{P-P}
R_{IN}→R_{OUT}	D2		V_{CC}=12V, SG2 : sine wave, 1kHz Total higher harmonic distortion=0.5%	2.0			Vrms
L_{IN}→L_{OUT}	D3		V_{CC}=12V, SG3 : sine wave, 1kHz Total higher harmonic distortion=0.5%	2.0			Vrms

∗1 Crosstalk (V_{IN}→V_{OUT})

Input a $1V_{P-P}$, 4.43MHz sine wave to SG2.

Obtain CT_{VV} using the following formula given output amplitude for combinations other than those below for SW control pin as V_O1, and for the combinations below as V_O2.

$$CT_{VV}=20\times\log(V_O2/V_O1)\ dB$$

1. $CT_{VV}1$

Measuring pin	Switch status				
	S2	V1	V2	V3	V4
TP8	A	L	L	L	H
	A	H	L	L	H
	A	H	H	L	H
	B	L	L	H	L
	B	L	H	H	L
	B	H	H	H	L
	C	L	L	H	H
	C	L	H	H	H
	C	H	L	H	H

2. $CT_{VV}2$

Measuring pin	Switch status				
	S2	V1	V2	V3	V4
TP3	A	L	H	L	L
	A	L	H	H	L
	A	L	H	H	H
	B	H	L	L	L
	B	H	L	L	H
	B	H	L	H	H
	C	H	H	L	L
	C	H	H	L	H
	C	H	H	H	L

*2 Crosstalk ($R_{IN} \rightarrow R_{OUT}$)

Input a 2.5V_{P-P}, 1kHz sine wave to SG3.

Obtain C_{TRR} using the following formula given output amplitude for combinations other than those below for SW control pin as V_O3, and for the combinations below as V_O4.

$$C_{TRR}=20 \times \log (V_O4/V_O3)\ dB$$

1. $C_{TRR}1$

Measuring pin	Switch status				
	S3	V1	V2	V3	V4
TP5	A	L	L	L	H
	A	H	L	L	H
	A	H	H	L	H
	B	L	L	H	L
	B	L	H	H	L
	B	H	H	H	L
	C	L	L	H	H
	C	L	H	H	H
	C	H	L	H	H

2. $C_{TRR}2$

Measuring pin	Switch status				
	S3	V1	V2	V3	V4
TP1	A	L	H	L	L
	A	L	H	H	L
	A	L	H	H	H
	B	H	L	L	L
	B	H	L	L	H
	B	H	L	H	H
	C	H	H	L	L
	C	H	H	L	H
	C	H	H	H	L

*3 Crosstalk ($L_{IN} \rightarrow L_{OUT}$)

Input a 2.5V_{P-P}, 1kHz sine wave to SG3.

Obtain C_{TLL} using the following formula given output amplitude for combinations other than those below for SW control pin as V_O5, and for the combinations below as V_O6.

$$C_{TLL}=20 \times \log (V_O6/V_O5)\ dB$$

1. $C_{TLL}1$

Measuring pin	Switch status				
	S1	V1	V2	V3	V4
TP6	A	L	L	L	H
	A	H	L	L	H
	A	H	H	L	H
	B	L	L	H	L
	B	L	H	H	L
	B	H	H	H	L
	C	L	L	H	H
	C	L	H	H	H
	C	H	L	H	H

2. $C_{TLL}2$

Measuring pin	Switch status				
	S1	V1	V2	V3	V4
TP4	A	L	H	L	L
	A	L	H	H	L
	A	L	H	H	H
	B	H	L	L	L
	B	H	L	L	H
	B	H	L	H	H
	C	H	H	L	L
	C	H	H	L	H
	C	H	H	H	L

*4 Crosstalk (V_{IN}-R_{OUT}, L_{OUT})

Input a 1Vp-p, 100kHz sine wave to SG2.

Obtain C_{TRV} (C_{TLV}) using the following formula given output amplitude for combinations other than those below for SW control pin as V_O7, and for the combinations below as V_O8.

$$C_{TRV}\,(C_{TLV}) = 20 \times \log (V_O8/V_O7)\ \text{dB}$$

1. C_{TRV}

Measuring pin	Switch status				
	S2	V1	V2	V3	V4
TP5	A	L	H	L	H
	B	H	L	H	L
	C	H	H	H	H
TP1	A	L	H	L	H
	B	H	L	H	L
	C	H	H	H	H

2. C_{TLV}

Measuring pin	Switch status				
	S2	V1	V2	V3	V4
TP6	A	L	H	L	H
	B	H	L	H	L
	C	H	H	H	H
TP4	A	L	H	L	H
	B	H	L	H	L
	C	H	H	H	H

Measuring Circuit