



# 512MB - 64Mx64 DDR SDRAM UNBUFFERED w/PLL

## FEATURES

- Double-data-rate architecture
- Speeds of 100MHz, 133MHz and 166MHz
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh
- Serial presence detect
- Power supply:  $V_{CC}$ : 2.5V  $\pm$  0.2V
- JEDEC standard 200 pin SO-DIMM package
  - Package height options:
    - AD4: 35.5 mm (1.38"),
    - BD4: 31.75 (1.25")

## DESCRIPTION

The W3EG6464S is a 64Mx64 Double Data Rate SDRAM memory module based on 512Mb DDR SDRAM component. The module consists of eight 64Mx8 DDR SDRAMs in 66 pin TSOP packages mounted on a 200 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

\* This product is under development, is not qualified or characterized and is subject to change without notice.

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## OPERATING FREQUENCIES

	DDR333@CL=2.5	DDR266@CL=2	DDR266@CL=2.5	DDR200@CL=2
Clock Speed	166MHz	133MHz	133MHz	100MHz
CL-tRCD-tRP	2.5-3-3	2-2-2	2.5-3-3	2-2-2

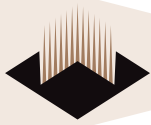


### PIN CONFIGURATION

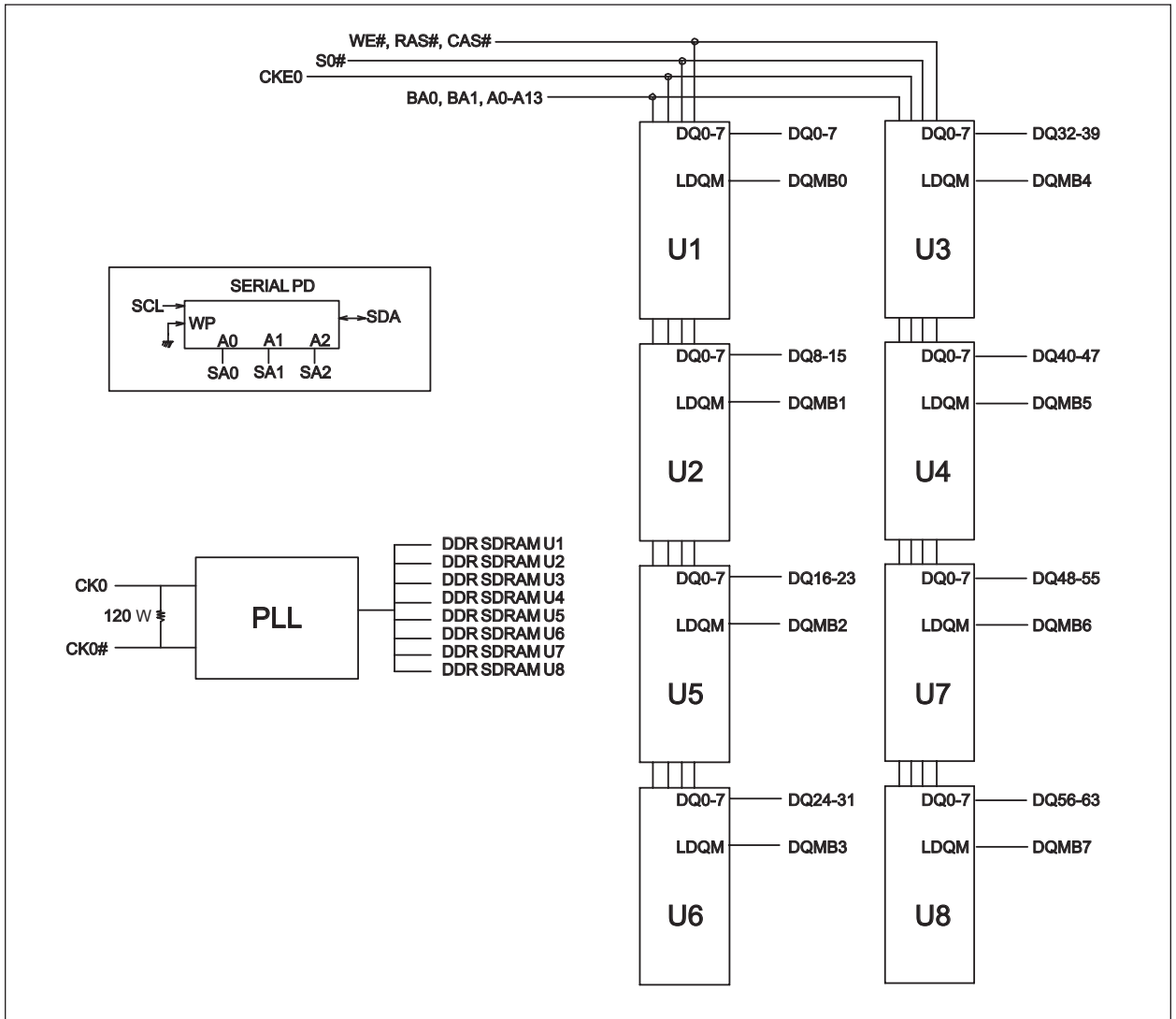
PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	VREF	51	Vss	101	A9	151	DQ42
2	VREF	52	Vss	102	A8	152	DQ46
3	Vss	53	DQ19	103	Vss	153	DQ43
4	Vss	54	DQ23	104	Vss	154	DQ47
5	DQ0	55	DQ24	105	A7	155	Vcc
6	DQ4	56	DQ28	106	A6	156	Vcc
7	DQ1	57	Vcc	107	A5	157	Vcc
8	DQ5	58	Vcc	108	A4	158	NC
9	Vcc	59	DQ25	109	A3	159	Vss
10	Vcc	60	DQ29	110	A2	160	NC
11	DQS0	61	DQS3	111	A1	161	Vss
12	DM0	62	DM3	112	A0	162	Vss
13	DQ2	63	Vss	113	Vcc	163	DQ48
14	DQ6	64	Vss	114	Vcc	164	DQ52
15	Vss	65	DQ26	115	A10/AP	165	DQ49
16	Vss	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	Vcc
18	DQ7	68	DQ31	118	RAS#	168	Vcc
19	DQ8	69	Vcc	119	WE#	169	DQS6
20	DQ12	70	Vcc	120	CAS#	170	DM6
21	Vcc	71	NC	121	CS0	171	DQ50
22	Vcc	72	NC	122	NC	172	DQ54
23	DQ9	73	NC	123	NC	173	Vss
24	DQ13	74	NC	124	NC	174	Vss
25	DQS1	75	Vss	125	Vss	175	DQ51
26	DM1	76	Vss	126	Vss	176	DQ55
27	Vss	77	DQS8	127	DQ32	177	DQ56
28	Vss	78	DM8	128	DQ36	178	DQ60
29	DQ10	79	NC	129	DQ33	179	Vcc
30	DQ14	80	NC	130	DQ37	180	Vcc
31	DQ11	81	Vcc	131	Vcc	181	DQ57
32	DQ15	82	Vcc	132	Vcc	182	DQ61
33	Vcc	83	NC	133	DQS4	183	DQS7
34	Vcc	84	NC	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	Vss
36	Vcc	86	NC	136	DQ38	186	Vss
37	CK0#	87	Vss	137	Vss	187	DQ58
38	Vss	88	Vss	138	Vss	188	DQ62
39	Vss	89	NC	139	DQ35	189	DQ59
40	Vss	90	Vss	140	DQ39	190	DQ63
41	DQ16	91	NC	141	DQ40	191	Vcc
42	DQ20	92	Vcc	142	DQ44	192	Vcc
43	DQ17	93	Vcc	143	Vcc	193	SDA
44	DQ21	94	Vcc	144	Vcc	194	SA0
45	Vcc	95	NC	145	DQ41	195	SCL
46	Vcc	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	VCCSPD
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	Vss	199	VCCID
50	DQ22	100	A11	150	Vss	200	NC

### PIN NAMES

A0-A12	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
DQS0-DQS8	Data Strobe Input/Output
CK0	Clock Input
CK0#	Clock Input
CKE0	Clock Enable input
CS0#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-DQM8	Data-In Mask
Vcc	Power Supply (2.5V)
VCCQ	Power Supply for DQS (2.5V)
Vss	Ground
VREF	Power Supply for Reference
VCCSPD	Serial EEPROM Power Supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
VCCID	Vcc Identification Flag
NC	No Connect



FUNCTIONAL BLOCK DIAGRAM





### ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V <sub>ss</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 3.6	V
Voltage on V <sub>CC</sub> supply relative to V <sub>ss</sub>	V <sub>CC</sub> , V <sub>CCQ</sub>	-1.0 to 3.6	V
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C
Power Dissipation	P <sub>D</sub>	8	W
Short Circuit Current	I <sub>OS</sub>	50	mA

Note:

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.  
 Functional operation should be restricted to recommended operating condition.  
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

### DC CHARACTERISTICS

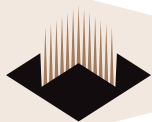
0°C ≤ T<sub>A</sub> ≤ 70°C, V<sub>CC</sub> = 2.5V ± 0.2V

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	2.3	2.7	V
Supply Voltage	V <sub>CCQ</sub>	2.3	2.7	V
Reference Voltage	V <sub>REF</sub>	V <sub>CCQ</sub> /2 - 50mV	V <sub>CCQ</sub> /2 + 50mV	V
Termination Voltage	V <sub>TT</sub>	V <sub>REF</sub> - 0.04	V <sub>REF</sub> + 0.04	V
Input High Voltage	V <sub>IH</sub>	V <sub>REF</sub> + 0.15	V <sub>CCQ</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	V <sub>REF</sub> - 0.15	V
Output High Voltage	V <sub>OH</sub>	V <sub>TT</sub> + 0.76	—	V
Output Low Voltage	V <sub>OL</sub>	—	V <sub>TT</sub> - 0.76	V

### CAPACITANCE

T<sub>A</sub> = 25°C, f = 1MHz, V<sub>CC</sub> = 3.3V, V<sub>REF</sub> = 1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C <sub>IN1</sub>	26	pF
Input Capacitance (RAS#, CAS#, WE#)	C <sub>IN2</sub>	26	pF
Input Capacitance (CKE0)	C <sub>IN3</sub>	26	pF
Input Capacitance (CK0,CK0#)	C <sub>IN4</sub>	5.5	pF
Input Capacitance (CS0#)	C <sub>IN5</sub>	26	pF
Input Capacitance (DQM0-DQM8)	C <sub>IN6</sub>	8	pF
Input Capacitance (BA0-BA1)	C <sub>IN7</sub>	26	pF
Data input/output capacitance (DQ0-DQ63)(DQS)	C <sub>OUT</sub>	8	pF

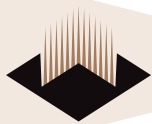


### IDD SPECIFICATIONS AND TEST CONDITIONS

Recommended operating conditions,  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ,  $V_{CCQ} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$

Parameter	Symbol	Conditions	DDR333 @CL=2.5 Max	DDR266 @CL=2 Max	DDR266 @CL=2.5 Max	DDR200 @CL=2 Max	Units
Operating Current	I <sub>DD0</sub>	One device bank; Active - Precharge; $t_{RC}=t_{RC}(\text{MIN})$ ; $t_{CK}=t_{CK}(\text{MIN})$ ; DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	TBD	1595	1595	1595	mA
Operating Current	I <sub>DD1</sub>	One device bank; Active-Read-Precharge; Burst = 2; $t_{RC}=t_{RC}(\text{MIN})$ ; $t_{CK}=t_{CK}(\text{MIN})$ ; Iout = 0mA; Address and control inputs changing once per clock cycle.	TBD	1795	1795	1795	mA
Precharge Power-Down Standby Current	I <sub>DD2P</sub>	All device banks idle; Power- down mode; $t_{CK}=t_{CK}(\text{MIN})$ ; CKE=(low)	TBD	48	48	48	mA
Idle Standby Current	I <sub>DD2F</sub>	CS# = High; All device banks idle; $t_{CK}=t_{CK}(\text{MIN})$ ; CKE = high; Address and other control inputs changing once per clock cycle. Vin = Vref for DQ, DQS and DM.	TBD	675	675	675	mA
Active Power-Down Standby Current	I <sub>DD3P</sub>	One device bank active; Power-down mode; $t_{CK}(\text{MIN})$ ; CKE=(low)	TBD	400	400	400	mA
Active Standby Current	I <sub>DD3N</sub>	CS# = High; CKE = High; One device bank; Active-Precharge; $t_{RC}=t_{RAS}(\text{MAX})$ ; $t_{CK}=t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	TBD	1035	1035	1035	mA
Operating Current	I <sub>DD4R</sub>	Burst = 2; Reads; Continous burst; One device bank active;Address and control inputs changing once per clock cycle; $t_{CK}=t_{CK}(\text{MIN})$ ; Iout = 0mA.	TBD	2035	2035	2035	mA
Operating Current	I <sub>DD4W</sub>	Burst = 2; Writes; Continous burst; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK}=t_{CK}(\text{MIN})$ ; DQ,DM and DQS inputs changing twice per clock cycle.	TBD	2275	2275	2275	mA
Auto Refresh Current	I <sub>DD5</sub>	$t_{RC}=t_{RC}(\text{MIN})$	TBD	2755	2755	2755	mA
Self Refresh Current	I <sub>DD6</sub>	CKE $\leq 0.2\text{V}$	TBD	315	315	315	mA
Operating Current	I <sub>DD7A</sub>	Four bank interleaving Reads (BL=4) with auto precharge with $t_{RC}=t_{RC}(\text{MIN})$ ; $t_{CK}=t_{CK}(\text{MIN})$ ; Address and control inputs change only during Active Read or Write commands.	TBD	4115	4115	4115	mA

\* For DDR333 consult factory



### DETAILED TEST CONDITIONS FOR DDR SDRAM I<sub>DD1</sub> & I<sub>DD7A</sub>

#### I<sub>DD1</sub> : OPERATING CURRENT : ONE BANK

1. Typical Case :  $V_{CC}=2.5V$ ,  $T=25^{\circ}C$
2. Worst Case :  $V_{CC}=2.7V$ ,  $T=10^{\circ}C$
3. Only one bank is accessed with  $t_{RC}$  (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle.  $I_{OUT} = 0mA$
4. Timing Patterns :
  - DDR200 (100 MHz, CL=2) :  $t_{CK}=10ns$ , CL2, BL=4,  $t_{RCD}=2*t_{CK}$ ,  $t_{RAS}=5*t_{CK}$   
Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
  - DDR266 (133MHz, CL=2.5) :  $t_{CK}=7.5ns$ , CL=2.5, BL=4,  $t_{RCD}=3*t_{CK}$ ,  $t_{RC}=9*t_{CK}$ ,  $t_{RAS}=5*t_{CK}$   
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
  - DDR266 (133MHz, CL=2) :  $t_{CK}=7.5ns$ , CL=2, BL=4,  $t_{RCD}=3*t_{CK}$ ,  $t_{RC}=9*t_{CK}$ ,  $t_{RAS}=5*t_{CK}$   
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
  - DDR333 (166MHz, CL=2.5) :  $t_{CK}=6ns$ , BL=4,  $t_{RCD}=10*t_{CK}$ ,  $t_{RAS}=7*t_{CK}$   
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

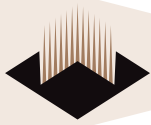
#### I<sub>DD7A</sub> : OPERATING CURRENT : FOUR BANKS

1. Typical Case :  $V_{CC}=2.5V$ ,  $T=25^{\circ}C$
2. Worst Case :  $V_{CC}=2.7V$ ,  $T=10^{\circ}C$
3. Four banks are being interleaved with  $t_{RC}$  (min), Burst Mode, Address and Control inputs on NOP edge are not changing.  $I_{OUT}=0mA$
4. Timing Patterns :
  - DDR200 (100 MHz, CL=2) :  $t_{CK}=10ns$ , CL2, BL=4,  $t_{RRD}=2*t_{CK}$ ,  $t_{RCD}=3*t_{CK}$ , Read with Autoprecharge  
Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
  - DDR266 (133MHz, CL=2.5) :  $t_{CK}=7.5ns$ , CL=2.5, BL=4,  $t_{RRD}=3*t_{CK}$ ,  $t_{RCD}=3*t_{CK}$   
Read with Autoprecharge  
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
  - DDR266 (133MHz, CL=2) :  $t_{CK}=7.5ns$ , CL2=2, BL=4,  $t_{RRD}=2*t_{CK}$ ,  $t_{RCD}=2*t_{CK}$   
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
  - DDR333 (166MHz, CL=2.5) :  $t_{CK}=6ns$ , BL=4,  $t_{RRD}=3*t_{CK}$ ,  $t_{RCD}=3*t_{CK}$ , Read with Autoprecharge  
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

Legend : A = Activate, R = Read, W = Write, P = Precharge, N = NOP

A (0-3) = Activate Bank 0-3

R (0-3) = Read Bank 0-3

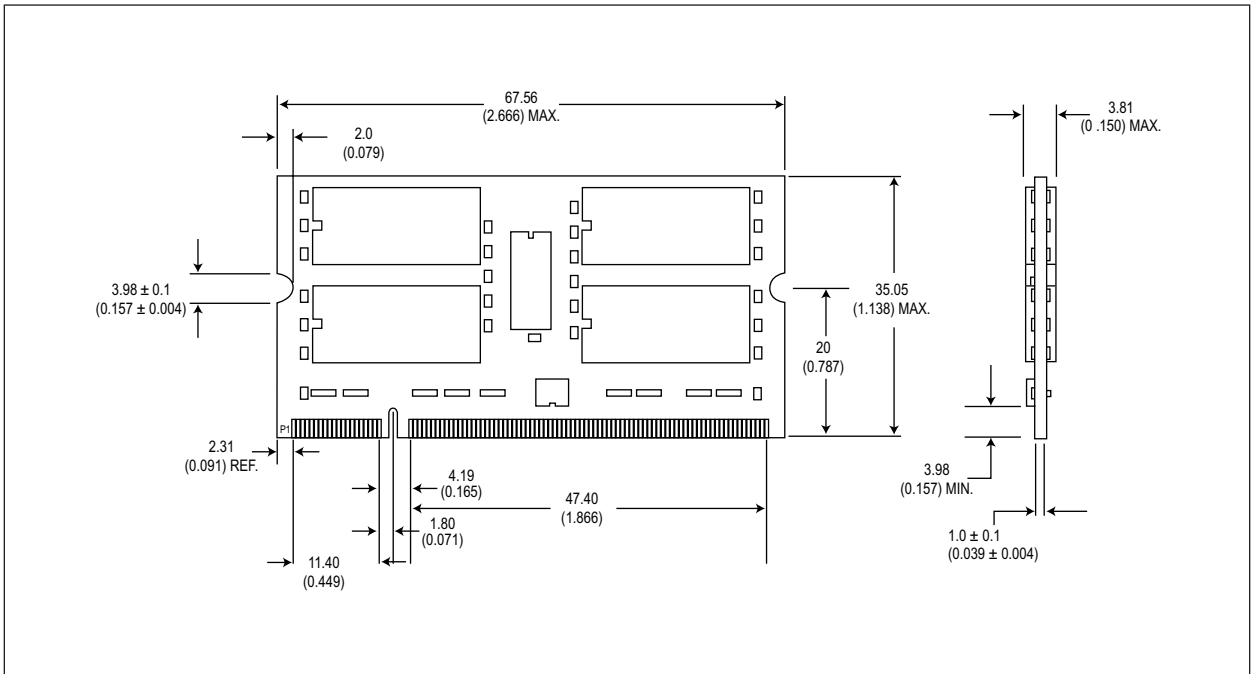


ORDERING INFORMATION FOR AD4

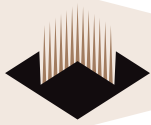
Part Number	Speed	Height*
W3EG6464S335AD4	166MHz/333Mbps, CL=2.5	35.5 (1.38)*
W3EG6464S262AD4	133MHz/266Mbps, CL=2	35.5 (1.38)
W3EG6464S265AD4	133MHz/266Mbps, CL=2.5	35.5 (1.38)
W3EG6464S202AD4	100MHz/200Mbps, CL=2	35.5 (1.38)

\* For DDR333 consult factory

PACKAGE DIMENSIONS FOR AD4



\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

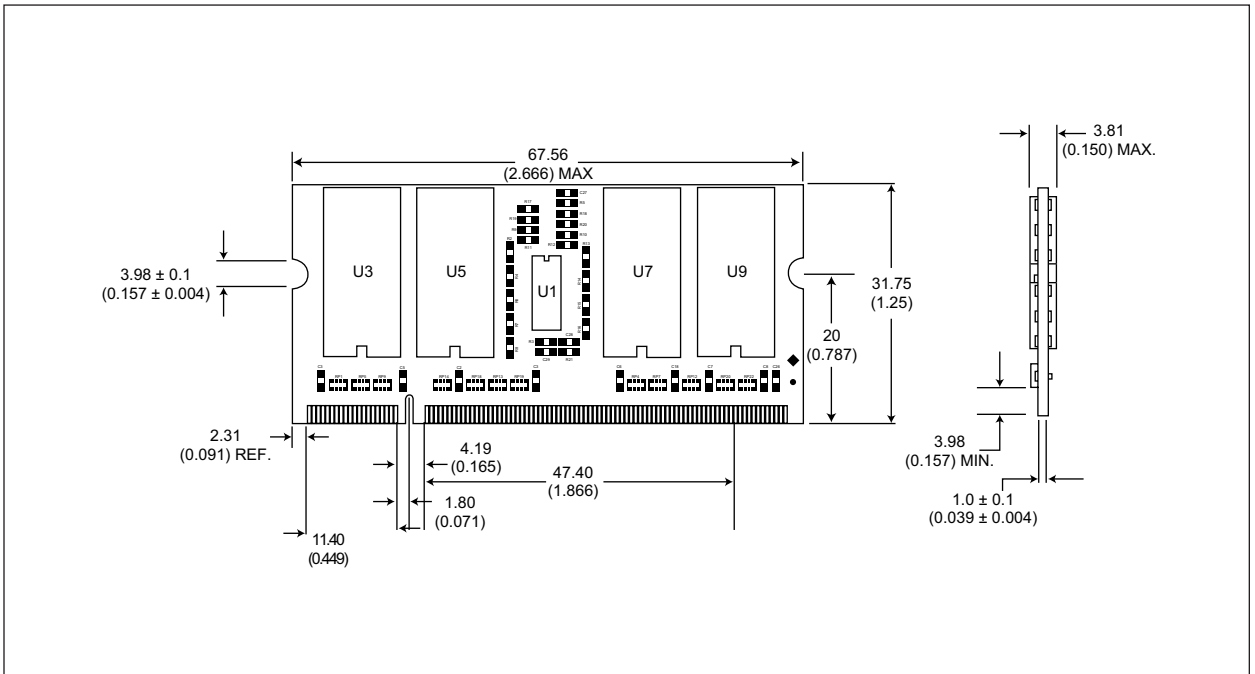


ORDERING INFORMATION FOR BD4

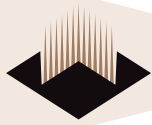
Part Number	Speed	Height*
W3EG6464S335BD4	166MHz/333Mbps, CL=2.5	31.75 (1.25)*
W3EG6464S262BD4	133MHz/266Mbps, CL=2	31.75 (1.25)
W3EG6464S265BD4	133MHz/266Mbps, CL=2.5	31.75 (1.25)
W3EG6464S202BD4	100MHz/200Mbps, CL=2	31.75 (1.25)

\* For DDR333 consult factory

PACKAGE DIMENSIONS FOR BD4



\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



### Document Title

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### Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	7-21-03	Advanced
Rev 1	Corrected incidentals (abbreviations, symbols, etc.) 1.1 corrected pages 1-8 1.2 added AD4 and BD4 package options 1.3 added document title page 1.4 removed "ED" from part marking	3-4-04	Preliminary