Freescale Semiconductor
Technical Data

Document Number: MMA7450L
Rev 0, 6/2007

RoHS

±2g/±4g/±8g Three Axis Low-g Digital Output Accelerometer

The MMA7450L is a Digital Output (I^2C/SPI), low power, low profile capacitive micromachined accelerometer featuring signal conditioning, a low pass filter, temperature compensation, self test, configurable to detect 0g through interrupt pins (INT1 or INT2), and pulse (click) detect for quick motion detection. The 0g offset can be customer calibrated using assigned 0g registers and g-Select which allows for command selection for 3 sensitivities (2g/4g/8g). Zero-g offset and sensitivity are factory set and require no external devices. The MMA7450L includes a Standby Mode that makes it ideal for handheld battery powered electronics.

MMA7450L

MMA7450L: XYZ AXIS ACCELEROMETER ±2G/±4G/±8G

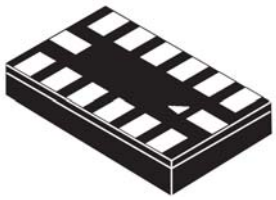
Features

- Digital Output (I^2C/SPI) - 10-Bit at 8g Mode
- 3mm x 5mm x 0.8mm LGA-14 Package
- Low Current Consumption: 400 μA
- Sleep Mode: 5 μA
- Low Voltage Operation: 2.4 V – 3.6 V
- Customer Assigned Registers for Offset Calibration
- Programmable Threshold Interrupt Output
- Level/Pulse Detection for Motion Recognition (Shock, Vibration, Freefall)
- Click Detection for Single or Double Click Recognition
- High Sensitivity (64 LSB/g @ 2g and @ 8g in 10-Bit Mode)
- Selectable Sensitivity (±2g, ±4g, ±8g)
- Self Test for X-Axis
- Robust Design, High Shocks Survivability (10,000 g)
- RoHS Compliant
- Environmentally Preferred Product
- Low Cost

Typical Applications

- Cell Phone/PMP/PDA: Image Stability, Text Scroll, Motion Dialing, E-Compass, Tap to Mute
- HDD: Freefall Detection
- Laptop PC: Freefall Detection, Anti-Theft
- Navigation and Dead Reckoning: Position Detection, Pedometer
- E-Compass Tilt Compensation
- 3D Gaming: Tilt and Motion Sensing, Event Recorder

Bottom View



14 LEAD
LGA
CASE 1935-01

Top View

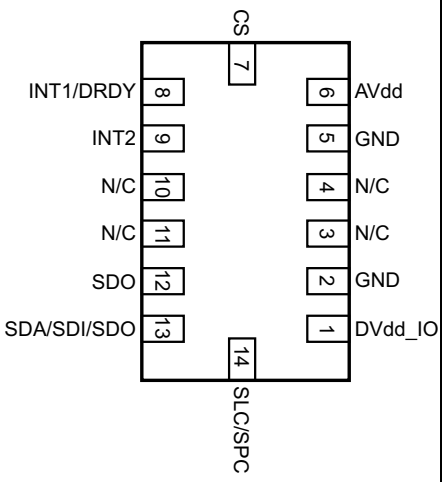


Figure 1. Pin Connections

ORDERING INFORMATION			
Part Number	**Temperature Range**	**Package**	**Shipping**
MMA7450LT	–20 to +65°C	LGA-14	Tray
MMA7450LR1	–20 to +65°C	LGA-14	Tape & Reel (7” Reel)
MMA7450LR2	–20 to +65°C	LGA-14	Tape & Reel (13” Reel)

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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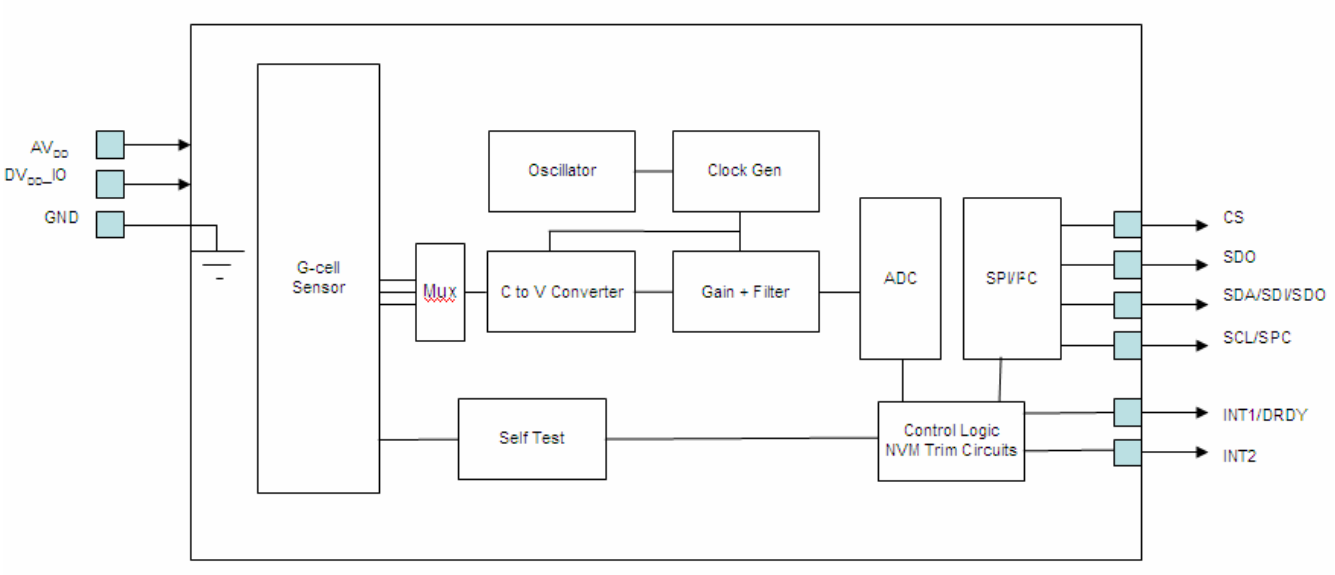


Figure 2. Simplified Accelerometer Functional Block Diagram

Table 1. Maximum Ratings

(Maximum ratings are the limits to which the device can be exposed without causing permanent damage.)

Rating	Symbol	Value	Unit
Maximum Acceleration (all axes)	g_{max}	10,000	g
Analog Supply Voltage	AV_{DD}	-0.3 to +3.6	V
Digital I/O pins Supply Voltage	DV_{DD_IO}	-0.3 to +3.6	V
Drop Test	D_{drop}	1.8	m
Storage Temperature Range	T_{stg}	-40 to +125	°C

ELECTRO STATIC DISCHARGE (ESD)

WARNING: This device is sensitive to electrostatic discharge.

Although the Freescale accelerometer contains internal 2000V ESD protection circuitry, extra precaution must be taken by the user to protect the chip from ESD. A charge of over 2000 volts can accumulate on the human body or associated test equipment. A charge of this magnitude can alter the performance or cause failure of the chip. When handling the accelerometer, proper ESD precautions should be followed to avoid exposing the device to discharges which may be detrimental to its performance.

Table 2. Operating Characteristics

Unless otherwise noted: –20°C ≤ T_A ≤ 65°C, 2.4 V ≤ AV_{DD} ≤ 3.6 V, Acceleration = 0g, Loaded output

Characteristic	Symbol	Min	Typ	Max	Unit
Analog Supply Voltage					
Standby Operation Mode	AV_{DD}	2.4	2.8	3.6	V
Enable Bus Mode	AV_{DD}		0		V
Digital I/O Pins Supply Voltage					
Standby Operation Mode	DV_{DD_IO}	1.71	1.8	AV_{DD}	V
Enable Bus Mode	DV_{DD_IO}	1.71	1.8	3.6	V
Supply Current Drain (AV_{DD}/GND)					
Operation Mode	I_{DD}	—	400	TBD	μA
Pulse Detect Function Mode	I_{DD}	—	550	TBD	μA
Standby Mode (except data loading and I^2C/SPI communication period)	I_{DD}	—	5	TBD	μA
Operating Temperature Range	T_A	-20	25	+85	°C
Acceleration Range	gFS	±2	—	—	g
X-Axis, Y-Axis, Z-Axis	gFS	±4	—	—	g
	gFS	±8	—	—	g
Output Signal (T_A=25°C, AV_{DD}=2.8 V)					
Zero g					
±2g range (25°C) 8bit	V_{OFF}	-16	—	+16	LSB
±4g range (25°C) 8bit	V_{OFF}	-8	—	+8	LSB
±8g range (25°C) 8bit	V_{OFF}	-4	—	+4	LSB
±8g range (25°C) 10bit	V_{OFF}	-16	—	+16	LSB
Resolution (T_A=25°C, AV_{DD}=2.8 V)					
±2g range (25°C) 8bit		—	15.6	—	mg
±4g range (25°C) 8bit		—	31.2	—	mg
±8g range (25°C) 8bit		—	62.4	—	mg
±8g range (25°C) 10bit		—	15.6	—	mg
Sensitivity (T_A=25°C, AV_{DD}=2.8 V)					
±2g range (25°C) 8bit	ΔV_{OUT}	—	64	—	LSB/g
±4g range (25°C) 8bit	ΔV_{OUT}	—	32	—	LSB/g
±8g range (25°C) 8bit	ΔV_{OUT}	—	16	—	LSB/g
±8g range (25°C) 10bit	ΔV_{OUT}	—	64	—	LSB/g
Self Test Output Response					
Zout	ΔST_Z	—	+64	—	LSB
Input High Voltage	V_{IH}	0.85DV_{DD}_io	—	DV_{DD}_io + 0.3	
Input Low Voltage	V_{IL}	-0.3V	—	0.3DV_{DD}_io	
PSRR (AV_{DD})					
0 to 20 kHz		—	TBD	—	dB
0 to 50 kHz		—	TBD	—	dB
Internal Clock Frequency	t_{CLK}	TBD	150	TBD	kHz
SPI Frequency					
DV_{DD_IO} < 2.4 V		—	4	—	MHz
DV_{DD_IO} > 2.4 V		—	8	—	MHz
Output Data Rate (X, Y, Z set)		—	125 or 250	—	Hz
Bandwidth for Data Measurement (User Selectable)		—	62.5	—	Hz
		—	125	—	Hz

Table 2. Operating Characteristics (Continued)

Unless otherwise noted: –20°C ≤ T_A ≤ 65°C, 2.4 V ≤ AV_{DD} ≤ 3.6 V, Acceleration = 0g, Loaded output

Characteristic	Symbol	Min	Typ	Max	Unit
Control Timing					
Wait Time for IIC/SPI ready after power on	t_{su}		1		ms
Turn On Response Time (Standby to Normal Mode)	t_{ru}			20	ms
Turn Off Response Time (Normal to Standby Mode)	t_{rd}			20	ms
Self Test Response Time	t_{st}				ms
Sensing Element Resonant Frequency					
XY	$f_{GCELLXY}$				kHz
Z	f_{GCELLZ}				kHz
Internal Sampling Frequency	f_{CLK}				kHz
Nonlinearity (2 g range)		-1	—	+1	%FS
Cross Axis Sensitivity		-5		+5	%
Orthogonality Error of Channels		TBD		TBD	°
Package to Die Misalignment			1		°
RF Field Influence to Sensor				TBD	LSB

1. These limits define the range of operation for which the part will meet specification.
2. Within the supply range of 2.4 and 3.6 V, the device operates as a fully calibrated linear accelerometer. Beyond these supply limits the device may operate as a linear device but is not guaranteed to be in calibration.
3. This value is measured with g-Select in 2g mode.
4. The device can measure both + and - acceleration. The output is at mid-supply with no acceleration. The output will increase above VDD/2 for positive acceleration. The output will decrease below VDD/2 for negative acceleration.
5. The response time is between 10% of full scale Vdd input voltage and 90% of the final operating output voltage.
6. The response time is between 10% of full scale standby mode input voltage and 90% of the final operating output voltage.
7. The response time is between 10% of the full scale self test input voltage and 90% of the self test output voltage.
8. A measure of the device ability to reject acceleration is applied 90° from the true axis of sensitivity.

Table 3. Function Parameters for Detection

V_L ≤ V_{DD} ≤ V_H; T_L ≤ T_A ≤ T_H unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit
Level Detection Detection Threshold Range		0		FS	G
Pulse Detection					
Pulse detection range (Adjustable range)		0.5		127	ms
Time step for pulse detection			0.5		ms
Threshold range for pulses		0		FS	g
Detection levels for threshold (5)			127		Levels
Latency timer (Adjustable range)		1		150	ms
Time Window (Adjustable range)		1		250	ms
Measurement bandwidth for detecting interrupt			600		Hz
Time step for latency timer and time window			1		ms

Note: The response time is between 10% of full scale Vdd input voltage and 90% of the final operating output voltage.

PRINCIPLE OF OPERATION

The Freescale accelerometer is a surface-micromachined integrated-circuit accelerometer. The device consists of a surface micromachined capacitive sensing cell (g-cell) and a signal conditioning ASIC contained in a single package. The sensing element is sealed hermetically at the wafer level using a bulk micromachined cap wafer. The g-cell is a mechanical structure formed from semiconductor materials (polysilicon) using semiconductor processes (masking and etching). It can be modeled as a set of beams attached to a movable central mass that move between fixed beams. The movable beams can be deflected from their rest position by subjecting the system to an acceleration (Figure 3).

As the beams attached to the central mass move, the distance from them to the fixed beams on one side will increase by the same amount that the distance to the fixed beams on the other side decreases. The change in distance is a measure of acceleration. The g-cell beams form two back-to-back capacitors (Figure 3). As the center beam moves with acceleration, the distance between the beams changes and each capacitor's value will change, ($C = A\varepsilon/D$). Where A is the area of the beam, ε is the dielectric constant, and D is the distance between the beams.

The ASIC uses switched capacitor techniques to measure the g-cell capacitors and extract the acceleration data from the difference between the two capacitors. The ASIC also signal conditions and filters (switched capacitor) the signal, providing a high level digital output voltage that is ratiometric and proportional to acceleration.

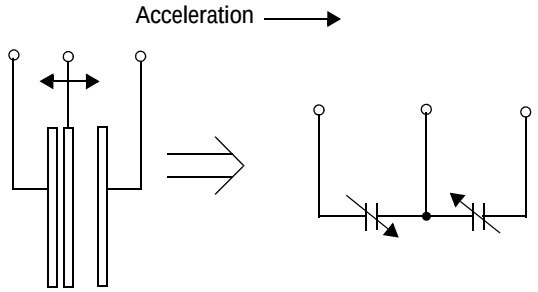


Figure 3. Simplified Transducer Physical Model

FEATURES

Self Test

The sensor provides a self test feature that allows the verification of the mechanical and electrical integrity of the accelerometer at any time before or after installation. This feature is critical in applications such as hard disk drive protection where system integrity must be ensured over the life of the product. Customers can use self test to verify the solderability to confirm that the part was mounted to the PCB correctly. To use this feature to verify the 0g-Detect function, the accelerometer should be held upside down so that the z axis experiences -1g. When the self test function is initiated through the mode control register, accessing the “self test” bit, an electrostatic force is applied to each axis to cause it to deflect. The z-axis is trimmed to deflect 1g. This procedure assures that both the mechanical (g-cell) and electronic sections of the accelerometer are functioning.

g-Select

The g-Select feature enables the selection between 3 sensitivities for measurement. Depending on the values in the Mode control register ($16), the MMA7450L’s internal gain will be changed allowing it to function with a 2g, 4g or 8g measurement sensitivity. This feature is ideal when a product has applications requiring two or more sensitivities for optimum performance and for enabling multiple functions. The sensitivity can be changed during the operation by modifying the two GLVL bits located in the mode control register.

$16: Mode control register (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
--	DRPD	SPI3W	STON	GLVL[1]	GLVL[0]	MODE[1]	MODE[0]	Function
0	0	0	0	0	0	0	0	Default

GLVL [1:0]

00: 8G is selected for measurement range.

01: 2G is selected for measurement range.

10: 4G is selected for measurement range.

Table 4. g-Select Description

g-Select	g-Range	Sensitivity
00	8 g	16 LSB/g
01	2 g	64 LSB/g
10	4 g	32 LSB/g

Table 5. Mode Descriptions

MODE [0:1]	Function
00	Standby Mode
01	Measurement Mode
10	Level Detection Mode
11	Pulse Detection Mode

Standby Mode

This digital output 3-axis accelerometer provides a standby mode that is ideal for battery operated products. When standby mode is active, the device outputs are turned off, providing significant reduction of operating current. When the device is in standby mode the current will be reduced to 5 µA typical. In standby mode the device can read and write to the registers with the I^2C/SPI available, but no new measurements can be taken in this mode as all current consuming parts are off. The mode of the device is controlled through the mode control register by accessing the two mode bits as shown in Table 5.

Measurement Mode

During measurement mode, continuous measurements on all three axes enabled. The g-range for 2g, 4g, or 8g are selectable with 8-bit data and the g-range of 8g is selectable with 10-bit data. The sample rate during measurement mode is 125 Hz. Therefore, when a conversion is complete (signaled by the DRDY flag), the next measurement will be ready 8 ms later.

When measurements on all three axes are complete, a logic high level is output to the DRDY pin, indicating “Measurement data is ready.” The DRDY status can be monitored by the DRDY bit in Status Register (Address: $09). The DRDY pin is kept high until one of the three Output Value Registers are read. If the next measurement data is written before the previous data is read, the DOVR bit in the Status Register will be set. Also note that In measurement mode, level detection mode and pulse detection mode are not available.

LEVEL DETECTION MODE

Level Detection Mode

In level detection mode, the measurements for x, y and z are all enabled with 2g/4g and 8g range available.The detection of thresholds for an acceleration signal level for the combinations of x and y or x, y, and z is enabled. This is used for motion detection where the threshold can be user set depending on the application or user specific requirements. When a motion event is detected, one of the interrupt pins (INT1 or INT2) will output a logic high output signaling the event is detected.

Setting for Motion Detection

To configure the MMA7450L for motion detection, after all three axes are enabled for detection, set the LDPOL bit in Control Register 2 (Address: $19) to 0. When the output value of one of the enabled axes exceeds the threshold limit value, either INT1 or INT2 pin will output a logic High indicating the event was detected.

- If LDPOL = 0 and all three axes are enabled for detection
- When the specified motion condition is detected, INT1 or INT2 will output a Logic high
- “XOUT ≥Threshold” or “YOUT ≥Threshold” or “ZOUT ≥Threshold”

Threshold limit value is common for all three axes. Positive/negative and absolute value option is available.

Assigning and Clearing the Interrupt Pins

INT1/INT2 pin assignment for level detection is controlled by Control Register 1 (Address:$18).

INTPIN:
0:INT1 will be used for event
1:INT2 will be used for event

Detection status is able to be monitored by Detection Source Register (Address:$0A). Once the configured event is detected, INT pin or register bit will not be cleared until the respective clear bit (CLRINT1 or CLRINT2) in Interrupt Latch Reset Register (Address: $17) is set. CLRINT1 and CLRINT2 should be cleared before starting next detection. Otherwise, INT pin or register will not set.

NOTE: Measurement period and bandwidth for level detection is different from data output rate and the bandwidth of “measurement.” Please refer to Functional Parameter for Detection for more information.

PULSE DETECTION MODE

Pulse Detection Mode

In pulse detection mode, both 2g/4g and 8g range are available. Measurements for x, y and z in 2g/4g or 8g mode are enabled. The level detection is also enabled in this mode. The pulse detected by the acceleration signal is enabled with single pulse and double pulse detection allowing the choice of either positive, negative or absolute value pulse detection.

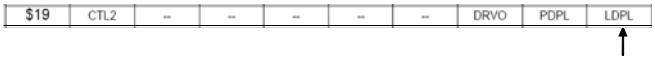
Setting for Motion Detection

For the PDPOL bit in Control Register 2 (Address: $19) the register should be set to “0” for motion detection. When the output value of one of the enabled axes exceeds the threshold limit value, logic high level is output to INT1 or INT2 pin and indicates the event was detected.

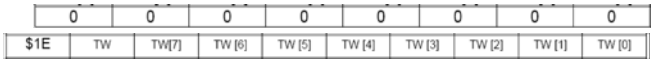
- If PDPOL = 0 and all three axes are enabled for detection
- When the condition below was detected, logic high level outputs to INT1 or INT2
- “XOUT ≥Threshold” or “YOUT ≥Threshold” or “ZOUT ≥Threshold”

Setting for Free Fall Detection

To configure the MMA7450L for freefall detection, set the PDPOL bit in Control Register 2 (Address: $19) to 1.



Next, set the register for Time Window for 2nd pulse value (Address $1E) to 0.



When the output values of all enabled axes are below the threshold limit continuously during the period specified in Latency Timer Value Register, logic high level is output to INT1 or INT2 pin indicating freefall was detected.

Filtering

The 3 axis accelerometer contains digital filtering.

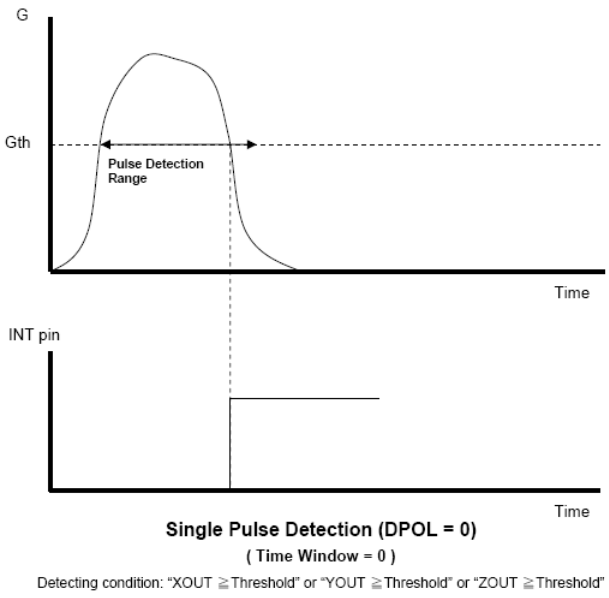


Figure 4. Single Pulse Detection

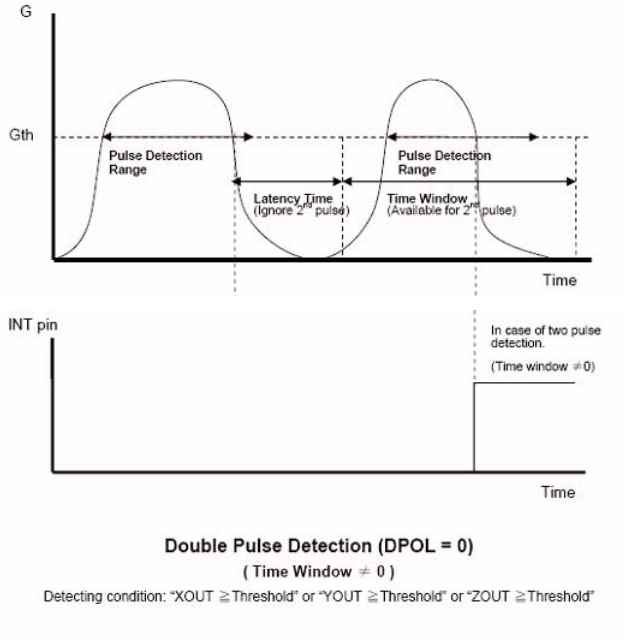


Figure 5. Double Pulse Detection

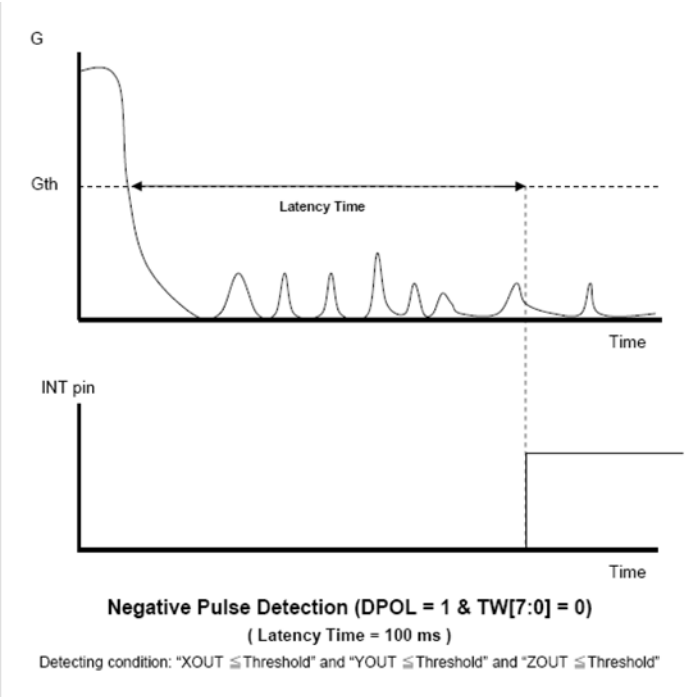


Figure 6. Negative Pulse Detection

DIGITAL INTERFACE

The MMA7450L has both an I²C and SPI digital output available for a communication interface. When CS pin is used for Slave Select, SPI communication is selected. When CS is high, I²C communication is selected and SPI is disabled.

NOTE: It is recommended to disable I²C during SPI communication to avoid communication errors between devices using a different SPI communication protocol. To disable I²C, set the I²CDIS bit in I²C Device Address register using SPI.

I²C SLAVE INTERFACE

I²C is a synchronous serial communication between a master device and one or more slave devices. The master is typically a microcontroller, which provides the serial clock signal and addresses the slave device(s) on the bus. The MMA7450L communicates only in slave operation where the device address is $1D. Multiple read and write modes are available. The protocol supports slave only operation. It does not support Hs mode, “10-bit addressing”, “general call” and :”START byte”.

SINGLE BYTE READ

The MMA7450L has an 8-bit ADC that can sample, convert and return sensor data on request. The transmission of an 8-bit command begins on the falling edge of SCL. After the eight clock cycles are used to send the command, note that the data returned is sent with the MSB first once the data is received. Figure 7 shows the timing diagram for the accelerometer 8-bit I²C read operation. The Master (or MCU) transmits a start condition (S) to the MMA7450L, slave address ($1D), with the R/W bit set to “0” for a write, and the MMA7450L sends an acknowledgement. Then the Master (or MCU) transmits the 8-bit address of the register to read and the MMA7450L sends an acknowledgement. The Master (or MCU) transmits a repeated start condition (SR) and then addresses the MMA7450L ($1D) with the R/W bit set to “1” for a read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer.

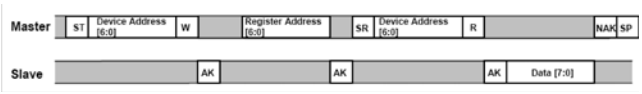


Figure 7. Single Byte Read - The Master is reading one address from the MMA7450L

MULTIPLE BYTES READ

The MMA7450L automatically increments the received register address commands after a read command is received. Therefore, after following the steps of a single byte read, multiple bytes of data can be read from sequential registers after each MMA7450L acknowledgment (ACK) is received until a NACK is received from the Master followed by a stop condition (SP) signalling an end of transmission. See Figure 8.

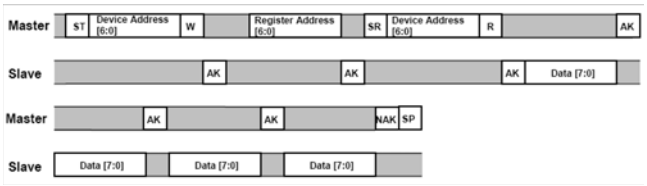


Figure 8. Multiple Bytes Read - The Master is reading multiple sequential registers from the MMA7450L

SINGLE BYTE WRITE

To start a write command, the Master transmits a start condition (ST) to the MMA7450L, slave address ($1D) with the R/W bit set to “0” for a write, the MMA7450L sends an acknowledgement. Then the Master (MCU) transmits the 8-bit address of the register to write to, and the MMA7450L sends an acknowledgement. Then the Master (or MCU) transmits the 8-bit data to write to the designated register and the MMA7450L sends an acknowledgement that it has received the data. Since this transmission is complete, the Master transmits a stop condition (SP) to the data transfer. The data sent to the MMA7450L is now stored in the appropriate register. See Figure 9.

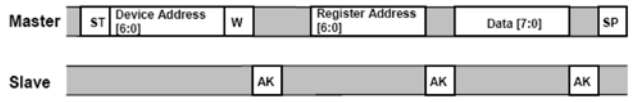


Figure 9. Single Byte Write - The Master (MCU) is writing to a single register of the MMA7450L

MULTIPLE BYTES WRITE

The MMA7450L automatically increments the received register address commands after a write command is received. Therefore, after following the steps of a single byte write, multiple bytes of data can be written to sequential registers after each MMA7450L acknowledgment (ACK) is received. See Figure 10.

Figure 10. Multiple Byte Writes - The Master (MCU) is writing to multiple sequential registers of the MMA7450L

SPI SLAVE INTERFACE

The MMA7450L also uses serial peripheral interface communication as a digital communication. The SPI communication is primarily used for synchronous serial communication between a master device and one or more slave devices. See Figure 16 for an example of how to configure one master with two MMA7450L devices. The MMA7450L is always operated as a slave device. Typically, the master device would be a microcontroller which would drive the clock (SPC) and chip select (CS) signals.

The SPI interface consists of two control lines and two data lines: CS, SPC, SDI, and SDO. The CS, also known as Chip Select, is the slave device enable which is controlled by the SPI master. CS is driven low at the start of a transmission. CS

is then driven high at the end of a transmission. SPC is the Serial Port Clock which is also controlled by the SPI master. SDI and SDO are the Serial Port Data Input and the Serial Port Data Output. The SDI and SDO data lines are driven at the falling edge of the SPC and should be captured at the rising edge of the SPC.

Read and write register commands are completed in 16 clock pulses or in multiples of 8, in the case of a multiple byte read/write.

SPI READ OPERATION

A SPI read transfer consists of a 1-bit Read/Write signal, a 6-bit address, and 1-bit don't care bit. (1-bit R/W=0 + 6-bits address + 1-bit don't care). The data to read is sent by the SPI interface during the next transfer. See Figure 11 and Figure 12 for the timing diagram for an 8-bit read in 4 wire and 3 wire modes, respectively.

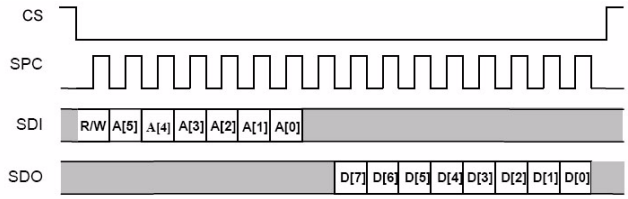


Figure 11. SPI Timing Diagram for 8-Bit Register Read (4 Wire Mode)

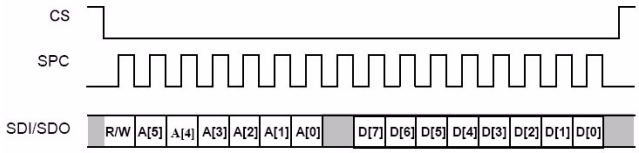


Figure 12. SPI Timing Diagram for 8-Bit Register Read (3 Wire Mode)

SPI WRITE OPERATION

In order to write to one of the 8-bit registers, an 8-bit write command must be sent to the MMA7450L. The write command consists of an MSB (0=read, 1=write) to indicate writing to the MMA7450L register, followed by a 6-bit address and 1 don't care bit.

The command should then be followed the 8-bit data transfer. See Figure 13 for the timing diagram for an 8-bit data write.

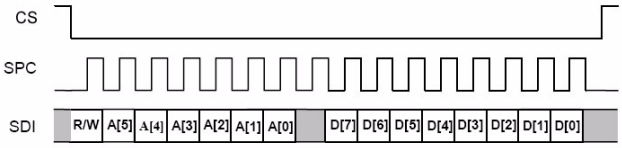


Figure 13. SPI Timing Diagram for 8-Bit Register Write (3 Wire Mode)

BASIC CONNECTIONS

Pin Descriptions

Top View

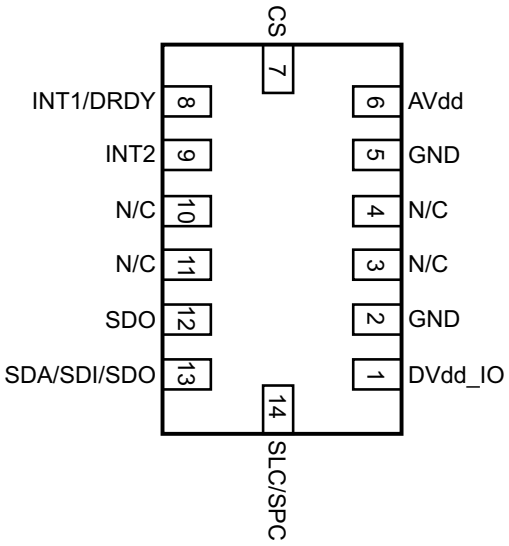


Figure 14. Pinout Description

Table 6. Pin Descriptions

Pin No.	Pin Name	Description
1	DVDD_IO	Digital power supply for I/O pads
3, 10, 11	NC	No Connection or connect to GND
4	IADDR0	I^2C Address bit 0 (optional)
2, 5	GND	Ground
6	AVDD	Analog power supply (main power supply)
7	CS	SPI enable, I^2C/SPI mode selection (1:1^{2}C, 0:SPI enabled)
8	INT1/DRDY	Interrupt1 / Data Ready
9	INT2	Interrupt2
12	SDO	SPI Serial Data Output
13	SDA/SDI/SDO	I^2C Serial Data (SDA), SPI Serial Data Input (SDI), 3-wire interface Serial Data Output (SDO)
14	SCL/SPC	I^2C Serial Clock (SCL), SPI Serial Clock (SPC)

Recommended PCB Layout for Interfacing Accelerometer to Microcontroller

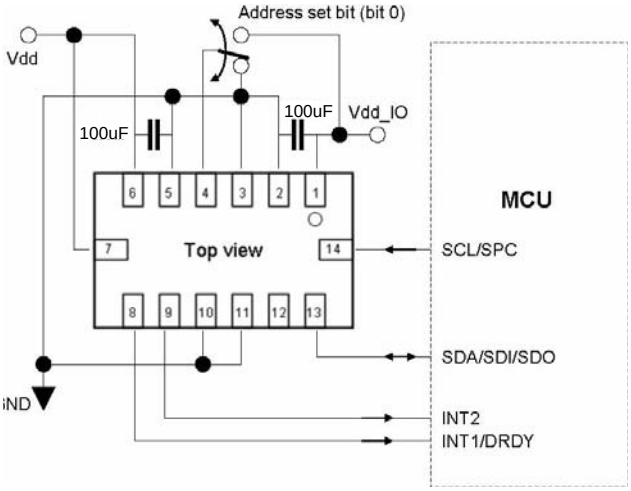


Figure 15. I^2C Connection to MCU

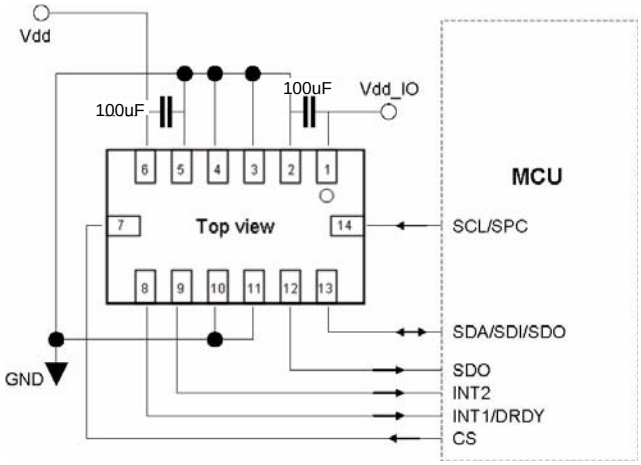


Figure 16. SPI Connection to MCU

NOTES:

1. Use 100 nF capacitor on V_{DD} to decouple the power source.
2. Physical coupling distance of the accelerometer to the microcontroller should be minimal.
3. Place a ground plane beneath the accelerometer to reduce noise, the ground plane should be attached to all of the open ended terminals shown in Figure 15 and Figure 16.
4. PCB layout of power and ground should not couple power supply noise.
5. Accelerometer and microcontroller should not be a high current path.
6. Any external power supply switching frequency should be selected such that they do not interfere with the internal accelerometer sampling frequency (sampling frequency). This will prevent aliasing errors.

Table 7. User Register Summary

Address	Name	Definition	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00	XOUTL	10 bits output value X LSB	XOUT[7]	XOUT[6]	XOUT[5]	XOUT[4]	XOUT[3]	XOUT[2]	XOUT[1]	XOUT[0]
$01	XOUTH	10 bits output value X MSB	--	--	--	--	--	--	XOUT[9]	XOUT[8]
$02	YOUTL	10 bits output value Y LSB	YOUT[7]	YOUT[6]	YOUT[5]	YOUT[4]	YOUT[3]	YOUT[2]	YOUT[1]	YOUT[0]
$03	YOUTH	10 bits output value Y MSB	--	--	--	--	--	--	YOUT[9]	YOUT[8]
$04	ZOUTL	10 bits output value Z LSB	ZOUT[7]	ZOUT[6]	ZOUT[5]	ZOUT[4]	ZOUT[3]	ZOUT[2]	ZOUT[1]	ZOUT[0]
$05	ZOUTH	10 bits output value Z MSB	--	--	--	--	--	--	ZOUT[9]	ZOUT[8]
$06	XOUT8	8 bits output value X	XOUT[7]	XOUT[6]	XOUT[5]	XOUT[4]	XOUT[3]	XOUT[2]	XOUT[1]	XOUT[0]
$07	YOUT8	8 bits output value Y	YOUT[7]	YOUT[6]	YOUT[5]	YOUT[4]	YOUT[3]	YOUT[2]	YOUT[1]	YOUT[0]
$08	ZOUT8	8 bits output value Z	ZOUT[7]	ZOUT[6]	ZOUT[5]	ZOUT[4]	ZOUT[3]	ZOUT[2]	ZOUT[1]	ZOUT[0]
$09	STATUS	Status registers	--	--	--	--	--	PERR	DOVR	DRDY
$0A	DETSRC	Detection source registers	LDX	LDY	LDZ	PDX	PDY	PDZ	INT1	INT2
$0B	TOUT	“Temperature output value” (Optional)	TMP[7]	TMP[6]	TMP[5]	TMP[4]	TMP[3]	TMP[2]	TMP[1]	TMP[0]
$0C		(Reserved)	--	--	--	--	--	--	--	--
$0D	I2CAD	I2C device address	I2CDIS	DAD[6]	DAD[5]	DAD[4]	DAD[3]	DAD[2]	DAD[1]	DAD[0]
$0E	USRINF	User information (Optional)	UI[7]	UI[6]	UI[5]	UI[4]	UI[3]	UI[2]	UI[1]	UI[0]
$0F	WHOAMI	“Who am I” value (Optional)	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]
$10	XOFFL	Offset drift X value (LSB)	XOFF[7]	XOFF[6]	XOFF[5]	XOFF[4]	XOFF[3]	XOFF[2]	XOFF[1]	XOFF[0]
$11	XOFFH	Offset drift X value (MSB)	--	--	--	--	--	XOFF[10]	XOFF[9]	XOFF[8]
$12	YOFFL	Offset drift Y value (LSB)	YOFF[7]	YOFF[6]	YOFF[5]	YOFF[4]	YOFF[3]	YOFF[2]	YOFF[1]	YOFF[0]
$13	YOFFH	Offset drift Y value (MSB)	--	--	--	--	--	YOFF[10]	YOFF[9]	YOFF[8]
$14	ZOFFL	Offset drift Z value (LSB)	ZOFF[7]	ZOFF[6]	ZOFF[5]	ZOFF[4]	ZOFF[3]	ZOFF[2]	ZOFF[1]	ZOFF[0]
$15	ZOFFH	Offset drift Z value (MSB)	--	--	--	--	--	ZOFF[10]	ZOFF[9]	ZOFF[8]
$16	MCTL	Mode control	LPEN	DRPD	SPI3W	STON	GLVL[1]	GLVL[0]	MOD[1]	MOD[0]
$17	INTRST	Interrupt latch reset	--	--	--	--	--	--	CLRINT2	CLRINT1
$18	CTL1	Control 1	--	THOPT	ZDA	YDA	XDA	INTRG[1]	INTRG[0]	INTPIN
$19	CTL2	Control 2	--	--	--	--	--	DRVO	PDPL	LDPL
$1A	LDTH	Level detection threshold limit value	LDTH[7]	LDTH[6]	LDTH[5]	LDTH[4]	LDTH[3]	LDTH[2]	LDTH[1]	LDTH[0]
$1B	PDTH	Pulse detection threshold limit value	PDTH[7]	PDTH[6]	PDTH[5]	PDTH[4]	PDTH[3]	PDTH[2]	PDTH[1]	PDTH[0]
$1C	PW	Pulse duration value	PD[7]	PD[6]	PD[5]	PD[4]	PD[3]	PD[2]	PD[1]	PD[0]
$1D	LT	Latency time value	LT[7]	LT[6]	LT[5]	LT[4]	LT[3]	LT[2]	LT[1]	LT[0]
$1E	TW	Time window for 2nd pulse value	TW[7]	TW[6]	TW[5]	TW[4]	TW[3]	TW[2]	TW[1]	TW[0]
$1F		(Reserved)	--	--	--	--	--	--	--	--

REGISTER DEFINITIONS

$00 : 10bits output value X LSB (Read only)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
XOUT [7]	XOUT [6]	XOUT [5]	XOUT [4]	XOUT [3]	XOUT [2]	XOUT [1]	XOUT[0]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): Zero G = 10'h000

Reading low byte XOUTL latches high byte XOUTH to allow 10-bit reads.

XOUTH should be read directly following XOUTL read.

$01 : 10bits output value X MSB (Read only)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
--	--	--	--	--	--	XOUT [9]	XOUT[8]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): Zero G = 10'h000

Reading low byte XOUTL latches high byte XOUTH to allow 10-bit reads.

XOUTH should be read directly following XOUTL read.

$02 : 10bits output value Y LSB (Read only)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
YOUT [7]	YOUT [6]	YOUT [5]	YOUT [4]	YOUT [3]	YOUT [2]	YOUT [1]	YOUT[0]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): Zero G = 10'h000

Reading low byte YOUTL latches high byte YOUTH to allow coherent 10-bit reads.

YOUTH should be read directly following YOUTL.

$03 : 10bits output value Y MSB (Read only)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
--	--	--	--	--	--	YOUT [9]	YOUT[8]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): Zero G = 10'h000

Reading low byte ZOUTL latches high byte ZOUTH to allow coherent 10-bit reads.

ZOUTH should be read directly following ZOUTL.

$04 : 10bits output value Z LSB (Read only)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
ZOUT [7]	ZOUT [6]	ZOUT [5]	ZOUT [4]	ZOUT [3]	ZOUT [2]	ZOUT [1]	ZOUT[0]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): Zero G = 10'h000

Reading low byte ZOUTL latches high byte ZOUTH to allow coherent 10-bit reads.

ZOUTH should be read directly following ZOUTL.

$05 : 10bits output value X MSB (Read only)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
--	--	--	--	--	--	ZOUT [9]	ZOUT[8]	Function
0	0	0	0	0	0	0	0	Default

$06: 8bits output value X (Read only)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
XOUT[7]	XOUT [6]	XOUT [5]	XOUT [4]	XOUT [3]	XOUT [2]	XOUT [1]	XOUT [0]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): Zero G = 8'h00

$07: 8bits output value Y (Read only)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
YOUT[7]	YOUT [6]	YOUT [5]	YOUT [4]	YOUT [3]	YOUT [2]	YOUT [1]	YOUT [0]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): Zero G = 8'h00

$08: 8bits output value Z (Read only)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
ZOUT[7]	ZOUT [6]	ZOUT [5]	ZOUT [4]	ZOUT [3]	ZOUT [2]	ZOUT [1]	ZOUT [0]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): Zero G = 8'h00

$09: Status register (Read only)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
--	--	--	--	--	PERR	DOVR	DRDY	Function
0	0	0	0	0	0	0	0	Default

DRDY

1: Data is ready

0: Data is not ready

DOVR

1: Data is over written

0: Data is not over written

PERR

1: Parity error is detected in trim data. Then, self test is disabled

0: Parity error is not detected in trim data

$0A: Detection source register (Read only)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
LDX	LDY	LDZ	PDX	PDY	PDZ	INT2	INT1	Function
0	0	0	0	0	0	0	0	Default

LDX

1: Level detection detected on X axis

0: Level detection not detected on X axis

LDY

1: Level detection detected on Y axis

0: Level detection not detected on Y axis

LDZ

1: Level detection detected on Z axis

0: Level detection not detected on Z axis

PDX *Note

1: Pulse is detected on X axis at single pulse detection

0: Pulse is not detected on X axis at single pulse detection

PDY *Note

1: Pulse is detected on Y axis at single pulse detection

0: Pulse is not detected on Y axis at single pulse detection

PDZ *Note

1: Pulse is detected on Z axis at single pulse detection

0: Pulse is not detected on Z axis at single pulse detection

Note: This bit value is not valid at double pulse detection

INT1

1: Interrupt assigned by "Detection control" register is detected

0: Interrupt assigned by "Detection control" register is not detected

INT2

1: Interrupt assigned by "Detection control" register is detected

0: Interrupt assigned by "Detection control" register is not detected

$0D: I2C Device Address (Bit 6-0: Read only, Bit 7: Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
I2CDIS	DVAD[6]	DVAD[5]	DVAD[4]	DVAD[3]	DVAD[2]	DVAD[1]	DVAD[0]	Function
0	0	0	1	1	1	0	1	Default

I2CDIS

0: I2C and SPI are available.

1: I2C is disabled.

DVAD[6:0]: I2C device address

$0E: User Information (Read Only: Optional)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
UI[7]	UI[6]	UI[5]	UI[4]	UI[3]	UI[2]	UI[1]	UI[0]	Function
0/OTP	0/OTP	0/OTP	0/OTP	0/OTP	0/OTP	0/OTP	0/OTP	Default

UI2[7:0]: User information

$0F: "Who Am I" value (Read only: Optional)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
ID[7]	ID [6]	ID [5]	ID [4]	ID [3]	ID [2]	ID [1]	ID [0]	Function
0/OTP	0/OTP	0/OTP	0/OTP	0/OTP	0/OTP	0/OTP	0/OTP	Default

$10: Offset drift X LSB (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
XOFF[7]	XOFF [6]	XOFF [5]	XOFF [4]	XOFF [3]	XOFF [2]	XOFF [1]	XOFF [0]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): User level offset trim value for X axis

Bit	XOFF[7]	XOFF[6]	XOFF[5]	XOFF[4]	XOFF[3]	XOFF[2]	XOFF[1]	XOFF[0]
Weight (*Note)	64 LSB	32 LSB	16 LSB	8 LSB	4 LSB	2 LSB	1 LSB	0.5 LSB

***Note:** Bit weight is for 2g 8bit data output. Typical value for reference only. Variation is specified in "Electrical Characteristics" section.

$11: Offset drift X MSB (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
--	--	--	--	--	XOFF [10]	XOFF [9]	XOFF [8]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): User level offset trim value for X axis

$12: Offset drift Y LSB (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
YOFF[7]	YOFF [6]	YOFF [5]	YOFF [4]	YOFF [3]	YOFF [2]	YOFF [1]	YOFF [0]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): User level offset trim value for Y axis

Bit	YOFF[7]	YOFF[6]	YOFF[5]	YOFF[4]	YOFF[3]	YOFF[2]	YOFF[1]	YOFF[0]
Weight (*Note)	64 LSB	32 LSB	16 LSB	8 LSB	4 LSB	2 LSB	1 LSB	0.5 LSB

***Note:** Bit weight is for 2g 8bit data output. Typical value for reference only. Variation is specified in "Electrical Characteristics" section.

$13: Offset drift Y MSB (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
--	--	--	--	--	YOFF [10]	YOFF [9]	YOFF [8]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): User level offset trim value for Y axis

Bit	YOFF[10]	YOFF[9]	YOFF[8]
Weight (*Note)	Polarity	256 LSB	128 LSB

***Note:** Bit weight is for 2g 8bit data output. Typical value for reference only. Variation is specified in "Electrical Characteristics" section.

$14: Offset drift Z LSB (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
ZOFF[7]	ZOFF[6]	ZOFF[5]	ZOFF[4]	ZOFF[3]	ZOFF[2]	ZOFF[1]	ZOFF[0]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): User level offset trim value for Z axis

Bit	ZOFF[7]	ZOFF[6]	ZOFF[5]	ZOFF[4]	ZOFF[3]	ZOFF[2]	ZOFF[1]	ZOFF[0]
Weight (*Note)	64 LSB	32 LSB	16 LSB	8 LSB	4 LSB	2 LSB	1 LSB	0.5 LSB

***Note:** Bit weight is for 2g 8bit data output. Typical value for reference only. Variation is specified in "Electrical Characteristics" section.

$15: Offset drift Z MSB (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
--	--	--	--	--	ZOFF[10]	ZOFF[9]	ZOFF[8]	Function
0	0	0	0	0	0	0	0	Default

Signed byte data (2's compliment): User level offset trim value for Z axis

Bit	ZOFF[10]	ZOFF[9]	ZOFF[8]
Weight (*Note)	Polarity	256 LSB	128 LSB

***Note:** Bit weight is for 2g 8bit data output. Typical value for reference only. Variation is specified in "Electrical Characteristics" section.

$16: Mode control register (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
--	DRPD	SPI3W	STON	GLVL[1]	GLVL[0]	MODE[1]	MODE[0]	Function
0	0	0	0	0	0	0	0	Default

MODE[1:0]	**Function**
00	Standby Mode
01	Measurement Mode
10	Level Detection Mode
11	Pulse Detection Mode

GLVL [1:0]

00: 8G is selected for measurement range. Detection is 8G range.

01: 2G is selected for measurement range. Detection is 8G range.

10: 4G is selected for measurement range. Detection is 8G range.

STON

0: Self test is not enabled

1: Self test is enabled

SPI3W

0: SPI is 4 wire mode

1: SPI is 3 wire mode

DRPD

0: Data ready status is output to INT1/DRDY PIN

1: Data ready status is not output to INT1/DRDY PIN

$17: Interrupt latch reset (Read/Write

D7	D6	D5	D4	D3	D2	D1	D0	Bit
--	--	--	--	--	--	CLR_INT2	CLR_INT1	Function
0	0	0	0	0	0	0	0	Default

CLR_INT1

1: Clear “INT1” and LDX/LDY/LDZ or PDX/PDY/PDZ bits in “Detection source” register depending on “Detection control” register setting.

0: Do not clear “INT1” LDX/LDY/LDZ or PDX/PDY/PDZ bits in “Detection source” register.

CLR_INT2

1: Clear “INT2” and LDX/LDY/LDZ or PDX/PDY/PDZ bits in “Detection source” register depending on “Detection control” register setting.

0: Do not clear “INT2” and LDX/LDY/LDZ or PDX/PDY/PDZ bits in “Detection source” register.

$18: Control 1 (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
DFBW	THOPT	ZDA	YDA	XDA	INTREG[1]	INTREG[0]	INTPIN	Function
0	0	0	0	0	0	0	0	Default

INTPIN

0: INT1 pin is routed to “INT1” register and INT2 pin is routed to “INT2” register.

1: INT2 pin is routed to “INT1” register and INT1 pin is routed to “INT2” register.

INTREG[1:0]	“INT1” register bit	“INT2” register bit
00	Level Detection	Pulse Detection
01	Pulse Detection	Level Detection
10	Single pulse detection (*Note)	Pulse Detection

Note: Assigned to single pulse detection even if double pulse detection is selected. “Double pulse detection selected” means “Time window for 2nd pulse” is not equal zero. When double pulse detection is selected, INT1 register bit is not able to be cleared by setting CLR_INT1 bit. It’s cleared by setting CLR_INT2 bit. In this case, setting CLR_INT2 clears both INT1 and INT2 register bits and reset detecting operation itself.

XDA

1: X axis is disabled for detection.

0: X axis is enabled for detection.

YDA

1: Y axis is disabled for detection.

0: Y axis is enabled for detection.

ZDA

1: Z axis is disabled for detection.

0: Z axis is enabled for detection.

THOPT (This bit is valid for level detection only, not valid for pulse detection)

0: Threshold value is absolute only

1: Positive/Negative threshold value is available.

DFBW

0: Digital filter band width is 62.5 Hz

1: Digital filter band width is 125 Hz

$19: Control 2 (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
--	--	--	--	--	DRVO	PDPL	LDPL	Function
0	0	0	0	0	0	0	0	Default

LDPOL

0: Level detection polarity is positive and detecting condition is OR 3 axes.

1: Level detection polarity is negative detecting condition is AND 3 axes.

PDPOL

0: Pulse detection polarity is positive and detecting condition is OR 3 axes.

1: Pulse detection polarity is negative and detecting condition is AND 3 axes.

DRVO

0: Standard drive strength on SDA/SDO pin

1: Strong drive strength on SDA/SDO pin

$1A: Level detection threshold limit value (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
LDTH[7]	LDTH[6]	LDTH[5]	LDTH[4]	LDTH[3]	LDTH[2]	LDTH[1]	LDTH[0]	Function
0	0	0	0	0	0	0	0	Default

LDTH[7:0]: Level detection threshold value. If THOPT bit in Detection Control Register is “0”, it is unsigned 7 bits value and LDTH[7] should be “0”. If THOPT bit is “1”, it is signed 8 bits value.

$1B: Pulse detection threshold limit value (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
XPDTH	PDTH[6]	PDTH[5]	PDTH[4]	PDTH[3]	PDTH[2]	PDTH[1]	PDTH[0]	Function
0	0	0	0	0	0	0	0	Default

PDTH[6:0]: Pulse detection threshold value (unsigned 7 bits).

XPDTH: This bit should be “0”.

$1C: Pulse duration value (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
PD[7]	PD[6]	PD[5]	PD[4]	PD[3]	PD[2]	PD[1]	PD[0]	Function
0	0	0	0	0	0	0	1	Default

Min: PD[7:0] = 4’h01 = 0.5 ms

Max: PD[7:0] = 4’hFF = 127 ms

1 LSB = 0.5 ms

$1D: Latency time value (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
LT[7]	LT[6]	LT[5]	LT[4]	LT[3]	LT[2]	LT[1]	LT[0]	Function
0	0	0	0	0	0	0	1	Default

Min: LT[7:0] = 8’h01 = 1 ms

Max: LT[7:0] = 8’hFF = 255 ms

1 LSB = 1 ms

$1E: Time window for 2nd pulse value (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0	Bit
TW[7]	TW[6]	TW[5]	TW[4]	TW[3]	TW[2]	TW[1]	TW[0]	Function
0	0	0	0	0	0	0	0	Default

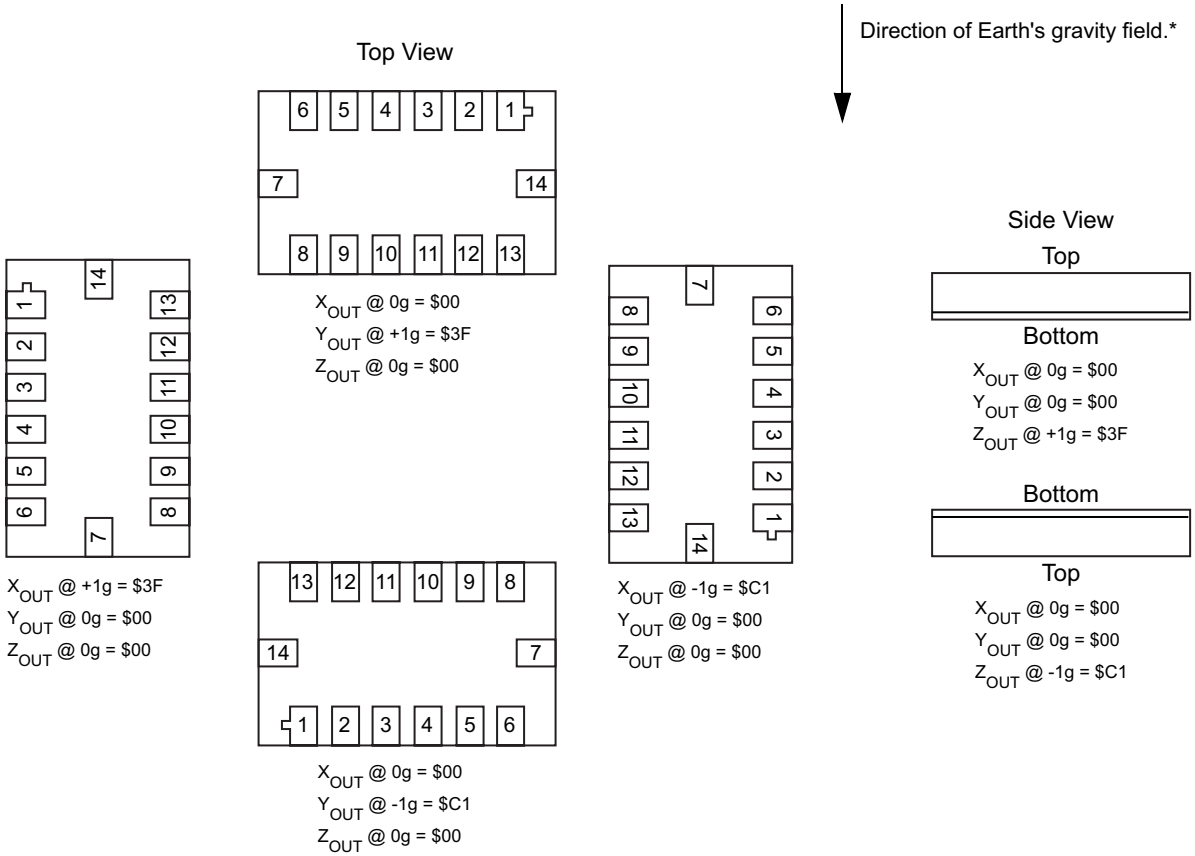
Min: TW[7:0] = 8’h01 = 0 ms (Single pulse detection)

Max: TW[7:0] = 8’hFF = 255 ms

1 LSB = 1 ms

SENSING DIRECTION AND OUTPUT RESPONSE

The following figure shows sensing direction and the output response for 2g mode.



* When positioned as shown, the Earth's gravity will result in a positive 1g output.

Figure 17. Sensing Direction and Output Response at 2g Mode

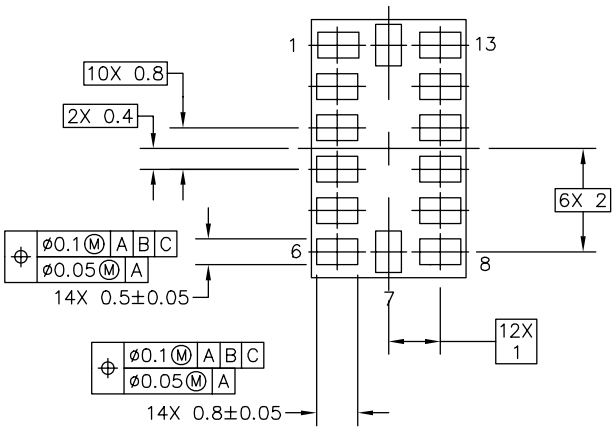
Table 8. Acceleration vs. Output

FS Mode	Acceleration	Output
2g Mode	-2g	$80
	-1g	$C1
	0g	$00
	+1g	$3F
	+2g	$7F
4g Mode	-4g	$80
	-1g	$E1
	0g	$00
	+1g	$1F
	+4g	$7F
8g Mode	-8g	$80
	-1g	$F1
	0g	$00
	+1g	$0F
	+8g	$7F

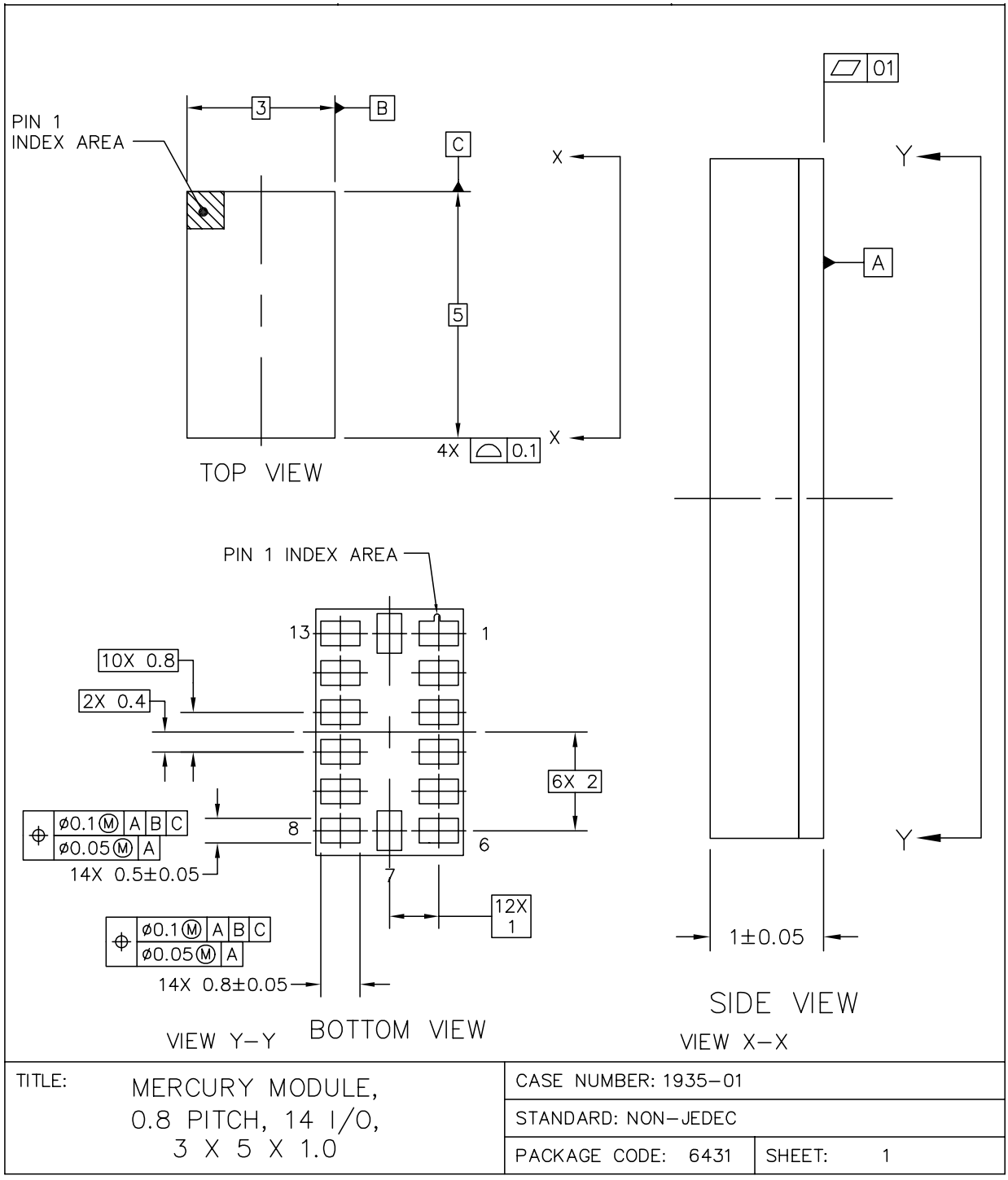
MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package.

With the correct footprint, the packages will self-align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.



PACKAGE DIMENSIONS



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		STANDARD: NON–JEDEC	
		PACKAGE CODE: 6431	SHEET: 1

CASE 1935-01
ISSUE 0
14-LEAD LGA

PACKAGE DIMENSIONS

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

TITLE:	MECURY MODULE, 0.8 PITCH, 14 I/O, 3 X 5 X 1.0	CASE NUMBER: 1935–01	
		STANDARD: NON–JEDEC	
		PACKAGE CODE: 6431	SHEET: 2

CASE 1935-01
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