KS57C2016
4-BIT CMOS Microcontroller

Product Specification

OVERVIEW

The KS57C2016 single-chip CMOS microcontroller is designed for very high performance using Samsung's newest 4-bit CPU core. With an up-to-20-digit LCD direct drive capability and up to 40 pins for LCD segment data output, a versatile 16-bit timer/counter with pulse width modulation and data capture functions, and its large ROM size, the "2016" offers you an excellent design solution for a wide variety of LCD applications.

Up to 56 pins of the 100-pin QFP package can be dedicated to I/O. Eight vectored interrupts provide fast response to internal and external events. In addition, the 2016's advanced CMOS technology ensures low power consumption and a wide operating voltage range.

FEATURES

Memory
- 512 × 4-bit RAM
- 16,384 × 8-bit ROM

56 I/O Pins
- I/O: 40 pins (8 n-channel open-drain pins)
- Input only: 4 pins
- Output only: 12 pins

LCD Controller/Driver
- Maximum 20-digit LCD direct drive capability
- 28, 32, 36, and 40 segment outputs selectable
- Display modes: Static, 1/2 duty (1/2 bias)
- 1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)

8-Bit Basic Timer
- 4 interval timer functions

8-Bit Timer/Counter
- Programmable 8-bit timer
- External event counter
- Arbitrary clock output
- External clock signal divider
- Serial I/O interface clock generator

16-Bit Timer/Counter
- Programmable 16-bit timer
- External event counter
- Arbitrary clock output
- External clock signal divider
- Capture function
- 16-bit PWM output function

Watch Timer
- Time interval generation: 0.5s, 3.9 ms at 32768 Hz
- 4 frequency outputs (BUZ)
- Clock generation for LCD

8-Bit Serial I/O Interface
- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal/external clock source

Interrupts
- 5 internal vectored interrupts
- 3 external vectored interrupts
- 2 quasi-interrupts

Bit Sequential Carrier
- Supports 16-bit serial data transfer in arbitrary format

Memory-Mapped I/O Structure
- Data memory bank 15

Two Power-Down Modes
- Idle (only CPU clock stops)
- Stop (system clock stops)

Oscillation Sources
- Crystal, ceramic, or RC for main system clock
- Crystal for subsystem clock
- Main system clock frequency: 4.19 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times
- 0.95, 1.91, 15.3 μs at 4.19 MHz
- 122 μs at 32.768 kHz

Operating Temperature
- – 40 °C to 85 °C

Operating Voltage Range
- 2.7 V to 6.0 V

Package Type
- 100-pin QFP

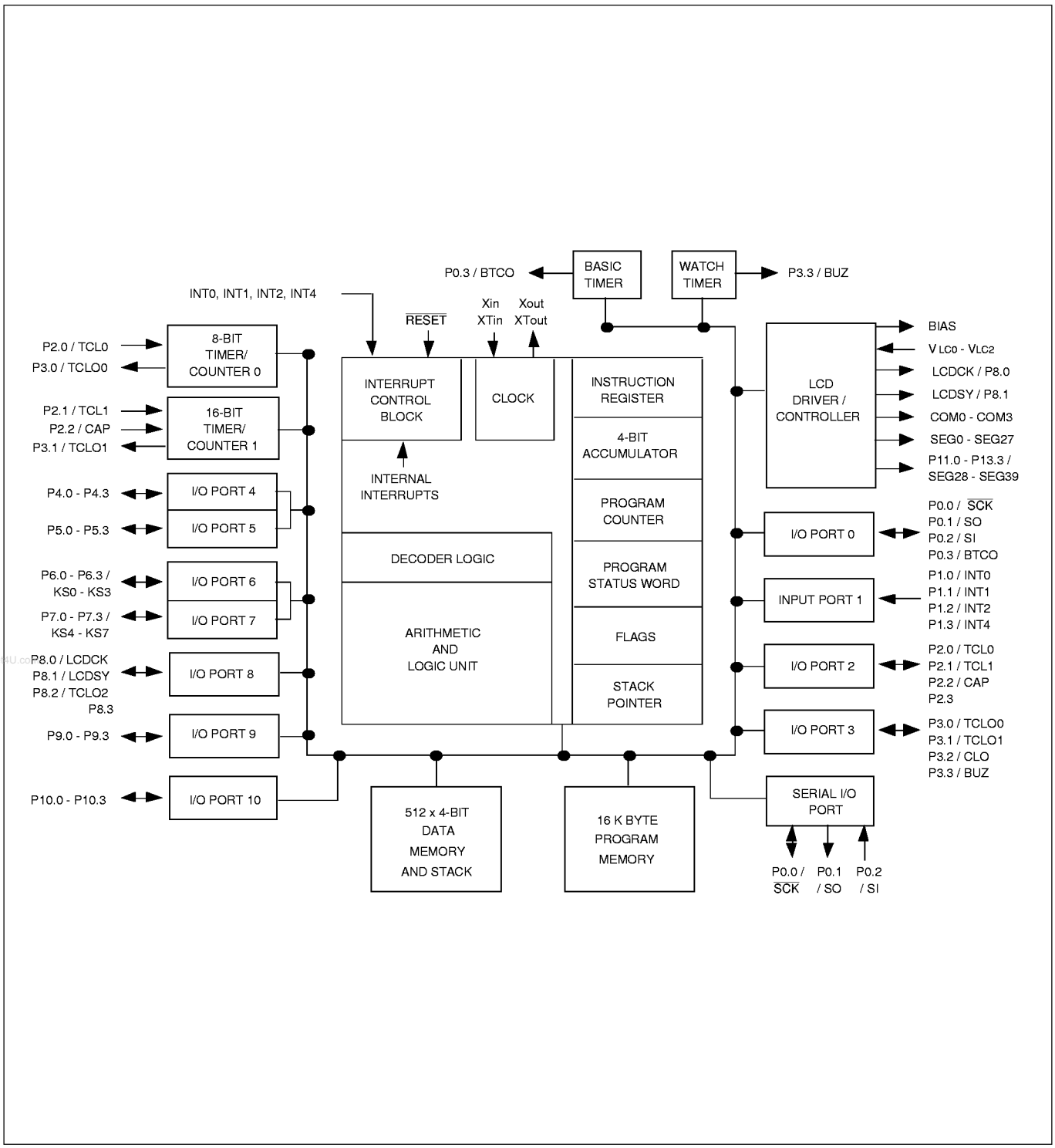


Figure 1. KS57C2016 Block Diagram

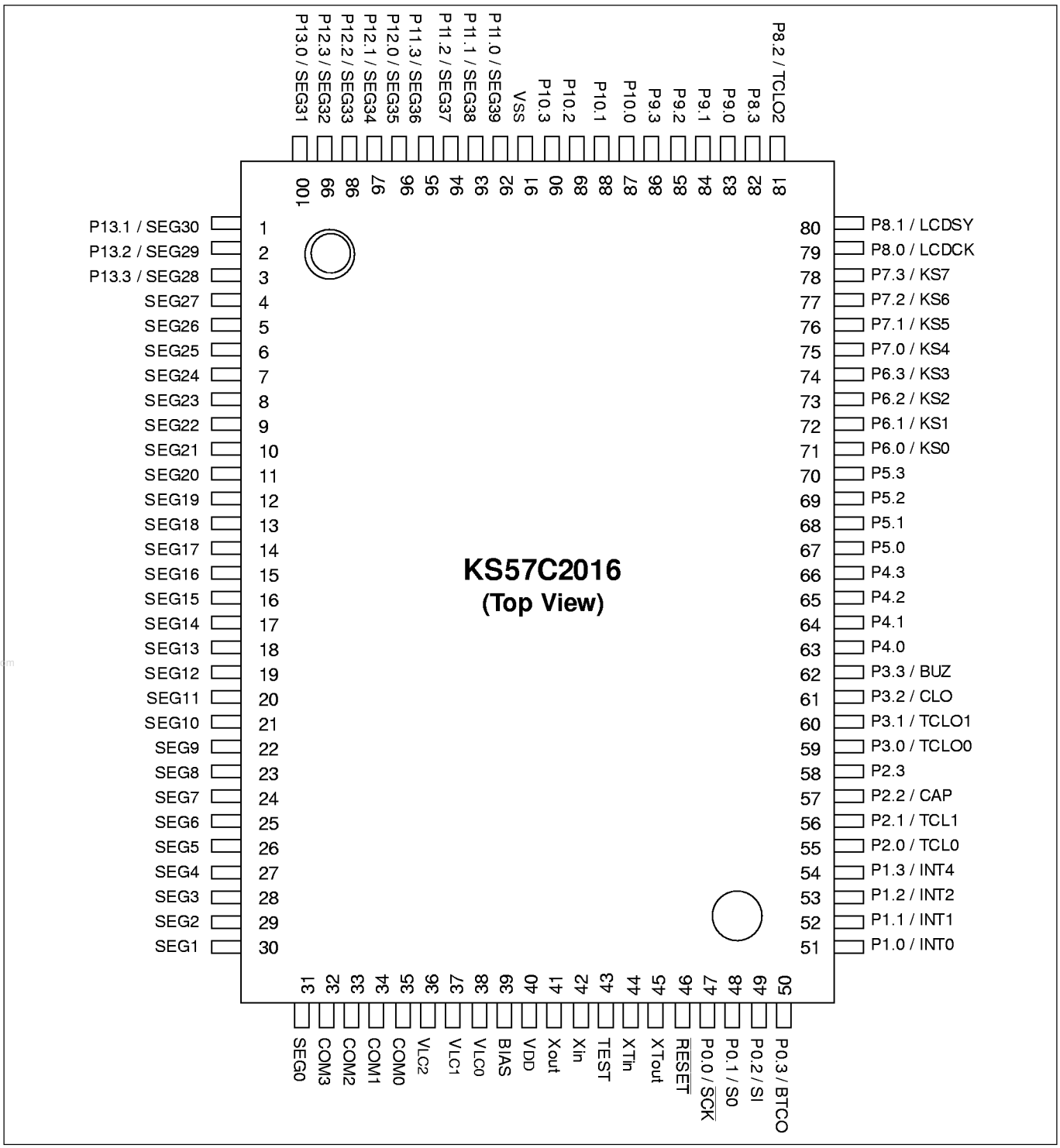


Figure 2. KS57C2016 Pin Assignments (100-QFP)

Table 1. KS57C2016 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable	47 48 49 50	$\overline{SCK}$ SO SI BTCO
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 3-bit pull-up resistors are assignable by software to pins P1.0, P1.1, and P1.2.	51 52 53 54	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	Same as port 0	55 56 57 58	TCL0 TCL1 CAP —
P3.0 P3.1 P3.2 P3.3	I/O	Same as port 0	59 60 61 62	TCLO0 TCLO1 CLO BUZ
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. N-channel open-drain output up to 9volts. 1-, 4-, and 8-bit read/write and test is possible. Ports 4 and 5 can be paired to support 8-bit data transfer. Pull-up resistors are assignable to individual pins by mask option.	63–66 67–70	— —
P6.0–P6.3 P7.0–P7.3	I/O	4-bit I/O ports. Port 6 pins are individually software configurable as input or output. 1-bit and 4-bit read/write and test is possible. 4-bit pull-up resistors are software assignable. Ports 6 and 7 can be paired to enable 8-bit data transfer.	71–74 75–78	KS0–KS3 KS4–KS7
P8.0 P8.1 P8.2 P8.3	I/O	Same as port 0.	79 80 81 82	LCDCK LCDSY TCLO2 —
P9.0–P9.3 P10.0–P10.3	I/O	Same as port 0.	84–86 87–90	— —
P11.0–P13.3	O	Output port for 1-bit data (for use as CMOS driver only)	92–100, 1–3	SEG28– SEG39
$\overline{SCK}$	I/O	Serial I/O interface clock signal	47	P0.0
SO	I/O	Serial data output	48	P0.1
SI	I/O	Serial data input	49	P0.2
BTCO	I/O	Basic interval timer clock output	50	P0.3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. Only INT0 is synchronized with the system clock.	51–52	P1.0, P1.1
INT2	I	Quasi-interrupt with detection of rising edges	53	P1.2
INT4	I	External interrupt with detection of rising or falling edges	54	P1.3

Table 1. KS57C2016 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
TCL0	I/O	External clock input for timer/counter 0	55	P2.0
TCL1	I/O	External clock input for timer/counter 1	56	P2.1
CAP	I/O	Capture pin for timer/counter 1 data capture values and external clock input for 8-bit timer/counter 1B	57	P2.2
TCLO0	I/O	Timer/counter 0 clock output	59	P3.0
TCLO1	I/O	Timer/counter 1 clock output	60	P3.1
TCLO2	I/O	8-bit timer/counter 1B clock output	81	P8.2
CLO	I/O	System clock output	61	P3.2
BUZ	I/O	2 kHz or 4 kHz frequency output for buzzer sound	62	P3.3
KS0–KS7	I/O	Quasi-interrupt input with falling edge detection	71–78	P6.0–P7.3
LCDCK	I/O	LCD clock output for display expansion	79	P8.0
LCDSY	I/O	LCD syncronization clock output for display expansion	80	P8.1
SEG0–SEG27	O	LCD segment data output	31, 30–4	—
SEG28–SEG39	O	1-bit LCD segment data output	92–100, 1–3	P11.0–P13.3
COM0–COM3	O	Common signal output for LCD display	35–32	—
V_{LC0}–V_{LC2}	—	LCD power supply. Voltage dividing resistors are assignable by mask option	38–36	—
TEST	I	Test signal input (must be connected to V_{SS})	43	—
V_{DD}	—	Main power supply	40	—
V_{SS}	—	Ground	91	—
$\overline{RESET}$	I	Reset signal	46	—
BIAS	—	LCD power control	39	—
X_{in}, X_{out}	—	Crystal, ceramic, or R/C oscillator signal for main system clock. (For external clock input, use X_{in} and input X_{in}'s reverse phase to X_{out})	42, 41	—
XT_{in}, XT_{out}	—	Crystal oscillator signal for subsystem clock. (For external clock input, use XT_{in} and input XT_{in}'s reverse phase to XT_{out})	44, 45	—

NOTE: Pull-up resistors for ports 0, 2, 3, and 6–10 are automatically disabled when they are configured to output mode.

Table 2. Supplemental KS57C2016 Pin Data

Pin Numbers	Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
1–3	P13.1–P13.3	SEG30–SEG28	O	Low	9
4–31	SEG27–SEG0	—	O	Low	7
35–32	COM0–COM3	—	O	Low	8
38–36	V_{LC0}–V_{LC2}	—	—	—	—
39	BIAS	—	—	—	—
40	V_{DD}	—	—	—	—
42, 41	X_{in}, X_{out}	—	—	—	—
43	TEST	—	I	—	—
44, 45	XT_{in}, XT_{out}	—	—	—	—
46	$\overline{RESET}$	—	I	—	2
47–50	P0.0–P0.3	$\overline{SCK}$, SO, SI, BTCO	I/O	Input	6
51–53	P1.0–P1.2	INT0, INT1, INT2	I	Input	3
54	P1.3	INT4	I	Input	2
55–58	P2.0–P2.2	TCL0, TCL1, CAP	I/O	Input	6
58	P2.3	—	I/O	Input	6
59–62	P3.0–P3.3	TCLO0, TCLO1, CLO, BUZ	I/O	Input	5
63–66	P4.0–P4.3	—	I/O	(1)	10
67–70	P5.0–P5.3	—	I/O	(1)	10
71–74	P6.0–P6.3	KS0–KS3	I/O	Input	6
75–78	P7.0–P7.3	KS4–KS7	I/O	Input	6
79–81	P8.0–P8.2	LCDCK, LCDSY, TCLO2	I/O	Input	5
82	P8.3	—	I/O	Input	5
83–86	P9.0–P9.3	—	I/O	Input	5
87–90	P10.0–P10.3	—	I/O	Input	5
91	V_{SS}	—	—	—	—
92–95	P11.0–P11.3	SEG39–SEG36	O	Low	9
96–99	P12.0–P12.3	SEG35–SEG32	O	Low	9
100	P13.0	SEG31	O	Low	9

NOTES:
1. When pull-up resistors are provided, high level; when pull-up resistors are not provided, high impedance.
2. Pin circuit diagrams are provided below.

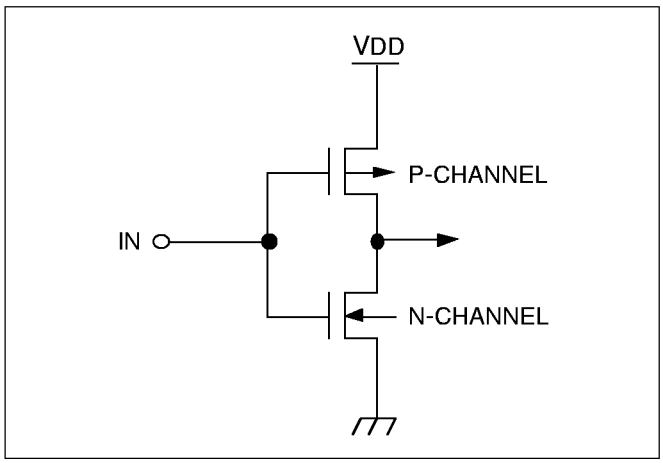


Figure 3. Pin Circuit Type 1

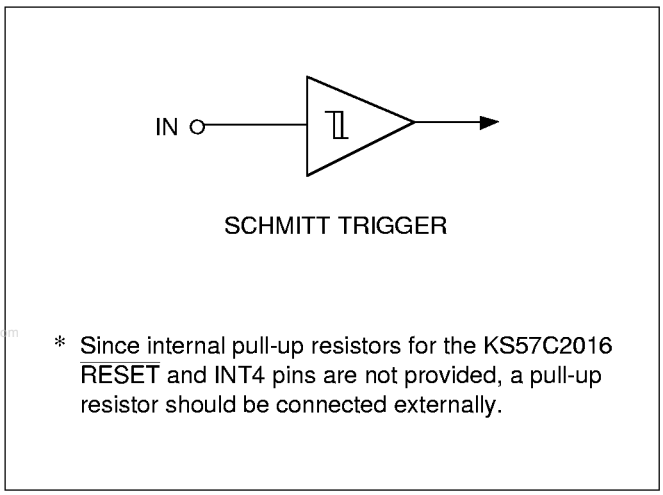


Figure 4. Pin Circuit Type 2

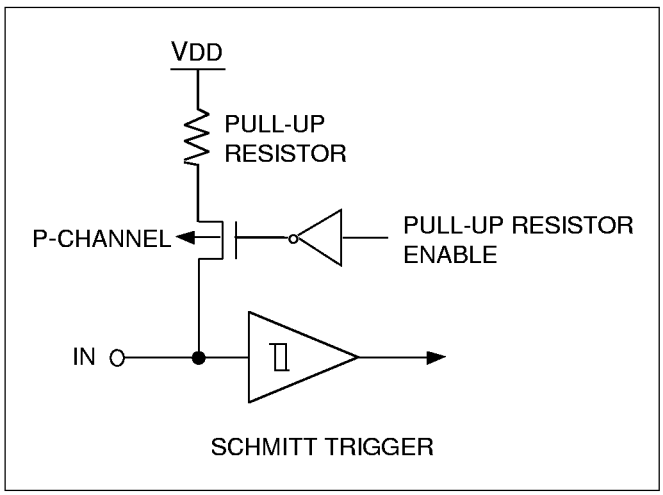


Figure 5. Pin Circuit Type 3

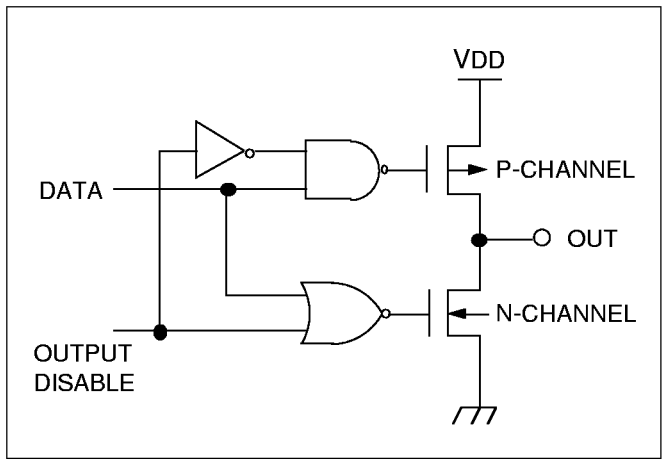


Figure 6. Pin Circuit Type 4

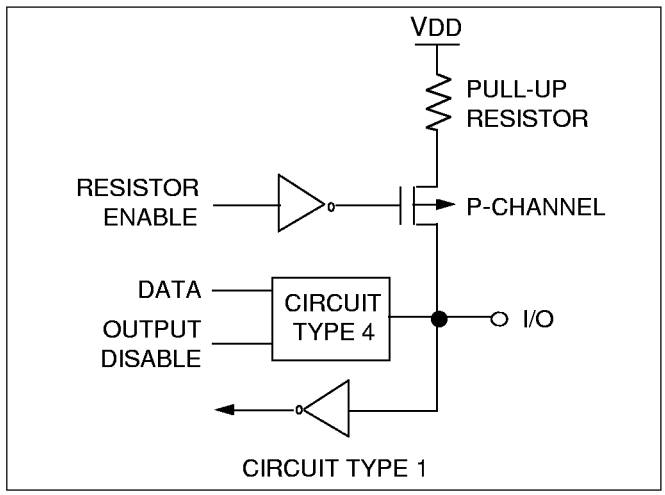


Figure 7. Pin Circuit Type 5

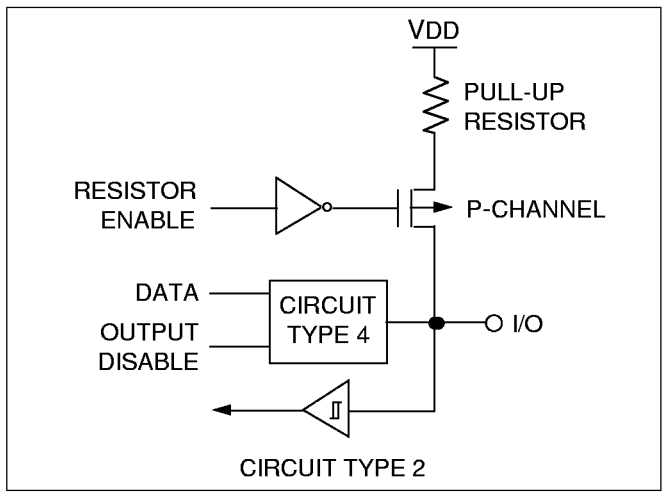


Figure 8. Pin Circuit Type 6

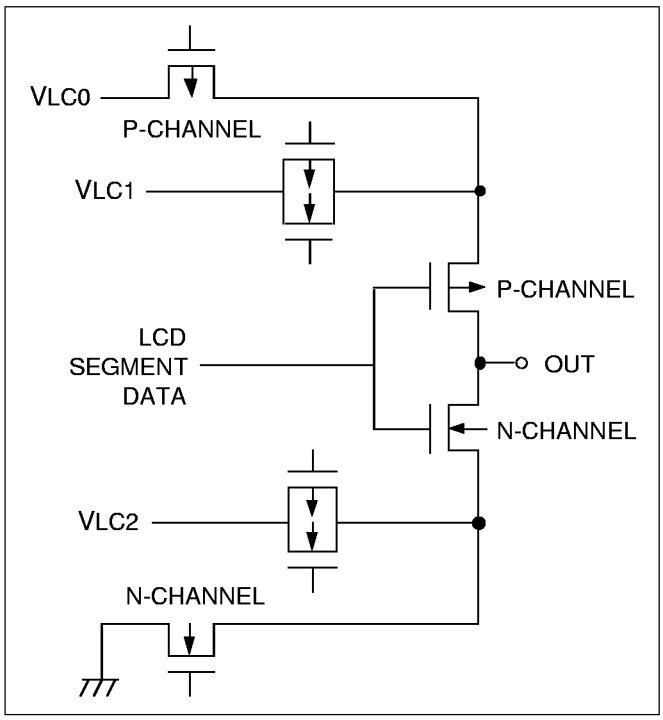


Figure 9. Pin Circuit Type 7

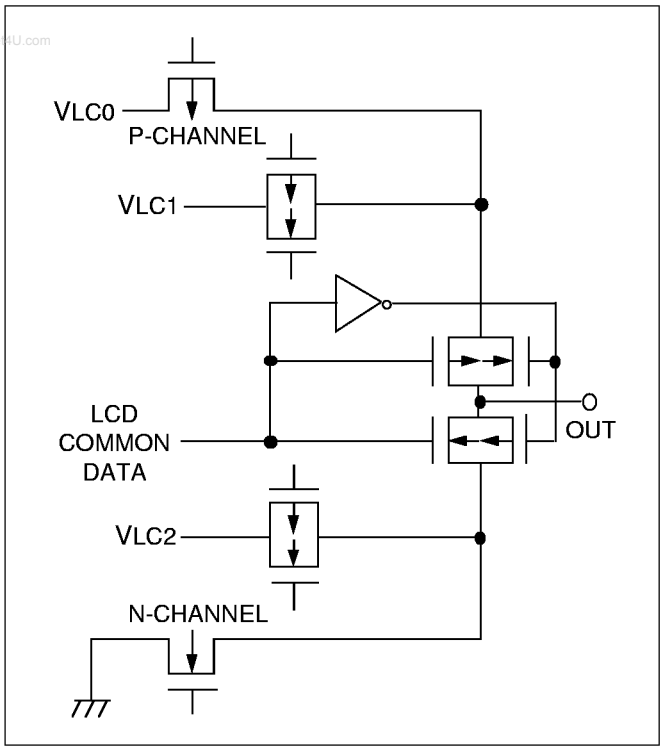


Figure 10. Pin Circuit Type 8

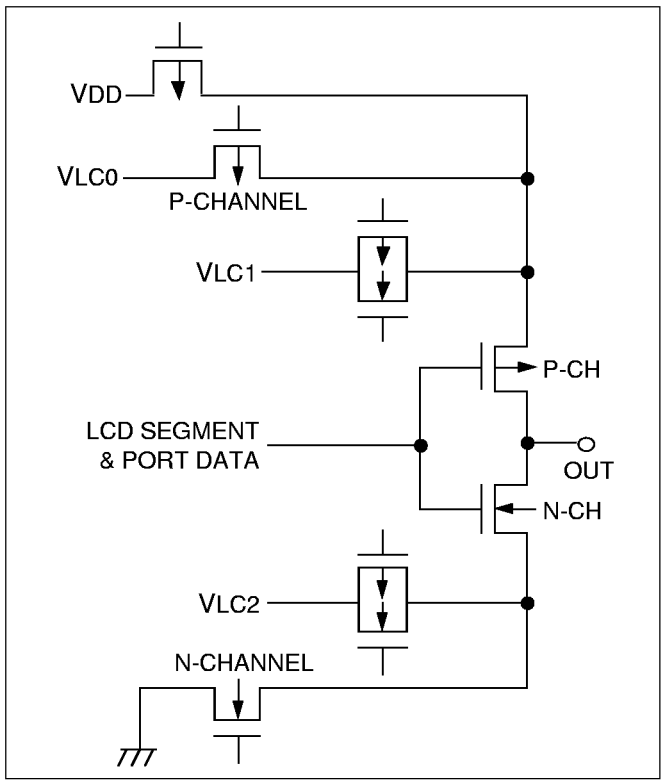


Figure 11. Pin Circuit Type 9

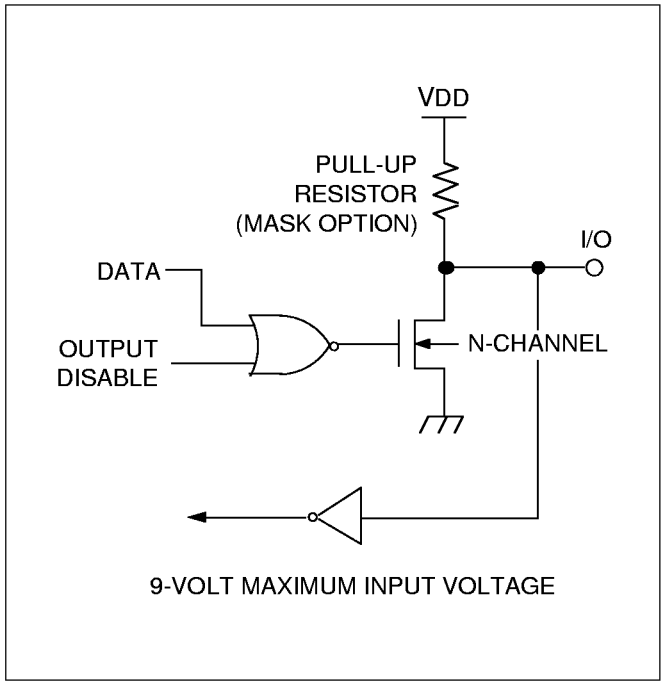


Figure 12. Pin Circuit Type 10

CAPACITOR CONNECTION METHOD

In KS57C2016 applications, capacitors should be connected as shown in Figure 13 in order to reduce noise and static electricity:

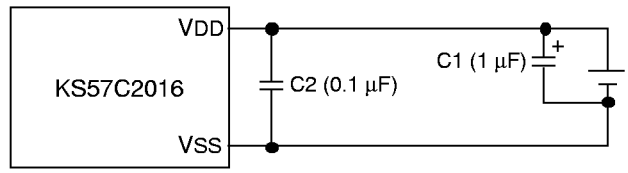


Figure 13. Capacitor Connection Diagram

When making a PCB using the KS57C2016, we recommend the following:

— Connect C1 as near as possible to the power input terminal.

— Connect C2 on the V_{DD} and V_{SS} line in the PCB.

— Make the V_{DD}–C2–V_{SS} line in the PCB as short as possible.

PROGRAM MEMORY (ROM)

The ROM map for the KS57C2016 is mask programmed at the factory. In its standard configuration, the device's 16,384 × 8-bit program memory has four areas that are directly addressable by the program counter (PC):

- 16-byte area for vector addresses
- 96-byte instruction reference area
- 16-byte general-purpose area
- 16,256-byte general-purpose area

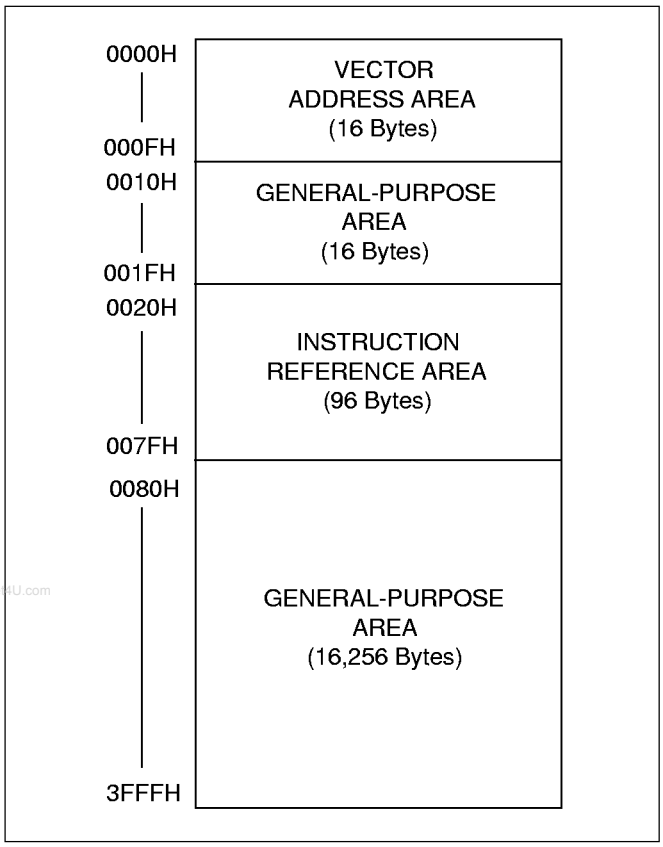


Figure 14. ROM Map

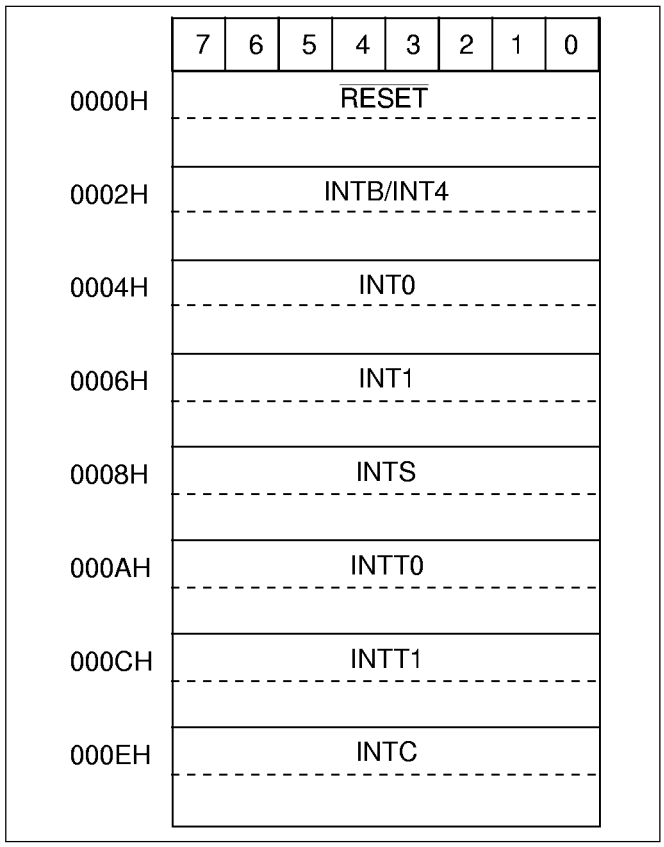


Figure 15. Vector Address Map

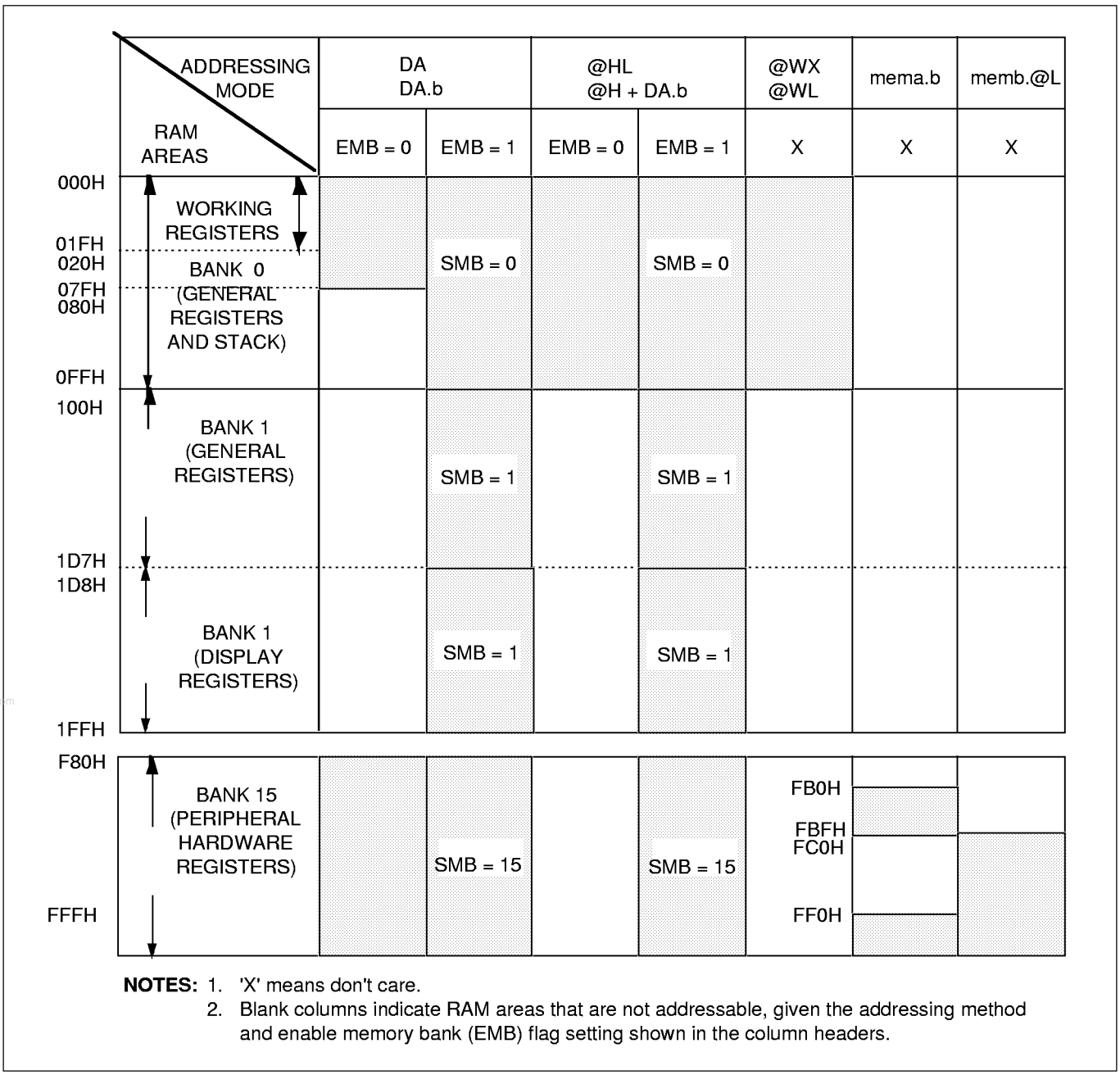
DATA MEMORY (RAM)

In its standard configuration, the 512× 4 -bit data memory has five areas:

- 32 ×4-bit working register area
- 224× 4 -bit general-purpose area (also used as stack area)
- 216× 4 -bit general-purpose area
- 40 ×4-bit area for LCD data
- 128× 4-bit area for memory-mapped I/O addresses

I/O MAP FOR HARDWARE REGISTERS

Table 3 contains detailed information about I/O mapping for peripheral hardware in bank 15 (register locations F80H–FFFH).



NOTES: 1. 'X' means don't care.
2. Blank columns indicate RAM areas that are not addressable, given the addressing method and enable memory bank (EMB) flag setting shown in the column headers.

Figure 16. Data Memory (RAM) Address Structure

Table 3. I/O Map for Memory Bank 15

Memory Bank 15						Addressing Mode			
Address	**Register**	**Name**				**R/W**	**1-Bit**	**4-Bit**	**8-Bit**
F81H–F80H	SP	Stack Pointer				R/W	No	No	Yes
F85H	BMOD	Basic Timer Mode Register				W	.3	Yes	No
F87H–F86H	BCNT	Basic Timer Counter Register				R	No	No	Yes
F89H–F88H	WMOD	Watch Timer Mode Register				W	.3 (1)	No	Yes
F8DH–F8CH	LMOD	LCD Mode Register				W	.3	No	Yes
F8EH	LCON	LCD Control Register				W	No	Yes	No
F91H–F90H	TMOD0	Timer/Counter 0 Mode Register				W	.3	No	Yes
F92H		TOE1	TOE0	BOE	TOE2	R/W	Yes	Yes	No
F95H–F94H	TCNT0	Timer/Counter 0 Counter Register				R	No	No	Yes
F97H–F96H	TREF0	Timer/Counter 0 Reference Reg				W	No	No	Yes
FA0H	TMOD1A	Timer/Counter 1 Mode Register A				R/W	.3	Yes	No
FA1H	TMOD1B	Timer/Counter 1 Mode Register B					No		
FA2H	TMOD1C	Timer/Counter 1 Mode Register C					.3		No
FA3H	TMOD1D	Timer/Counter 1 Mode Register D					No		
FA5H–FA4H	TCNT1A	Timer/Counter 1 Counter Register A				R	No	No	Yes
FA7H–FA6H	TCNT1B	Timer/Counter 1 Counter Register B							Yes
FA9H–FA8H	TREF1A	Timer/Counter 1 Reference Reg A				R/W	No	No	Yes
FABH–FAAH	TREF1B	Timer/Counter 1 Reference Reg B							Yes
FADH–FACH	CREG1A	Capture Register 1A				R	No	No	Yes
FAFH–FAEH	CREG1B	Capture Register 1B							Yes
FB0H	PSW	IS1	IS0	EMB	ERB	R/W	Yes	Yes	Yes
FB1H		C (2)	SC2	SC1	SC0	R	No	No	
FB2H	IPR	Interrupt Priority Register				W	IME	Yes	No
FB3H	PCON	Power Control Register				W	No	Yes	No
FB4H	IMOD0	External Interrupt 0 Mode Register				W	No	Yes	No
FB5H	IMOD1	External Interrupt 1 Mode Register				W	No	Yes	No
FB6H	IMOD2	External Interrupt 2 Mode Register				W	N o	Yes	No
FB7H	SCMOD	System Clock Mode Register				W	Yes	No	No
FB8H		IE4	IRQ4	IEB	IRQB	R/W	Yes	Yes	No
FBAH		"0"	"0"	IEW	IRQW	R/W	Yes	Yes	No
FBBH		IEC	IRQC	IET1	IRQT1				
FBCH		"0"	"0"	IET0	IRQT0				

Table 3. I/O Map for Memory Bank 15 (Continued)

Memory Bank 15						Addressing Mode			
Address	Register	Name				R/W	1-Bit	4-Bit	8-Bit
FBDH		"0"	"0"	IES	IRQS	R/W	Yes	Yes	No
FBEH		IE1	IRQ1	IE0	IRQ0				
FBFH		"0"	"0"	IE2	IRQ2				
FC0H	BSC0	Bit Sequential Carrier 0				R/W	Yes	Yes	Yes
FC1H	BSC1	Bit Sequential Carrier 1							
FC2H	BSC2	Bit Sequential Carrier 2							Yes
FC3H	BSC3	Bit Sequential Carrier 3							
FD0H	CLMOD	Clock Mode Register				W	No	Yes	No
FD2H	CREG2A	Capture Register 2A				R	No	No	Yes
FD4H	CREG2B	Capture Register 2B							Yes
FD6H	CINTR	Capture Interrupt Register				R/W	Yes	Yes	No
FDDH–FDCH	PUMOD0	Pull-up Mode Register 0				W	No	No	Yes
FDFH–FDEH	PUMOD1	Pull-up Mode Register 1							
FE1H–FE0H	SMOD	SIO Mode Register				W	.3	No	Yes
FE5H–FE4H	SBUF	SIO Buffer Register				R/W	No	No	Yes
FE9H–FE8H	PMG1	Port Mode Group 1				W	No	No	Yes
FEBH–FEAH	PMG2	Port Mode Group 2							
FEDH–FECH	PMG3	Port Mode Group 3							
FEFH–FEEH	PMG4	Port Mode Group 4							
FF0H	P0	Port 0				R/W	Yes	Yes	No
FF1H	P1	Port 1				R			
FF2H	P2	Port 2				R/W			No
FF3H	P3	Port 3				R/W			
FF4H	P4	Port 4				R/W			Yes
FF5H	P5	Port 5				R/W			
FF6H	P6	Port 6				R/W			Yes
FF7H	P7	Port 7				R/W			
FF8H	P8	Port 8				R/W			No
FF9H	P9	Port 9				R/W			
FFAH	P10	Port 10				R/W			

NOTES:
1. Bit 3 in the WMOD register is read-only.
2. The carry flag can be read or written by specific bit manipulation instructions only.

BIT SEQUENTIAL CARRIER (BSC)

The bit sequential carrier (BSC) is a 16-bit general register that is mapped in data memory bank 15. Using the BSC, you can specify sequential addresses and bit locations using 1-bit indirect addressing (memb.@L).

BSC bit addressing is independent of the current EMB value. In this way, programs can process 16-bit data by moving the bit location sequentially and then incrementing or decrementing the value of the L register.

For 8-bit manipulations, the 4-bit register names BSC0 and BSC2 must be specified and the upper and lower 8 bits manipulated separately. If the values of the L register are 0H at BSC0.@L, the address and bit location assignment is FC0H.0. If the L register content is FH at BSC0.@L, the address and bit location assignment is FC3H.3.

Table 4. BSC Register Organization

Name	Address	Bit 3	Bit 2	Bit 1	Bit 0
BSC0	FC0H	BSC0.3	BSC0.2	BSC0.1	BSC0.0
BSC1	FC1H	BSC1.3	BSC1.2	BSC1.1	BSC1.0
BSC2	FC2H	BSC2.3	BSC2.2	BSC2.1	BSC2.0
BSC3	FC3H	BSC3.3	BSC3.2	BSC3.1	BSC3.0

☞ PROGRAMMING TIP — Using the BSC Register to Output 16-Bit Data

To use the bit sequential carrier (BSC) register to output 16-bit data (5937H) to the P3.0 pin:


```
        BITS    EMB
        SMB     15
        LD      EA,#37H         ;
        LD      BSC0,EA         ;   BSC0 ← A, BSC1 ← E
        LD      EA,#59H         ;
        LD      BSC2,EA         ;   BSC2 ← A, BSC3 ← E
        SMB     0
        LD      L,#0H           ;
AGN     LDB     C,BSC0.@L       ;
        LDB     P3.0,C          ;   P3.0 ← C
        INCS    L
        JR      AGN
        RET
```

INTERRUPTS

The KS57C2016 has three external interrupts, five internal interrupts and two quasi-interrupts. Table 5 shows the conditions for each interrupt generation. The request flags that allow these interrupts to be generated are cleared by hardware when the service routine is vectored. The quasi-interrupt's request flags must be cleared by software.

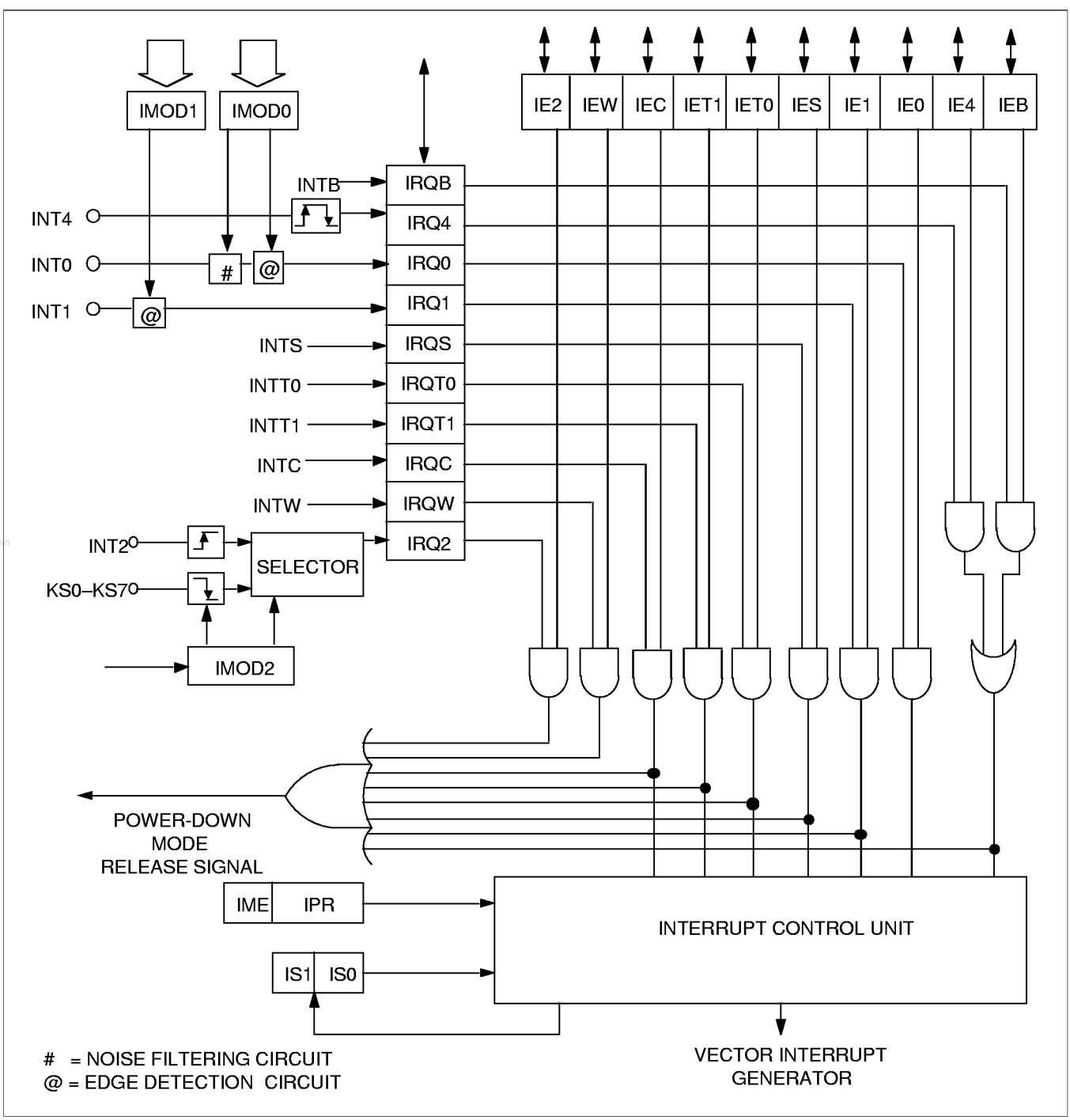


Figure 17. Interrupt Control Circuit Diagram

Table 5. Interrupt Request Flag Conditions and Priorities

Interrupt Source	Internal / External	Condition for IRQx Flag Setting	Interrupt Priority	Request Flag Name
INTB	I	Reference time interval signal from basic timer	1	IRQB
INT4	E	Both rising and falling edges detected at INT4	1	IRQ4
INT0	E	Rising or falling edge detected at INT0 pin	2	IRQ0
INT1	E	Rising or falling edge detected at INT1 pin	3	IRQ1
INTS	I	Completion signal for serial transmit-and-receive or receive-only operation	4	IRQS
INTT0	I	Signals for TCNT0 and TREF0 registers match	5	IRQT0
INTT1	I	Signals for TCNT1 and TREF1 registers match	6	IRQT1
INTC	I	When a capture function occurs (rising or falling edge detected at CAP pin)	7	IRQC
INT2 *	E	Rising edge detected at INT2 or else a falling edge is detected at any of the KS0–KS7 pins	—	IRQ2
INTW	I	Time interval of 0.5 s or 3.19 ms	—	IRQW

* The quasi-interrupt INT2 is only used for testing incoming signals.

INTERRUPT ENABLE FLAGS (IEx)

IEx flags, when set to "1", enable specific interrupt requests to be serviced. When the interrupt request flag is set to "1", an interrupt will not be serviced until its corresponding IEx flag is also enabled.

Table 6. Interrupt Enable and Request Flag

Address	Bit 3	Bit 2	Bit 1	Bit 0
FB8H	IE4	IRQ4	IEB	IRQB
FBAH	0	0	IEW	IRQW
FBBH	IEC	IRQC	IET1	IRQT1
FBCH	0	0	IET0	IRQT0
FBDH	0	0	IES	IRQS
FBEH	IE1	IRQ1	IE0	IRQ0
FBFH	0	0	IE2	IRQ2

NOTES:
1. IEx refers to all interrupt enable flags.
2. IRQx refers to all interrupt request flags.
3. IEx = "0" is interrupt disable mode.
4. IEx = "1" is interrupt enable mode.

INTERRUPT PRIORITY

The IPR register contains a global disable bit, IME, which disables all interrupt at once. If you clear the interrupt status flags (IS1 and IS0) to "0" in a interrupt service routine, a high-priority interrupt can be interrupted by low-priority interrupt (multi-level interrupt). Before the IPR can be modified by 4-bit write instructions, all interrupts must first be disabled by a DI instruction.

When all interrupts are low priority (the lower three bits of the IPR register are "0"), the interrupt requested first will have high priority. Therefore, the first-requested interrupt cannot be superseded by any other interrupt.

If two or more interrupt requests are received simultaneously, the priority level is determined according to the standard interrupt priorities, where the default priority is assigned by hardware when the lower three IPR bits = "0".

In this case, the higher-priority interrupt request is serviced and the other interrupt is inhibited. Then, when the high-priority interrupt is returned from its service routine by an IRET instruction, the inhibited service routine is started.

Table 7. Interrupt Priority Register Settings

IPR.2	IPR.1	IPR.0	Result of IPR Bit Setting
0	0	0	Process all interrupt requests at low priority
0	0	1	INTB and INT4
0	1	0	INT0
0	1	1	INT1
1	0	0	INTS
1	0	1	INTT0
1	1	0	INTT1
1	1	1	INTC

Table 8. Default Priorities

Source	Default Priority
INTB, INT4	1
INT0	2
INT1	3
INTS	4
INTT0	5
INTT1	6
INTC	7

☞ PROGRAMMING TIP — Setting the INT Interrupt Priority

Set the INT1 interrupt to high priority:

```
BITS    EMB
SMB     15
DI                  ;   IPR.3 (IME) ← 0
LD      A,#3H
LD      IPR,A
EI                  ;   IPR.3 (IME) ← 1
```

EXTERNAL INTERRUPTS

The external interrupt mode registers (IMOD0 and IMOD1) are used to control the triggering edge of the input signal at INT0 and INT1 respectively. The INT4 interrupt is an exception because its input signal generates an interrupt request on both rising and falling edges.

When a sampling clock rate of fxx/64 is used for INT0, an interrupt request flag must be cleared before 16 machine cycles have elapsed. Since the INT0 pin has a clock-driven noise filtering circuit built into it, please take the following precautions when you use it:

— To trigger an interrupt, the input signal width at INT0 must be at least two times wider than the pulse width of the clock selected by IMOD0. This is true even when the INT0 pin is used for general-purpose input.

— Since the INT0 input sampling clock does not operate during Stop or Idle mode, you cannot use INT0 to release power-down mode.

When modifying the IMOD0 and IMOD1 registers, it is possible to accidentally set an interrupt request flag. To avoid unwanted interrupts, take these precautions when writing your programs:

1. Disable all interrupts with a DI instruction.
2. Modify the IMOD0 or IMOD1 register.
3. Clear all relevant interrupt request flags.
4. Enable the interrupt by setting the appropriate IEx flag.
5. Enable all interrupts with an EI instruction.

Table 9. IMOD0 and IMOD1 Register Organization (4-Bit W)

IMOD0.3	0	IMOD0.1	IMOD0.0	Effect of IMOD0 Settings
0				Select CPU clock for sampling
1				Select fxx/64 sampling clock
	0	0	0	Rising edge detection
	0	0	1	Falling edge detection
	0	1	0	Both rising and falling edge detection
	0	1	1	IRQ0 flag cannot be set to "1"

0	0	0	IMOD1.0	Effect of IMOD1 Settings
0	0	0	0	Rising edge detection
0	0	0	1	Falling edge detection

EXTERNAL INTERRUPT 2 MODE REGISTER

The external interrupt 2 (INT2) mode register (IMOD2) is used to select INT2 and KS pins as interrupt input.

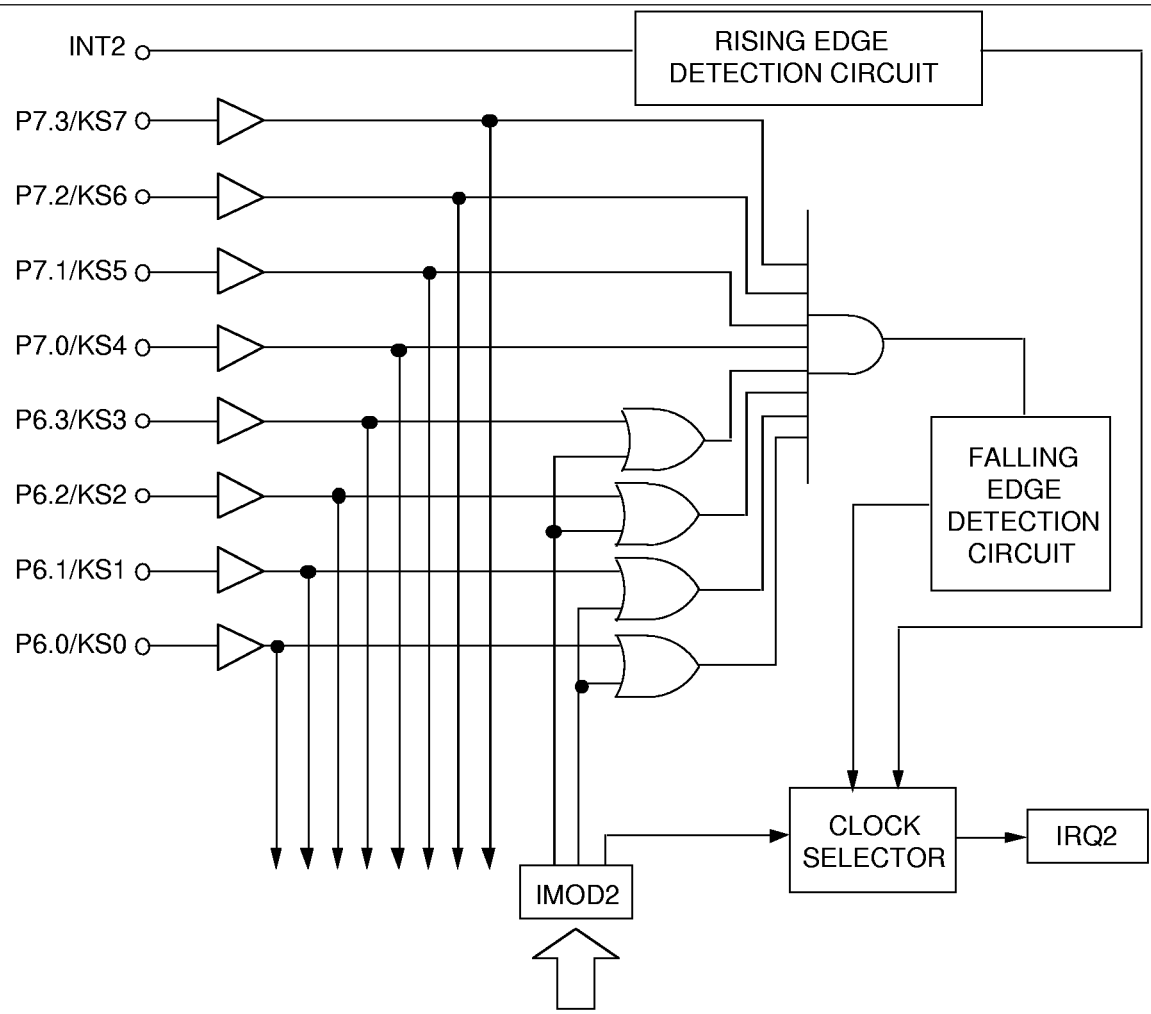
If a rising edge is detected at the INT2 pin, or when a falling edge is detected at any one of the KS0–KS7 pins, the IRQ2 flag is set to "1". This generates an interrupt request and a release signal for power-down mode.

To generate a key interrupt on a falling edge at KS0-KS7, all KS0-KS7 pins must be configured to input mode. KS4-KS7, in particular, must always be set to input mode.

If one or more of the pins which are configured as key Interrupt (KS0–KS7) are in Low input or Low output state, the key Interrupt can not be occured.

Table 10. IMOD2 Register Bit Settings (4-Bit W)

0	0	IMOD2.1	IMOD2.0	Effect of IMOD2 Settings
0	0	0	0	Select rising edge at INT2 pin
0	0	0	1	Select falling edge at KS4–KS7
0	0	1	0	Select falling edge at KS2–KS7
0	0	1	1	Select falling edge at KS0–KS7



NOTE: To generate a key interrupt on a falling edge at KS0–KS7, all KS0–KS7 pins must be configured to input mode. KS4–KS7, in particular, must always be configured to input mode.

Figure 17-1. Circuit Diagram for INT2 and KS0-KS7

OSCILLATOR CIRCUITS

The KS57C2016 microcontroller has two oscillator circuits: a main system clock circuit, and a subsystem clock circuit. The main system clock clock frequency can be divided by 4, 8, or 64 by manipulating PCON bits 1 and 0.

The system clock mode control register, SCMOD, lets you select the main system clock (fx) or a subsystem clock (fxt) as the CPU clock and to start (or stop) main system clock oscillation.

The watch timer, buzzer and LCD display operate normally with a subsystem clock source, since they operate at very slow speeds and with very low power consumption (as low as 122 μs at 32.768 kHz).

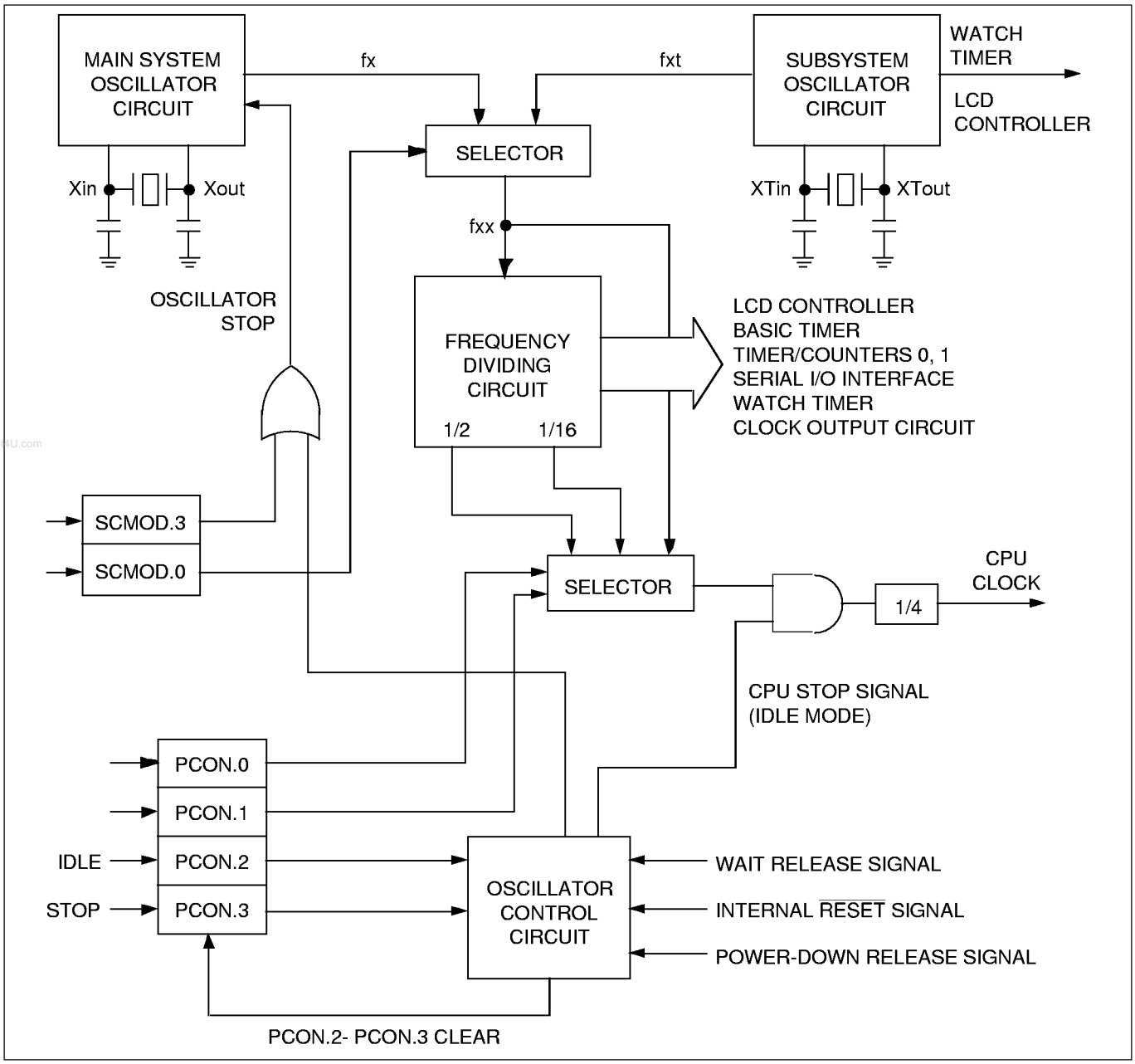


Figure 18. Clock Circuit Diagram

MAIN SYSTEM OSCILLATOR CIRCUITS

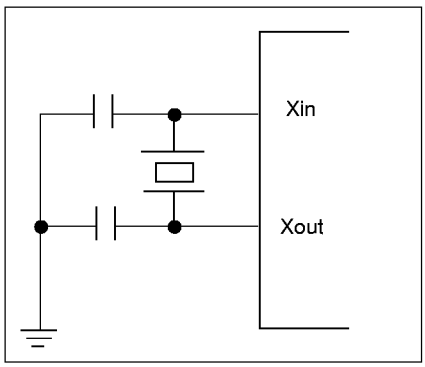


Figure 19. Crystal/Ceramic Oscillator (fx)

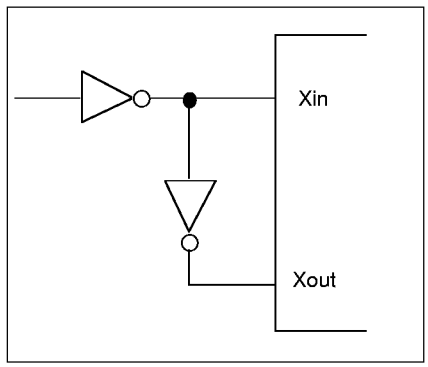


Figure 20. External Oscillator (fx)

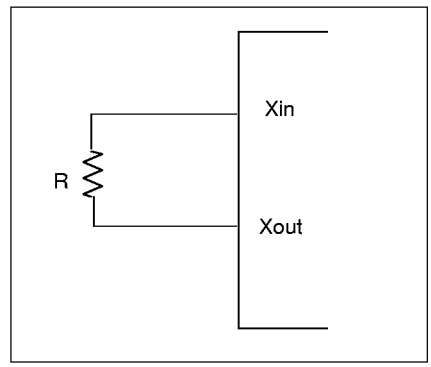


Figure 21. RC Oscillator (fx)

SUBSYSTEM OSCILLATOR CIRCUITS

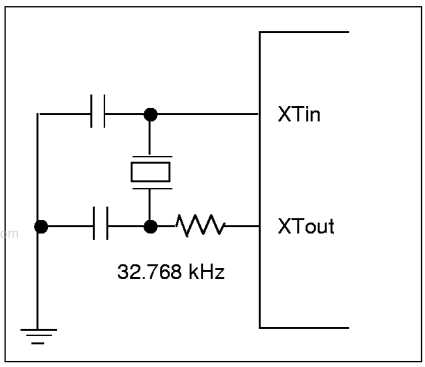


Figure 22. Crystal/Ceramic Oscillator (fxt)

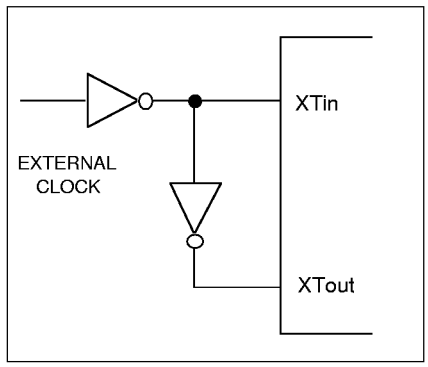


Figure 23. External Oscillator (fxt)

POWER CONTROL REGISTER (PCON)

The power control register, PCON, is used to select the CPU clock frequency and to control CPU operating and power-down modes.

PCON bits 3 and 2 are controlled by the STOP and IDLE instructions which engage the Idle and Stop power-down modes. Idle and Stop modes can be initiated by these instructions, regardless of the current value of the enable memory bank flag (EMB).

Table 11. Power Control Register (PCON) Organization

PCON Bit Settings		Resulting CPU Operating Mode
PCON.3	PCON.2	
0	0	Normal CPU operating mode
0	1	Idle power-down mode
1	0	Stop power-down mode

PCON Bit Settings		Resulting CPU Clock Frequency	
PCON.1	PCON.0	If SCMOD.0 = "0"	If SCMOD.0 = "1"
0	0	fx/64	—
1	0	fx/8	—
1	1	fx/4	fxt/4

☞ PROGRAMMING TIP — Setting the CPU Clock

To set the CPU clock to 0.95 μs at 4.19 MHz:

```
BITS    EMB
SMB     15
LD      A,#3H
LD      PCON,A
```

INSTRUCTION CYCLE TIMES

The unit of time that equals one machine cycle varies depending on whether the main system clock (fx) or a subsystem clock (fxt) is used, and on how the oscillator clock signal is divided (by 4, 8, or 64).

Table 12. Instruction Cycle Times for CPU Clock Rates

Selected CPU Clock	Resulting Frequency	Oscillation Source	Cycle Time (μs)
fx/64	65.5 kHz	fx = 4.19 MHz	15.3
fx/8	524.0 kHz		1.91
fx/4	1.05 MHz		0.95
fxt/4	8.19 kHz	fxt = 32.768 kHz	122.0

SYSTEM CLOCK MODE REGISTER (SCMOD)

The system clock mode register, SCMOD, is used to select the CPU clock and to control main system clock oscillation. Only its least significant and most significant bits can be manipulated by 1-bit write instructions. Bit 1 and bit 2 in the SCMOD register are always "0".

Subsystem clock oscillation cannot, of course, be stopped internally. Also, if you have selected fx as the CPU clock, setting SCMOD.3 to "1" will not stop main system clock oscillation. This can only be done by a STOP instruction.

Table 13. System Clock Mode Register (SCMOD) Organization (1-Bit W)

SCMOD Register Bit Settings		Resulting Clock Selection	
SCMOD.3	SCMOD.0	CPU Clock	fx Oscillation
0	0	fx	On
0	1	fxt	On
1	1	fxt	Off

SWITCHING THE CPU CLOCK

Together, bit settings in the power control register, PCON, and the system clock mode register, SCMOD, determine whether a main system or a subsystem clock is selected as the CPU clock. This makes it possible to switch dynamically between main and subsystem clocks and to modify operating frequencies.

NOTE

A clock switch operation does not go into effect immediately when you make the SCMOD and PCON register modifications — the previously selected clock continues to run for a certain number of machine cycles.

For example, you are using the default CPU clock (normal operating mode and a main system clock of fx/64) and you want to switch from the fx clock to a subsystem clock and to stop the main system clock. To do this, you first need to set SCMOD.0 to "1". This switches the clock from fx to fxt but allows main system clock oscillation to continue. Before the switch actually goes into effect, a certain number of machine cycles must elapse. After this time interval, you can disable main system clock oscillation by setting SCMOD.3 to "1".

This same 'stepped' approach must be taken to switch from a subsystem clock to the main system clock: first, clear SCMOD.3 to "0" to enable main system clock oscillation. Then, after a certain number of machine cycles have elapsed, select the main system clock by clearing all SCMOD values to logic zero.

Following a $\overline{\text{RESET}}$, CPU operation starts with the lowest main system clock frequency of 15.3 μs at 4.19MHz after the standard oscillation stabilization interval of 31.3 ms has elapsed. Table 14 details the number of machine cycles that must elapse before a CPU clock switch modification goes into effect.

Table 14. Elapsed Machine Cycles During CPU Clock Switch

<table>
<tr><td colspan="2" rowspan="2">AFTER
BEFORE</td><td colspan="6">SCMOD.0 = 0</td><td>SCMOD.0 = 1</td></tr>
<tr><td colspan="2">PCON.1 = 0</td><td colspan="2">PCON.1 = 1</td><td colspan="2">PCON.1 = 1</td><td></td></tr>
<tr><td rowspan="6">SCMOD.0 = 0</td><td>PCON.1 = 0</td><td colspan="2" rowspan="2">N/A</td><td colspan="2" rowspan="2">1 MACHINE CYCLE</td><td colspan="2" rowspan="2">1 MACHINE CYCLE</td><td rowspan="2">N/A</td></tr>
<tr><td>PCON.0 = 0</td></tr>
<tr><td>PCON.1 = 1</td><td colspan="2" rowspan="2">8 MACHINE CYCLES</td><td colspan="2" rowspan="2">N/A</td><td colspan="2" rowspan="2">8 MACHINE CYCLES</td><td rowspan="2">N/A</td></tr>
<tr><td>PCON.0 = 0</td></tr>
<tr><td>PCON.1 = 1</td><td colspan="2" rowspan="2">16 MACHINE CYCLES</td><td colspan="2" rowspan="2">16 MACHINE CYCLES</td><td colspan="2" rowspan="2">N/A</td><td rowspan="2">fx / 4fxt</td></tr>
<tr><td>PCON.0 = 1</td></tr>
<tr><td>SCMOD.0 = 1</td><td></td><td colspan="2">N/A</td><td colspan="2">N/A</td><td colspan="2">fx / 4fxt (M/C)</td><td>N/A</td></tr>
</table>

NOTES:
1. Even if oscillation is stopped by setting SCMOD.3 during main system clock operation, Stop mode is not entered.
2. Since the Xin input is connected internally to V_{SS} to avoid current leakage due to the crystal oscillator in Stop mode, do not set SCMOD.3 to "1" when an external clock is used as the main system clock.
3. When the system clock is switched to the subsystem clock, it is necessary to disable any interrupts which may occur during the time intervals shown in Table 14.
4. 'N/A' means 'not available'.

☞ PROGRAMMING TIP — Switching Between Main System and Subsystem Clock

1. Switch from the main system clock to the subsystem clock:

```
MA2SUB  BITS   SCMOD.0     ; Switches to subsystem clock
        CALL   DLY80       ; Delay 80 machine cycles
        BITS   SCMOD.3     ; Stop the main system clock
        RET
DLY80   LD     A,#0FH
DEL1    NOP
        NOP
        DECS   A
        JR     DEL1
        RET
```

2. Switch from the subsystem clock to the main system clock:

```
SUB2MA  BITR   SCMOD.3     ; Start main system clock oscillation
        CALL   DLY80       ; Delay 80 machine cycles
        BITR   SCMOD.0     ; Switch to main system clock
        RET
```

CLOCK OUTPUT CIRCUIT

The clock output circuit is used to output clock pulses to the CLO pin. The clock output mode register, CLMOD, is used to enable or disable clock output to the CLO pin and to select the CPU clock source and frequency.

To output a frequency, the clock output pin CLO/P3.2 must be set to output mode and the latch for the pin must be cleared to "0". Bit 2 in the CLMOD register must always be "0".

Table 15. Clock Output Mode Register (CLMOD) Organization

CLMOD Bit Settings		Resulting Clock Output	
CLMOD.1	**CLMOD.0**	**Clock Source**	**Frequency**
0	0	CPU clock (fx/4, fx/8, fx/64)	1.05 MHz, 524 kHz, 65.5 kHz, 8.19 kHz
0	1	fxx/8	524 kHz, 4.096 kHz
1	0	fxx/16	262 kHz, 2.048 kHz
1	1	fxx/64	65.5 kHz, 0.512 kHz

CLMOD.3	Result of CLMOD.3 Setting
0	Clock output is disabled
1	Clock output is enabled

NOTE: Frequencies assume that fx is 4.19 MHz and fxt is 32.768 kHz.

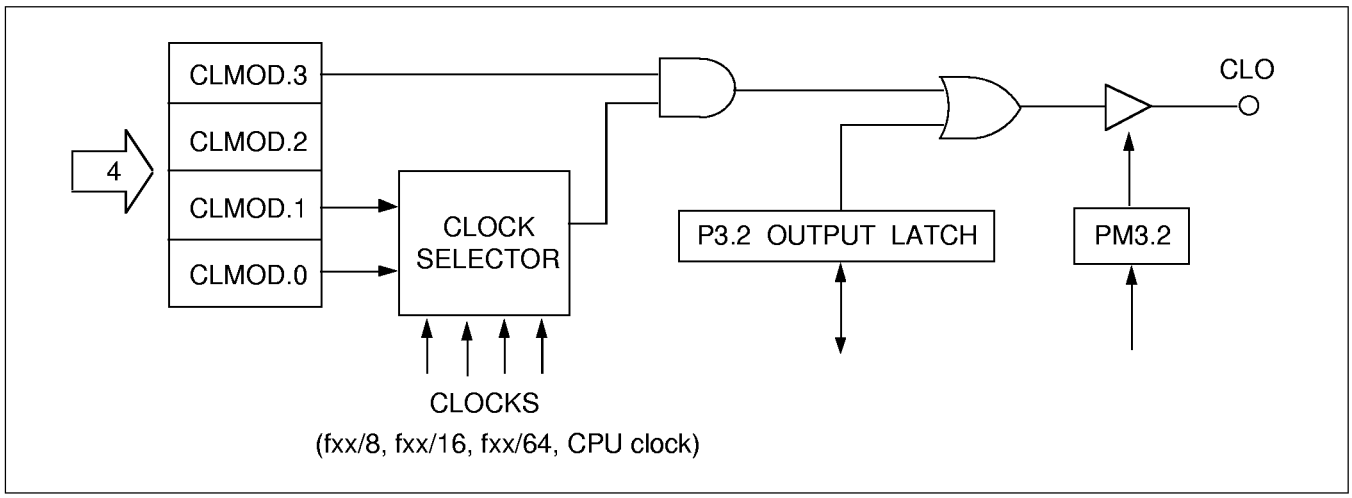


Figure 24. CLO Output Pin Circuit Diagram

☞ PROGRAMMING TIP — CPU Clock Output to the CLO Pin

To output the CPU clock to the CLO pin:

```
BITS    EMB             ;   Or BITR EMB
SMB     15
LD      EA,#40H
LD      PMG2,EA         ;   P3.2 ← Output mode
BITR    P3.2            ;   Clear P3.2 output latch
LD      A,#9H
LD      CLMOD,A
```

POWER-DOWN

The KS57C2016 microcontroller has two power-down modes to reduce power consumption: Idle and Stop. In Idle mode, the CPU clock stops while peripherals and the oscillator continue to operate normally.

In Stop mode, system clock oscillation is halted (assuming it is currently operating), and peripheral hardware components are powered-down. The effect of Stop mode on specific peripheral hardware components — CPU, basic timer, serial I/O, timer/counters, and watch timer — and on external interrupt requests, is detailed in Table 16.

Table 16. Hardware Operation During Power-Down Modes

Operation	Stop Mode (STOP)	Idle Mode (IDLE)
System clock status	Can be changed only if the main system clock is used	Can be changed if the main system clock or subsystem clock is used
Clock oscillator	Main system clock oscillation stops	CPU clock oscillation stops (main and subsystem clock oscillation continues)
Basic timer	Basic timer stops	Basic timer operates (with IRQB set at each reference interval)
Serial interface	Operates only if external $\overline{SCK}$ input is selected as the serial I/O clock	Operates if a clock other than the CPU clock is selected as the serial I/O clock
Timer/counter 0	Operates only if TCL0 is selected as the counter clock	Timer/counter 0 operates
Timer/counter 1	Operates only if TCL1 is selected as the counter clock	Timer/counter 1 operates
Watch timer	Operates only if subsystem clock (fxt) is selected as the counter clock	Watch timer operates
LCD controller	Operates only if a subsystem clock is selected as LCDCK	LCD controller operates
External interrupts	INT1, INT2, and INT4 are acknowledged; INT0 is not serviced	INT1, INT2, and INT4 are acknowledged; INT0 is not serviced
CPU	All CPU operations are disabled	All CPU operations are disabled
Mode release signal	Interrupt request signals (except INT0) are enabled by an interrupt enable flag or by $\overline{RESET}$ input	Interrupt request signals (except INT0) are enabled by an interrupt enable flag or by $\overline{RESET}$ input

☞ PROGRAMMING TIP — Reducing Power Consumption for Key Input Interrupt Processing

The following code shows real-time clock and interrupt processing for key inputs to reduce power consumption. In this example, the system clock source is switched from the main system clock to a subsystem clock and the LCD display is turned on:

```
KEYCLK  DI
        CALL    MA2SUB      ;  Main system clock → subsystem clock switch subroutine
        SMB     15
        LD      EA,#00H
        LD      P4,EA       ;  All key strobe outputs to low level
        LD      A,#3H
        LD      IMOD2,A     ;  Select KS0–KS7 enable
        SMB     0
        BITR    IRQW
        BITR    IRQ2
        BITS    IEW
        BITS    IE2
CLKS1   CALL    WATDIS      ;  Execute clock and display changing subroutine
        BTSTZ   IRQ2
        JR      CIDLE
        CALL    SUB2MA      ;  Subsystem clock → main system clock switch subroutine
        EI
        RET
CIDLE   IDLE                ;  Engage idle mode
        NOP
        NOP
        JPS     CLKS1
```

RECOMMENDED CONNECTIONS FOR UNUSED PINS

To reduce overall power consumption, please configure unused pins according to the guidelines described in Table 17.

Table 17. Unused Pin Connections for Reduced Power Consumption

Pin/Share Pin Names	Recommended Connection
P0.0 / $\overline{SCK}$ P0.1 / SO P0.2 / SI P0.3 / BTCO	Input mode: Connect to V_{DD} Output mode: No connection
P1.0 / INT0 – P1.2 / INT2	Connect to V_{DD}
P1.3 / INT4	Connect to V_{SS}
P2.0 / TCL0 P2.1 / TCL1 P2.2 / CAP P2.3 P3.0 / TCLO0 P3.1 / TCLO1 P3.2 / CLO P3.3 / BUZ P4.0–P4.3 P5.0–P5.3 P6.0 / KS0 – P6.3 / KS3 P7.0 / KS4 – P7.3 / KS7 P8.0–P8.3 P9.0–P9.3 P10.0–P10.1	Input mode: Connect to V_{DD} Output mode: No connection
SEG0–SEG27 SEG28 / P11.0 – SEG39 / P13.3 COM0–COM3	No connection
V_{LC0}–V_{LC2}	Connect to V_{SS}
BIAS	If all of the V_{LC0}–V_{LC2} pins are unused, connect BIAS to V_{SS}
XT_{in}	Connect XT_{in} to V_{SS} or V_{DD}
XT_{out}	No connection
TEST	Connect to V_{SS}

RESET

Table 18 provides detailed information about hardware register values after a RESET occurs during power-down mode or during normal operation.

Table 18. Hardware Register Values After RESET

Hardware Component or Subcomponent	If RESET Occurs During Power-Down Mode	If RESET Occurs During Normal Operation
Program counter (PC)	Lower six bits of address 0000H are transferred to PC13–8, and the contents of 0001H to PC7–0.	Lower six bits of address 0000H are transferred to PC13–8, and the contents of 0001H to PC7–0.
Program Status Word (PSW):		
Carry flag (C)	Retained	Undefined
Skip flag (SC0–SC2)	0	0
Interrupt status flags (IS0, IS1)	0	0
Bank enable flags (EMB, ERB)	Bit 6 of address 0000H in program memory is transferred to the ERB flag, and bit 7 of the address to the EMB flag.	Bit 6 of address 0000H in program memory is transferred to the ERB flag, and bit 7 of the address to the EMB flag.
Stack pointer (SP)	Undefined	Undefined
Data Memory (RAM):		
General registers E, A, L, H, X, W, Z, Y	Values retained	Undefined
General-purpose registers	Values retained (note1)	Undefined
Bank selection registers (SMB, SRB)	0, 0	0, 0
BSC register (BSC0–BSC3)	0	0
Clocks:		
Power control register (PCON)	0	0
Clock output mode register (CLMOD)	0	0
System clock mode register (SCMOD)	0	0
Interrupts:		
Interrupt request flags (IRQx)	0	0
Interrupt enable flags (IEx)	0	0
Interrupt priority flag (IPR)	0	0
Interrupt master enable flag (IME)	0	0
INT0 mode register (IMOD0)	0	0
INT1 mode register (IMOD1)	0	0
INT2 mode register (IMOD2)	0	0

Note1: The values of the 0F8H-0FDH are not retained when a RESET signal is input.

Table 18. Hardware Register Values After RESET (Continued)

Hardware Component or Subcomponent	If RESET Occurs During Power-Down Mode	If RESET Occurs During Normal Operation
I/O Ports:		
Output buffers	Off	Off
Output latches	0	0
Port mode flags (PM)	0	0
Pull-up resistor mode reg (PUMOD0/1)	0	0
Basic Timer:		
Count register (BCNT)	Undefined	Undefined
Mode register (BMOD)	0	0
Output enable flag (BOE)	0	0
Timer/Counters 0 and 1:		
Count registers (TCNT0/1)	0	0
Reference registers (TREF0/1)	FFH, FFFFH	FFH, FFFFH
Mode registers (TMOD0/1)	0	0
Output enable flags (TOE0,1, and 2)	0	0
Watch Timer:		
Watch timer mode register (WMOD)	0	0
LCD Driver/Controller:		
LCD mode register (LMOD)	0	0
LCD control register (LCON)	0	0
Display data memory	Values retained	Undefined
Output buffers	Off	Off
Serial I/O Interface:		
SIO mode register (SMOD)	0	0
SIO interface buffer (SBUF)	Values retained	Undefined
Capture Registers 0 and 1		
CREG0/1	0	0

I/O PORTS

The KS57C2016 has 14 ports. There are 4 input pins, 12 output pins, 32 configurable I/O pins, and 8 n-channel open-drain I/O pins, giving a maximum number of 56 pins.

PORT MODE FLAGS (PM FLAGS)

Port mode flags (PM) are used to configure I/O ports to input or output mode by setting or clearing the corresponding I/O buffer. If a PM bit is "0", the corresponding I/O pin is set to input mode. If the PM bit is "1", the pin is set to output mode: PM3.0 for P3.0, PM4.0 for P4.0, and so on.

Table 19. Port Mode Group Flags

PM Group ID	Address	Bit 3	Bit 2	Bit 1	Bit 0
PMG1	FE8H	PM0.3	PM0.2	PM0.1	PM0.0
	FE9H	PM7	"0"	PM5	PM4
PMG2	FEAH	PM2.3	PM2.2	PM2.1	PM2.0
	FEBH	PM3.3	PM3.2	PM3.1	PM3.0
PMG3	FECH	PM6.3	PM6.2	PM6.1	PM6.0
	FEDH	PM8.3	PM8.2	PM8.1	PM8.0
PMG4	FEEH	PM9.3	PM9.2	PM9.1	PM9.0
	FEDH	PM10.3	PM10.2	PM10.1	PM10.0

☞ **PROGRAMMING TIP — Configuring I/O Ports as Input or Output**

Configure P0.3 and P2 as an output port and the other ports as input ports:

```
BITS    EMB
SMB     15
LD      EA,#08H
LD      PMG1,EA         ;   P0.3 ← Output, P0.0–0.2, P4, P5, P7 ← Input
LD      EA,#0FH
LD      PMG2,EA         ;   P2.0–2.3 ← Output, P3.0–3.3 ← Input
LD      EA,#00H
LD      PMG3,EA         ;   P6 and P8 ← Input
LD      PMG4,EA         ;   P9 and P10 ← Input
```

PULL-UP RESISTOR MODE REGISTERS

The 8-bit pull-up resistor mode registers (PUMOD0 and PUMOD1) are used to assign internal pull-up resistors by software to specific ports. Ports 4 and 5 are an exception, since these port pins may only be assigned internal pull-up resistors via mask option.

PUMOD0 bits 4 and 5 should always be cleared to logic zero. When a PUMODn bit is "1", a pull-up resistor is assigned to the corresponding I/O port: PUR3 for port 3, PUR2 for port 2, and so on.

When a configurable I/O port pin is used as an output pin, its assigned pull-up resistor is automatically disabled, even though the pin's pull-up may be enabled by a corresponding PUMOD bit setting.

Table 20. Pull-Up Resistor Mode Register (PUMOD) Organization

PUMOD ID	Address	Bit 3	Bit 2	Bit 1	Bit 0
PUMOD0	FDCH	PUR3	PUR2	PUR1	PUR0
	FDDH	PUR7	PUR6	"0"	"0"
PUMOD1	FDEH	"0"	PUR10	PUR9	PUR8
	FDFH	"0"	"0"	"0"	"0"

☞ PROGRAMMING TIP — Enabling and Disabling I/O Port Pull-Up Resistors

P6 and P7 enable pull-up resistors, P0–P3 disable pull-up resistors.

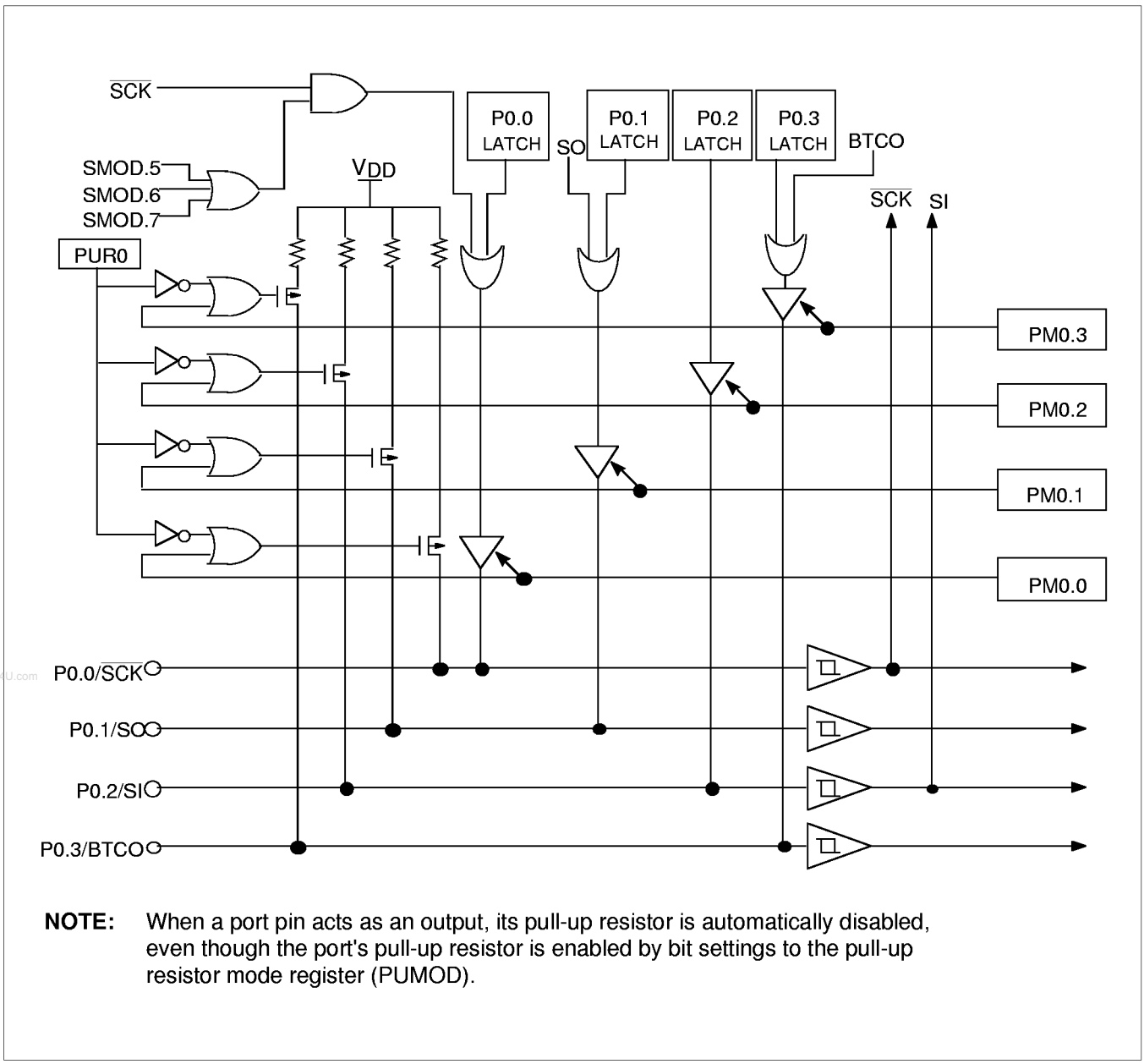

```
BITS    EMB
SMB     15
LD      EA,#0C0H
LD      PUMOD0,EA       ;   P6 and P7 enable
```

PIN ADDRESSING FOR OUTPUT PORTS 11–13

The addresses for the ports 11–13 1-bit output pin buffers are located in bank 1 of data memory instead of bank 15. The LCD mode register, LMOD is used to control whether the pin address is used for LCD data output or for normal data output.

The LSB (bit 0) of the each register location is used as the port buffer for either LCD segment output or normal 1-bit data output. Locations that are unused for LCD or normal 1-bit data output can be used as normal data memory. Pin addresses that are not used for LCD segment output can be used for normal 1-bit output.

PORT 0 CIRCUIT DIAGRAM



NOTE: When a port pin acts as an output, its pull-up resistor is automatically disabled, even though the port's pull-up resistor is enabled by bit settings to the pull-up resistor mode register (PUMOD).

Figure 25. Port 0 Circuit Diagram

PORT 1 CIRCUIT DIAGRAM

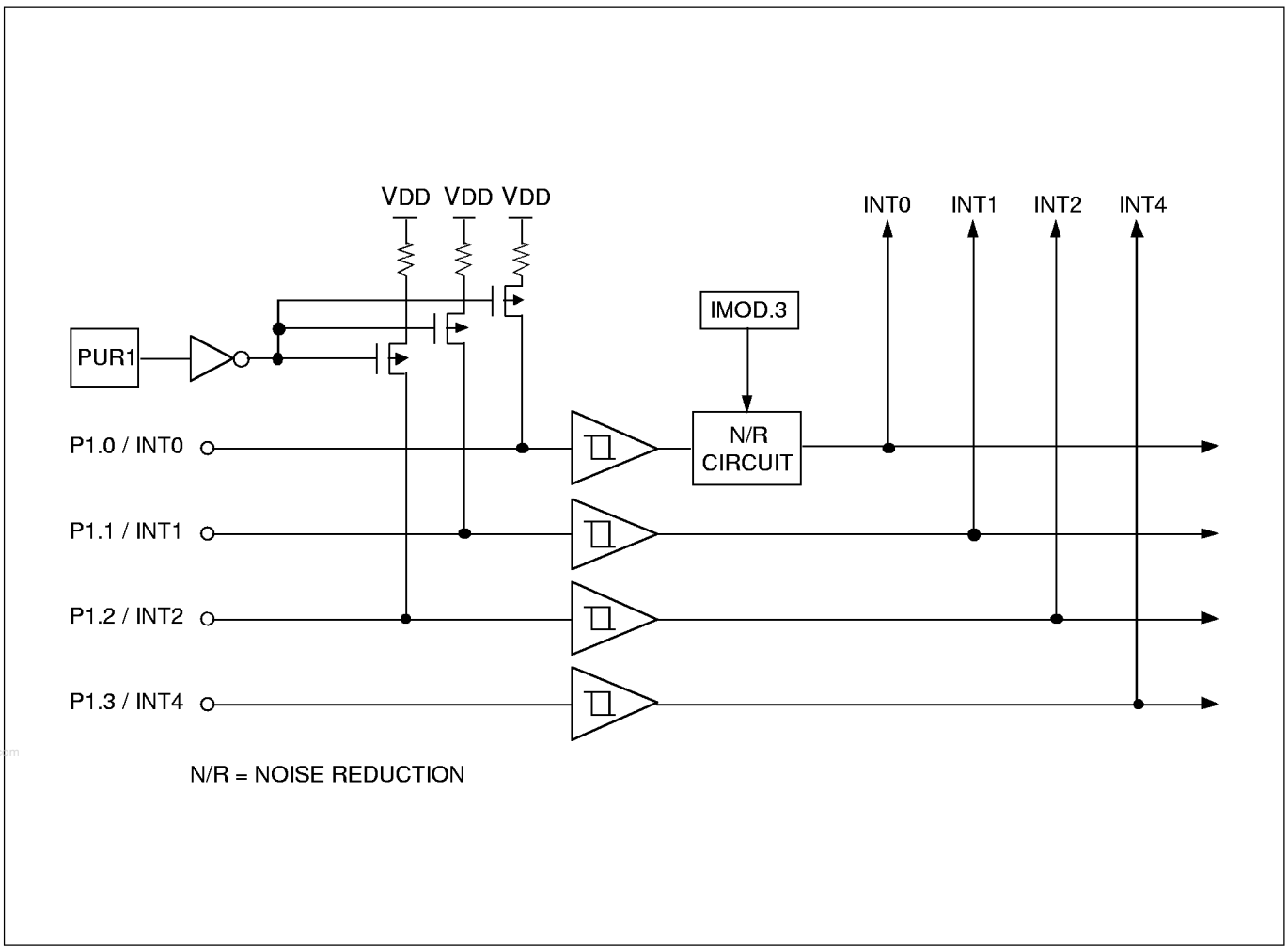
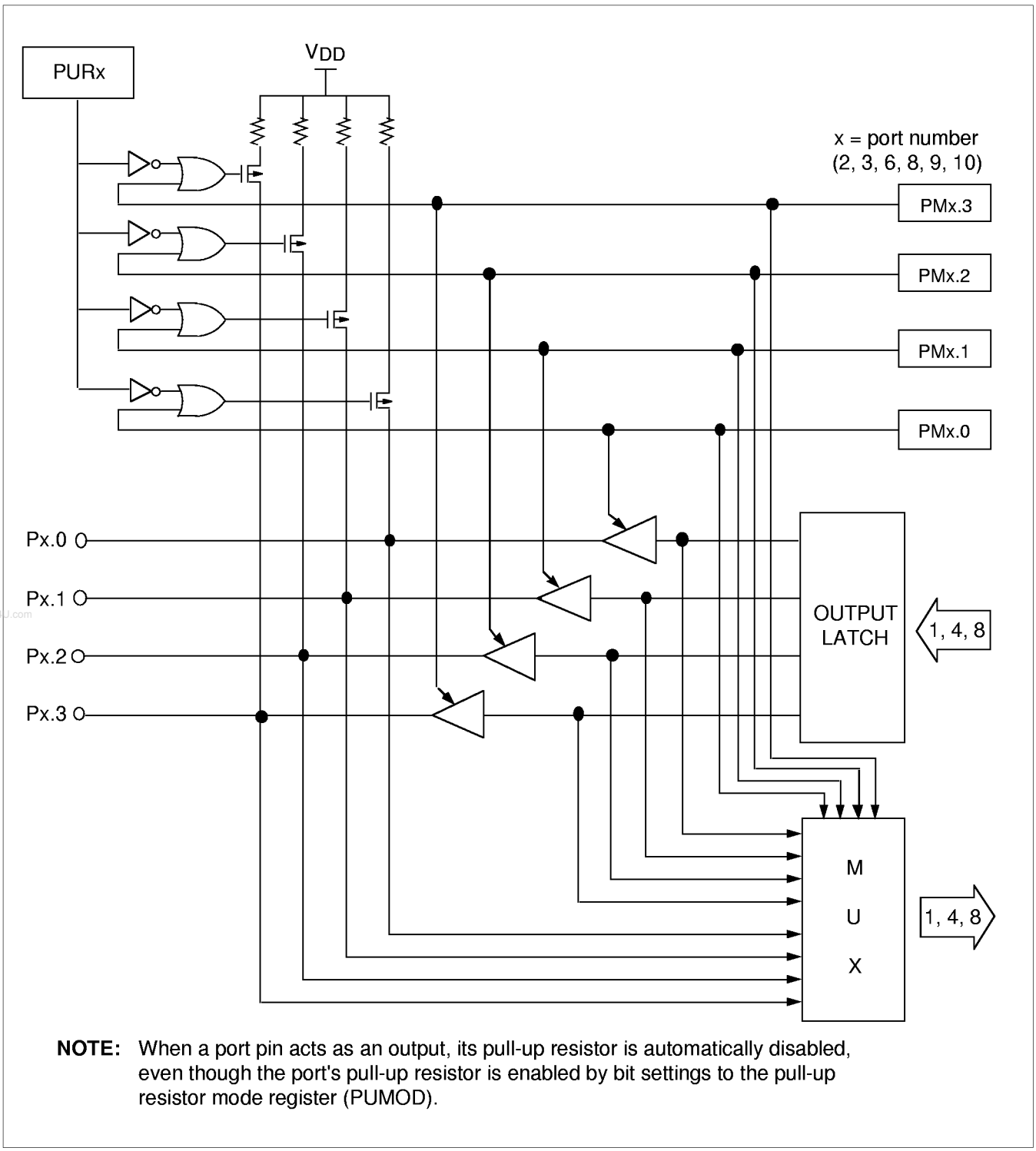


Figure 26. Port 1 Circuit Diagram

PORT 2, 3, 6, 8, 9, 10 CIRCUIT DIAGRAM



NOTE: When a port pin acts as an output, its pull-up resistor is automatically disabled, even though the port's pull-up resistor is enabled by bit settings to the pull-up resistor mode register (PUMOD).

Figure 27. Port 2, 3, 6, 8, 9, and 10 Circuit Diagram

PORT 4, 5 CIRCUIT DIAGRAM

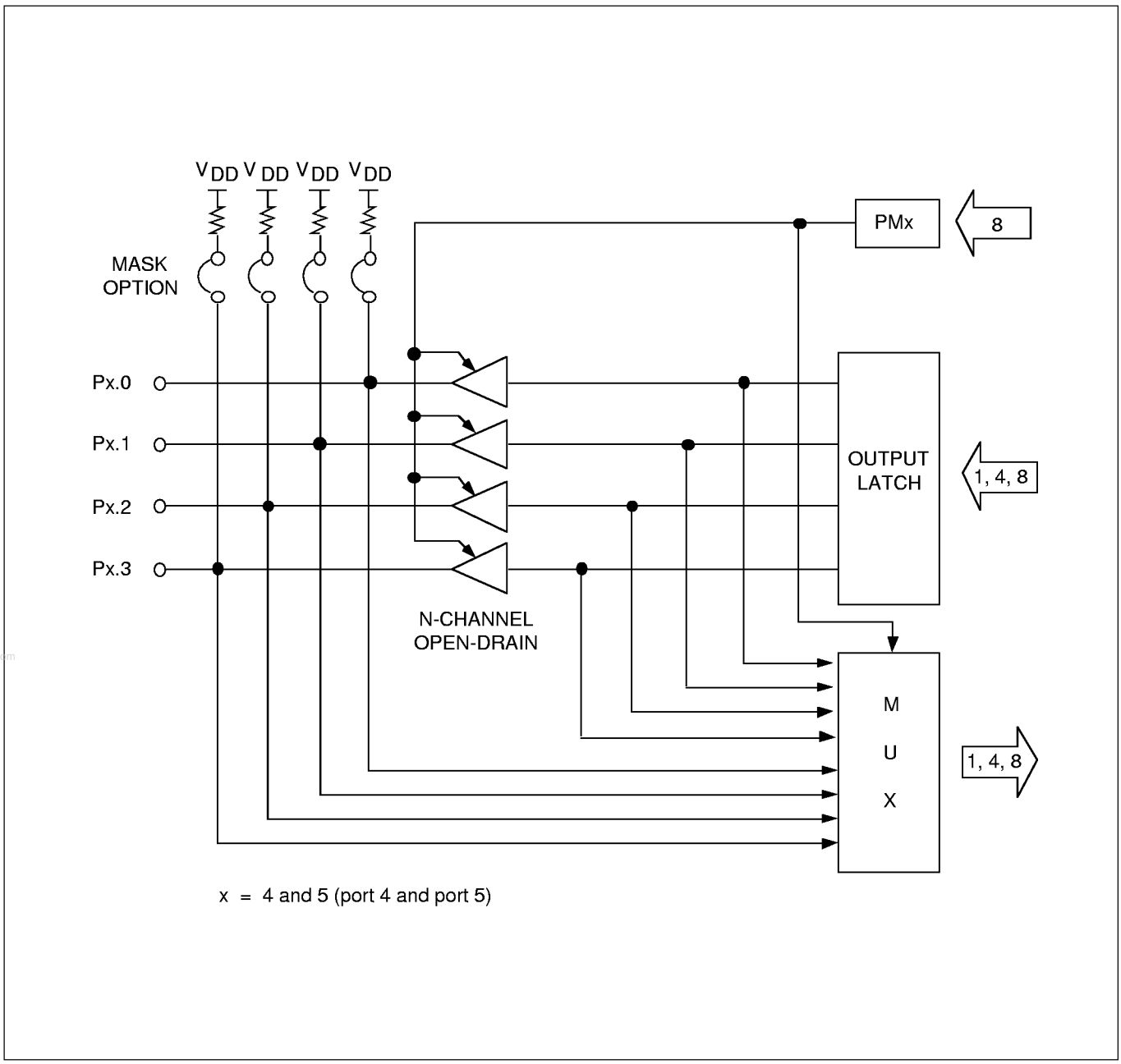
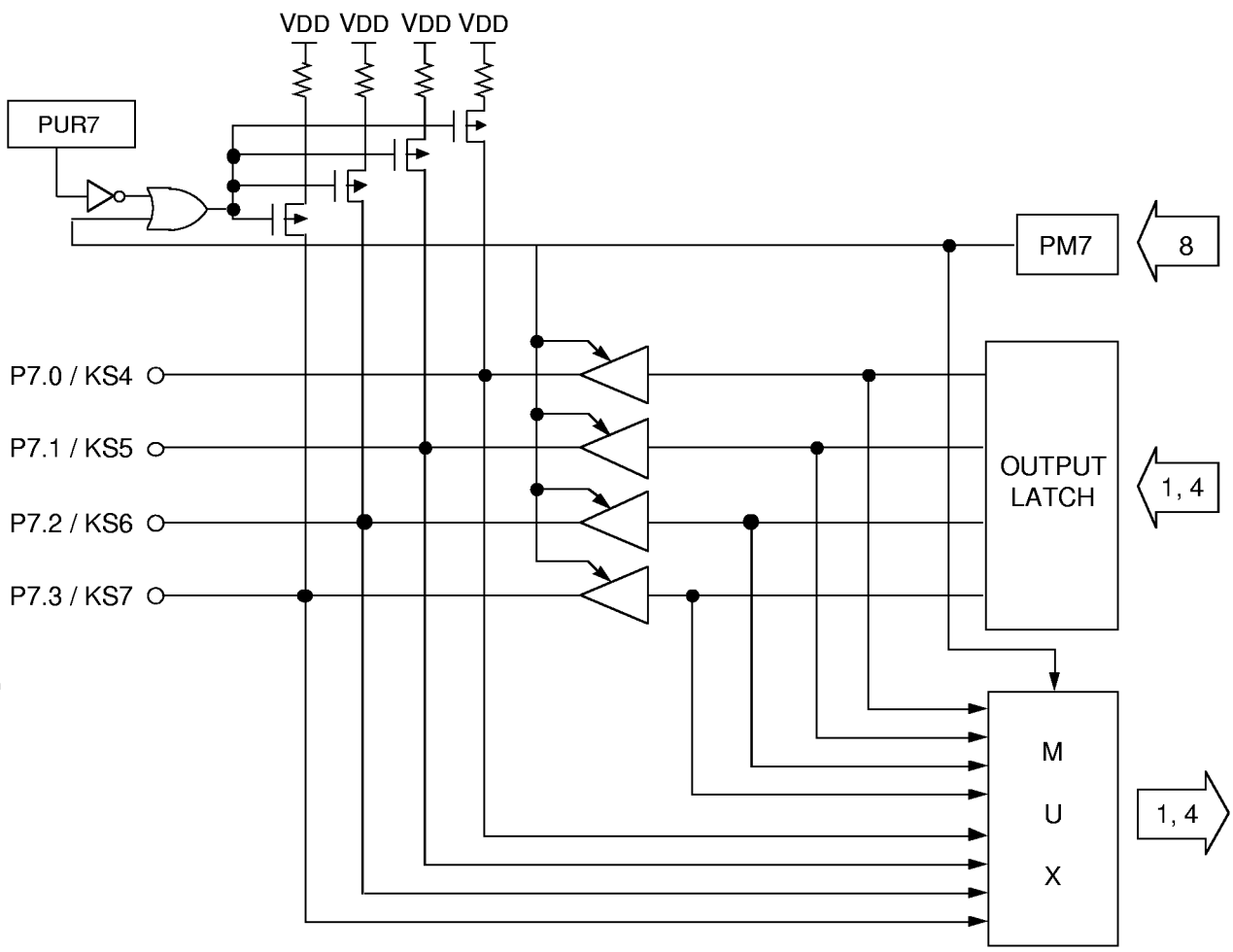


Figure 28. Port 4 and 5 Circuit Diagram

PORT 7 CIRCUIT DIAGRAM



NOTE: When a port pin acts as an output, its pull-up resistor is automatically disabled, even though the port's pull-up resistor is enabled by bit settings to the pull-up resistor mode register (PUMOD).

Figure 29. Port 7 Circuit Diagram

BASIC TIMER (BT)

The basic timer generates interrupt requests at precise intervals. You can use the basic timer as a "watchdog" timer for monitoring system events or use BT output to stabilize clock oscillation when Stop mode is released by an interrupt and following RESET.

Interval Timer Function

The measurement of elapsed time intervals is the basic timer's primary function. The standard interval is 256 BT clock pulses. To restart the basic timer, set bit 3 of the mode register BMOD to "1". The 8-bit counter register, BCNT, is incremented each time a clock signal is detected that corresponds to the frequency selected by BMOD. BCNT continues incrementing as it counts BT clocks until an overflow occurs. An overflow causes the BT interrupt request flag (IRQB) to be set to "1" to signal that the designated time interval has elapsed. An interrupt request is then generated, BCNT is cleared to "0", and counting continues from 00H.

Watchdog Timer Function

The basic timer can also be used as a "watchdog" timer to signal the occurrence of specific system events. Each time BCNT overflows, an overflow signal is sent to the basic timer clock output pin, BTCO. To enable BTCO output operation, clear the output latch for pin P0.3 to "0" and set the port mode flag for P0.3 (PM0.3) to "1".

Oscillation Stabilization Interval Control

Setting bits 2–0 of the BMOD register determines the time interval (also referred to as 'wait time') required to stabilize clock signal oscillation when power-down mode is released by an interrupt. When a RESET signal is generated, the standard stabilization interval for system clock oscillation following a RESET is 31.3ms at 4.19 MHz.

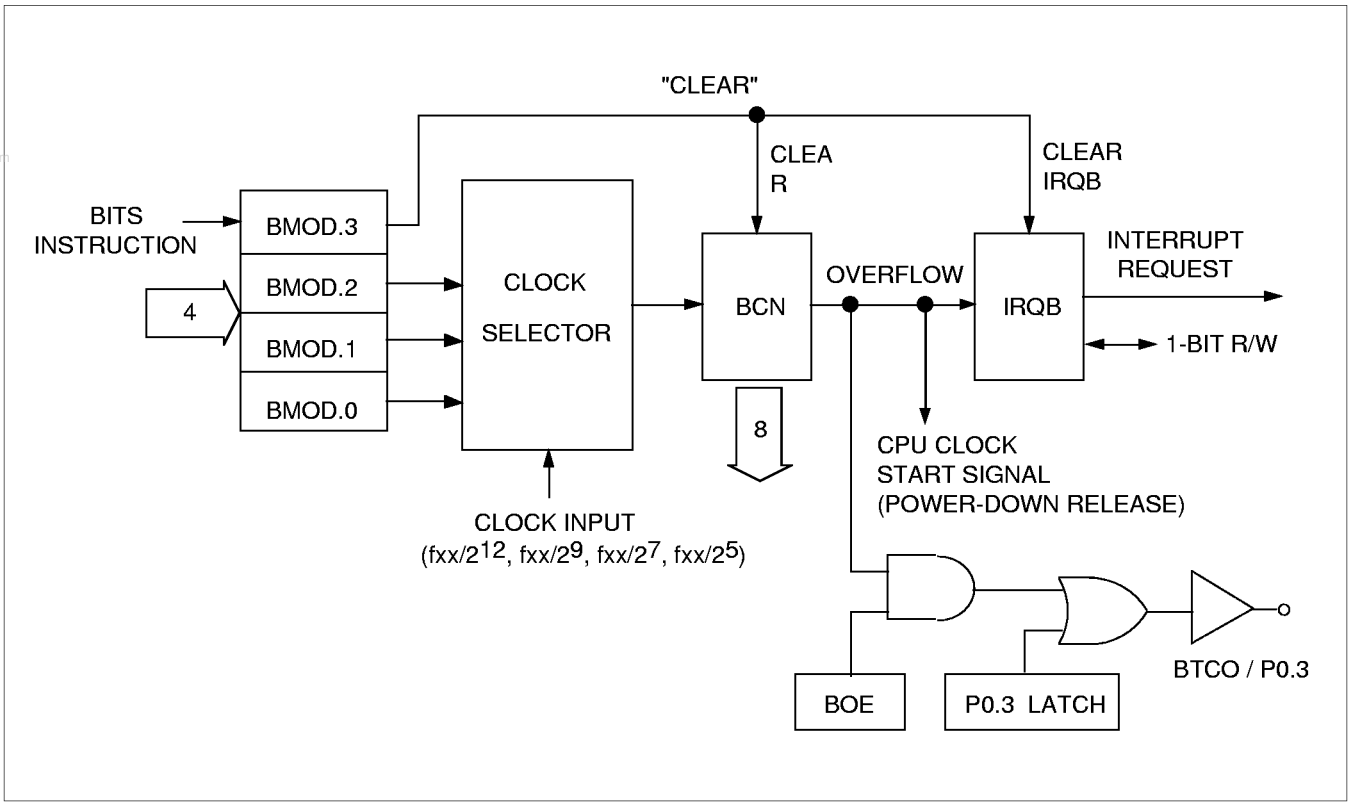


Figure 30. Basic Timer Circuit Diagram

BASIC TIMER MODE REGISTER (BMOD)

The basic timer mode register, BMOD, is used to select input frequency and oscillation stabilization time. The most significant bit of the BMOD register, BMOD.3, is used to start the basic timer again. When BMOD.3 is set to "1", the contents of the BT counter register (BCNT) and the BT interrupt request flag (IRQB) are both cleared to "0", and timer operation is restarted.

Table 21. Basic Timer Mode Register (BMOD) Organization

BMOD.3	Basic Timer Restart Bit
1	Restart basic timer; clear IRQB, BCNT, and BMOD.3 to "0"

BMOD.2	BMOD.1	BMOD.0	Basic Timer Input Clock	Oscillation Stabilization
0	0	0	$fxx/2^{12}$ (1.02 kHz)	$2^{20}/fxx$ (250 ms)
0	1	1	$fxx/2^{9}$ (8.18 kHz)	$2^{17}/fxx$ (31.3 ms)
1	0	1	$fxx/2^{7}$ (32.7 kHz)	$2^{15}/fxx$ (7.82 ms)
1	1	1	$fxx/2^{5}$ (131 kHz)	$2^{13}/fxx$ (1.95 ms)

NOTES:
1. Clock frequencies and stabilization intervals assume a system oscillator clock frequency (fxx) of 4.19 MHz.
2. fxx = selected system clock frequency.
3. Oscillation stabilization time is the time required to stabilize clock signal oscillation after stop mode is released. The data in the table column 'Oscillation Stabilization' can also be interpreted as "Interrupt Interval Time."
4. The standard stabilization time for system clock oscillation following a RESET is 31.3 ms at 4.19 MHz.

BASIC TIMER COUNTER (BCNT)

BCNT is an 8-bit counter register for the basic timer. When BCNT has incremented to hexadecimal 'FFH', it is cleared to '00H' and an overflow is generated. The overflow causes the interrupt request flag, IRQB, to be set to "1". When the interrupt request is generated, BCNT immediately resumes counting incoming clock signals.

NOTE

Always execute a BCNT read operation twice to eliminate the possibility of reading unstable data while the counter is incrementing. If, after two consecutive reads, the BCNT values match, you can select the latter value as valid data. Until the results of the consecutive reads match, however, the read operation must be repeated until the validation condition is met.

BASIC TIMER OUTPUT ENABLE FLAG (BOE)

The BOE flag value enables and disables basic timer output to the BTCO/P0.3. When BOE is "0", basic timer output to the BTCO pin is disabled; when it is "1", BT output to the BTCO pin is enabled.

F92H — 1-Bit R/W

TOE1	TOE0	**BOE**	0

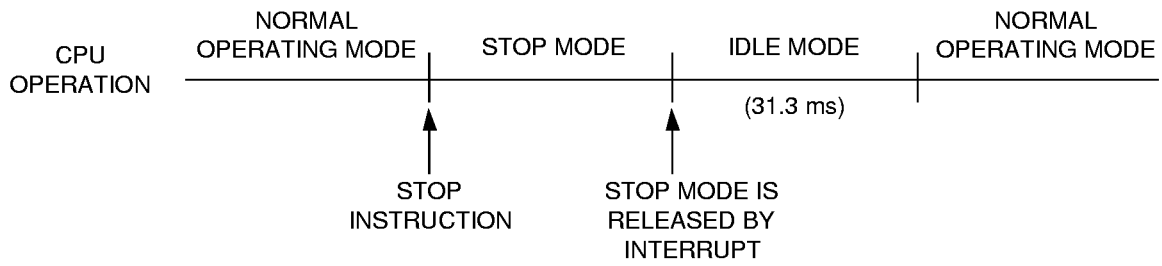
☞ PROGRAMMING TIP — Using the Basic Timer

1. To read the basic timer count register (BCNT):

```
        BITS    EMB
        SMB     15
BCNTR   LD      EA,BCNT
        LD      YZ,EA
        LD      EA,BCNT
        CPSE    EA,YZ
        JR      BCNTR
```

2. When Stop mode is released by an interrupt, set the oscillation stabilization interval to 31.3 ms:

```
        BITS    EMB
        SMB     15
        LD      A,#0BH
        LD      BMOD,A          ;   Wait time is 31.3 ms
        STOP                    ;   Set stop power-down mode
        NOP
        NOP
```



3. To set the basic timer interrupt interval time to 1.95 ms (at 4.19 MHz):

```
        BITS    EMB
        SMB     15
        LD      A,#0FH
        LD      BMOD,A
        EI
        BITS    IEB             ;   Basic timer interrupt enable flag is set to "1"
```

4. Clear BCNT and the IRQB flag and restart the basic timer:

```
        BITS    EMB
        SMB     15
        BITS    BMOD.3
```

8-BIT TIMER/COUNTER 0 (TC0)

Timer/counter 0 (TC0) is used to count system 'events' by identifying the transition (high-to-low or low-to-high) of incoming square wave signals. To indicate that an event has occurred, or that a specified time interval has elapsed, TC generates an interrupt request. By counting signal transitions and comparing the current counter value with the reference register value, TC can be used to measure specific time intervals.

Timer/counter 0 can supply a clock signal to the clock selector circuit of the serial I/O interface for data shifter and clock counter operations. (These internal SIO operations are controlled in turn by the SIO mode register, SMOD). This clock generation function lets you adjust data transmission rates across the serial interface.

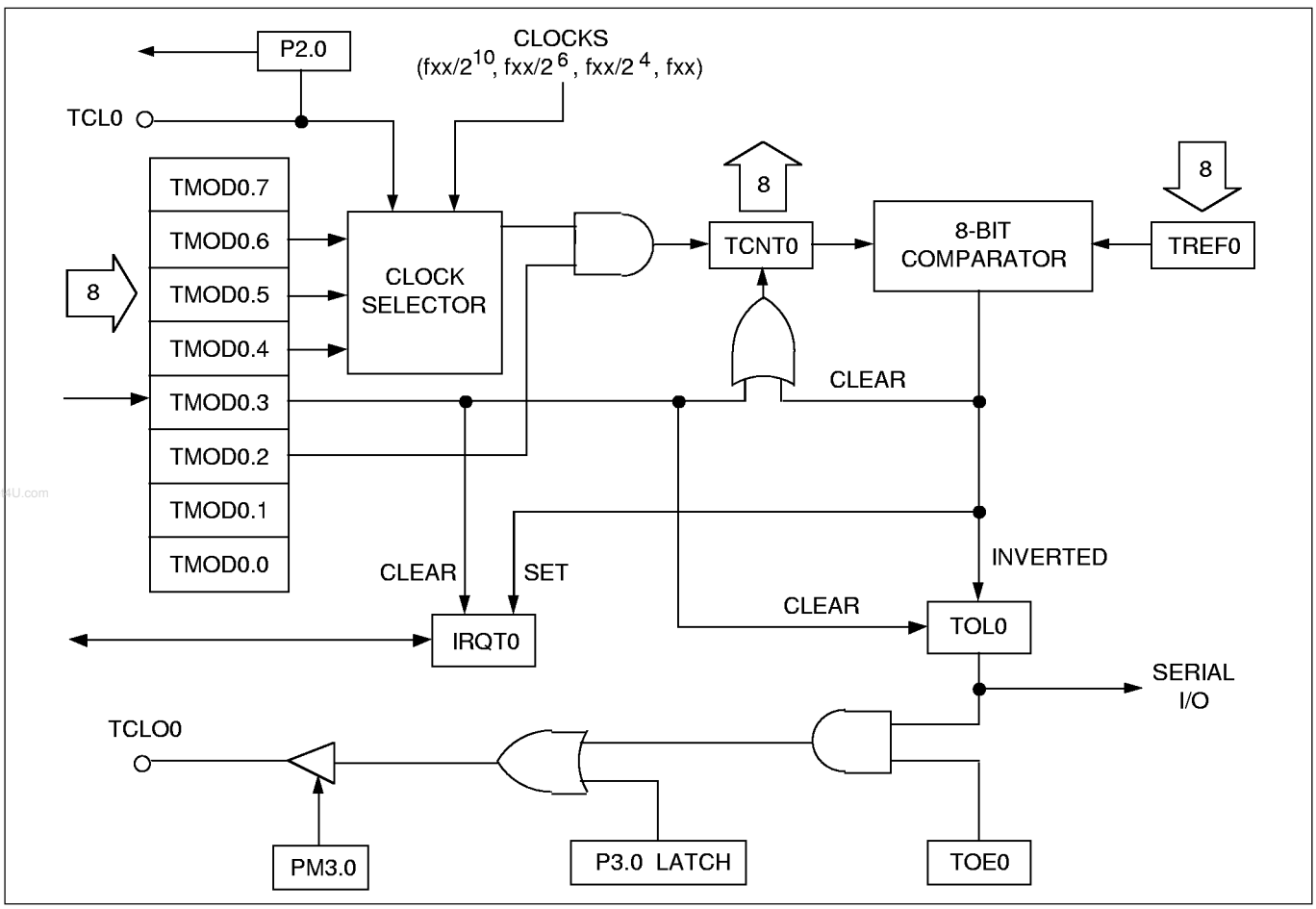


Figure 31. TC0 Circuit Diagram

PROGRAMMABLE TIMER/COUNTER FUNCTION

Timer/counter 0 can be programmed to generate interrupt requests at various intervals based on the selected system clock frequency. Its 8-bit TC0 mode register TMOD0 is used to activate the timer/counter and to select the clock frequency. The reference register TREF0 stores the value for the number of clock pulses to be generated between interrupt requests.

The counter register, TCNT0, counts the incoming clock pulses, which are compared to the TREF0 value as TCNT0 is incremented. When there is a match (TREF0 = TCNT0), the TC0 interrupt request flag (IRQT0) is set to logic one, the status of TOL0 is inverted, and the interrupt is generated. The content of TCNT0 is then cleared to 00H and TC0 continues counting.

TC0 EVENT COUNTER FUNCTION

Timer/counter 0 can monitor or detect system 'events' by using the external clock input at the TCL0 pin as the counter source. With the exception of the different TMOD0.4–TMOD0.6 settings, the operation sequence for TC0's event counter function is identical to its programmable timer/counter function. To activate the TC0 event counter function, P2.0/TCL0 must be set to input mode.

Using timer/counter 0, a modifiable clock frequency can be output to the TC0 clock output pin, TCLO0. To enable the output to the TCLO0/P3.0, the I/O mode flag for P3.0 (PM3.0) must be set to output mode and output latch value for P3.0 must be cleared to "0" after the timer output enable flag (TOE0) is set to "1".

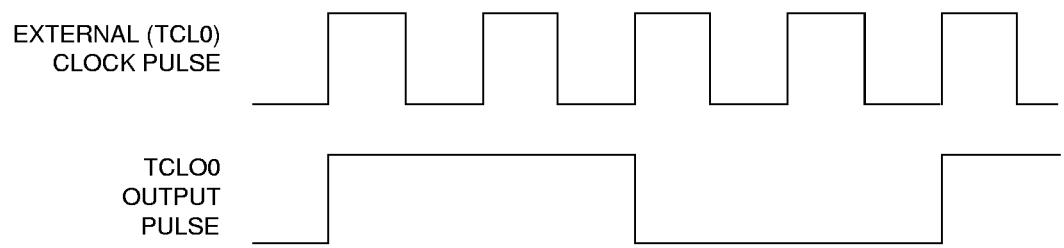
☞ PROGRAMMING TIP — TC0 Signal Output to the TCLO0 Pin

Output a 30 ms pulse width signal to the TCLO0 pin:

```
BITS    EMB
SMB     15
LD      EA,#79H
LD      TREF0,EA
LD      EA,#4CH
LD      TMOD0,EA
LD      EA,#10H
LD      PMG2,EA         ;   P3.0 ← output mode
BITR    P3.0            ;   P3.0 clear
BITS    TOE0
```

☞ PROGRAMMING TIP — External TCL0 Clock Output to the TCLO0 Pin

Output external TCL0 clock pulse to the TCLO0 pin (divided by four):




```
BITS    EMB
SMB     15
LD      EA,#01H
LD      TREF0,EA
LD      EA,#0CH
LD      TMOD0,EA
LD      EA,#10H
LD      PMG2,EA         ;   P3.0 ← output mode
BITR    P3.0            ;   P3.0 clear
BITS    TOE0
```


TC0 MODE REGISTER (TMOD0)

TMOD0 is the 8-bit mode control register for timer/counter 0. When TMOD0.3 is set to "1", the contents of TCNT0, IRQT0, and TOL0 are cleared, counting starts from 00H, and TMOD0.3 is automatically reset to "0" for normal TC0 operation. When TC0 operation stops (TMOD0.2 = "0"), the contents of the TC0 counter register TCNT0 are retained until TC0 is re-enabled.

Table 22. TC0 Mode Register (TMOD0) Organization

Bit Name	Setting	Resulting TC0 Function	Address
TMOD0.7	0	Always logic zero	F91H
TMOD0.6 TMOD0.5 TMOD0.4	0,1	Specify input clock edge and internal frequency	
TMOD0.3	1	Clear TCNT0, IRQT0, and TOL0; then resume counting. (This bit is automatically cleared to "0" when counting resumes.)	F90H
TMOD0.2	0	Disable timer/counter 0; retain TCNT0 contents	
	1	Enable timer/counter 0	
TMOD0.1	0	Always logic zero	
TMOD0.0	0	Always logic zero	

Table 23. TMOD0.6, TMOD0.5, and TMOD0.4 Bit Settings

TMOD0.6	TMOD0.5	TMOD0.4	Resulting Counter Source and Clock Frequency
0	0	0	External clock input (TCL0) on rising edges
0	0	1	External clock input (TCL0) on falling edges
1	0	0	fxx/2^{10} (4.09 kHz)
1	0	1	fxx /2^{6} (65.5 kHz)
1	1	0	fxx/2^{4} (262 kHz)
1	1	1	fxx = 4.19 MHz

NOTE: 'fxx' = selected system clock of 4.19 MHz.

☞ PROGRAMMING TIP — Restarting TC0 Counting Operation

1. Set TC0 timer interval to 4.09 kHz:

```
BITS    EMB
SMB     15
LD      EA,#4CH
LD      TMOD0,EA
EI
BITS    IET0
```

2. Clear TCNT0, IRQT0, and TOL0. Then, restart the TC0 counting operation:

```
BITS    EMB
SMB     15
BITS    TMOD0.3
```


TC0 REFERENCE REGISTER (TREF0)

TREF0 is used to store a reference value to be compared to the incrementing TCNT0 register in order to identify an elapsed time interval.

Use the following formula to calculate the correct value to load to the TREF0 reference register:

TC0 timer interval =

$$(\text{TREF0 value} + 1) \times \frac{1}{\text{TMOD0frequencysetting}}$$

Assuming TREF0 value $\neq$ 0

TC0 OUTPUT ENABLE FLAG (TOE0)

The 1-bit timer/counter 0 output enable flag TOE0 controls output from timer/counter 0 to the TCLO0 pin.

F92H — 1-Bit R/W

TOE1	**TOE0**	BOE	TOE2

When you set the TOE0 flag to "1", the contents of TOL0 can be output to the TCLO0 pin.

☞ PROGRAMMING TIP — Setting a TC0 Timer Interval

To set a 30 ms timer interval for TC0, given fx = 4.19 MHz, follow these steps.

1. Select the timer/counter 0 mode register with a maximum setup time of 62.5 ms (assume that the TC0 counter clock = $fx/2^{10}$, and TREF0 is set to FFH):

2. Calculate the TREF0 value:

$$30\ ms = \frac{TREF0value+1}{4.09kHz}$$

$$TREF0 + 1 = \frac{30ms}{244\mu s} = 122.9 = 7AH$$

$$TREF0\ value = 7AH - 1 = 79H$$

3. Load the value 79H to the TREF0 register:

```
BITS    EMB
SMB     15
LD      EA,#79H
LD      TREF0,EA
LD      EA,#4CH
LD      TMOD0,EA
```

16-BIT TIMER/COUNTER (TC1)

Timer/counter 1 is used to count system 'events' by identifying the transition (high-to-low or low-to-high) of incoming square wave signals. By counting signal transitions, it can be used to measure time intervals. Timer/counter 1 is also used for PWM output, which generates pulses of programmable length and interval. 16-bit, or 8-bit PWM output mode can be selected by TMOD1 register setting.

A reference value, which is compared with counter register value, is written to reference register (TREF1). The counter (TCNT1) is automatically incremented by counter logic. When an overflow occurs, the counter is cleared to zero, and the counting operation resumes.

TIMER/COUNTER 1 FUNCTION GROUP

Timer/counter 1 consists of two function groups, called function group A and function group B:

Function group A contains the following components:

— 16-bit timer/counter (TC1)
— 16-bit PWM/capture (PWM/capture)
— 8-bit timer/counter (TC1A)
— 8-bit PWM (PWMA)

Function group B contains the following components:

— 8-bit timer/counter (TC1B)
— 8-bit PWM (PWMB)

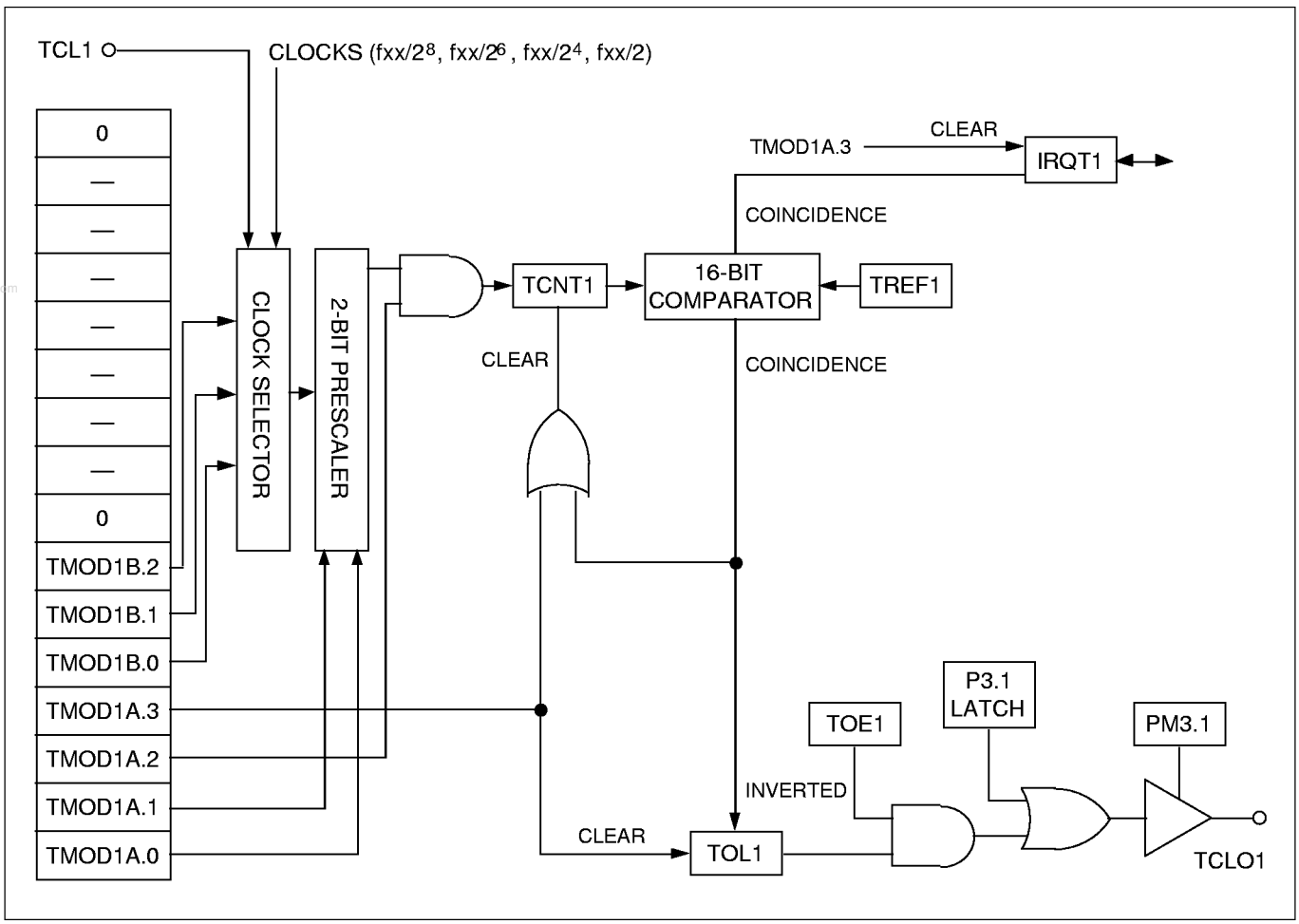


Figure 32. Timer/Counter 1 Circuit Diagram (16-Bit TC1 Mode)

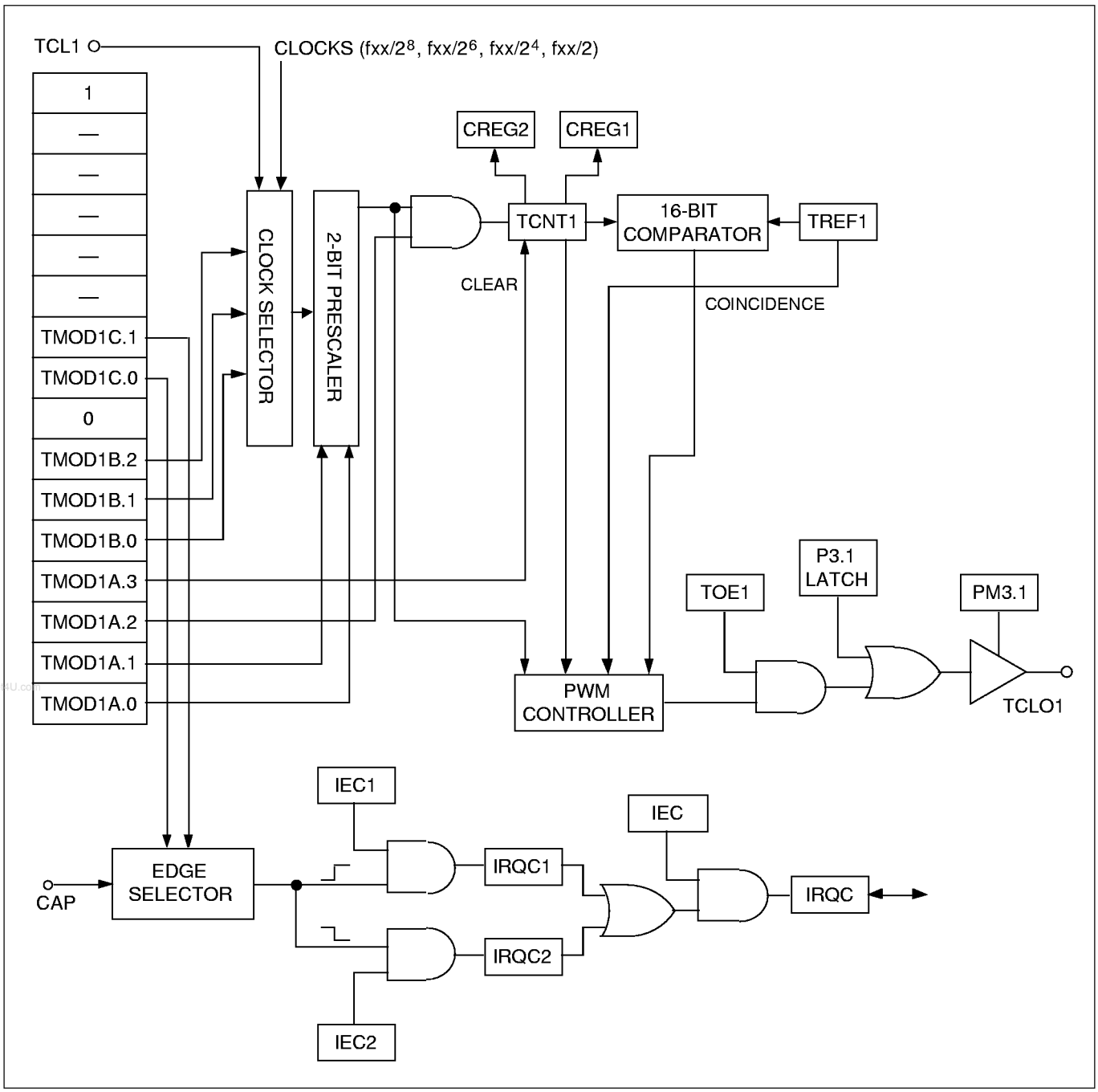


Figure 33. Timer/Counter 1 Circuit Diagram (16-Bit PWM/Capture Mode)

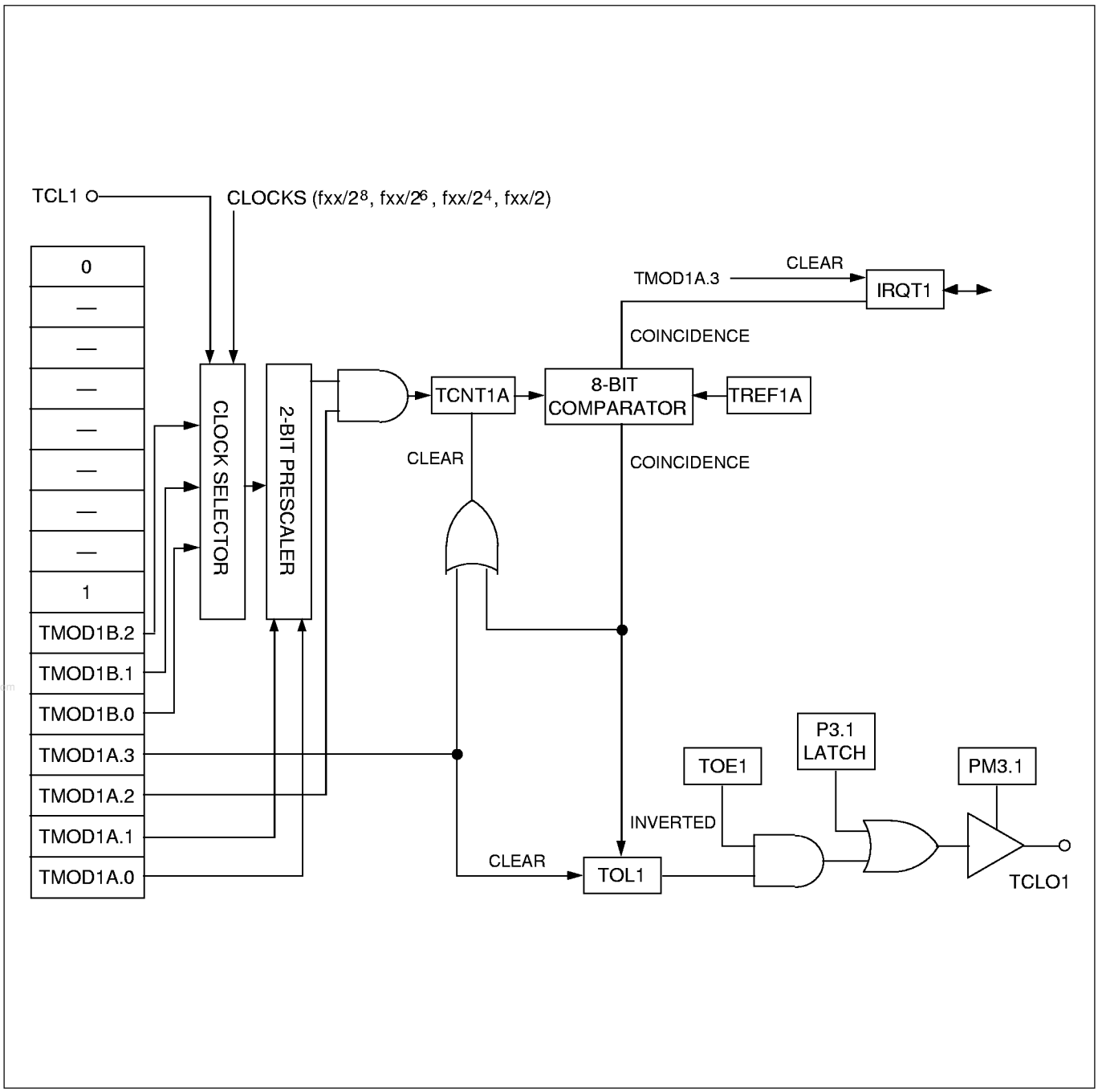


Figure 34. Timer/Counter 1 Circuit Diagram (8-Bit TC1A Mode)

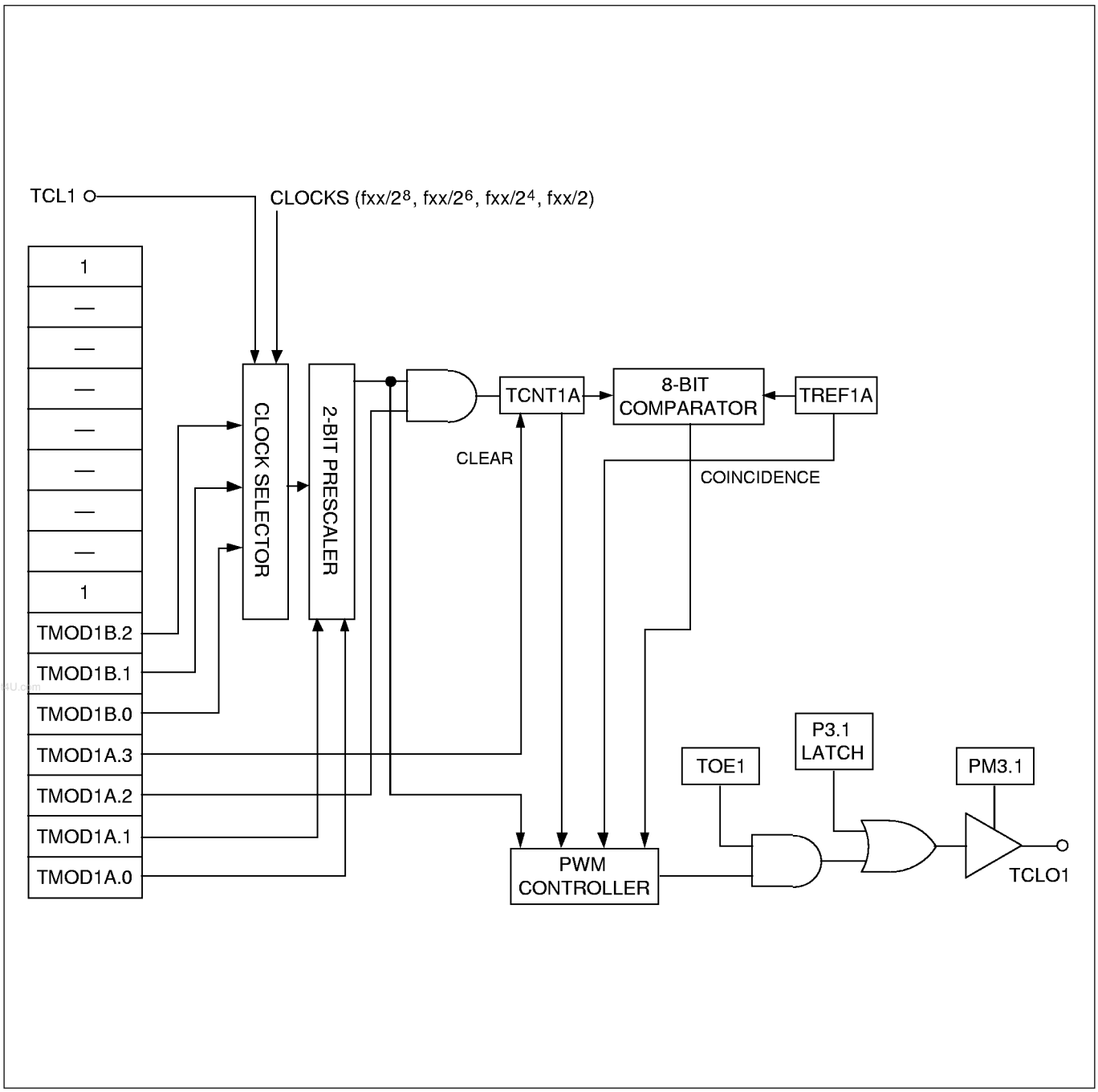


Figure 35. Timer/Counter 1 Circuit Diagram (8-Bit PWMA Mode)

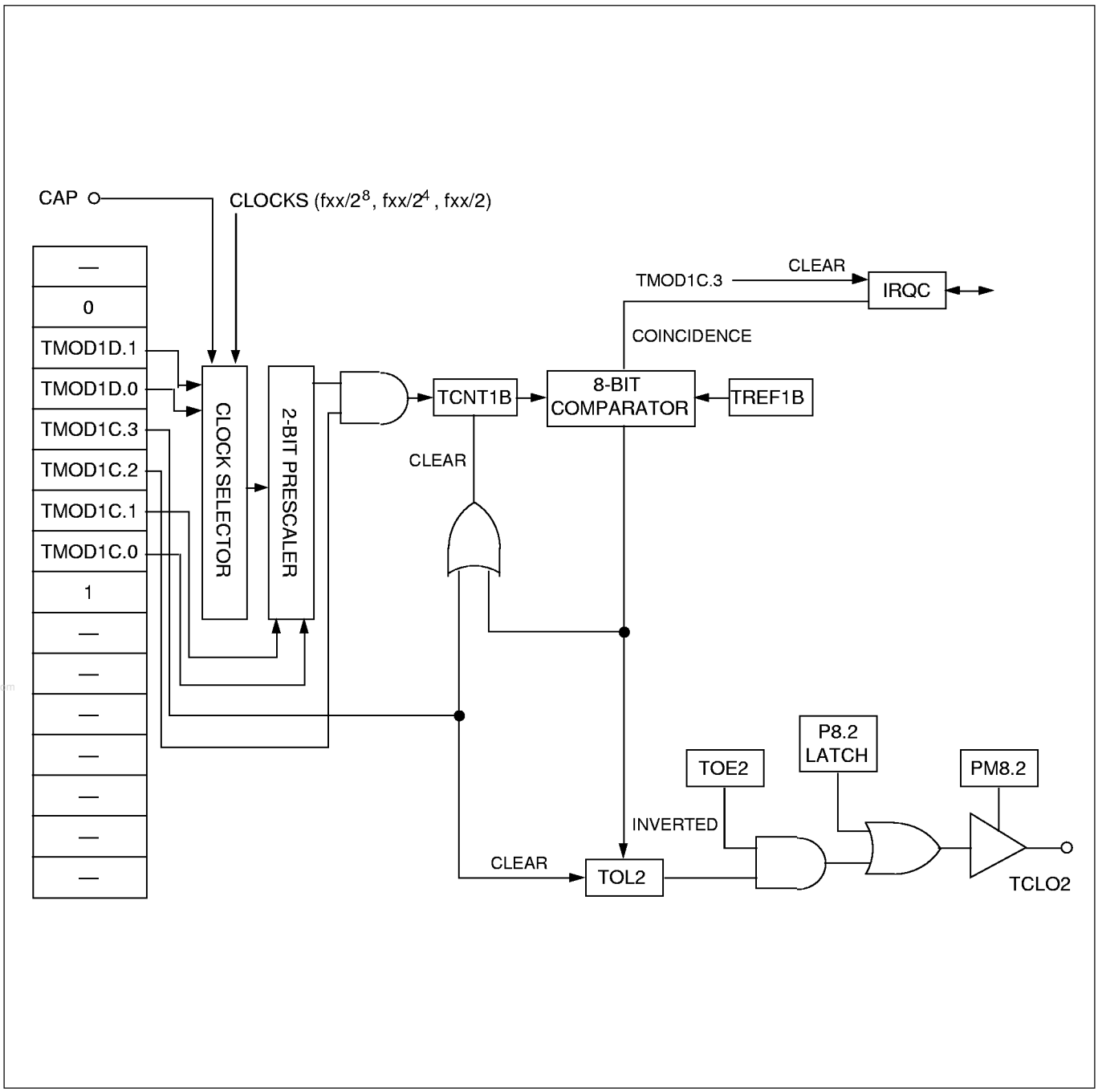


Figure 36. Timer/Counter 1 Circuit Diagram (8-Bit TC1B Mode)

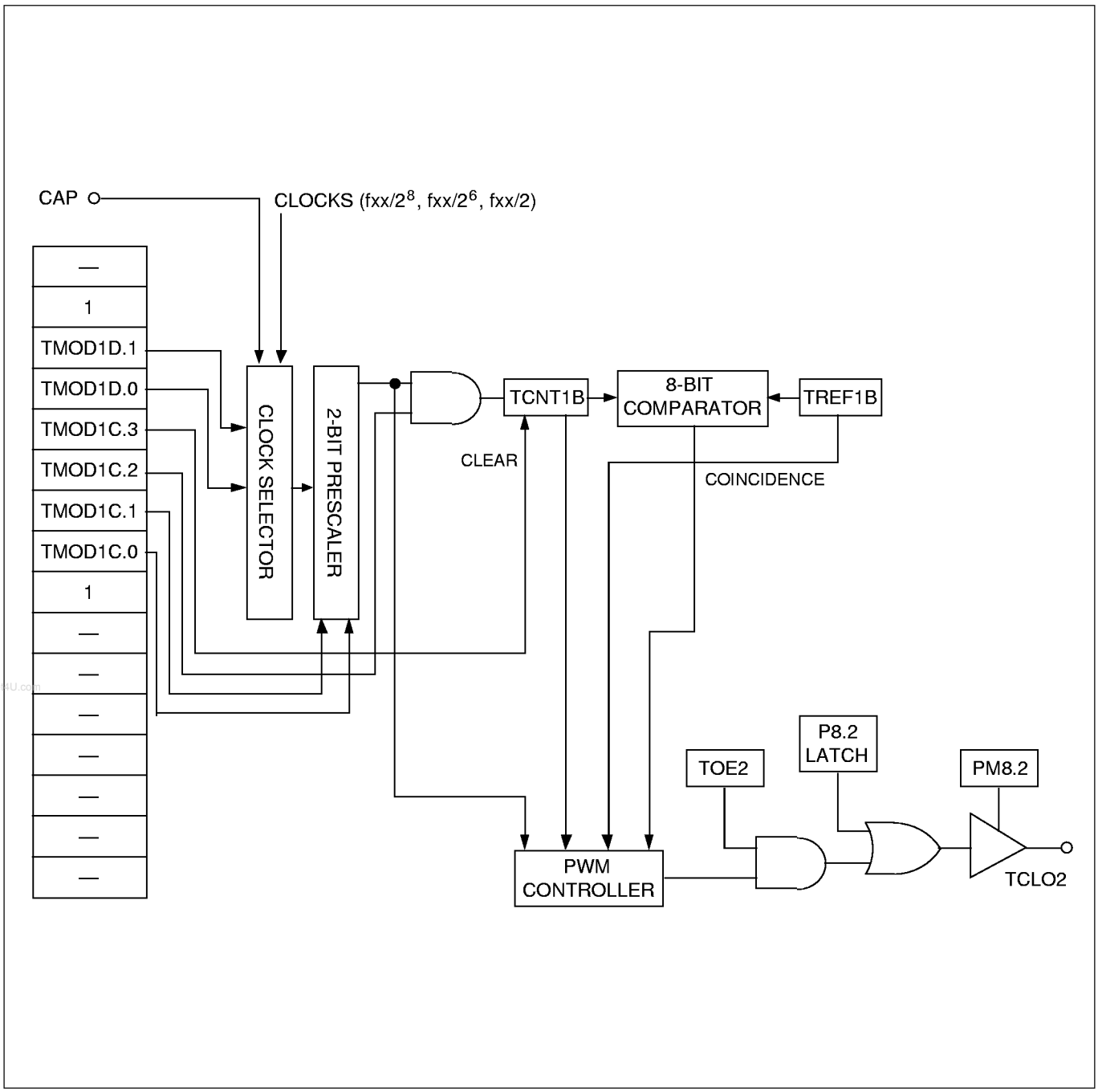


Figure 37. Timer/Counter 1 Circuit Diagram (8-Bit PWMB Mode)

TIMER/COUNTER 1 COUNTER REGISTER (TCNT1)

The 16-bit counter register, TCNT1, consists of two 8-bit counter registers: TCNT1B (upper 8 bits of TCNT1), TCNT1A (lower 8 bits of TCNT1). Whenever start bit in the mode register is set to "1", TCNT1 is cleared to "0" and counting begins. When TCNT1 = TREF1, an overflow occurs in the TCNT1 register, the interrupt request flag, IRQT1, is set to "1", and an interrupt request is generated to indicate that the specified timer/counter interval has elapsed. If 8-bit TC1B mode is selected for timer/counter operation, IRQC flag is set to "1" instead of IRQT1 to activate an interrupt.

Table 24. Counter Register and Interrupt for Each Function

Function	Counter Register	Interrupt for TC	INT Request Flag
16-bit TC1	16-bit TCNT1	INTT1	IRQ1
16-bit PWM/Capture		INTC	IRQC
8-bit TC1A 8-bit PWMA	TCNT1A: Lower 8 bits of TCNT1	INTT1	IRQT1 —
8-bit TC1B 8-bit PWMB	TCNT1B: Upper 8 bits of TCNT1	INTC	IRQC —

TIMER/COUNTER 1 REFERENCE REGISTER (TREF1)

TREF1 is used to store a reference value that is compared to the contents of counter register in order to identify an elapsed time interval. Use the following formula to calculate the correct value to load to the TREF1 reference register:

Timer interval =

$$(\text{TREF1 value} + 1) \times \frac{1}{\text{TMOD1frequencysetting}}$$

Assuming the TREF1 value $\neq$ 0

Table 25. Reference Register for Each Function

Function	Reference Register
16-bit TC1 16-bit PWM/capture	16-bit TREF1
8-bit TC1A 8-bit PWMA	TREF1A: Lower 8 bits of TREF1
8-bit TC1B 8-bit PWMB	TREF1B: Upper 8 bits of TREF1

TIMER/COUNTER 1 OUTPUT ENABLE FLAG (TOE1, TOE2)

The timer/counter 1 output enable flags TOE1 and TOE2 control output from timer/counter 1 to the TCLO1 and TCLO2 pins.

F92H — 1,/4-Bit R/W

TOE1	TOE0	BOE	**TOE2**

When you set the TOE1 flag to "1", TC1 or TC1A data at timer/counter output latch (TOL1) can be output to the TCLO1 pin. Also, PWM/capture or PWMA output is enabled from TCLO1 pin. If TOE2 is set to "1", TC1B data at timer/counter output latch (TOL2) can be output to the TCLO2 pin and PWMB output is enabled from TCLO2 pin.

TIMER/COUNTER 1 MODE REGISTER (TMOD1)

The timer/counter 1 mode register (TMOD1) consists of four 4-bit mode registers. When timer/counter 1 operation stops (TMOD1A.2, TMOD1C.2 = "0"), the contents of counter register are retained until timer/counter 1 is re-enabled.

Table 26. TMOD1A Register Organization

2-Bit Prescaler Bits for Function Group A

TMOD1A.1	TMOD1A.0	2-Bit Prescaler	Affected Function
0	0	Divide by 1	Function group A: TC1, PWM/Capture, TC1A, PWMA
0	1	Divide by 2	
1	0	Divide by 3	
1	1	Divide by 4	

Counter Enable/disable Bit for Function Group A

TMOD1A.2	0	Disable counter operation	Function group A
	1	Enable counter operation	

Operation Start Bit for Function Group A

TMOD1A.3	When TMOD1A.3 is set to "1", the contents of TCNT1, IRQT1, IRQC, TOL1, CREG1, and CREG2 are cleared, counting starts from 0000H, and TMOD1A.3 is automatically cleared to "0". (Bit-addressable)	Function group A

Table 27. TMOD1B Register Organization

Clock Selection Bits for Function Group A

TMOD1B.2	TMOD1B.1	TMOD1B.0	Clock Frequency	Affected Function
0	—	0	Rising edge at TCL1 pin	Function group A: TC1, PWM/Capture, TC1A, PWMA
0	—	1	Falling edge at TCL1 pin	
1	0	0	fxx/2^8 (16.4 kHz at 4.19 MHz)	
1	0	1	fxx/2^6 (65.5 kHz at 4.19 MHz)	
1	1	0	fxx/2^4 (261.9 kHz at 4.19 MHz)	
1	1	1	fxx/2 (2.1 MHz at 4.19 MHz)	

NOTE: '—' means don't care

16-Bit/8-Bit Operating Mode Selection Bit

TMOD1B.3	0	16-bit operation
	1	8-bit operation

Table 28. TMOD1C Register Organization

2-Bit Prescaler or Capture Mode Edge Selection Bits

TMOD1C.1	TMOD1C.0	2-Bit Prescaler (When function group B is selected)	Capture Mode (When 16-Bit PWM/capture mode is selected)
0	0	Divide by 1	Disable capture mode
0	1	Divide by 2	Load counter values into CREG1 on rising edge and into CREG2 on falling edge at CAP pin
1	0	Divide by 3	—
1	1	Divide by 4	—

Counter Enable/Disable Bit for Function Group B

TMOD1C.2	0	Disable counter operation	Function B
	1	Enable counter operation	

Operation Start Bit for Function Group B

TMOD1C.3	When TMOD1C.3 is set to "1", the contents of TCNT1B, IRQC, and TOL2 are cleared , counting starts from 00H, and TMOD1C.3 is automatically reset to "0" (bit-addressable)	Function B

Table 29. TMOD1D Register Organization

Clock Selection Bits for Function Group B

TMOD1D.1	TMOD1D.0	Clock Frequency	Affected Function
0	0	Rising edge at CAP pin	Function group B: TC1B, PWMB
0	1	fxx/2^8 (16.4 kHz at 4.19 MHz)	
1	0	fxx/2^4 (261.9 kHz at 4.19 MHz)	
1	1	fxx/2 (2.1 MHz at 4.19 MHz)	

Timer/Counter or PWM Function Selection Bit for Function Group B

TMOD1D.2	0	Select timer/counter mode	Function B
	1	Select PWM mode	

Timer/Counter or PWM/Capture Function Selection Bit for Function Group A

TMOD1D.3	0	Select timer/counter mode	Function A
	1	Select PWM/capture mode	

TIMER/COUNTER 1 FUNCTION SUMMARY

By setting TMOD1 register, timer/counter 1 can be selected as timer/counter or PWM output mode. When timer/counter 1 is configured for 8-bit operating mode, specific functions are paired for PWM output or timer/counter mode. Table 30 shows corresponding pins and interrupt for each function.

Table 30. Timer/Counter 1 Functions

Function	Output Pin	Input Pin	Interrupt	Function Group
16-bit timer/counter 1	TCLO1	TCL1	INTT1	A
16-bit PWM/capture	TCLO1	CAP	INTC	A
8-bit timer/counter 1A	TCLO1	TCL1	INTT1	A
8-bit timer/counter 1B	TCLO2	CAP	INTC	B
8-bit timer/counter 1A	TCLO1	TCL1	INTT1	A
8-bit PWMB	TCLO2	CAP	—	B
8-bit PWMA	TCLO1	TCL1	—	A
8-bit timer/counter 1B	TCLO2	CAP	INTC	B
8-bit PWMA	TCLO1	TCL1	—	A
8-bit PWMB	TCLO2	CAP	—	B

TIMER/COUNTER 1 PROGRAMMABLE TIMER/COUNTER FUNCTION

Timer/counter 1 can be programmed to generate interrupt requests at variable intervals. The reference register (TREF1) is used to store the value for the desired number of clock pulses between interrupt requests.

The counter register (TCNT1) counts the incoming clock pulses, which are compared to the TREF1 value. When there is a match, an interrupt request is generated.

If TC1 or TC1A is used to generate an interrupt request, the timer/counter 1 interrupt request flag (IRQT1) is set to "1" by the match signal, the status of TOL1 is inverted, and the interrupt is generated.

When TC1B is used to generate an interrupt request, the TC1B interrupt request flag (IRQC) is set to "1" by the match signal, the status of TOL2 is inverted, and the interrupt is generated. After interrupt generation, the counter is cleared to "0", and counting continues.

TIMER/COUNTER 1 OPERATING PROCEDURE

How to Enable the 16-Bit TC1

To enable TC1 operation, TMOD1 should be set as follows:

FA0H	1	1	x	x	TMOD1A
FA1H	0	x	x	x	TMOD1B
FA2H	—	—	—	—	TMOD1C
FA3H	0	—	—	—	TMOD1D

NOTES:
1. 'x' means the appropriate values for prescaler division factor and clock selection.
2. '—' means don't care.

TCNT1 and IRQT1 are cleared to "0", and TC1 operation starts. TC1 clock is output to TCLO1. If TMOD1A.2 is "0", clock signal input to the counter register TCNT1 is stopped. The current TCNT1 value is retained and can be read if necessary.

☞ PROGRAMMING TIP — 16-Bit TC1 Function

Given the following values:

- — Timer/counter clock: Internal fxx/2^8 (fxx = 4.19 MHz)
- — Prescaler value: 1/2 divider
- — TOL clock output pin : P3.1/TCLO1
- — 30 ms timer interval time

1. Calculate the TREF1 value:

$$30\ ms = \frac{TREF1+1}{16.4kHz}$$

$$TREF1 + 1 = \frac{30ms}{60\mu s} = 500 = 1F4H$$

$$TREF1\ value = 1F4H - 1 = 1F3H$$

2. Load the value 01F3H to the TREF1 register:

```
                DI
                SMB     15
                LD      EA,#0F3H
                LD      TREF1A,EA
                LD      EA,#01H
                LD      TREF1B,EA       ;   TREF1 ← #01F3H
                LD      A,#4H
                LD      TMOD1B,A        ;   16-bit, fxx/2^8 select
                LD      A,#0DH
                LD      TMOD1A,A        ;   1/2 divider, enable, start timer/counter operation
                BITR    P3.1            ;   P3.1/TCLO1 clear
                LD      EA,#20H
                LD      PMG2,EA         ;   P3.1 ← output
                BITS    TOE1            ;   TOE1 enable
                EI
                BITS    IET1            ;   IET1 enable
;
INTT1                                   ;   Timer/counter interrupt service routine
                IRET
```

How to Enable 8-Bit TC1A and 8-Bit TC1B

To enable TC1A and TC1B operation, TMOD1 should be set as follows:

FA0H	1	1	x	x	TMOD1A
FA1H	1	x	x	x	TMOD1B
FA2H	1	1	x	x	TMOD1C
FA3H	0	0	x	x	TMOD1D

NOTE: 'x' means the appropriate value for prescaler division factor and clock selection.

TCNT1A, TCNT1B, IRQT1, IRQC are cleared to "0", and 8-bit timer/counter operation starts. If TMOD1A.2 and TMOD1C.2 are "0", clock signal input to the counter registers TCNT1A and TCNT1B is stopped. The current counter values are retained and can be read if necessary.

Table 31. TC1A and TC1B Function Summary

Timer/Counter	External Clock Input Pin	Clock Output Pin	Interrupt Request Flag	Interrupt
TC1A	TCL1	TCLO1	IRQT1	INTT1
TC1B	CAP	TCLO2	IRQC	INTC

NOTE: When TC1B is selected, the IRQC is not a capture interrupt request flag but 8-bit timer/counter (TC1B) interrupt request flag.

☞ PROGRAMMING TIP — 8-Bit TC1A and 8-Bit TC1B Function

1. TC1A function:
   - — Timer/counter clock — Internal fxx/2^8 (fxx = 4.19 MHz)
   - — Prescaler value — 1/1 divider
   - — TOL clock output pin — P3.1/TCLO1
   - — 12 ms timer interval time

$$12\ ms = \frac{TREF1A+1}{16.4kHz} \quad \therefore \quad TREF1A\ value = C8H - 1 = C7H$$

2. TC1B function:
   - — Timer/counter clock — Internal fxx/2^8 (fxx = 4.19 MHz)
   - — Prescaler value — 1/1 divider
   - — TOL clock output pin — P8.2/TCLO2
   - — 5 ms timer interval time

$$5\ ms = \frac{TREF1B+1}{16.4kHz} \quad \therefore \quad TREF1B\ value = 53H - 1 = 52H$$

```
        DI
        SMB     15
        LD      EA,#0C7H
        LD      TREF1A,EA       ;   TC1A 12 ms timer interval time set
        LD      EA,#52H
        LD      TREF1B,EA       ;   TC1B 5 ms timer interval time set
        LD      A,#0CH
        LD      TMOD1B,A        ;   TC1A, 8-bit, fxx/2^8 select
        LD      A,#0CH
        LD      TMOD1A,A        ;   TC1A, 1/1 divider, enable, start
        LD      A,#1H
        LD      TMOD1D,A        ;   TC1B, fxx/2^8 select
        LD      A,#0CH
        LD      TMOD1C,A        ;   TC1B, 1/1 divider, enable, start
        BITR    P3.1            ;   P3.1/TCLO1 clear
        LD      EA,#20H
        LD      PMG2,EA         ;   P3.1 ← output
        BITS    TOE1            ;   TOE1 enable
        BITR    P8.2            ;   P8.2 clear
        LD      EA,#40
        LD      PMG3,EA         ;   P8.2 ← output
        BITS    TOE2            ;   TOE2 enable for output P8.2
        BITS    IET1            ;   TC1A interrupt IET1 enable
        BITS    IEC             ;   TC1B interrupt IEC enable
        EI
INTT1                           ;   TC1A interrupt service routine
        IRET
INTC                            ;   TC1B interrupt service routine
        IRET
```

How to Enable 8-Bit TC1A and 8-Bit PWMB

To enable TC1A and PWMB operation, TMOD1 should be set as follows:

FA0H	1	1	x	x	TMOD1A
FA1H	1	x	x	x	TMOD1B
FA2H	1	1	x	x	TMOD1C
FA3H	0	1	x	x	TMOD1D

NOTE: 'x' means the appropriate value for prescaler division factor and clock selection.

TCNT1A, TCNT1B, and IRQT1 are cleared to logic zero; then, TC1A and PWMB operation starts. If TMOD1A.2 and TMOD1C.2 are set to zero, clock signal inputs to the counter registers TCNT1A and TCNT1B is halted. The current counter values are retained and can be read if necessary.

Table 32. TC1A and PWMB Function Summary

Function	External Clock Input Pin	Clock Output Pin	Interrupt Request Flag	Interrupt
TC1A	TCL1	TCLO1	IRQT1	INTT1
PWMB	CAP	TCLO2	—	—

How to Enable 8-Bit TC1B and 8-Bit PWMA

To enable TC1B and PWMA operation, TMOD1 should be set as follows:

FA0H	1	1	x	x	TMOD1A
FA1H	1	x	x	x	TMOD1B
FA2H	1	1	x	x	TMOD1C
FA3H	1	0	x	x	TMOD1D

NOTE: 'x' means the appropriate value for prescaler division factor and clock selection.

TCNT1B, TCNT1A, and IRQC are cleared to "0"; then, TC1B and PWMA operation starts. If TMOD1A.2 and TMOD1C.2 are "0", clock signal input to the counter registers TCNT1A and TCNT1B is stopped. The current counter values are retained and can be read if necessary.

Table 33. TC1B and PWMA Function Summary

Function	External Clock Input Pin	Clock Output Pin	Interrupt Request Flag	Interrupt
TC1B	CAP	TCLO2	IRQC	INTC
PWMA	TCL1	TCLO1	—	—

☞ PROGRAMMING TIP — 8-Bit TC1A and 8-Bit PWMB Function

1. TC1A function:
   - — Timer/counter clock — Internal fxx/2^8 (fxx = 4.19 MHz)
   - — Prescaler value — 1/1 divider
   - — TOL clock output pin — P3.1/TCLO1
   - — 12 ms timer interval time

$$12\ ms = \frac{TREF1A+1}{16.4kHz} \quad \therefore \quad TREF1A\ value = C8H - 1 = C7H$$

2. PWMB function:
   - — Timer/counter clock — Internal fxx/2^8
   - — Prescaler value — 1/1 divider
   - — PWM clock output pin — P8.2/TCLO2
   - — Duty value

```
        DI
        SMB     15
        LD      EA,#0C7H
        LD      TREF1A,EA       ;   TC1A 12 ms timer interval time set
        LD      EA,#01H
        LD      TREF1B,EA       ;   PWM duty value set
        LD      A,#0CH
        LD      TMOD1B,A        ;   TC1A, 8-bit, fxx/2^8 select
        LD      A,#0CH
        LD      TMOD1A,A        ;   TC1A, 1/1 divider, enable, start
        LD      A,#5H
        LD      TMOD1D,A        ;   8-bit PWMB, fxx/2^8 select
        LD      A,#0CH
        LD      TMOD1C,A        ;   8-bit PWMB, 1/1 divider, enable, start
        BITR    P3.1            ;   P3.1/TCLO1 clear
        LD      EA,#20H
        LD      PMG2,EA         ;   P3.1 ← output
        BITS    TOE1            ;   TOE1 enable
        BITR    P8.2            ;   P8.2 clear
        LD      EA,#40H
        LD      PMG3,EA         ;   P8.2 ← output
        BITS    TOE2            ;   TOE2 enable for PWM output P8.2
        BITS    IET1            ;   TC1A interrupt IET1 enable
        EI
INTT1                           ;   TC1A interrupt service routine
        IRET
```

TIMER/COUNTER 1 EVENT COUNTER FUNCTION

Timer/counter 1 can be used to monitor system 'events' by using the external clock input at the TCL1 and CAP pins as the counter source.

With the exception of the different TMOD1B.0–TMOD1B.2 and TMOD1D.0–TMOD1D.1 settings, the operation sequence for TC1B event count function is identical to TC1 and TC1A. Remember that TMOD1B.3 must be set to "1" for 8-bit operation.

TIMER/COUNTER 1 CLOCK FREQUENCY OUTPUT

Using timer/counter 1, you can also output a modifiable clock frequency to the timer/counter 1 clock output pins, TCLO1 and TCLO2.

To enable the output to the TCLO1 and TCLO2 pins, timer output pins (TCLO0/P3.1 and TCLO/P8.2) must be set to output mode, latches for the pins should be cleared to "0", and timer output must be enabled.

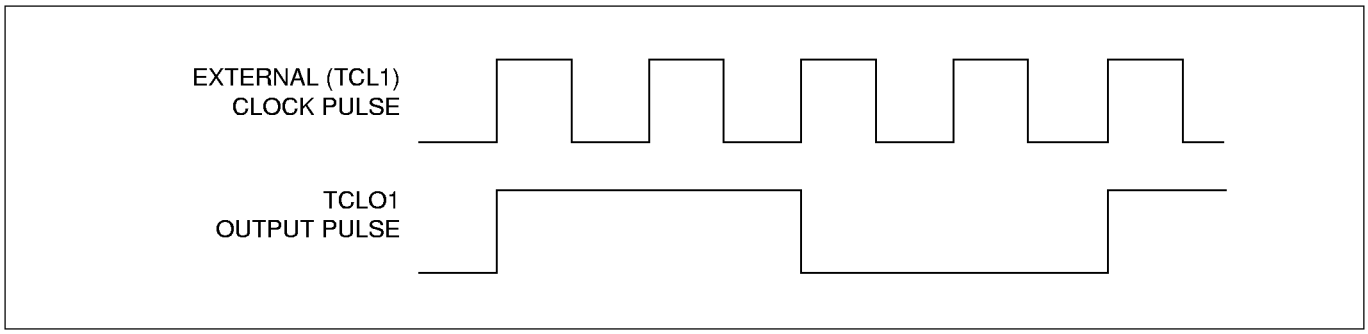
☞ PROGRAMMING TIP — Timer/Counter Signal Output to the TCLO1 Pin (TC1 Mode)

Output a 30 ms pulse width signal to the TCLO1 pin:

```
BITS    EMB
SMB     15
LD      EA,#0E9H
LD      TREF1A,EA
LD      EA,#01H
LD      TREF1B,EA
LD      A,#0CH
LD      TMOD1A,A
LD      A,#4H
LD      TMOD1B,A
LD      A,#0H
LD      TMOD1D,A
LD      A,#20H
LD      PMG2,EA          ;   P3.1 ← Output mode
BITR    P3.1             ;   P3.1 clear
BITS    TOE1
```

☞ PROGRAMMING TIP — External TCL1 Clock Output to the TCLO1 Pin (TC1A Mode)

Output the external TCL1 clock source to the TCLO1 pin (divided by four):




```
BITS    EMB
SMB     15
LD      EA,#01H
LD      TREF1A,EA
LD      A,#0CH
LD      TMOD1A,EA
LD      A,#8H
LD      TMOD1B,EA
LD      A,#0H
LD      TMOD1D,A
LD      EA,#20H
LD      PMG2,EA          ;   P3.1 ← output mode
BITR    P3.1             ;   P3.1 clear
BITS    TOE1
```

PWM OUTPUT FUNCTION

Timer/counter 1 can be used for PWM output — to generate pulses of programmable lengths and intervals. The 16-bit or 8-bit PWM mode is selected by the TMOD1 register setting.

The counter register counts modulus 256, that is, from 0 to 255. The value of the counter register is compared to the contents of the TREF1 register. If the content of reference register is greater than the counter value, the corresponding TCLO1 or TCLO2 output is set to High level. If the content of the reference register is equal to, or less than the counter value, the output will be Low level.

The PWM output can be set continuously low by loading the reference register with 00H and continuously high except the 256th pulse of the counter clock by loading the reference register with FFH. The pulse width ratio (duty cycle) is therefore defined by the contents of the TREF1 register. The pulse width ratio is in the range 0 to 1 and may be programmed in increments of 1/256.

$$\text{High/low ratio of output} = \frac{(\text{TREF1})}{256-(\text{TREF1})}$$

where the TREF1 value $\neq$ 0

The counter is automatically cleared when an overflow occurs, and it then resumes counting from zero. When the counter is re-enabled after being stopped, it continues the count from the count value it contained when it was stopped.

When 16-bit PWM mode is selected, the lower 8 bit of the TCNT1 is used as a 8-bit counter and the upper 8 bits of the TCNT1 is used for pulse expansion. These upper 8 bits are compared with the upper 8 bits of the reference register.

Based on the value of the upper 8 bits of the reference register, the n-th high pulse widths are periodically expanded by the selected frequency period. The pulse expansion is repeated with a period of 256 cycles.

Table 34 shows which cycles are expanded according to the reference register value. If 8-bit PWM mode is selected, the only upper or lower 8 bits of the counter and reference registers are available.

Figures 32 and 33 show the 16-bit and 8-bit PWM outputs which result with a 4 MHz clock frequency.

Table 34. PWM Function Summary

Function	Counter Register	Reference Register	PWM Output Pin	TMOD1 Setting
16-bit PWM/capture	16-bit TCNT1	16-bit TREF1	TCLO1	TMOD1A ← 11xx TMOD1B ← 0xxx TMOD1C ← –––– TMOD1D ← 1–––
8-bit PWMA	8-bit TCNT1A	8-bit TREF1A	TCLO1	TMOD1A ← 11xx TMOD1B ← 1xxx TMOD1C ← –––– TMOD1D ← 1–––
8-bit PWMB	8-bit TCNT1B	8-bit TREF1B	TCLO2	TMOD1A ← –––– TMOD1B ← 1––– TMOD1C ← 11xx TMOD1D ← –1xx

NOTES:
1. 'x' means the appropriate value for prescaler division factor and clock selection.
2. '—' means don't care.

Table 35. 16-Bit PWM Output Stretch Values

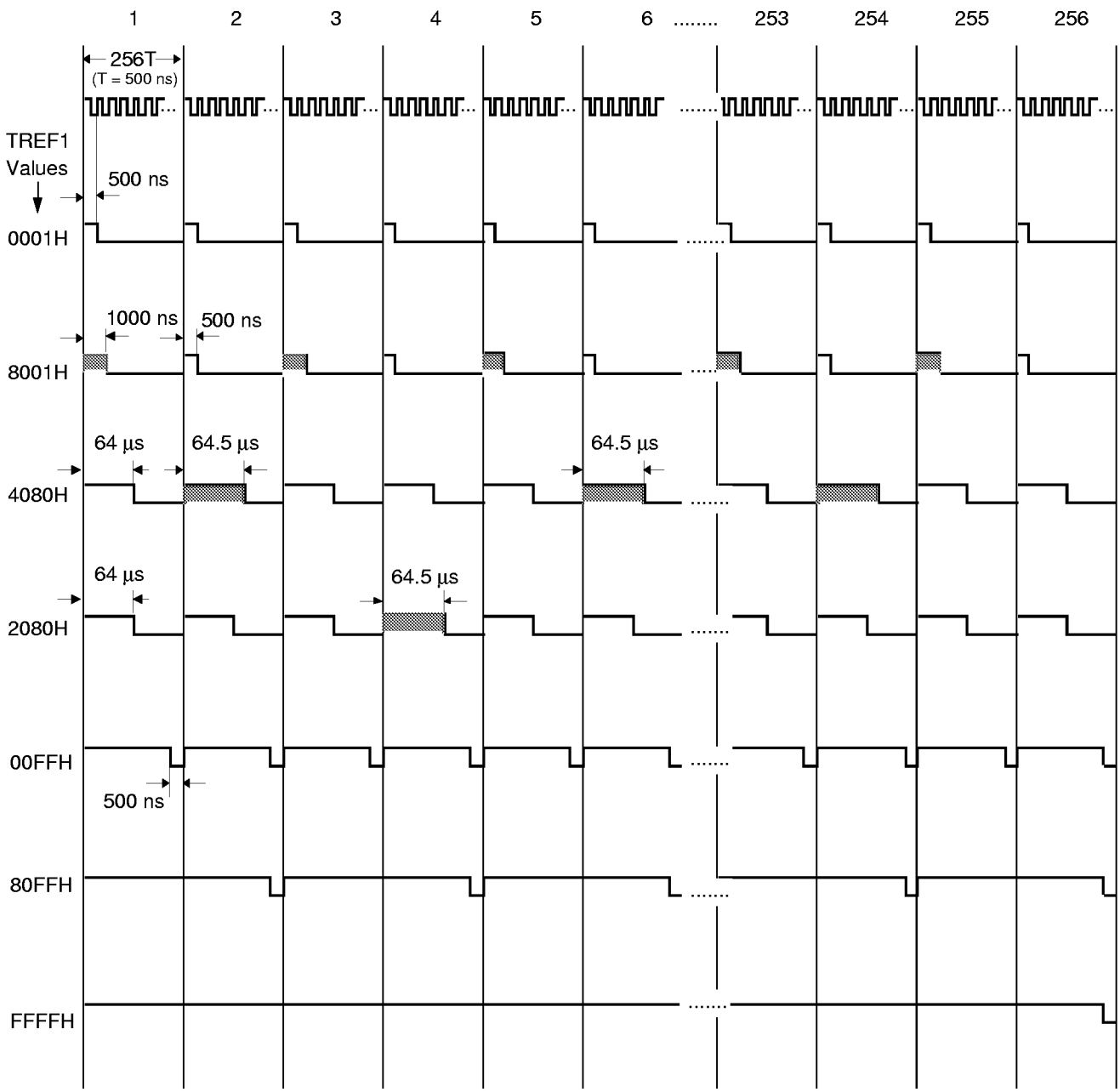
TREF1B Register Bit	Expanded Cycle Number By TREF1B Setting
TREF1B.7	1, 3, 5, 7, 9, 11, 13, ... 243, 245, 247, 249, 251, 253, 255
TREF1B.6	2, 6, 10, 14, 18, 22, ... 234, 238, 242, 246, 250, 254
TREF1B.5	4, 12, 20, 28, 36, ... 220. 228, 236, 244, 252
TREF1B.4	8, 24, 40, 56, ... 200, 216, 232, 248
TREF1B.3	16, 48, 80, 112, 144, 176
TREF1B.2	32, 96, 160, 224
TREF1B.1	64, 192
TREF1B.0	128

NOTE: Even if FFH is loaded into TREF1B, the 256th cycle is not expanded.

☞ PROGRAMMING TIP — Setting TREF1B to Expand PWM Output Pulse

To expand the pulses 64, 128, and 192, load 3H to TREF1B:

```
BITS    EMB
SMB     15
(TMOD1 Setting)
LD      TREF1A,#data
LD      EA,#03H
LD      TREF1B,EA          ;    Expand the 64th, 128th, and 192nd pulses
•
•
•
```



* The PWM outputs are shown when fxx/2 is selected as a counter clock source (fxx = 4 MHz).

means the pulse expanded by selected clock source (fxx/2) according to TREF1B shown in Table 11–18. Specially, the last three waveforms of the figure show PWM waveforms expanded by different values of TREF1B when TREF1A cotains FFH.

Figure 38. PWM Waveform for 16-bit Operation

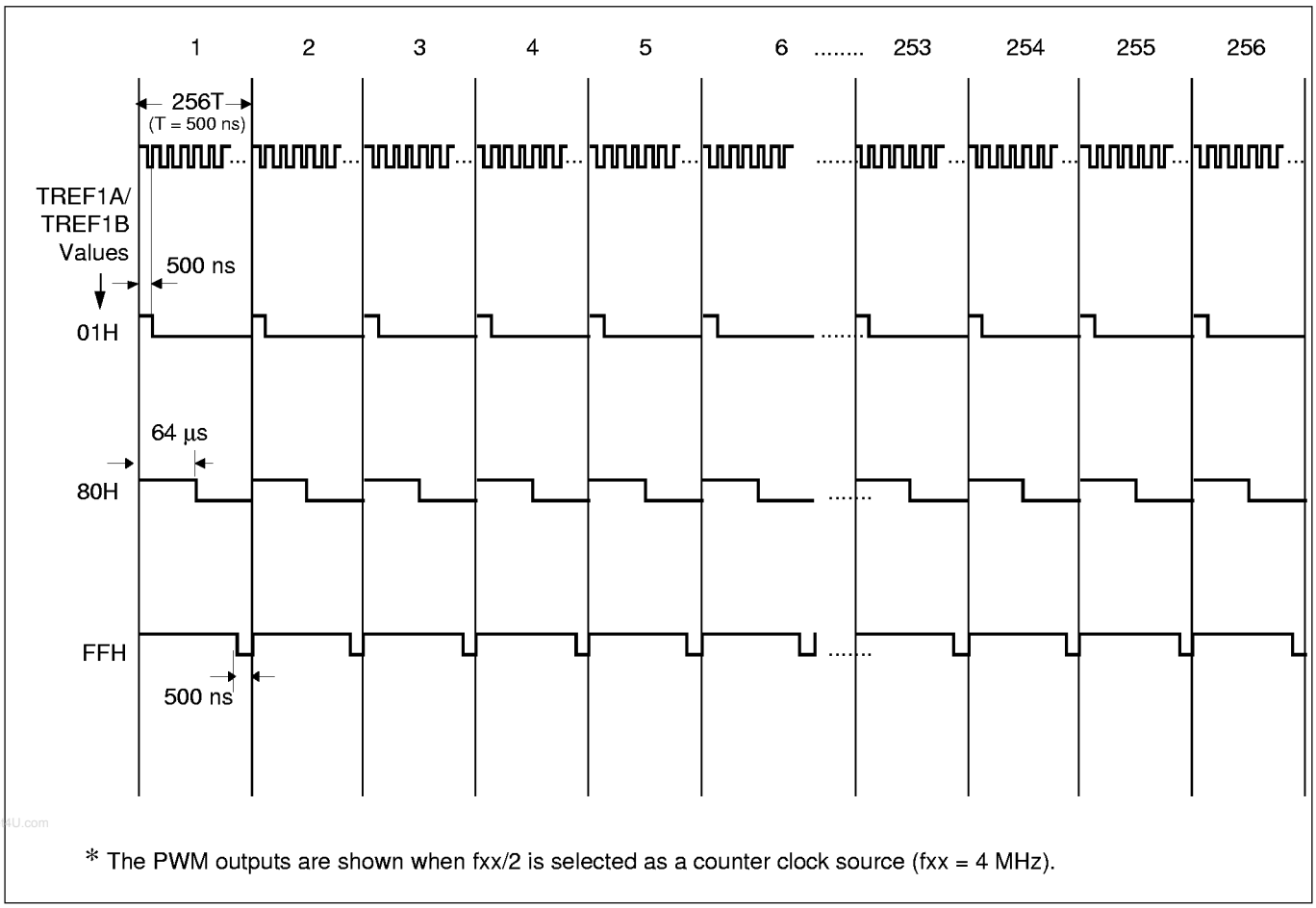


Figure 39. PWM Waveform for 8-bit Operation

CAPTURE REGISTER (CREG1, CREG2)

Timer/counter 1 can be used for a capture function by setting TMOD1D.3 when the 16-bit PWM/capture function is selected. Timer/counter 1 will capture the current value of the TCNT1 into the capture register 1, CREG1, on the rising edge of an incoming signal at the CAP pin. On falling edges, it captures into capture register 2, CREG 2. Rising or falling edge selection is controlled by bits TMOD1C.0–TMOD1C.1. Capture mode is disabled by clearing TMOD1C.0–TMOD1C.1 to logic zero.

When a rising or falling edge is detected at the CAP pin, the individual capture interrupt request flag (IRQC1, IRQC2) is set to "1" and ORed to set the capture interrupt request flag (IRQC). An interrupt is generated by the IRQC flag setting if the capture interrupt enable bit, IEC, is set to "1". To generate capture interrupts, the individual capture interrupt enable flags must first be set to "1".

FD6H

IEC2	IRQC2	IEC1	IRQC1

The 16-bit capture register (CREG1, CREG2) can be read by 8-bit RAM control instructions only. CREG1 is comprised of registers CREG1A and CREG1B and CREG2 of registers CREG2A and CREG2B.

The capture function can be used to detect incoming signals, and to measure the pulse width of incoming signals. This allows you to read the capture register value and calculate the elapsed time between pulses.

PWM OUTPUT OPERATING PROCEDURE

How to Enable the 16-Bit PWM/Capture Function

To enable PWM/capture operation, TMOD1 should be set as follows:

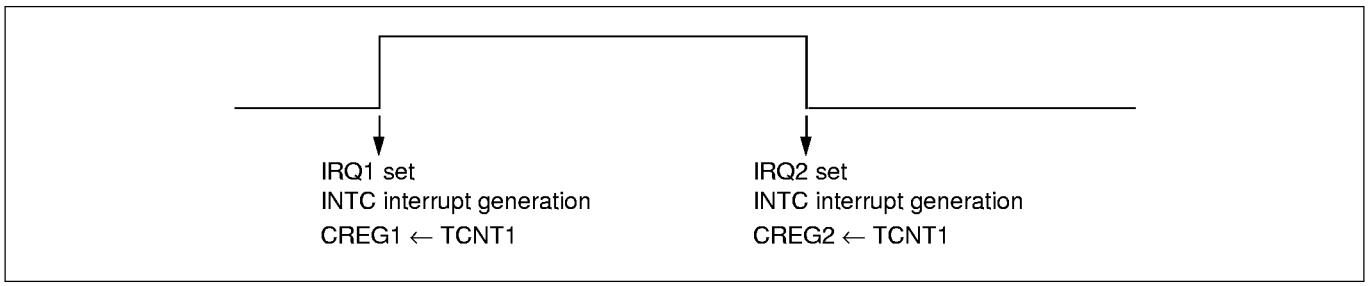
FA0H	1	1	0	1	TMOD1A
FA1H	0	x	x	x	TMOD1B
FA2H	—	—	x	x	TMOD1C
FA3H	1	—	—	—	TMOD1D

NOTES:
1. 'x' means the appropriate value for prescaler division factor and clock selection.
2. '—' means don't care.

TCNT1 and IRQC are cleared to "0", and PWM is output from TCLO1 pin. If capture interrupt enable flag, IEC is set to "1", the capture interrupt request flag, and IRQC is set to "1", an interrupt is generated when a rising or falling edge is detected at the CAP pin.

☞ PROGRAMMING TIP — 16-Bit PWM/Capture Function

1. PWM function:
   - — PWM clock source: $fxx/2^8$
   - — PWM clock output pin: P3.1/TCLO1
   - — Prescaler value: 1/2 divider
2. Capture function:
   - — Capture timing check clock source: $fxx/2^8$
   - — Capture trigger input pin: P3.2/CAP
   - — Trigger source: Rising and falling edges




```
DI
SMB     15
LD      EA,#0F3H
LD      TREF1A,EA
LD      EA,#01H
LD      TREF1B,EA       ;   TREF1 ← PWM data
```

☞ PROGRAMMING TIP — 16-Bit PWM/Capture Function (Continued)

```
                LD      A,#4H
                LD      TMOD1B,A        ;   16-bit, fxx/2^8 select
                LD      A,#0DH
                LD      TMOD1A,A        ;   1/2 divider, enable, start
                BITR    P3.1            ;   P3.1/TCLO1 clear
                LD      EA,#20H
                LD      PMG2,EA         ;   P3.1 ← output, P3.2/CAP ← input
                BITS    TOE1            ;   TOE1 enable
                LD      A,#8H
                LD      TMOD1D,A        ;   Capture clock fxx/2^8, PWM/capture mode
                LD      A,#0DH
                LD      TMOD1C,A        ;   Capture trigger rising and falling
                BITS    IEC1            ;   Rising edge interrupt enable flag set
                BITS    IEC2            ;   Falling edge interrupt enable flag set
                BITS    IET1            ;   IET1 enable
                BITS    IEC             ;   Capture interrupt enable flag
                EI
INTT1           •                       ;   Timer/counter interrupt service routine
                •                       ;   When capture TCNT1 overflow generated
                •
                IRET
INTC  PUSH      SB
                PUSH    EA
                PUSH    HL
                PUSH    WX
                PUSH    YZ
                SMB     15
                BTST    IRQC1           ;   Check capture rising edge check
                JPS     INTC1
                BITR    IRQC1           ;   Yes, capture rising edge, IRQC1 clear
                LD      EA,CREG1B
                LD      HL,EA
                LD      EA,CREG1A
                SMB     0
                LD      CIBUF1,EA       ;   CIBUF1 ← CREG1A
                LD      EA,HL
                LD      CIBUF2,EA       ;   CIBUF2 ← CREG1B
INCRET          POP     YZ
                POP     WX
                POP     HL
                POP     EA
                POP     SB
                IRET
;
INTC1           BITR    IRQC2           ;   Capture falling edge interrupt, IRQC2 clear
                LD      EA,CREG2B
                LD      YZ,EA
                LD      EA,CREG2A
                SMB     0
                LD      CEBUF1,EA       ;   CEBUF1 ← CREG2A
                LD      EA,YZ
                LD      CEBUF2,EA       ;   CEBUF2 ← CREG2B
                JPS     INCRET
```

How to Enable 8-Bit PWMA and 8-Bit PWMB

To enable PWMA and PWMB operation, TMOD1 should be set as follows:

FA0H	1	1	x	x	TMOD1A
FA1H	1	x	x	x	TMOD1B
FA2H	1	1	x	x	TMOD1C
FA3H	1	1	x	x	TMOD1D

NOTE: 'x' means the appropriate values for prescaler division factor and clock selection.

TCLO1 and TCLO2 pins are used for PWM outputs. The lower 8 bits of the counter and reference registers are used for PWMA output, and the upper 8 bits used for PWMB.

Table 36. PWMA and PWMB Function Summary

Function	Clock Input Pin	Clock Output Pin	Interrupt Request Flag	Interrupt
PWMA	TCL1	TCLO1	—	—
PWMB	CAP	TCLO2	—	—

☞ PROGRAMMING TIP — 8-Bit PWMA and 8-Bit PWMB Function

1. PWMA function:
   - — Timer/counter clock — Internal fxx/2^8
   - — Prescaler value — 1/1 divider
   - — PWMA clock output pin — P3.1/TCLO1
   - — Duty value
2. PWMB function:
   - — Timer/counter clock — Internal fxx/2^8
   - — Prescaler value — 1/1 divider
   - — PWMB clock output pin — P8.2/TCLO2
   - — Duty value

```
DI
SMB     15
LD      EA,#0C7H
LD      TREF1A,EA       ;   PWMA duty value set
LD      EA,#01H
LD      TREF1B,EA       ;   PWMB duty value set
LD      EA,#0CH
LD      TMOD1B,EA       ;   PWMA, 8-bit, fxx/2^8 select
LD      EA,#0CH
LD      TMOD1A,EA       ;   PWMA, 1/1 divider, enable, start
LD      EA,#0DH
LD      TMOD1D,EA       ;   8-bit PWMB, fxx/2^8 select
LD      EA,#0CH
LD      TMOD1C,EA       ;   8-bit PWMB, 1/1 divider, enable, start
BITR    P3.1            ;   P3.1/TCLO1 clear
LD      EA,#20H
LD      PMG2,EA         ;   P3.1 ← output
BITS    TOE1            ;   TOE1 enable
BITR    P8.2            ;   P8.2 clear
LD      EA,#40H
LD      PMG3,EA         ;   P8.2 ← output
BITS    TOE2            ;   TOE2 enable for PWM output P8.2
EI
```

WATCH TIMER

Watch timer functions include real-time and watch-time measurement and interval timing for the system clock. It is also used as a clock source for generating buzzer output. To start watch timer operation, set bit 2 of the watch timer mode register, WMOD.2, to "1". The watch timer starts, the interrupt request flag IRQW is automatically set to "1", and interrupt requests commence in 0.5-second intervals. Since the watch timer functions as a quasi-interrupt instead of a vectored interrupt, the IRQW flag should be cleared to "0" by program software as soon as a requested interrupt service routine has been executed.

The watch timer can generate a steady 2 kHz, 4 kHz, 8 kHz, or 16 kHz signal to the BUZ pin. To generate a BUZ signal, the output latch for I/O port 3.3 is cleared to "0" and the port 3.3 output mode flag (PM3.3) set to 'output' mode

By setting WMOD.1 to "1", the watch timer will function in high-speed mode, generating an interrupt every 3.91 ms. High-speed mode is useful for timing events for program debugging sequences.

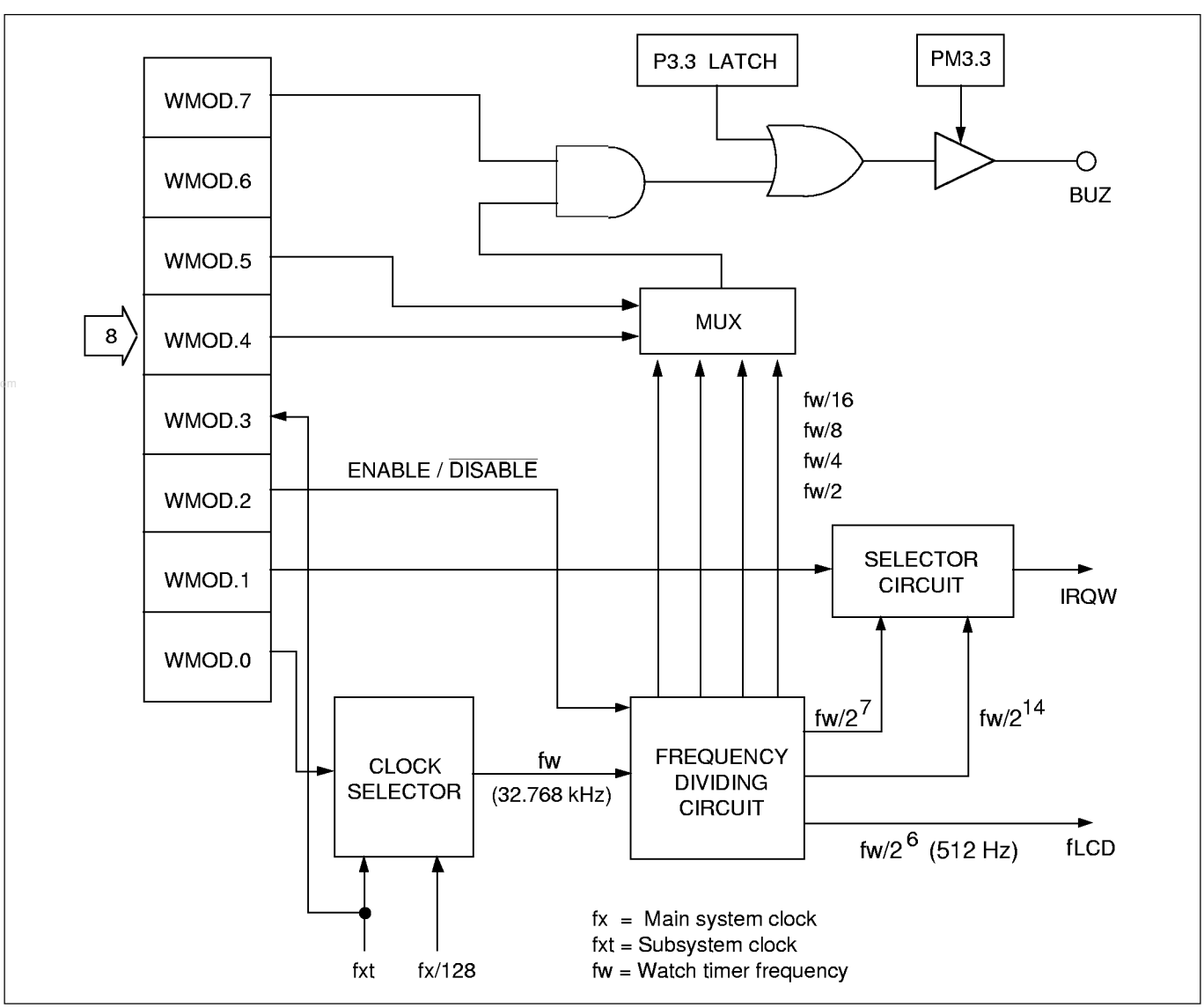


Figure 40. Watch Timer Circuit Diagram

WATCH TIMER MODE REGISTER (WMOD)

The watch timer mode register WMOD is used to select specific watch timer operations.

Table 37. Watch Timer Mode Register (WMOD) Organization (8-Bit W)

Bit Name	Values		Function	Address
WMOD.7	0		Disable buzzer (BUZ) signal output	F89H
	1		Enable buzzer (BUZ) signal output	
WMOD.6	0		Always logic zero	
WMOD.5 – .4	0	0	2 kHz buzzer (BUZ) signal output	
	0	1	4 kHz buzzer (BUZ) signal output	
	1	0	8 kHz buzzer (BUZ) signal output	
	1	1	16 kHz buzzer (BUZ) signal output	
WMOD.3	0		Input level to XT_{in} pin is low (read-only bit)	F88H
	1		Input level to XT_{in} pin is high (read-only bit)	
WMOD.2	0		Disable watch timer; clear frequency dividing circuits	
	1		Enable watch timer	
WMOD.1	0		Normal mode; sets IRQW to 0.5 s	
	1		High-speed mode; sets IRQW to 3.91 ms	
WMOD.0	0		Select (fx/128) as the watch timer clock (fw)	
	1		Select subsystem clock as watch timer clock (fw)	

NOTE: Main system clock frequency (fx) is assumed to be 4.19 MHz; subsystem clock (fxx) is assumed to be 32.768 kHz.

☞ PROGRAMMING TIP — Using the Watch Timer

1. Select a subsystem clock as the LCD display clock, a 0.5 second interrupt, and 2 kHz buzzer enable:

```
BITS    EMB
SMB     15
LD      EA,#80H
LD      PMG2,EA         ;   P3.3 ← output mode
BITR    P3.3
LD      EA,#85H
LD      WMOD,EA
BITS    IEW
```

2. Sample real-time clock processing method:

```
CLOCK   BTSTZ   IRQW    ;   0.5 second check
        RET             ;   No, return
        •               ;   Yes, 0.5 second interrupt generation
        •
        •               ;   Increment HOUR, MINUTE, SECOND
```

LCD CONTROLLER/DRIVER

The KS57C2016 microcontroller can directly drive an up-to-20-digit (160-segment) LCD panel. Data written to the LCD display RAM can be transferred to the segment signal pins automatically without program control.

When a subsystem clock is selected as the LCD clock source, the LCD display is enabled even during Stop and Idle modes.

LCD RAM ADDRESS AREA

RAM addresses 1D8H–1FFH are used as LCD data memory. These locations can be addressed by 1-bit or 4-bit instructions. When the bit value of a display segment is "1", the LCD display is turned on; when the bit value is "0", the display is turned off.

Display RAM data are sent out through segment pins SEG0–SEG39 using a direct memory access (DMA) method that is synchronized with the f_{LCD} signal. RAM addresses in this location that are not used for LCD display can be allocated to general-purpose use.

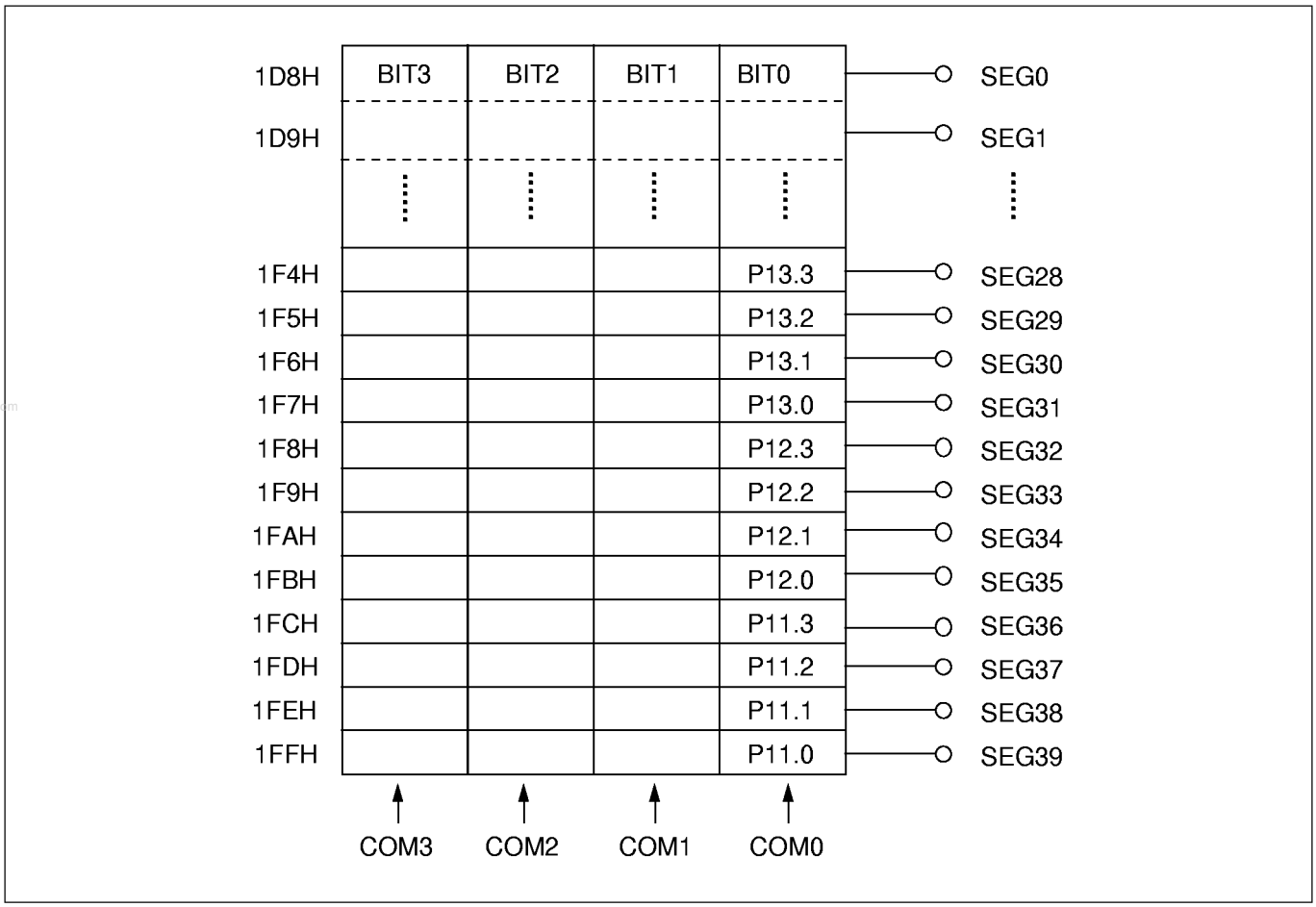


Figure 41. LCD Display Data RAM Organization

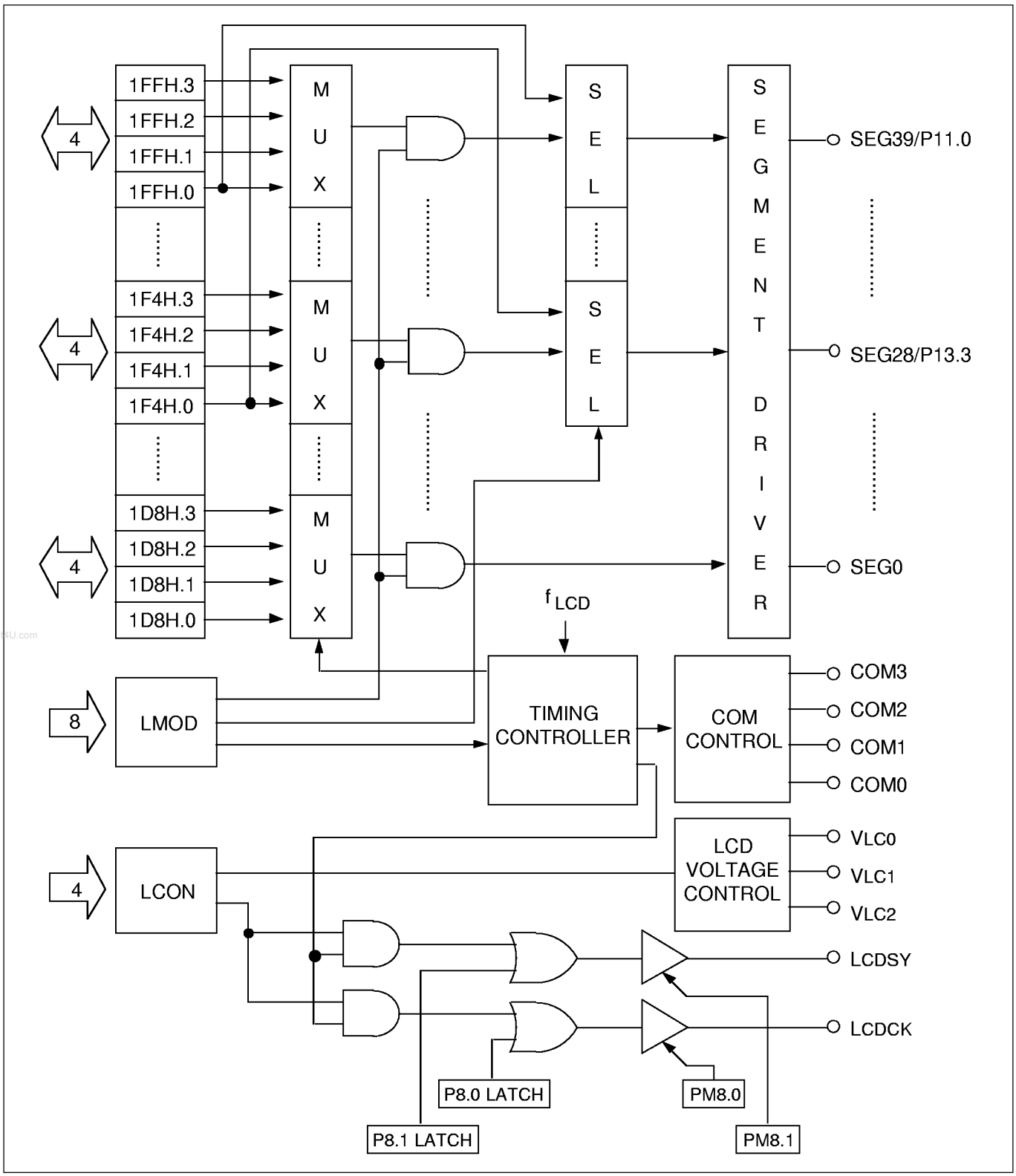


Figure 42. LCD Circuit Diagram

LCD CONTROL REGISTER (LCON)

You use the LCON register to turn the LCD display on and off, to output LCD clock (LCDCK) and synchronizing signal (LCDSY) for LCD display expansion, and to control the flow of current to dividing resistors in the LCD circuit. When LCON.0 is logic zero, the LCD display is turned off and the current to the dividing resistors is cut off, despite the current LMOD.3 value.

Table 38. LCD Control Register (LCON) Organization

LCON Bit	Setting	Description
LCON.3	0	This bit is used for internal testing only; set to logic zero.
LCON.2	0	Disable LCDCK and LCDSY signal outputs.
	1	Enable LCDCK and LCDSY signal outputs.
LCON.1	0	Always set to logic zero.
LCON.0	0	LCD output low; turn display off, cut off current to dividing resistors, and output ports 11–13 latch contents.
	1	If LMOD.3 = "0": LCD output low; turn display off; output ports 11–13 latch contents; If LMOD.3 = "1": COM and SEG output in display mode; turn display on output ports 11–13 latch contents.

Table 39. Relationship of LCON.0 and LMOD.3 Bit Settings

LCON.0	LMOD.3	COM0–COM3	SEG0–SEG39	P11.0–P13.3
0	x	Output low; LCD display off	Output low; LCD display off	Output latch contents; cut off current to dividing resistors
1	0	Output low; LCD display off	Output low; LCD display off	Output latch contents; LCD display off
	1	COM output corresponds to display mode	SEG output corresponds to display mode	Output latch contents; LCD display on

NOTE: 'x' means 'don't care.'

Table 40. LCD Clock Signal (LCDCK) Frame Frequency

LCDCK Frequency	Static	1/2 Duty	1/3 Duty	1/4 Duty
fw/2^9 (64 Hz)	64	32	21	16
fw/2^8 (128 Hz)	128	64	43	32
fw/2^7 (256 Hz)	256	128	85	64
fw/2^6 (512 Hz)	512	256	171	128

NOTES:
1. 'fw' is the watch timer clock frequency of 32.768 kHz.
2. The watch timer clock frequency for LCDCK is shown in parentheses in column one.

LCD MODE REGISTER (LMOD)

The LCD mode register LMOD is used to control LCD controller. Since LCD clock (LCDCK) is generated by dividing the watch timer clock (fw), the watch timer must be enabled when the LCD display is turned on. during Idle and Stop modes if a subsystem clock is used as the watch timer source.

Table 41. LCD Mode Control Register (LMOD) Organization (8-Bit W)

LMOD.7	LMOD.6	LCD Output Segments and 1-Bit Output Pins
0	0	Segments 28–31, 32–35, and 36–39
0	1	Segments 28–31 and 32–35; 1-bit output at P11.0–P11.3
1	0	Segments 28–31; 1-bit output at P12.0–P12.3 and P11.0–P11.3
1	1	1-bit output only at P13.0–P13.3, P12.0–P12.3, and P11.0–P11.3

LMOD.5	LMOD.4	LCD Clock (LCDCK) Frequency
0	0	32.768 kHz watch timer clock (fw)/2^9 = 64 Hz
0	1	fw/2^8 = 128 Hz
1	0	fw/2^7 = 256 Hz
1	1	fw/2^6 = 512 Hz

LMOD.3	LMOD.2	LMOD.1	LMOD.0	Duty and Bias Selection for LCD Display
0	x	x	x	LCD display off
1	0	0	0	1/4 duty, 1/3 bias
1	0	0	1	1/3 duty, 1/3 bias
1	0	1	0	1/2 duty, 1/2 bias
1	0	1	1	1/3 duty, 1/2 bias
1	1	0	0	Static

NOTE: 'x' means 'don't care'.

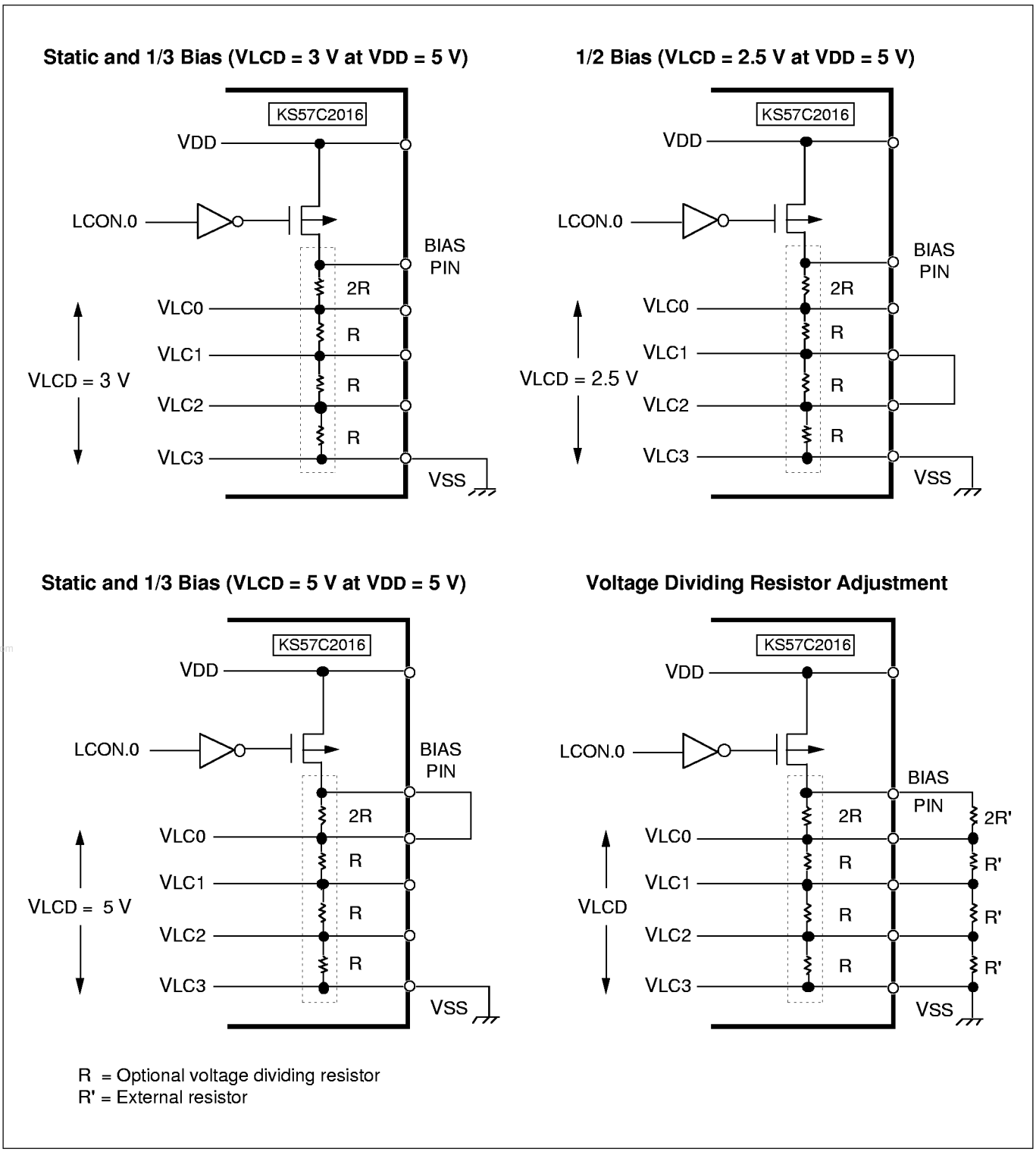


Figure 43. Voltage Dividing Resistor Circuit Diagrams

LCD DRIVE VOLTAGE

The LCD display is turned on only when the voltage difference between the common and segment signals is greater than V_{LCD}. The LCD display is turned off when the difference between the common and segment signal voltages is less than V_{LCD}.

NOTE

The LCD panel display may deteriorate if a DC voltage is applied that lies between the common and segment signal voltage. Therefore, always drive the LCD panel with AC voltage.

LCD VOLTAGE DIVIDING RESISTORS

On-chip voltage dividing resistors for the LCD circuit can be configured by mask option selection. Using these optional internal voltage dividing resistors, you can drive either a 3-volt or a 5-volt LCD display using external biasing. Bias pins are connected externally to the V_{LCD} pin so that it can handle the different LCD drive voltages. To cut off the current supply to the voltage dividing resistors, clear LCON.0 when you turn the LCD display off.

COMMON (COM) SIGNALS

The common signal output pin selection (COM pin selection) varies according to the selected duty cycle.

Table 42. Common Signal Pins Used Per Duty Cycle

Display Mode	COM0 Pin	COM1 Pin	COM2 Pin	COM3 Pin
Static	Selected	N/C	N/C	N/C
1/2 duty	Selected	Selected	N/C	N/C
1/3 duty	Selected	Selected	Selected	N/C
1/4 duty	Selected	Selected	Selected	Selected

NOTE: 'NC' means that no connection is required.

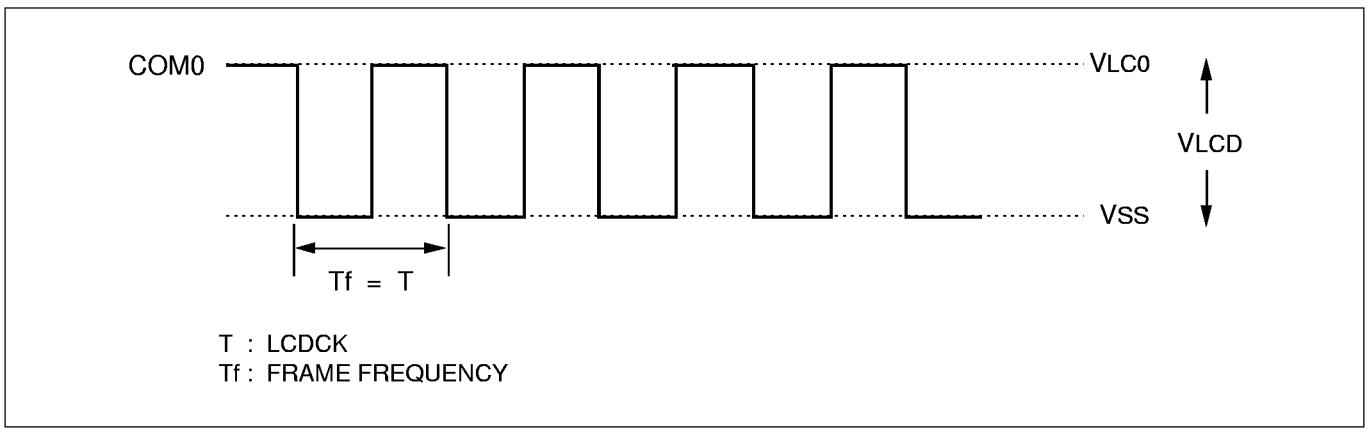


Figure 44. LCD Common Signal Waveform (Static)

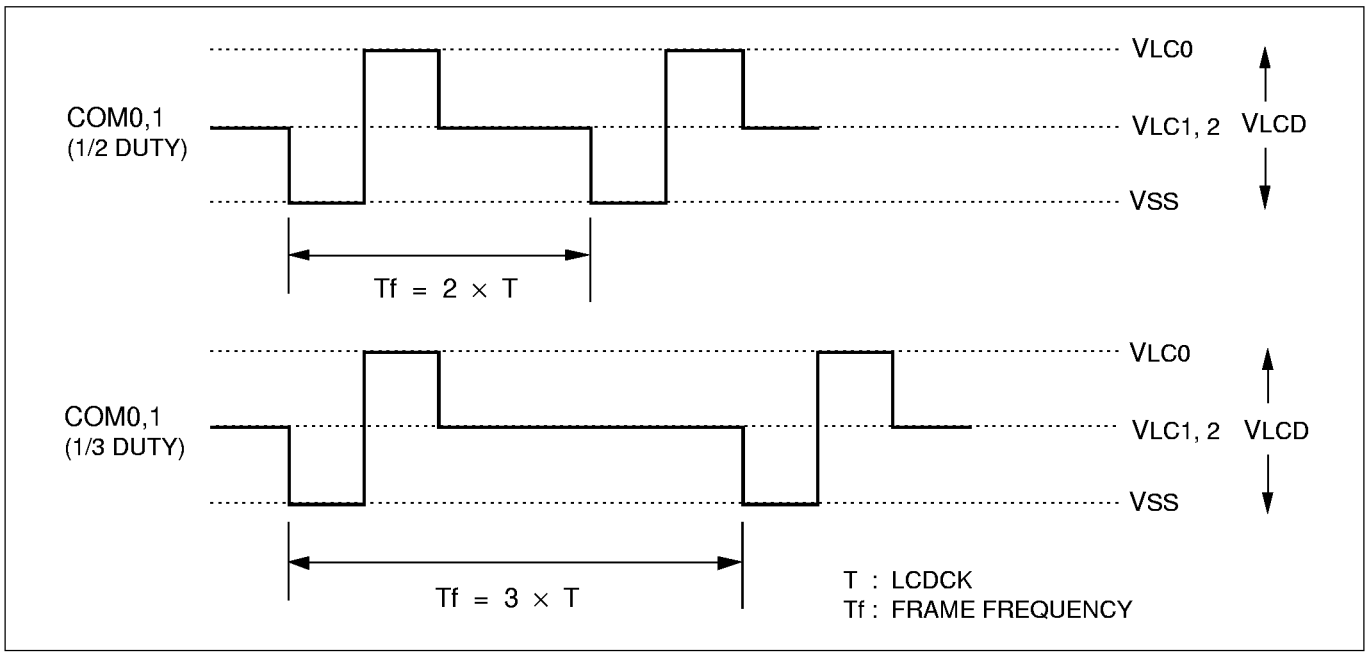


Figure 45. LCD Common Signal Waveforms at 1/2 Bias (1/2, 1/3 Duty)

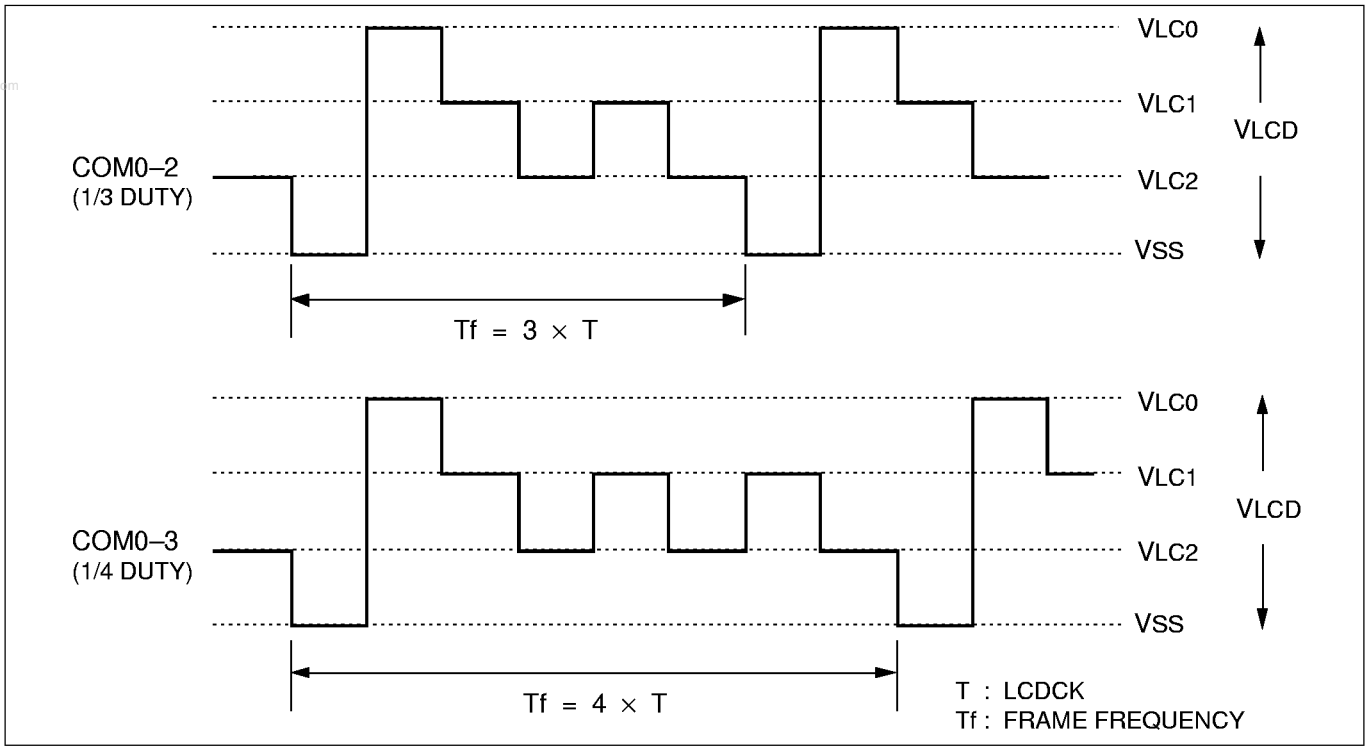


Figure 46. LCD Common Signal Waveforms at 1/3 Bias (1/3, 1/4 Duty)

SEGMENT (SEG) SIGNALS

The 40 LCD segment signal pins are connected to corresponding display RAM locations at 1D8H–1FFH. Bits 0–3 of the display RAM are synchronized with the common signal output pins COM0, COM1, COM2, and COM3.

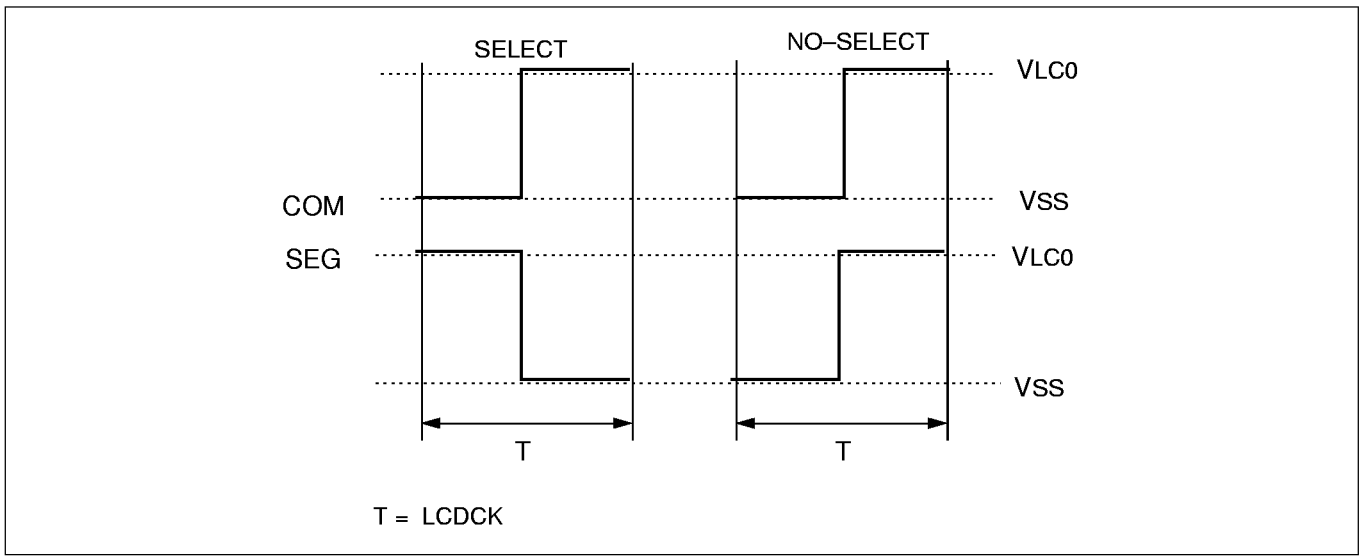


Figure 47. Select/No-Select Bias Signals in Static Display Mode

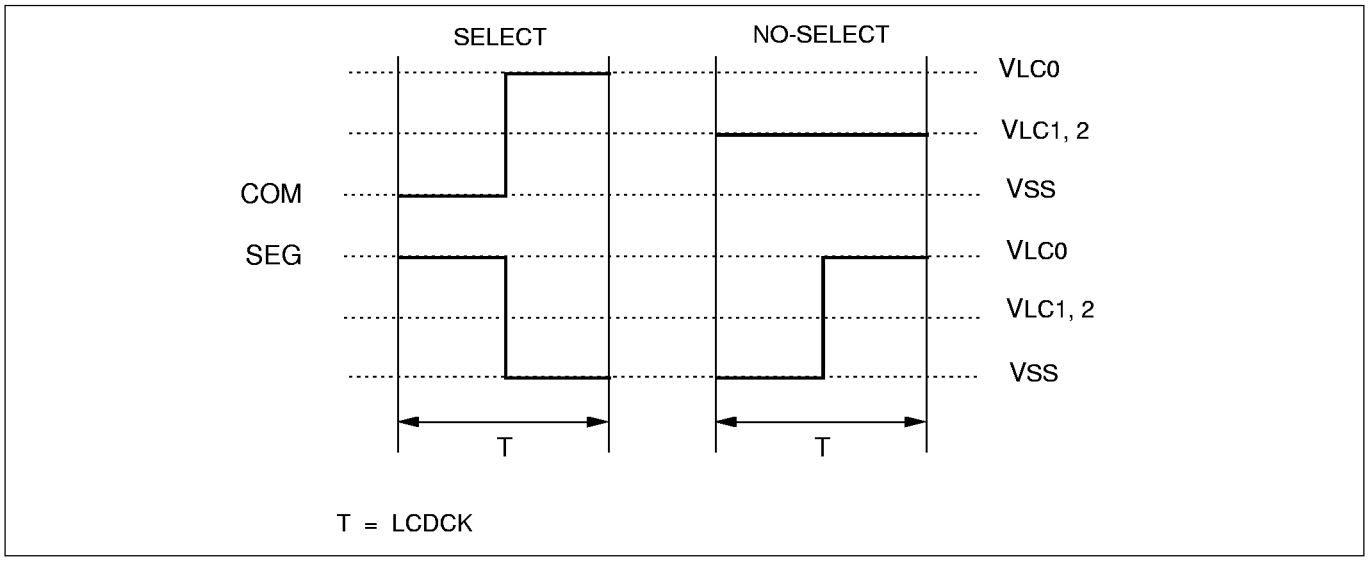


Figure 48. Select/No-Select Bias Signals in 1/2 Bias Display Mode

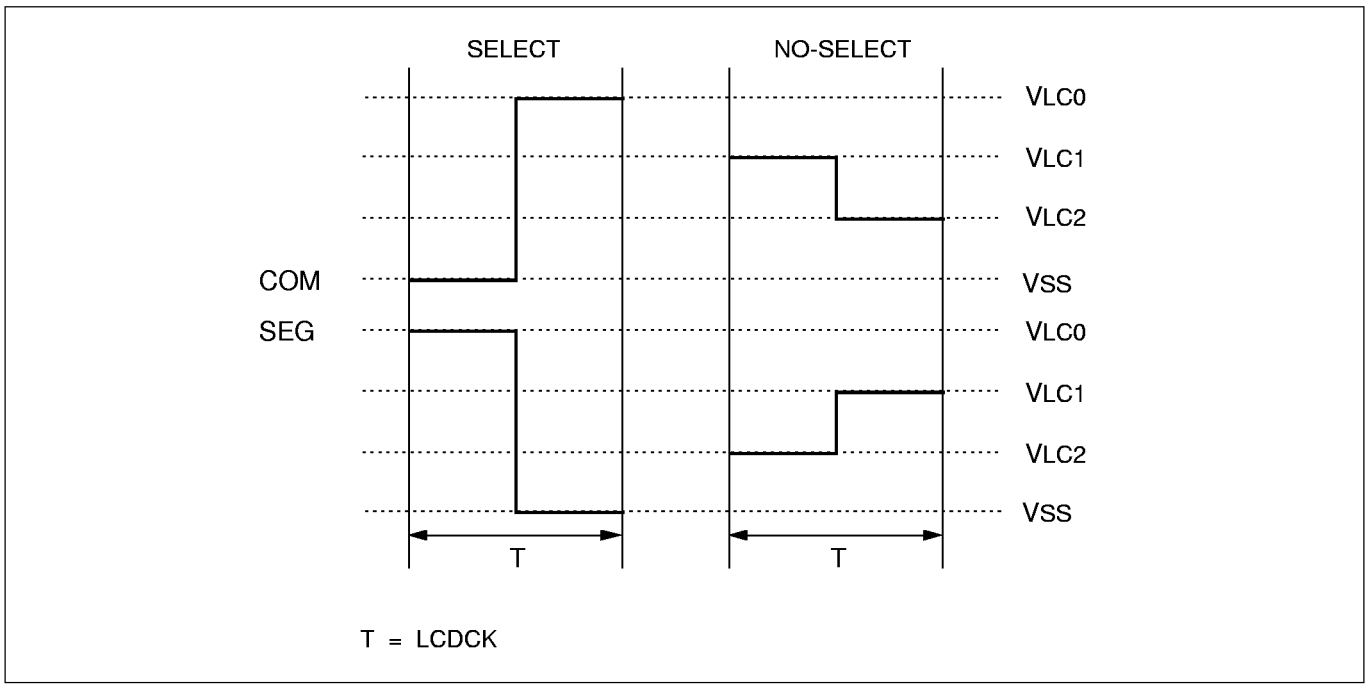


Figure 49. Select/No-Select Signals in 1/3 Bias Display Mode

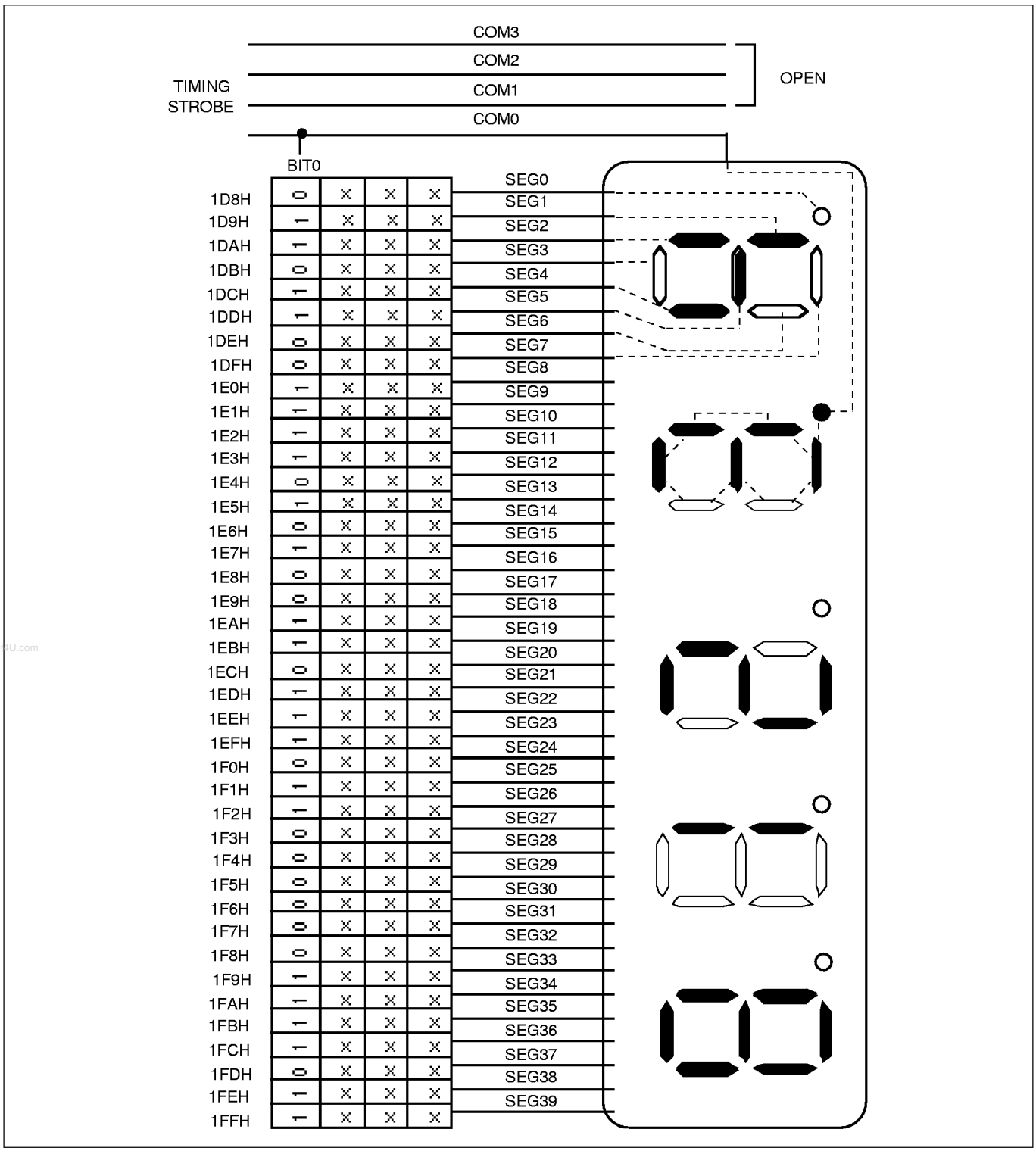


Figure 50. LCD Connection Example (Static)

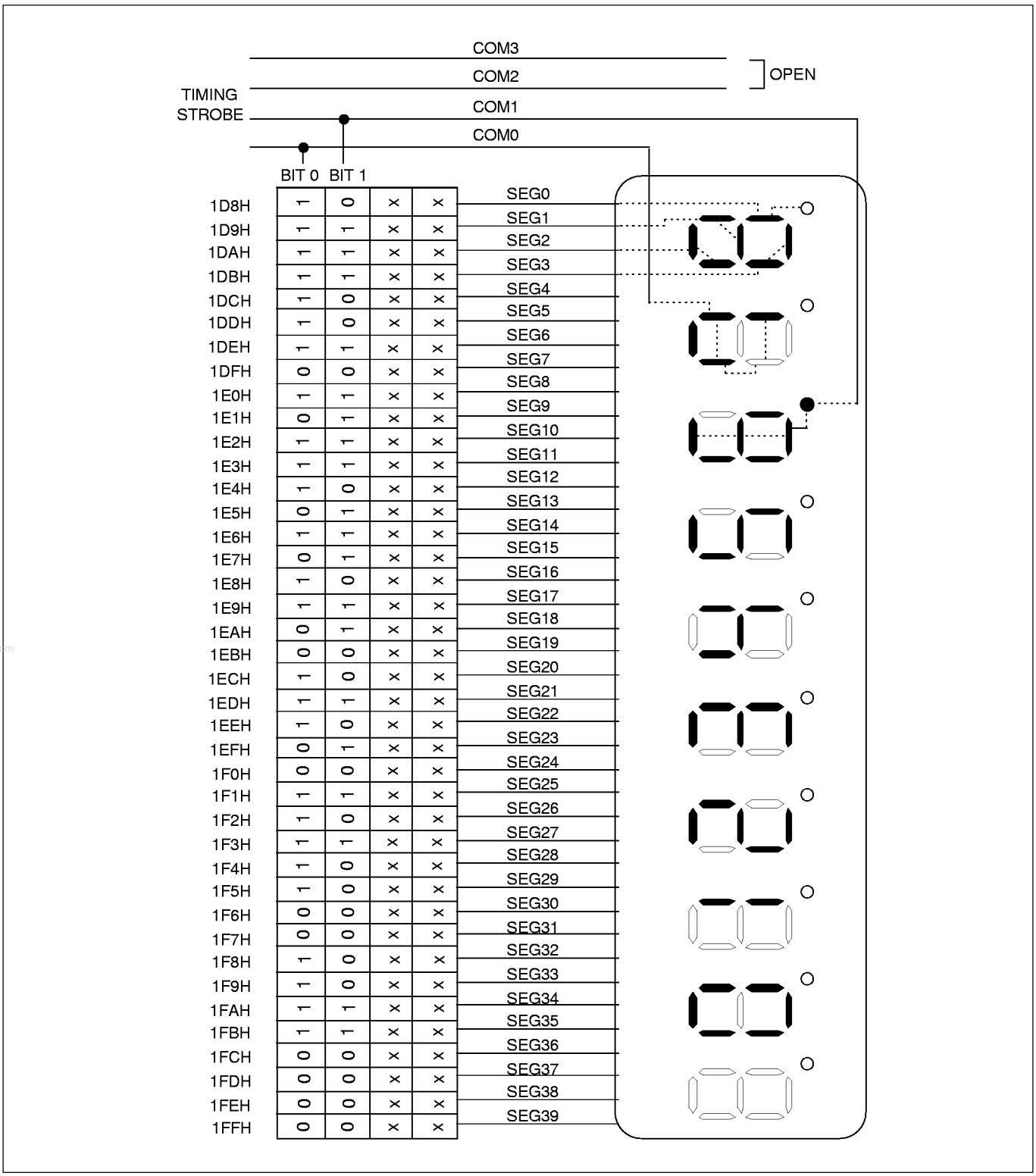


Figure 51. LCD Connection Example (1/2 Duty, 1/2 Bias)

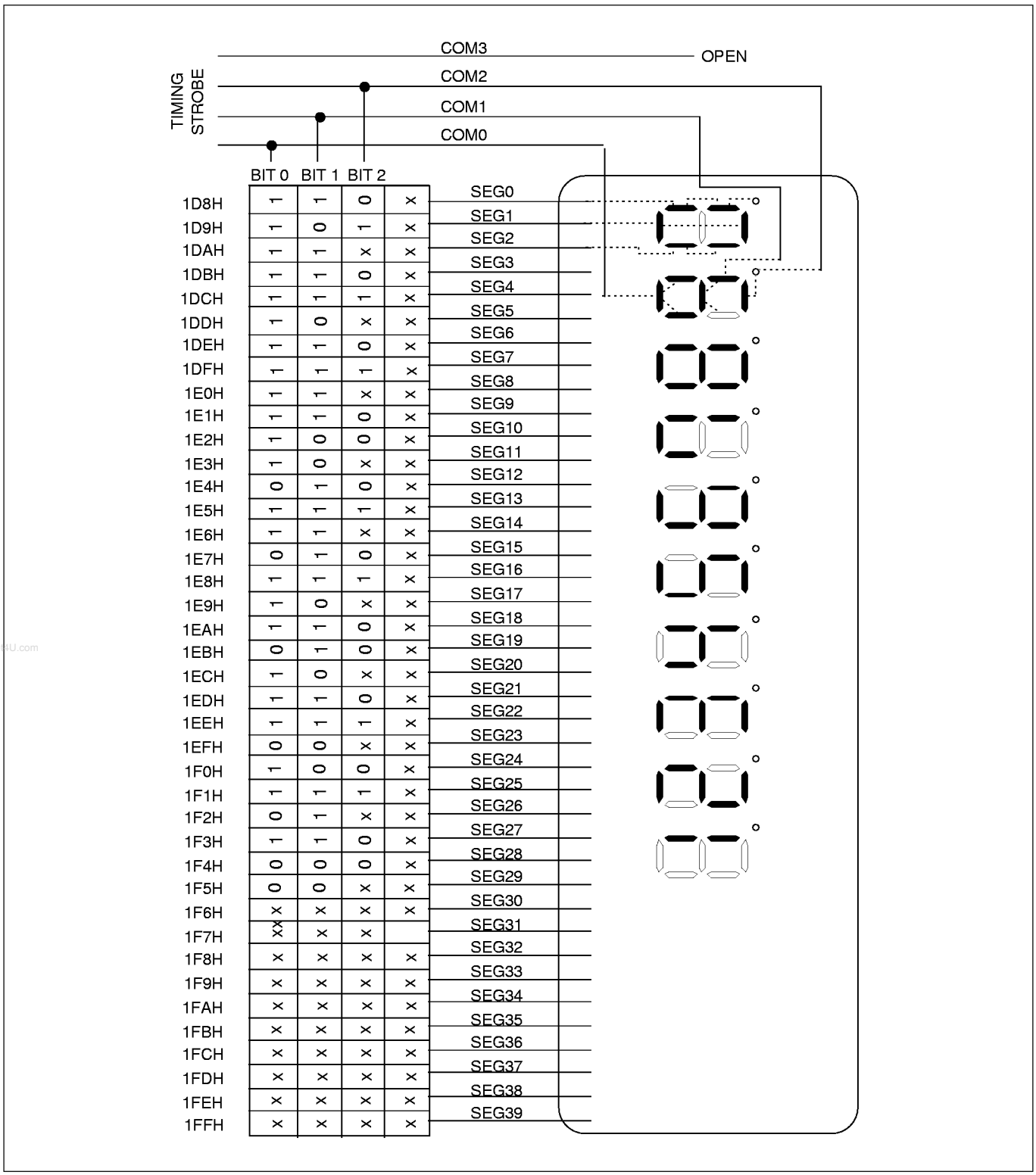


Figure 52. LCD Connection Example (1/3 Duty, 1/3 Bias)

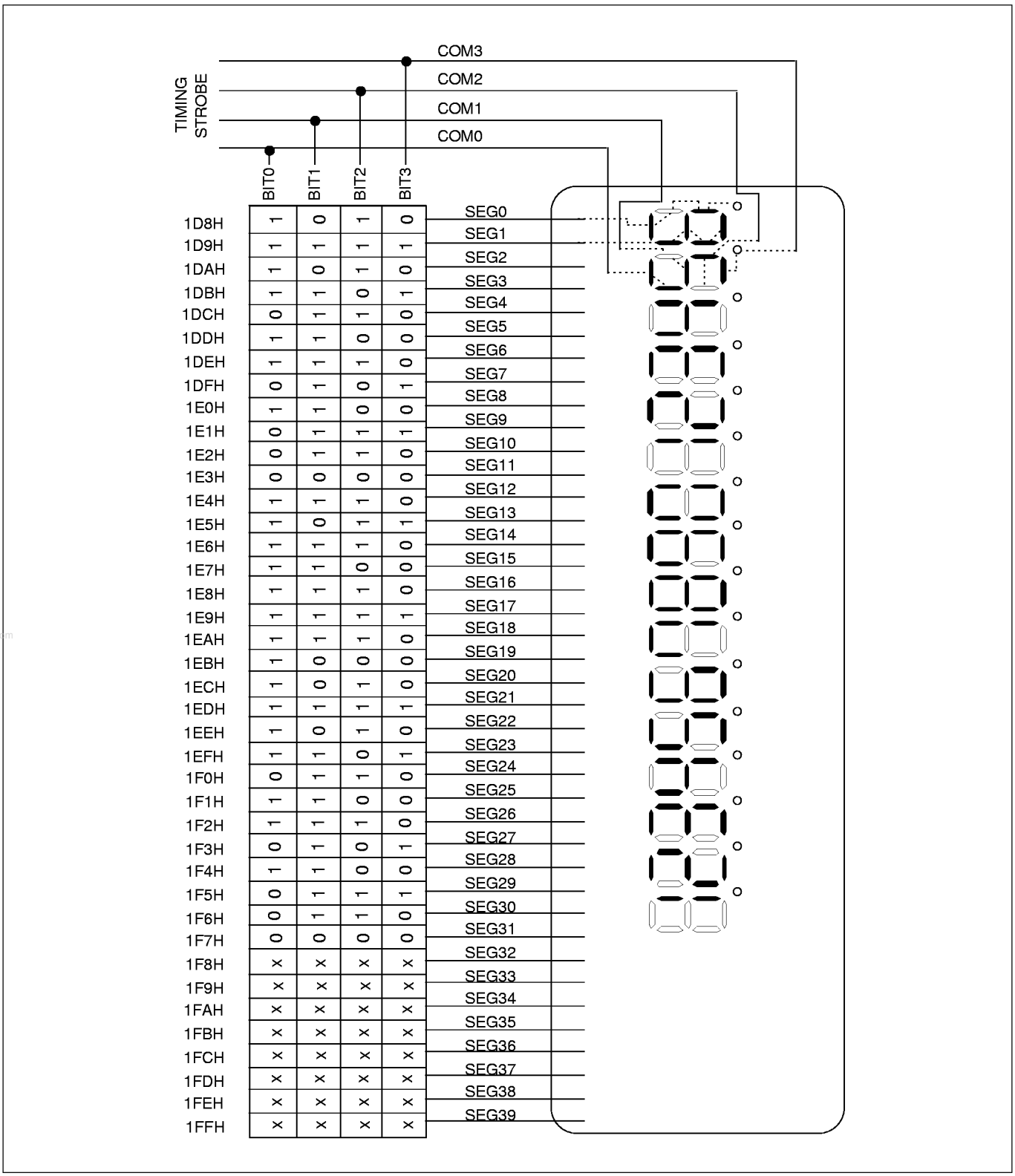


Figure 53. LCD Connection Example (1/4 Duty, 1/3 Bias)

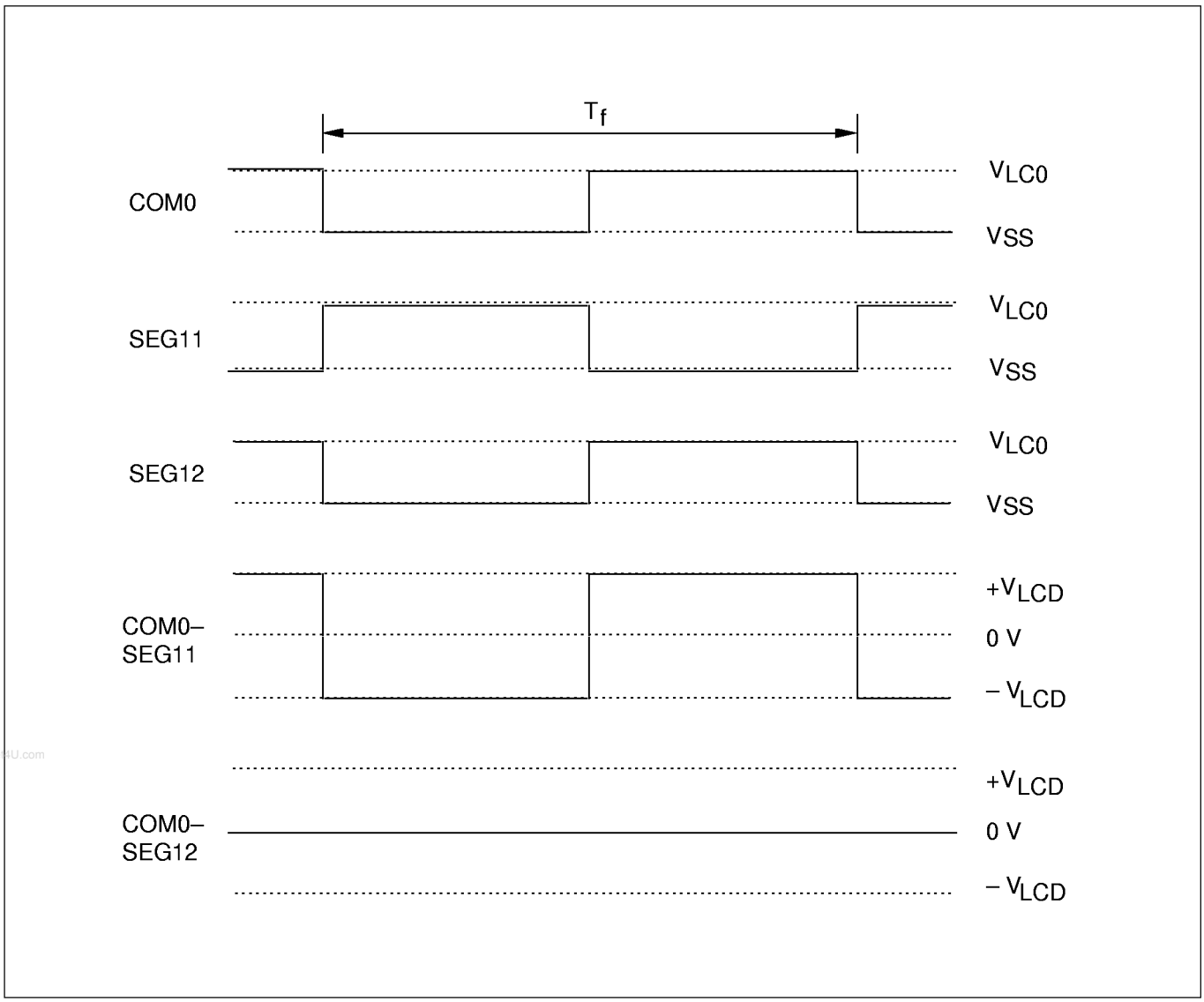


Figure 54. LCD Signal Waveforms in Static Mode

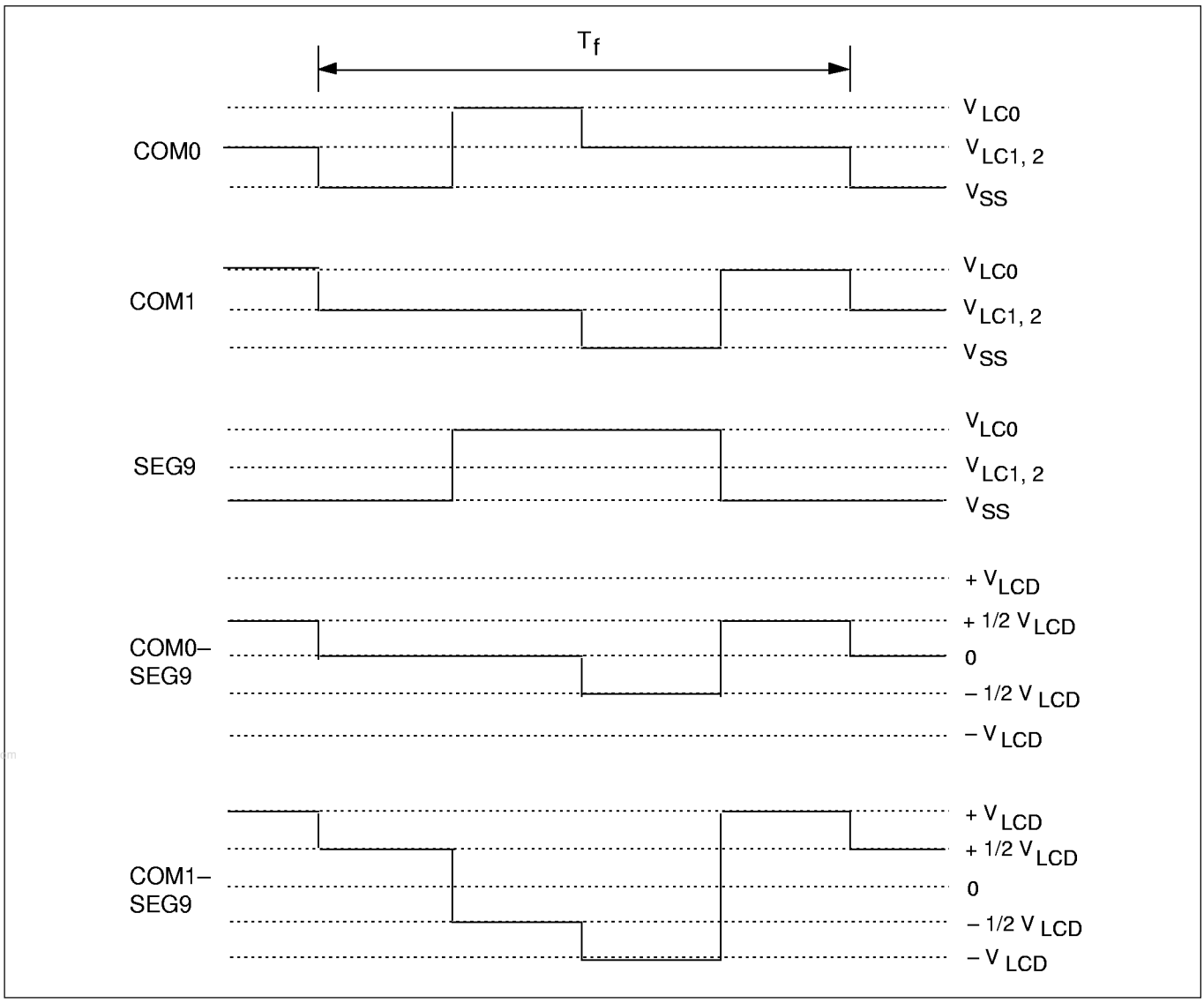


Figure 55. LCD Signal Waveforms at 1/2 Duty, 1/2 Bias

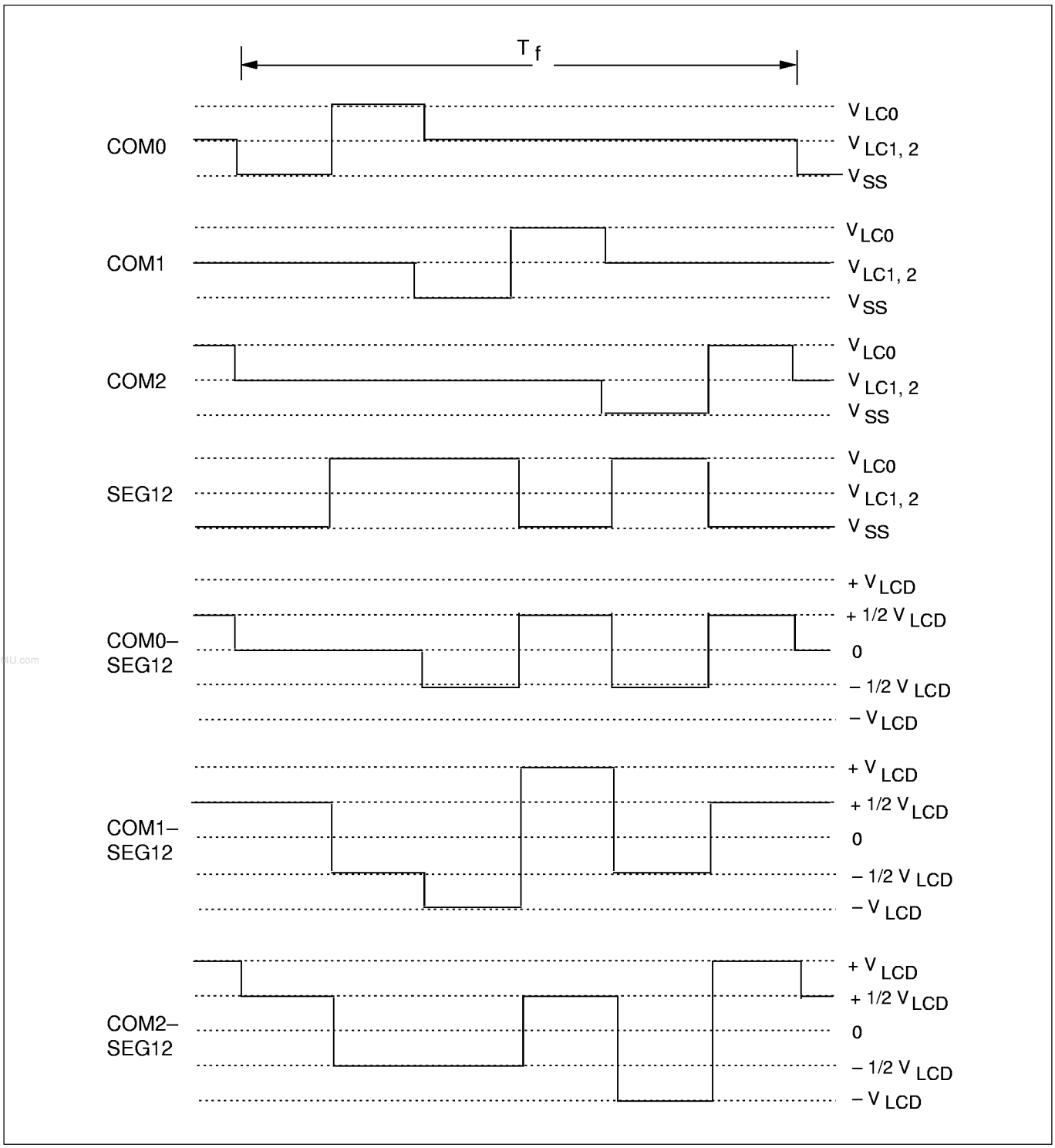


Figure 56. LCD Signal Waveforms at 1/3 Duty, 1/2 Bias

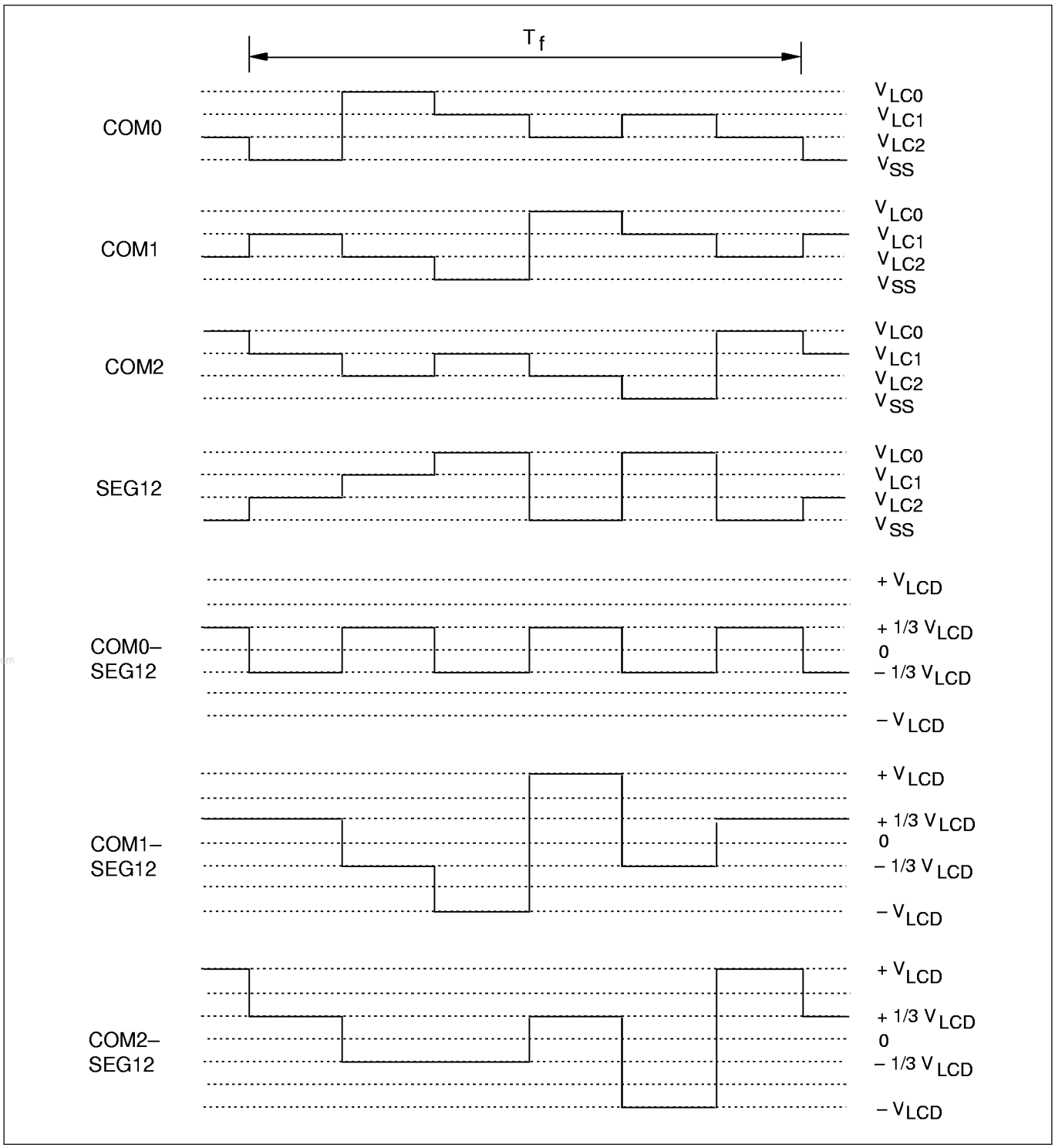


Figure 57. LCD Signal Waveforms at 1/3 Duty, 1/3 Bias

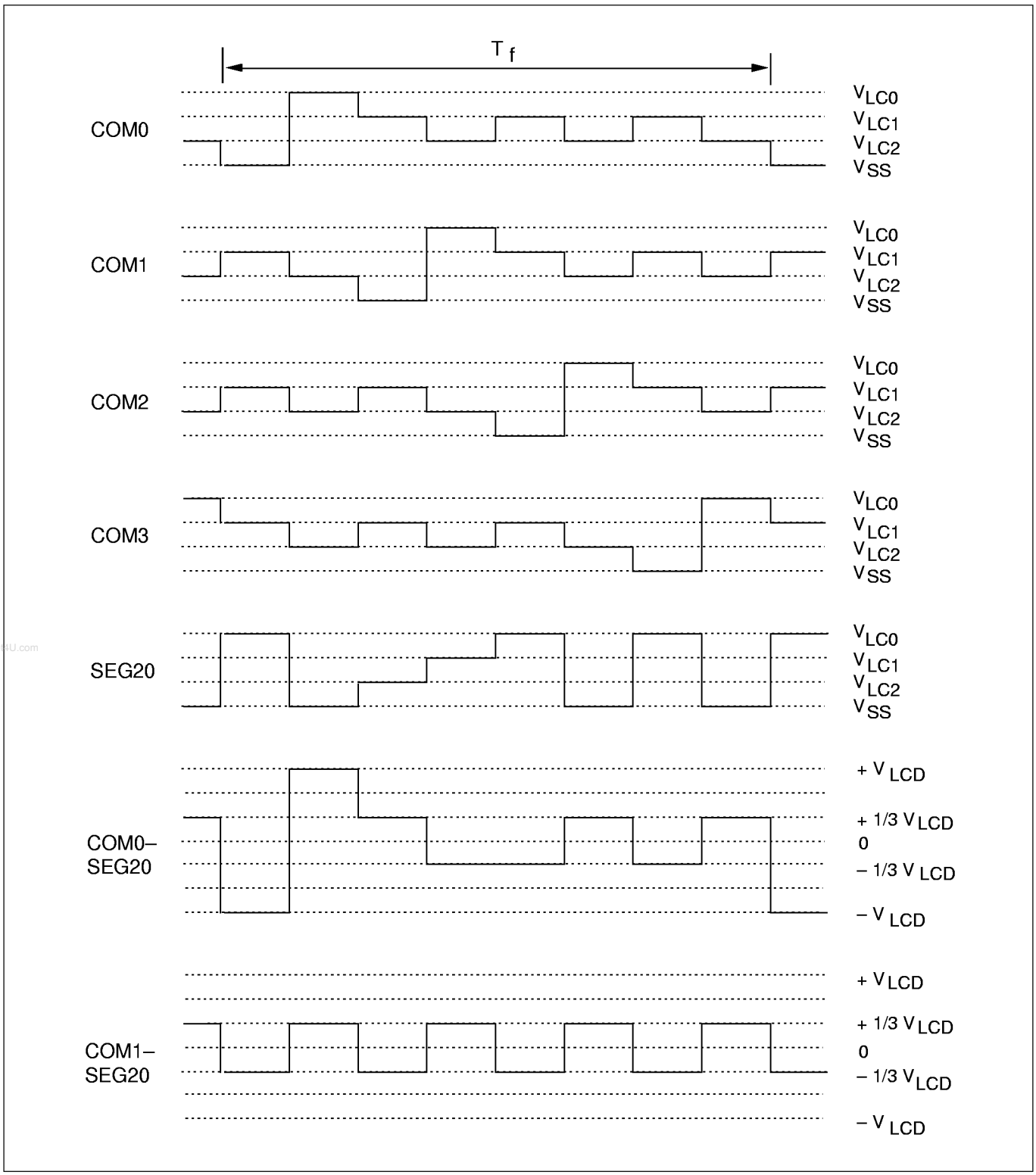


Figure 58. LCD Signal Waveforms at 1/4 Duty, 1/3 Bias

SERIAL I/O INTERFACE

Using the serial I/O interface, you can exchange 8-bit data with an external device. The serial interface can run off an internal or an external clock source, or the TOL0 signal that is generated by the 8-bit timer/counter 0, TC0. If you use the TOL0 clock signal, you can modify its frequency to adjust the serial data transmission rate.

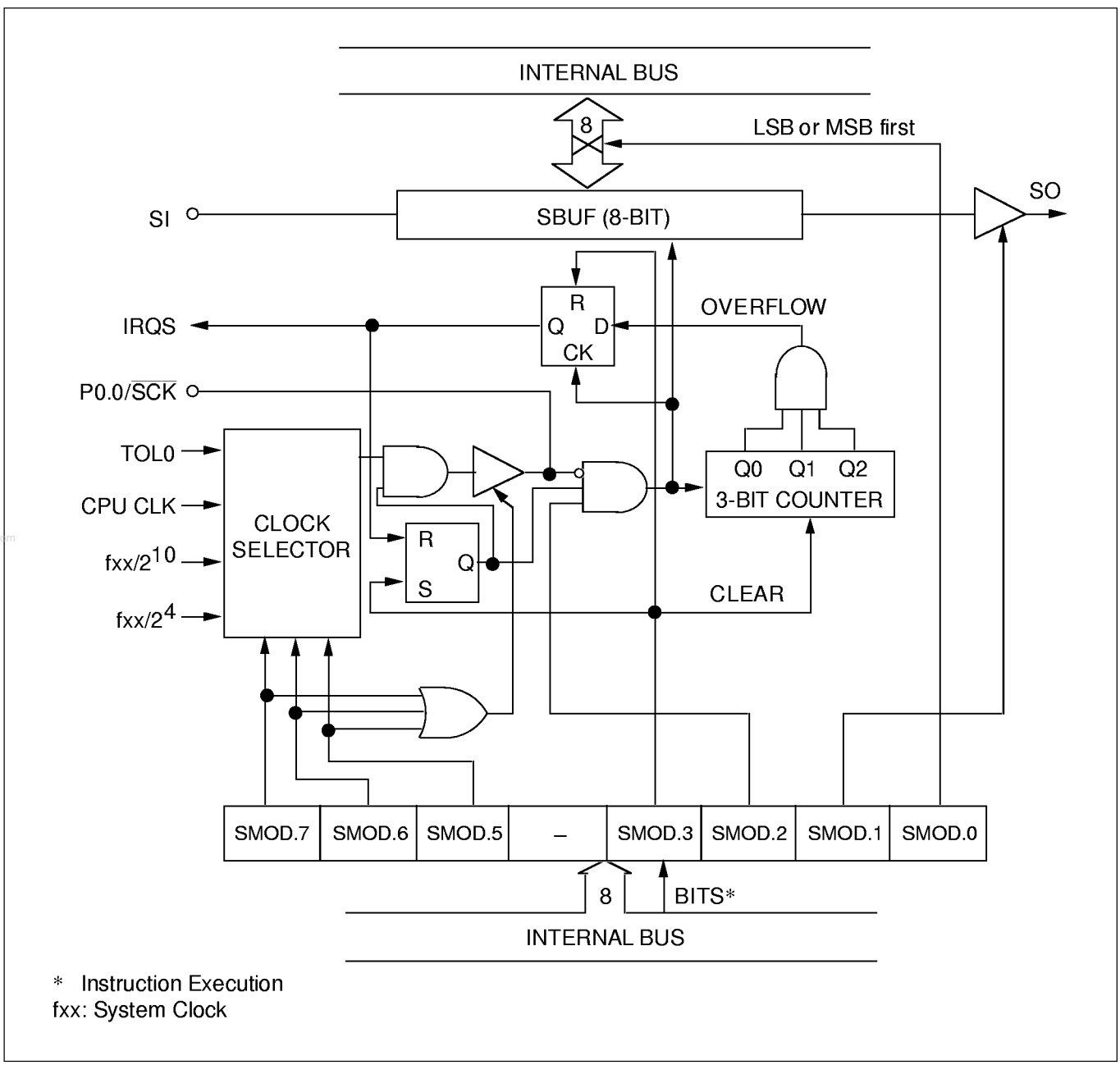


Figure 59. Serial I/O Interface Circuit Diagram

SERIAL I/O MODE REGISTER (SMOD)

The serial I/O mode register (SMOD) specifies the operation mode of the serial interface. SMOD register settings enable you to select either MSB-first or LSB-first serial transmission, and to operate in transmit-and-receive mode or receive-only mode.

When SMOD.3 is set to "1", the contents of the serial interface interrupt request flag, IRQS, and the 3-bit serial clock counter are cleared, and SIO operations are initiated. When the SIO transmission starts, SMOD.3 is cleared to "0".

SERIAL I/O BUFFER REGISTER (SBUF)

When the serial interface operates in transmit-and-receive mode (SMOD.1 = "1"), transmit data in the SIO buffer register are output to the SO pin at the rate of one bit for each falling edge of the SIO clock. Receive data is simultaneously input from the SI pin to SBUF at the rate of one bit for each rising edge of the SIO clock.

When receive-only mode is used, incoming data is input to the SIO buffer at the rate of one bit for each rising edge of the SIO clock. SBUF can be read or written using 8-bit RAM control instructions.

Table 43. SIO Mode Register (SMOD) Organization

SMOD.0	0	Most significant bit (MSB) is transmitted first
	1	Least significant bit (LSB) is transmitted first
SMOD.1	0	Receive-only mode
	1	Transmit-and-receive mode
SMOD.2	0	Disable the data shifter and clock counter; retain contents of IRQS flag when serial transmission is halted
	1	Enable the data shifter and clock counter; set IRQS flag to "1" when serial transmission is halted
SMOD.3	1	Clear IRQS flag and 3-bit clock counter to "0"; initiate transmission and then reset this bit to logic zero
SMOD.4	0	Bit not used; value is always "0"

SMOD.7	SMOD.6	SMOD.5	Clock Selection	R/W Status of SBUF
0	0	0	External clock at $\overline{SCK}$ pin	SBUF is enabled when SIO operation is halted or when $\overline{SCK}$ goes high.
0	0	1	Use TOL0 clock from TC0	
0	1	x	CPU clock: fxx/4, fxx/8, fxx/64	Enable SBUF read/write
1	0	0	4.09 kHz clock: $fxx/2^{10}$	SBUF is enabled when SIO operation is halted or when $\overline{SCK}$ goes high.
1	1	1	262 kHz clock: $fxx/2^4$	

NOTES:
1. 'fxx' = system clock; 'x' means 'don't care.'
2. kHz frequency ratings assume a system clock (fxx) running at 4.19 MHz.
3. The SIO clock selector circuit cannot select a $fxx/2^4$ clock if the CPU clock is fxx/64.

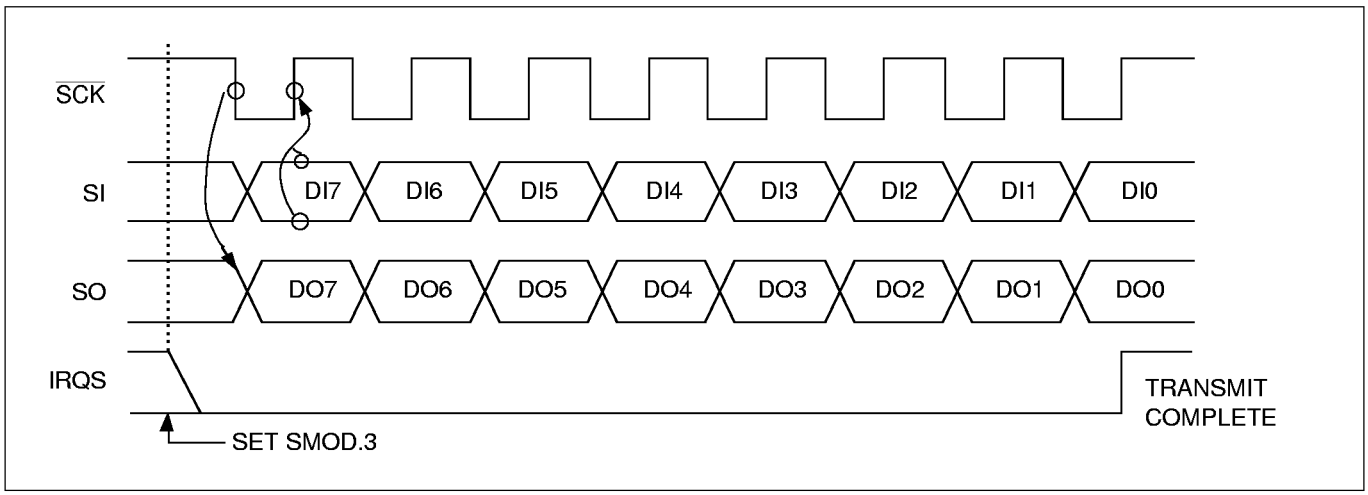


Figure 60. SIO Timing in Transmit/Receive Mode

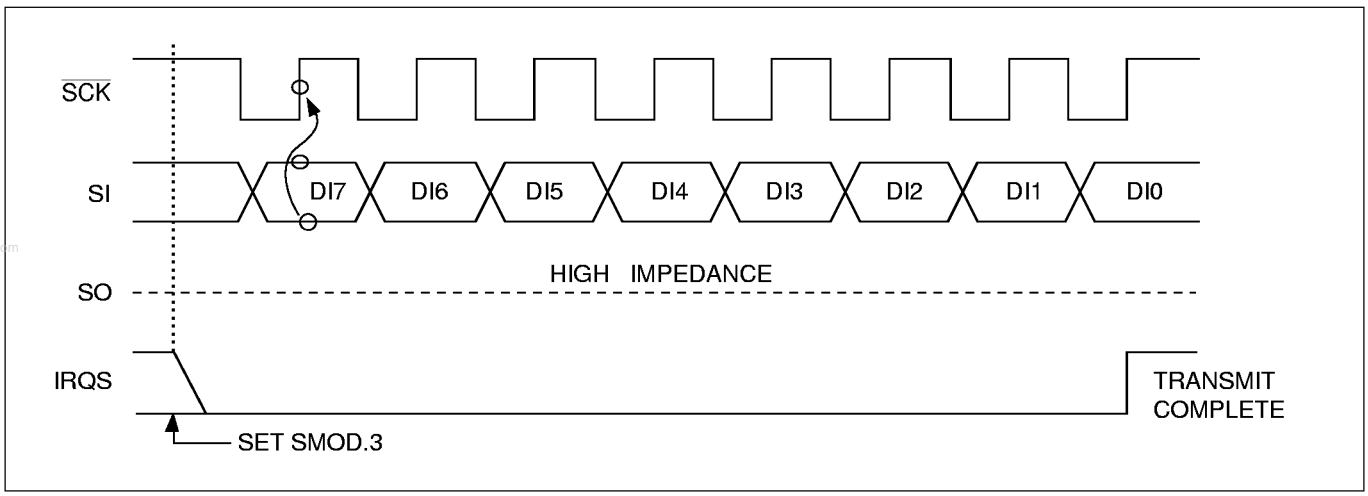
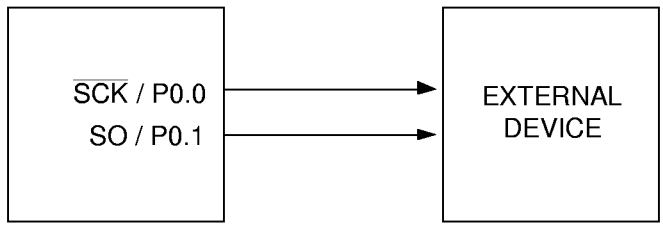


Figure 61. SIO Timing in Receive-Only Mode

☞ PROGRAMMING TIP — Setting Transmit/Receive Modes for Serial I/O

1. Transmit the data value 48H through the serial I/O interface using an internal clock frequency of fx/2^4 and in MSB-first mode:

```
BITS    EMB
SMB     15
LD      EA,#03H
LD      PMG1,EA         ;  P0.0 / SCK and P0.1 / SO ← Output
LD      EA,#48H         ;
LD      SBUF,EA         ;
LD      EA,#0EEH
LD      SMOD,EA         ;  SIO data transfer
```



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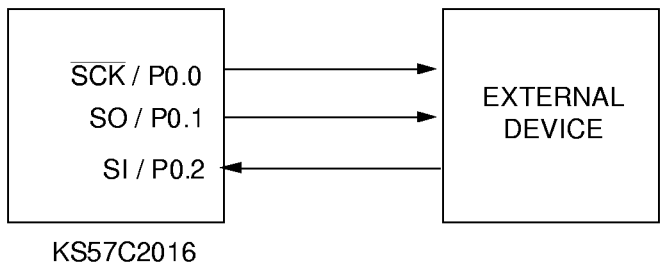
☞ **PROGRAMMING TIP — Setting Transmit/Receive Modes for Serial I/O (Continued)**

2. Use CPU clock to transfer and receive serial data at high speed:

```
        BITR    EMB
        LD      EA,#03H
        LD      PMG1,EA         ; P0.0 / SCK and P0.1 / SO ← Output, P0.2 / SI ← Input
        LD      EA,TDATA        ; TDATA address = Bank0(20H–7FH)
        LD      SBUF,EA
        LD      EA,#4FH
        LD      SMOD,EA         ; SIO start
        BITR    IES             ; SIO Interrupt Enable
STEST   BTSTZ   IRQS
        JR      STEST
        LD      EA,SBUF
        LD      RDATA,EA        ; RDATA address = Bank0 (20H–7FH)
```

3. Transmit and receive an internal clock frequency of 4.09 kHz (at 4.19 MHz) in LSB-first mode:

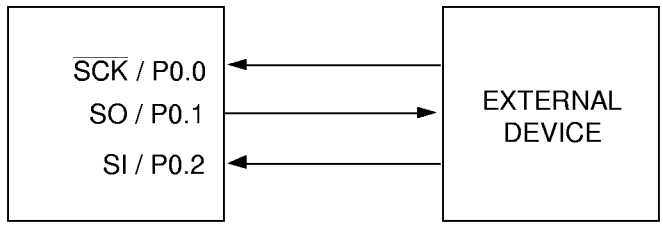
```
        BITR    EMB
        LD      EA,#03H
        LD      PMG1,EA         ; P0.0 / SCK and P0.1 / SO ← Output, P0.2 / SI ← Input
        LD      EA,TDATA        ; TDATA address = Bank0 (20H–7FH)
        LD      SBUF,EA
        LD      EA,#8FH
        LD      SMOD,EA         ; SIO start
        EI
        BITS    IES             ; SIO Interrupt Enable
        •
        •
        •
INTS    PUSH    SB              ; Store SMB, SRB
        PUSH    EA              ; Store EA
        BITR    EMB
        LD      EA,TDATA        ; EA ← Transmit data
                                ; TDATA address = Bank0 (20H–7FH)
        XCH     EA,SBUF         ; Transmit data ↔ Receive data
        LD      RDATA,EA        ; RDATA address = Bank0 (20H–7FH)
        BITS    SMOD.3          ; SIO start
        POP     EA
        POP     SB
        IRET
```



☞ PROGRAMMING TIP — Setting Transmit/Receive Modes for Serial I/O (Concluded)

4. Transmit and receive an external clock in LSB-first mode:

```
        BITR    EMB
        LD      EA,#02H
        LD      PMG1,EA         ; P0.1/ SO ← Output, P0.0/ SCK and P0.2/ SI← Input
        LD      EA,TDATA        ; TDATA address = Bank0 (20H–7FH)
        LD      SBUF,EA
        LD      EA,#0FH
        LD      SMOD,EA         ; SIO start
        EI
        BITS    IES             ; SIO Interrupt Enable
        •
        •
        •
INTS    PUSH    SB              ; Store SMB, SRB
        PUSH    EA              ; Store EA
        BITR    EMB
        LD      EA,TDATA        ; EA ← Transmit data
                                ; TDATA address = Bank0 (20H–7FH)
        XCH     EA,SBUF         ; Transmit data ↔ Receive data
        LD      RDATA,EA        ; RDATA address = Bank0 (20H–7FH)
        BITS    SMOD.3          ; SIO start
        POP     EA
        POP     SB
        IRET
```

ELECTRICAL DATA

Table 44. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	—	– 0.3 to + 7.0	V
Input Voltage	V_{I1}	Applies to I/O ports 4 and 5 only. (Pull-up resistors are individually assignable to pins at ports 4 and 5, or they can remain open-drain)	– 0.3 to V_{DD} + 0.3 (With pull-up resistor) – 0.3 to + 9.0 (Open-drain)	V
	V_{I2}	All I/O ports except 4 and 5	– 0.3 to V_{DD} + 0.3	
Output Voltage	V_O	—	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active	– 15	mA
		All I/O ports active	– 30	
Output Current Low	I_{OL}	One I/O port active	+ 30 (Peak value)	mA
			+ 15 *	
		Total for ports 0, 2, 3, 5, and 8	+ 100 (Peak value)	
			+ 60 *	
		Total for ports 4, 6, 7, 9, and 10	+ 100	
Operating Temperature	T_A	—	– 40 to + 85	°C
Storage Temperature	T_{stg}	—	– 65 to + 150	°C

* The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 45. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except those specified below for V_{IH2}–V_{IH4}	0.7V_{DD}	—	V_{DD}	V
	V_{IH2}	Ports 0, 1, 2, 6, 7, and $\overline{\text{RESET}}$	0.8V_{DD}		V_{DD}	
	V_{IH3}	Ports 4 and 5 with pull-up resistors assigned	0.7V_{DD}		V_{DD}	
		Ports 4 and 5 are open-drain	0.7V_{DD}		9	
	V_{IH4}	X_{in}, X_{out}, and XT_{in}	V_{DD} – 0.5		V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except those specified below for V_{IL2}–V_{IL3}	—	—	0.3V_{DD}	V
	V_{IL2}	Ports 0, 1, 2, 6, 7, and $\overline{\text{RESET}}$			0.2V_{DD}	
	V_{IL3}	X_{in}, X_{out}, and XT_{in}			0.4	

Table 45. D.C. Electrical Characteristics (Continued)

(T_A = −40 °C to +85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Voltage	V_{OH1}	V_{DD} = 4.5 V to 6.0 V I_{OH} = −1 mA Ports 0, 2–3, 6–10, and BIAS	V_{DD} − 1.0	—	—	V
		I_{OH} = −100 μA	V_{DD} − 0.5			
	V_{OH2}	V_{DD} = 4.5 V to 6.0 V I_{OH} = −100 μA Ports 11–13 only	V_{DD} − 2.0			
		I_{OH} = −30 μA	V_{DD} − 1.0			
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 15 mA Ports 4 and 5 only	—	0.4	2	V
		I_{OL} = 1.6 mA Ports 0, 2, 3, and 6–10		—	0.4	
		I_{OL} = 400 μA Ports 0, 2, 3, and 6–10			0.2	
	V_{OL2}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 100 μA Port 11, 12, and 13 only			1	
		I_{OL} = 50 μA			1	
Input High Leakage Current	I_{LIH1}	V_I = V_{DD} All input pins except those specified below for I_{LIH2}–I_{LIH3}	—	—	3	μA
	I_{LIH2}	V_I = V_{DD} X_{in}, X_{out}, XT_{in}, and $\overline{RESET}$ only			20	
	I_{LIH3}	V_I = 9 V Ports 4 and 5 are open-drain			20	
Input Low Leakage Current	I_{LIL1}	V_I = 0 V All input pins except X_{in}, X_{out}, and XT_{in}	—	—	−3	μA
	I_{LIL2}	V_I = 0 V X_{in}, X_{out}, XT_{in}, and $\overline{RESET}$ only			−20	
Output High Leakage Current	I_{LOH1}	V_O = V_{DD} All output pins except for port 4 and port 5	—	—	3	μA
	I_{LOH2}	Ports 4 and 5 are open-drain V_O = 9 V			20	
Output Low Leakage Current	I_{LOL}	V_O = 0 V	—	—	−3	μA

Table 45. D.C. Electrical Characteristics (Concluded)

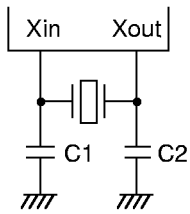
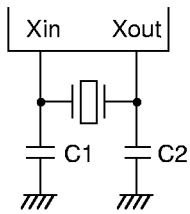
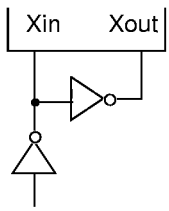
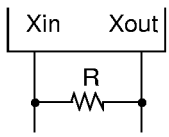
(T_A = −40 °C to +85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Pull-Up Resistor	R_{L1}	V_I = 0 V; V_{DD} = 5 V ± 10% Port 0, 1 (not P1.3), 2, 3, 6–10	15	40	80	KΩ
		V_{DD} = 3 V ± 10%	30	—	200	
	R_{L2}	V_O = V_{DD} − 2 V V_{DD} = 5 V ± 10% Ports 4 and 5 only	15	40	70	
		V_{DD} = 3 V ± 10%	10	—	60	
LCD Drive Voltage	V_{LCD}	—	2.5	—	V_{DD}	V
LCD Voltage Dividing Resistor	R_{LCD}	—	50	100	140	KΩ
COM Output Impedance	R_{COM}	V_{DD} = 5 V ± 10%	—	3	6	KΩ
		V_{DD} = 3 V ± 10%		10	15	
SEG Output Impedance	R_{SEG}	V_{DD} = 5 V ± 10%	—	3	20	KΩ
		V_{DD} = 3 V ± 10%		10	60	
Supply Current (1)	I_{DD1} (2)	V_{DD} = 5 V ± 10% (3) 4.19 MHz crystal oscillator C1 = C2 = 22 pF	—	2.5	8	mA
		V_{DD} = 3 V ± 10% (4)		0.62	1.2	
	I_{DD2} (2)	Idle mode; V_{DD} = 5 V ± 10% 4.19 MHz crystal oscillator C1 = C2 = 22 pF		1.2	1.8	
		V_{DD} = 3 V ± 10%		0.58	1.0	
	I_{DD3} (5)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator	—	30	90	μA
	I_{DD4} (5)	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		5	15	
	I_{DD5}	Stop mode; XT_{in} = 0 V V_{DD} = 5 V ± 10%		0.5	5	
		V_{DD} = 3 V ± 10%		0.1	3	

NOTES:
1. Currents in the following circuits are not included; on-chip pull-up resistors, internal LCD voltage dividing resistors, output port drive currents.
2. Data includes power consumption for subsystem clock oscillation.
3. For high-speed controller operation, the power control register (PCON) must be set to 0011B.
4. For low-speed controller operation, the power control register (PCON) must be set to 0000B.
5. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.

Table 46. Oscillator Characteristics

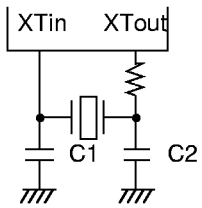
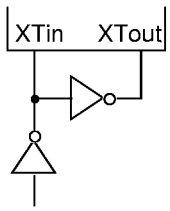
(T_A = −40 °C +85 °C, V_{DD} = 2.7 V to 6.0 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	—	0.4	—	4.5	MHz
		Stabilization time (2)	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	—	—	4	ms
Crystal Oscillator		Oscillation frequency (1)	—	0.4	4.19	4.5	MHz
		Stabilization time (2)	V_{DD} = 4.5 V to 6.0 V	—	—	10	ms
			V_{DD} = 2.7 V to 4.5 V	—	—	30	
External Clock		X_{in} input frequency (1)	—	0.4	—	4.5	MHz
		X_{in} input high and low level width (t_{XH}, t_{XL})	—	111	—	1250	ns
RC Oscillator		Frequency	V_{DD} = 5 V	0.4	—	2	MHz

NOTES:
1. Oscillation frequency and X_{in} frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs, or when Stop mode is terminated.

Table 47. Subsystem Clock Oscillator Characteristics

(T_A = −40 °C +85 °C, V_{DD} = 2.7 V to 6.0 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	—	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 4.5 V to 6.0 V	—	1.0	2	s
			V_{DD} = 2.7 V to 4.5 V	—	—	10	
External Clock		XT_{in} input frequency (1)	—	32	—	100	kHz
		XT_{in} input high and low level width (t_{XH}, t_{XL})	—	5	—	15	μs

NOTES:

1. Oscillation frequency and XT_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs.

Table 48. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	—	—	15	pF
Output Capacitance	C_{OUT}		—	—	15	pF
I/O Capacitance	C_{IO}		—	—	15	pF

Table 49. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (1)	t_{CY}	V_{DD} = 4.5 V to 6.0 V	0.95	—	64	µs
		V_{DD} = 2.7 V to 4.5 V	3.8		64	
		With subsystem clock (fxt)	114	122	125	
TCL0, TCL1 Input Frequency	f_{TI0}, f_{TI1}	V_{DD} = 4.5 V to 6.0 V	0	—	1	MHz
		V_{DD} = 2.7 V to 4.5V			275	kHz
TCL0, TCL1 Input High, Low Width	t_{TIH0}, t_{TIL0} t_{TIH1}, t_{TIL1}	V_{DD} = 4.5 V to 6.0 V	0.48	—	—	µs
		V_{DD} = 2.7 V to 4.5 V	1.8			
$\overline{SCK}$ Cycle Time	t_{KCY}	V_{DD} = 4.5 V to 6.0 V External $\overline{SCK}$ source	800	—	—	ns
		Internal $\overline{SCK}$ source	950			
		V_{DD} = 2.7 V to 4.5 V External $\overline{SCK}$ source	3200			
		Internal $\overline{SCK}$ source	3800			
$\overline{SCK}$ High, Low Width	t_{KH}, t_{KL}	V_{DD} = 4.5 V to 6.0 V External $\overline{SCK}$ source	400	—	—	ns
		Internal $\overline{SCK}$ source	$t_{KCY}/2 - 50$			
		V_{DD} = 2.7 V to 4.5 V External $\overline{SCK}$ source	1600			
		Internal $\overline{SCK}$ source	$t_{KCY}/2 - 150$			
SI Setup Time to $\overline{SCK}$ High	t_{SIK}	External $\overline{SCK}$ source	100	—	—	ns
		Internal $\overline{SCK}$ source	150			
SI Hold Time to $\overline{SCK}$ High	t_{KSI}	External $\overline{SCK}$ source	400	—	—	ns
		Internal $\overline{SCK}$ source	400			
Output Delay for $\overline{SCK}$ to SO	t_{KSO}	V_{DD} = 4.5 V to 6.0 V External $\overline{SCK}$ source	—	—	300	ns
		Internal $\overline{SCK}$ source			250	
		V_{DD} = 2.7 V to 4.5 V External $\overline{SCK}$ source			1000	
		Internal $\overline{SCK}$ source			1000	

Table 49. A.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0	(2)	—	—	µs
		INT1, INT2, INT4, KS0–KS7	10			
$\overline{RESET}$ Input Low Width	t_{RSL}	Input	10	—	—	µs

NOTES:
1. Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock (fx) source.
2. Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128/fx as assigned by the IMOD0 register setting.

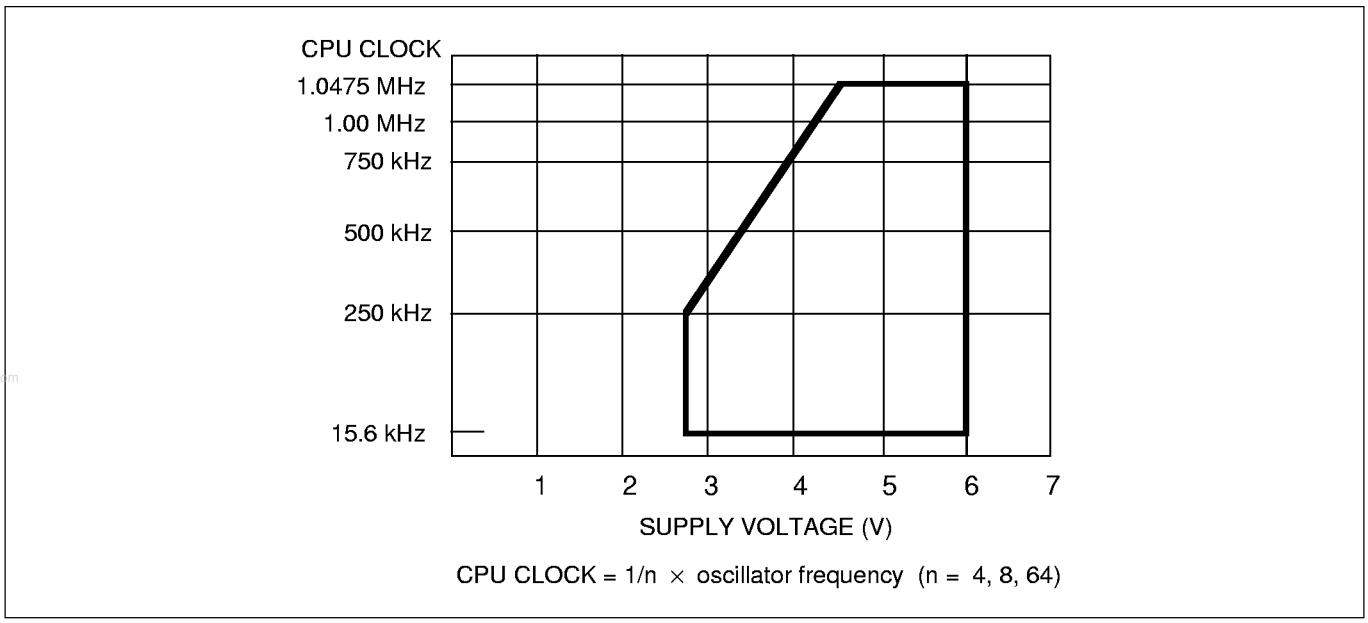


Figure 62. Standard Operating Voltage Range

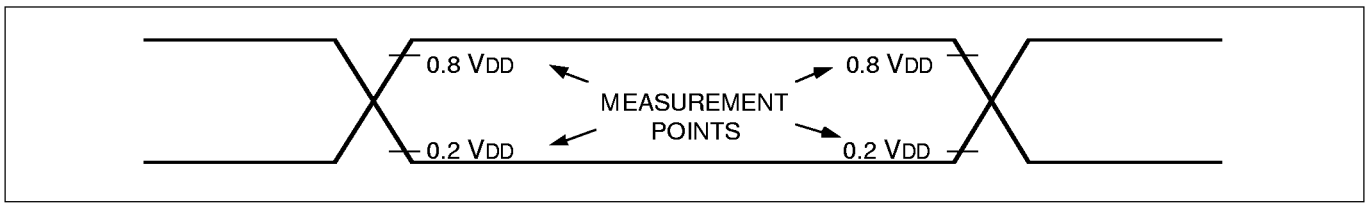


Figure 63. A.C. Timing Measurement Points (Except for $\overline{RESET}$, P6, P7, and X_{in})

Table 50. RAM Data Retention Supply Voltage in Stop Mode

(T_A = −40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	—	2.0	—	6.0	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V	—	0.1	10	µA
Release signal set time	t_{SREL}	—	0	—	—	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	—	2^{17} / fx	—	ms
		Released by interrupt	—	(2)	—	

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

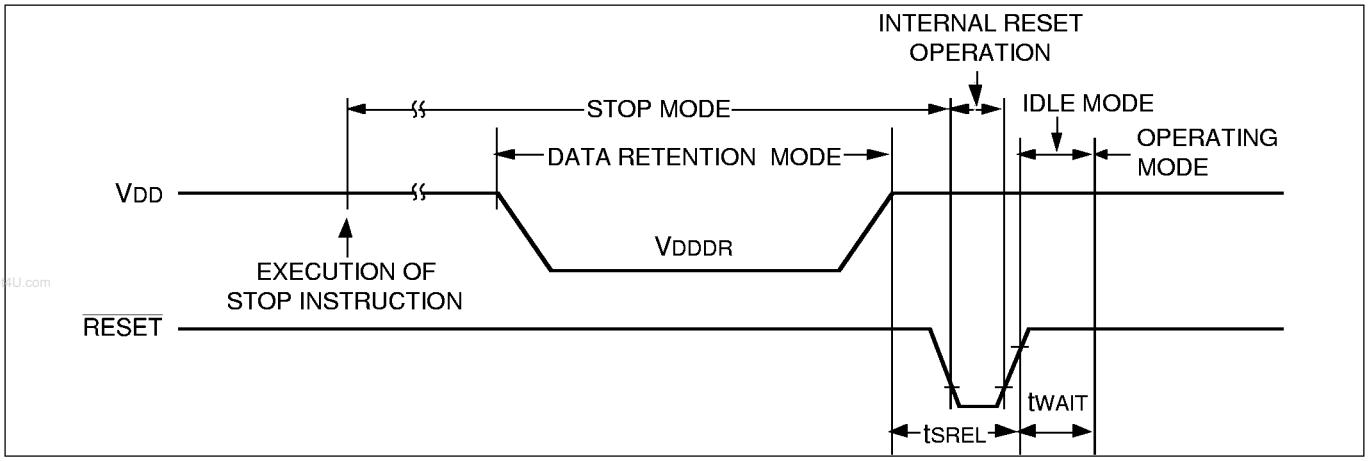


Figure 64. Stop Mode Release Timing When Initiated By RESET

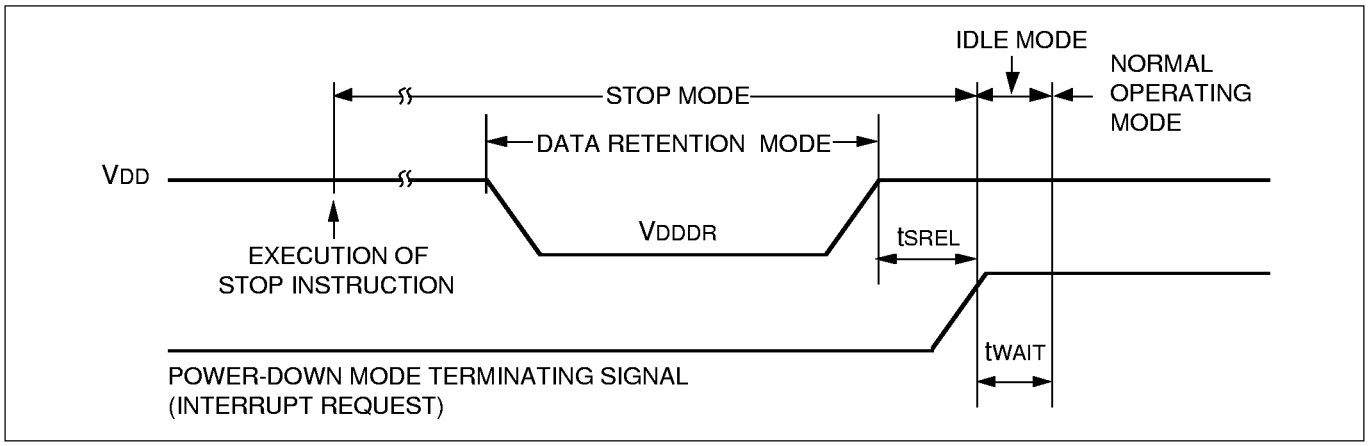


Figure 65. Stop Mode Release Timing When Initiated By Interrupt Request

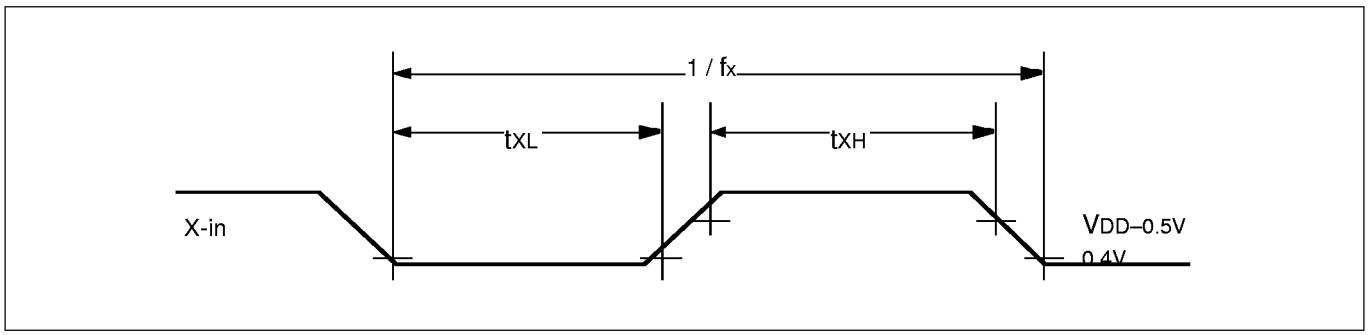


Figure 66. Clock Timing Measurement at X_{in}

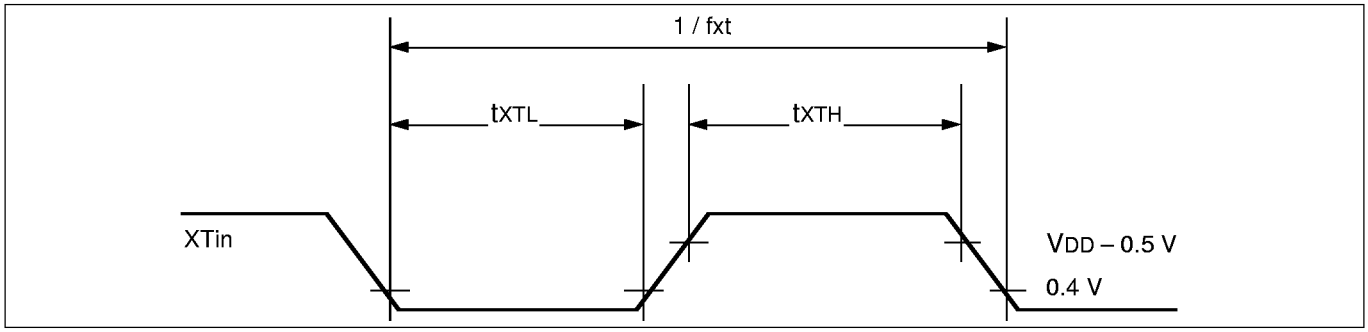


Figure 67. Clock Timing Measurement at XT_{in}

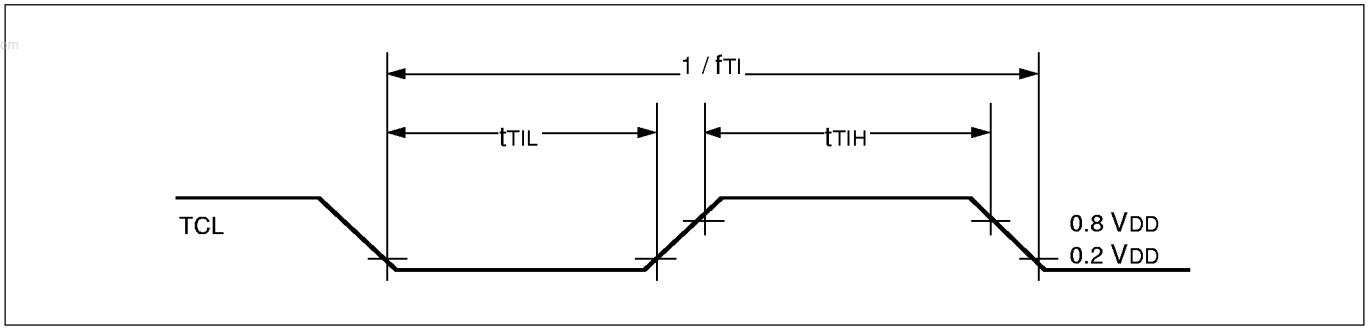


Figure 68. TCL Timing

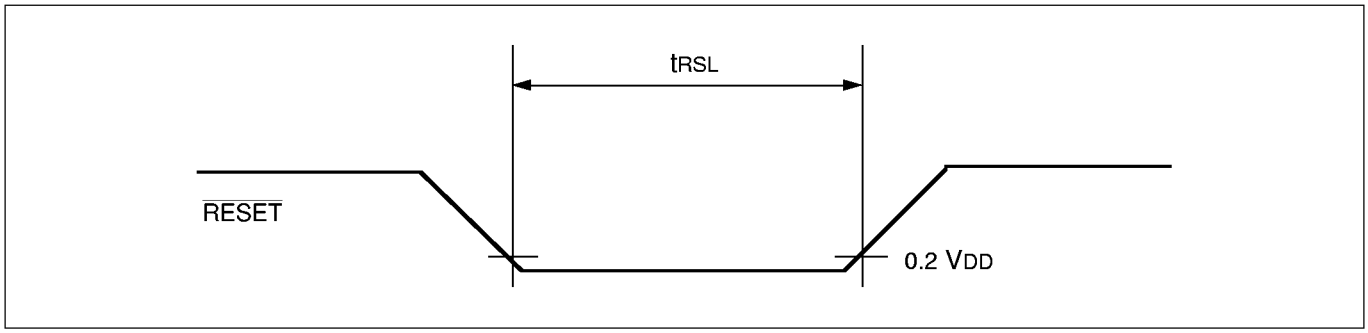


Figure 69. Input Timing for $\overline{\text{RESET}}$ Signal

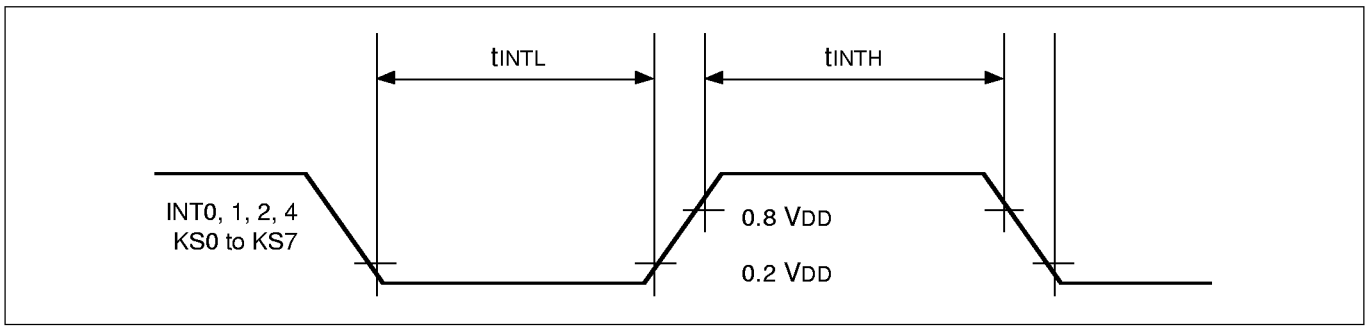


Figure 70. Input Timing for External Interrupts and Quasi-Interrupts

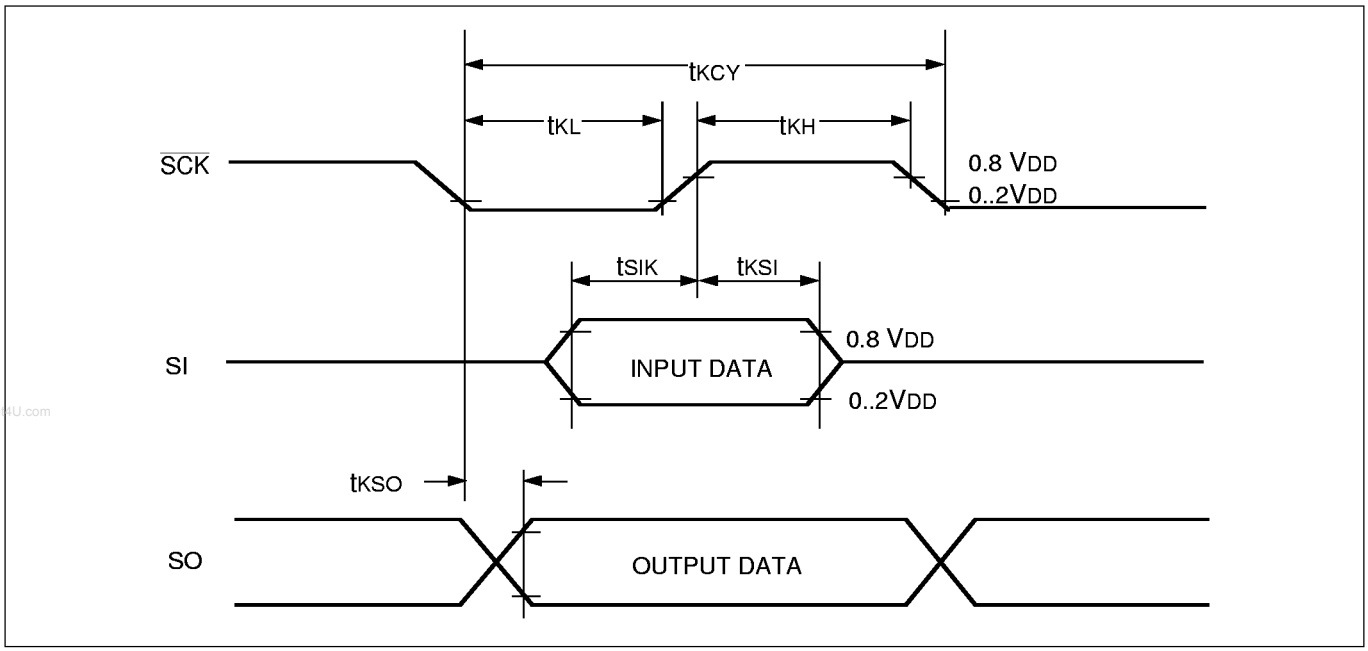


Figure 71. Serial Data Transfer Timing

CHARACTERISTIC CURVES

NOTE

The characteristic values shown in the following graphs are based on actual test measurements. They do not, however, represent guaranteed operating values.

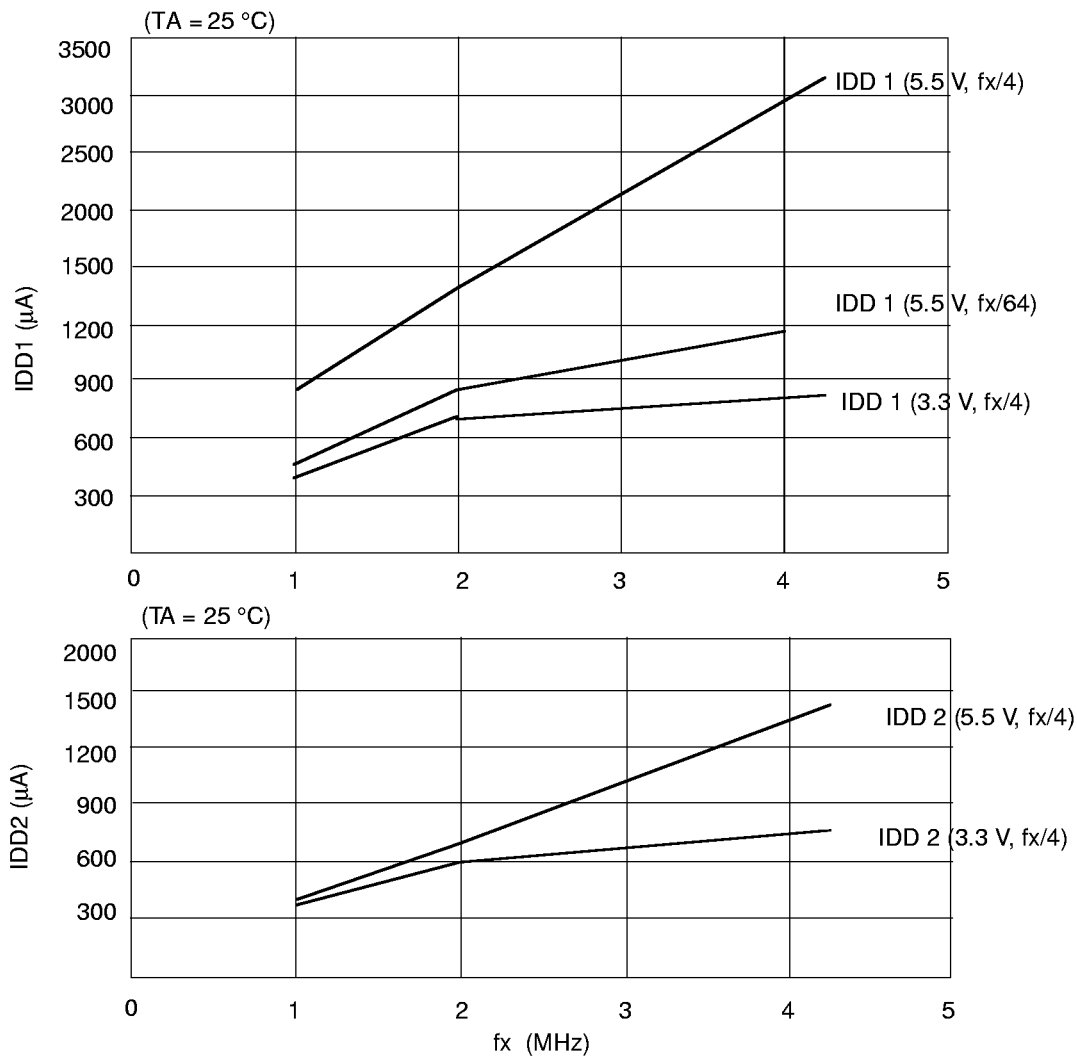


Figure 72. I_{DD} VS. Frequency

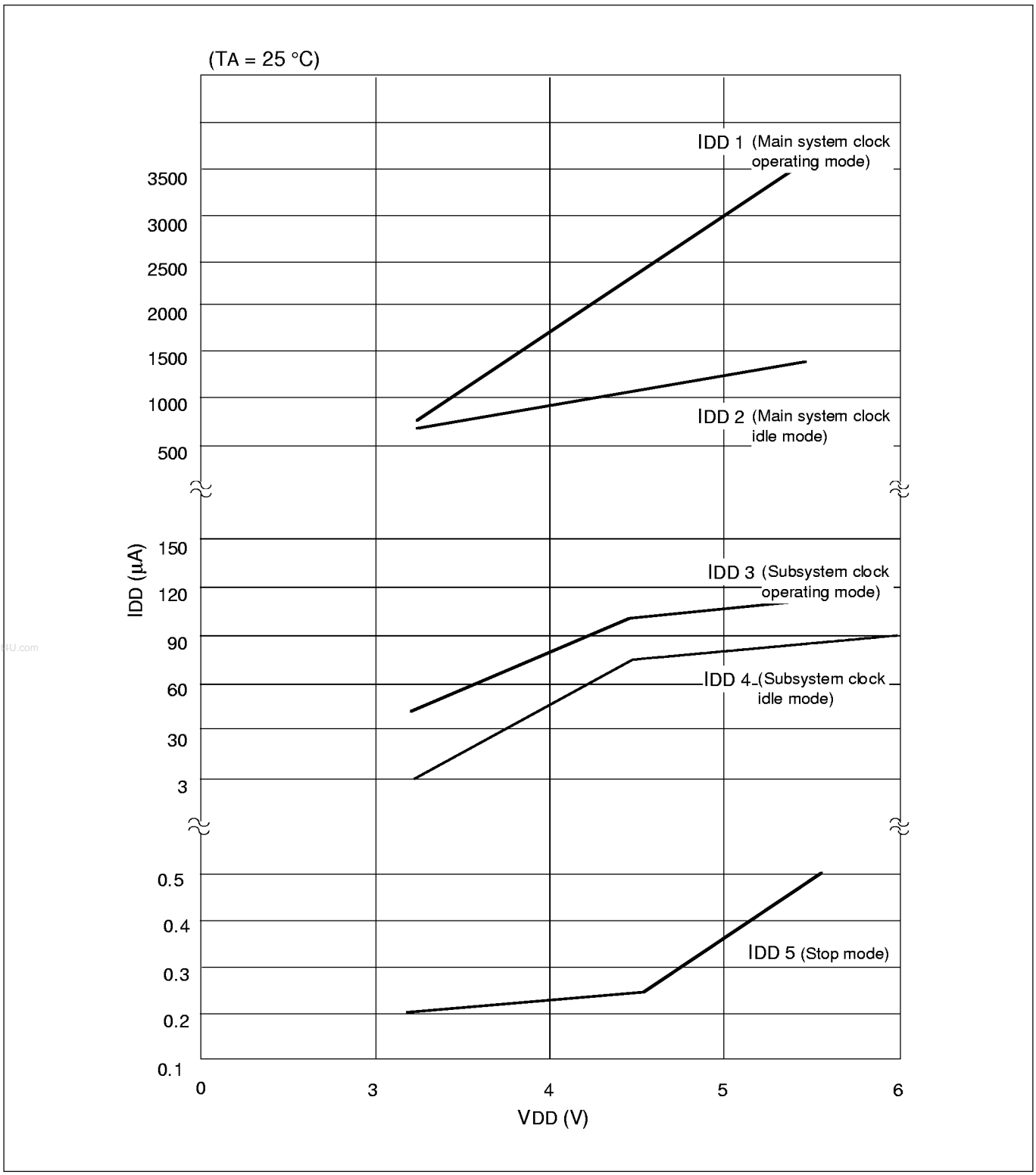
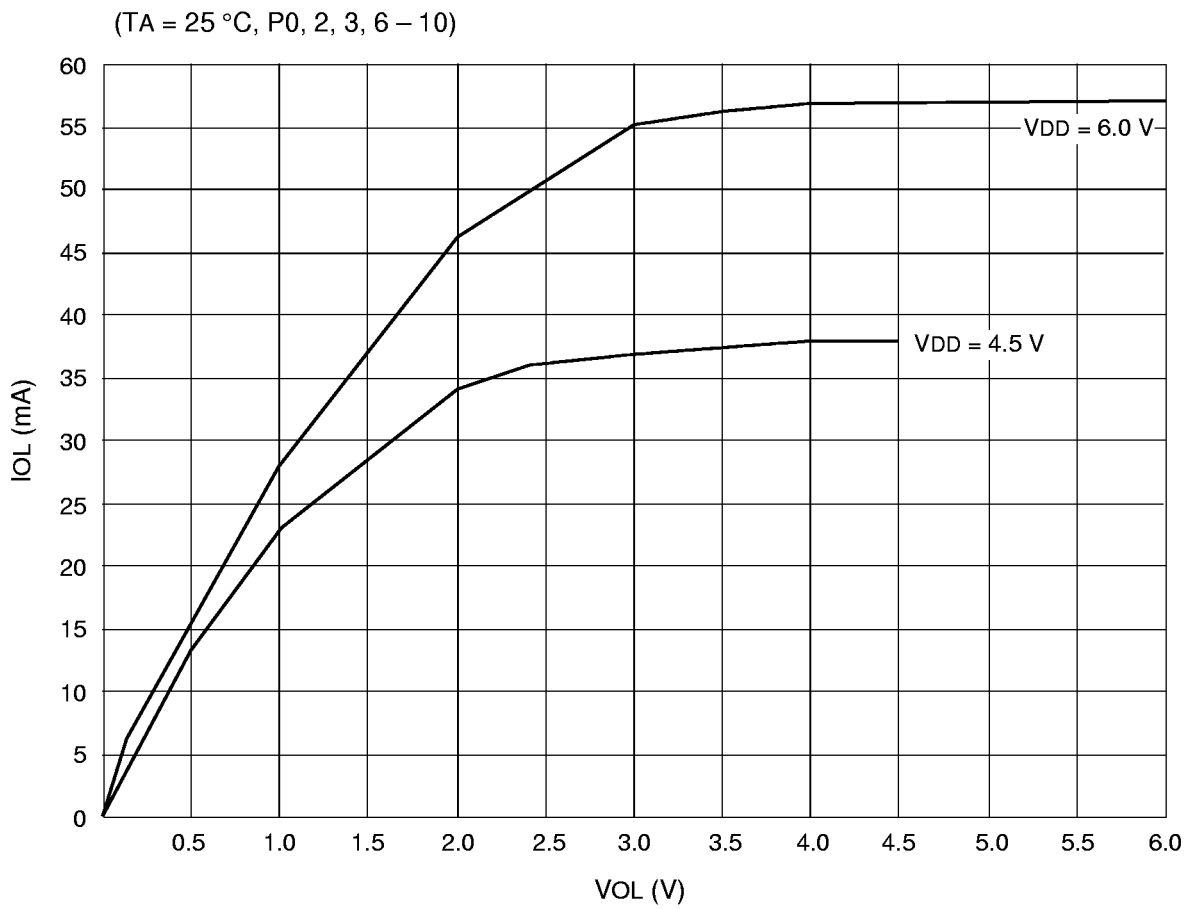
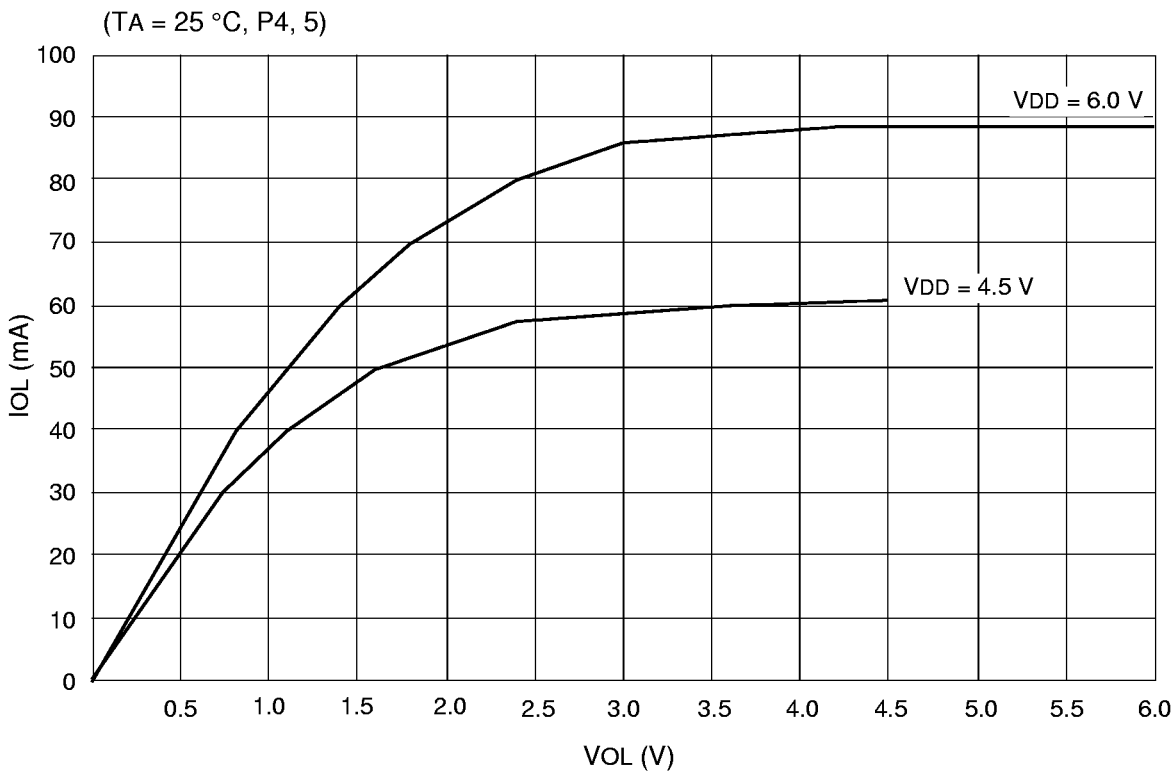


Figure 73. I_{DD} VS. V_{DD}



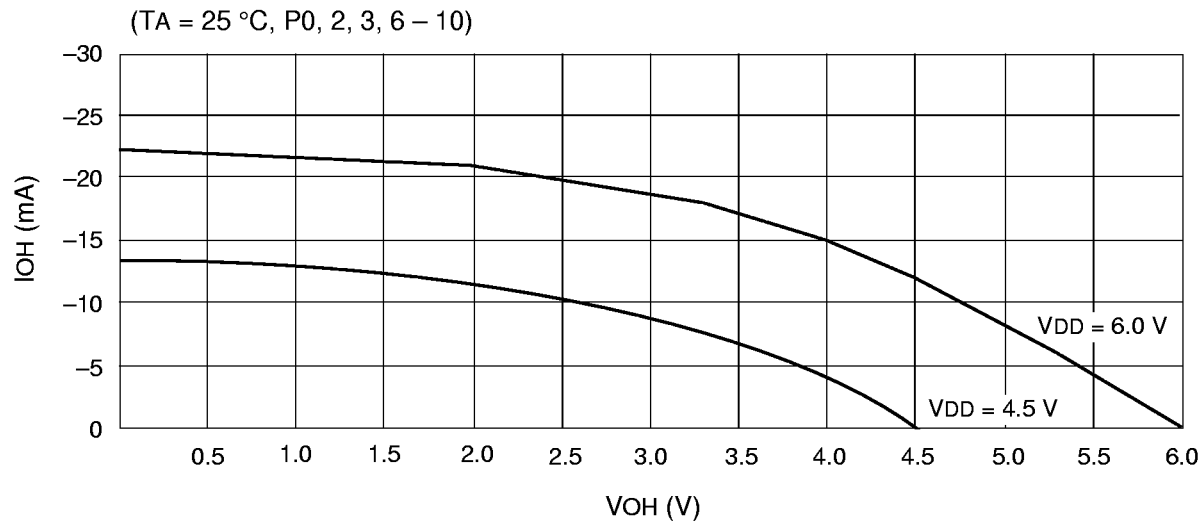
VDD	VOL	IOL
6.0 V	0.014 V	400 µA
	0.05 V	1.6 mA
4.5 V	0.014 V	400 µA
	0.057 V	1.6 mA

Figure 74. I_{OL} vs. V_{OL} (P0, 2, 3, and 6–10)



VDD	VOL	IOL
6.0 V	0.30 V	15 mA
4.5 V	0.35 V	15 mA

Figure 75. I_{OL} vs. V_{OL} (P4 and 5)



VDD	VOH	IOH
6.0 V	6 V	– 100 μA
	5.9 V	– 1 mA
4.5 V	4.49 V	– 100 μA
	4.38 V	– 1 mA

Figure 76. I_{OH} vs. V_{OH} (P0, 2, 3, and 6–10)

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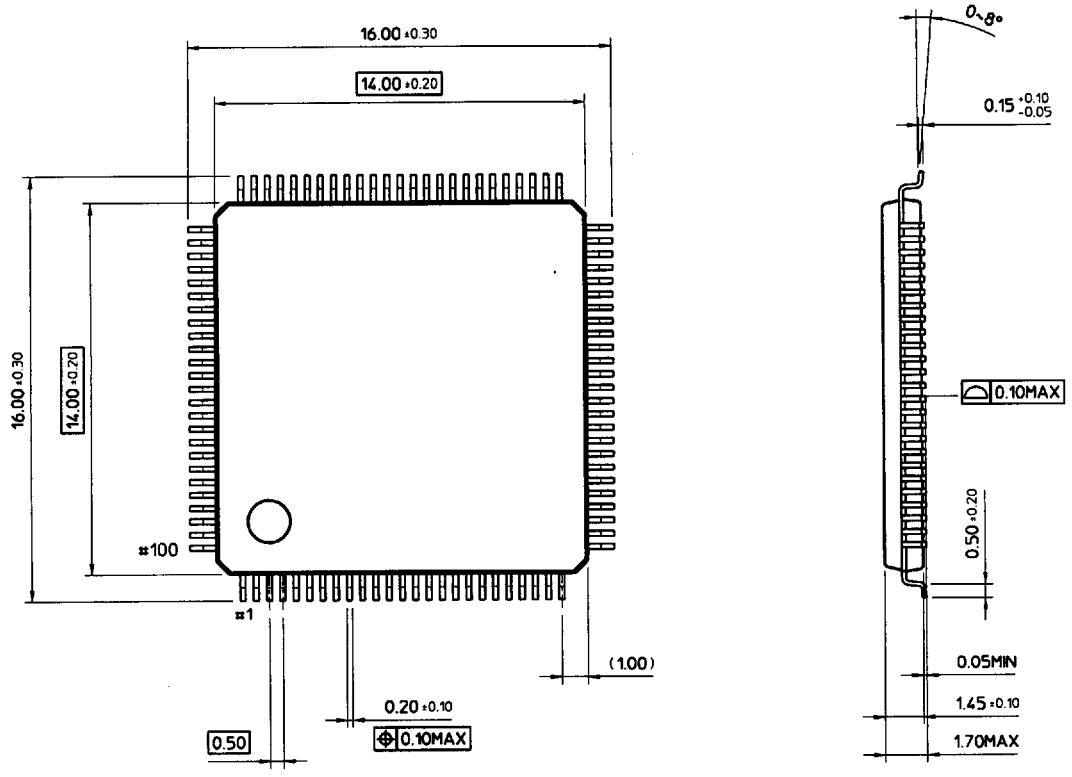
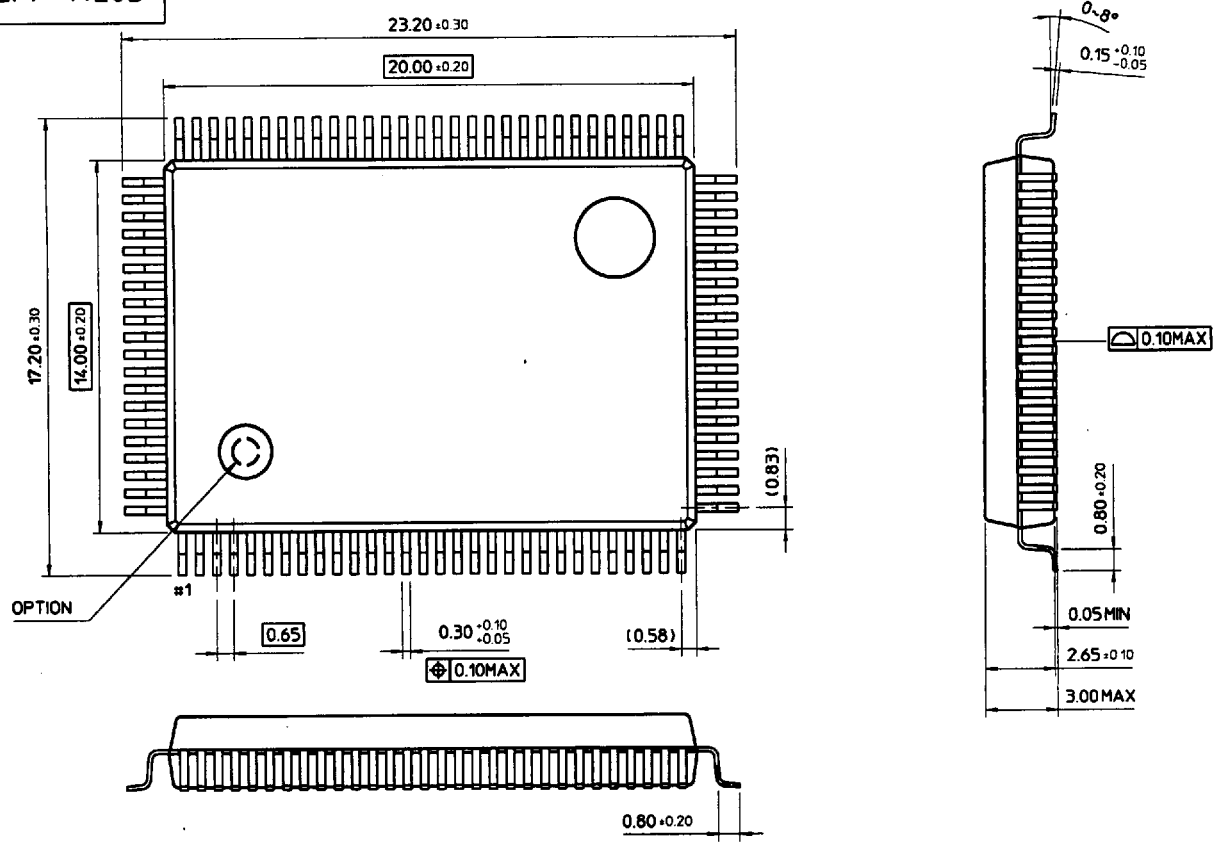


100-QFP-1420B



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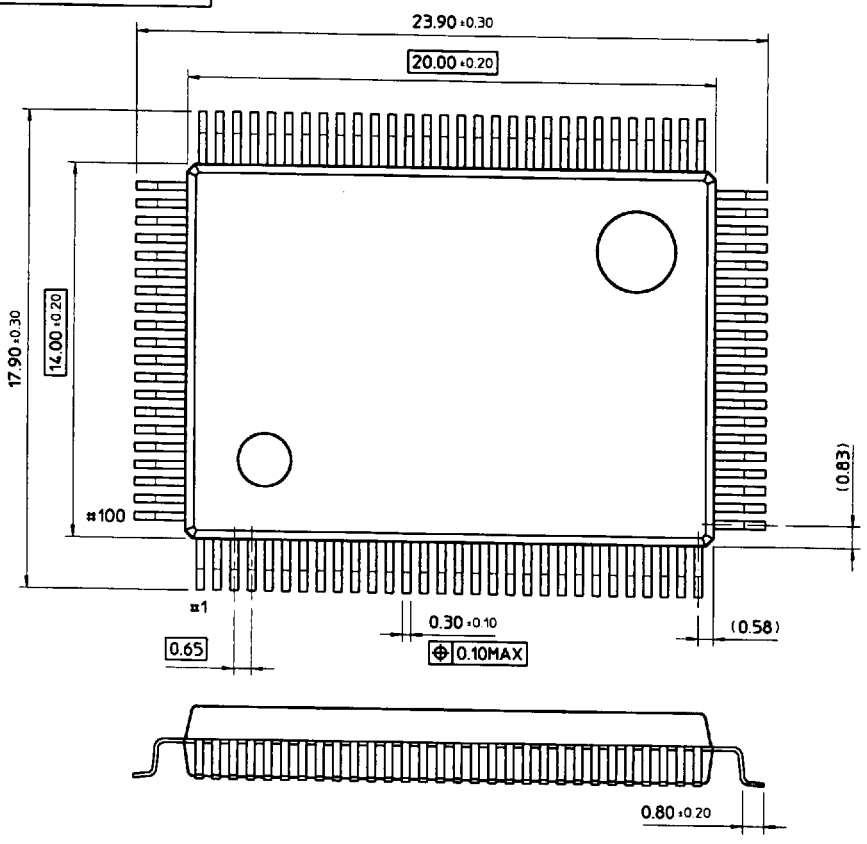
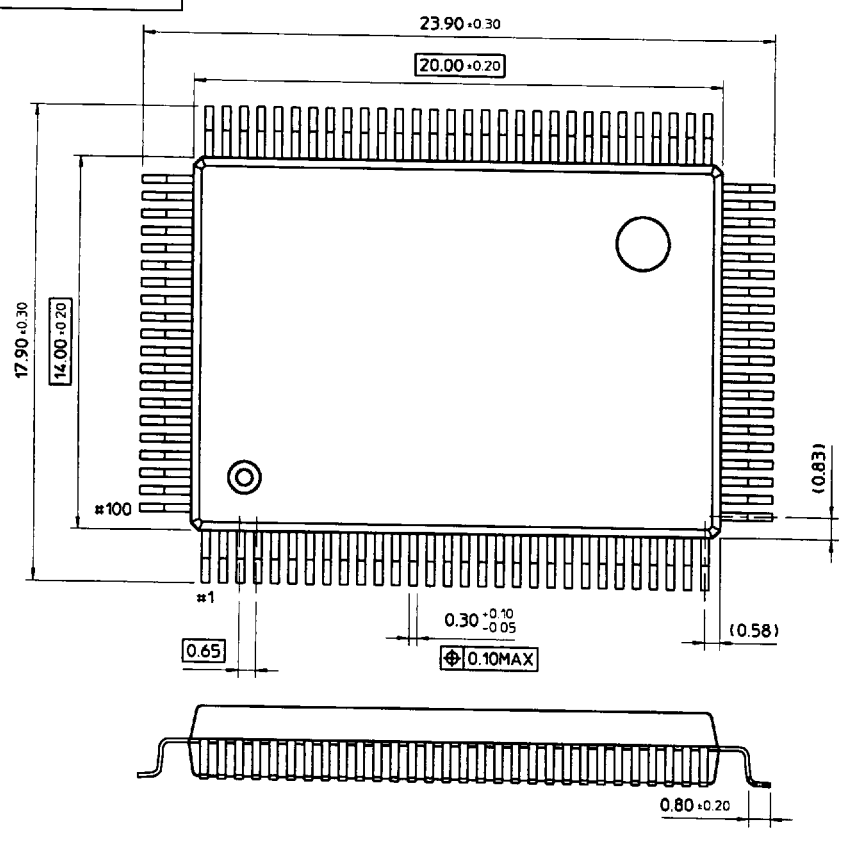


100-QFP-1420D



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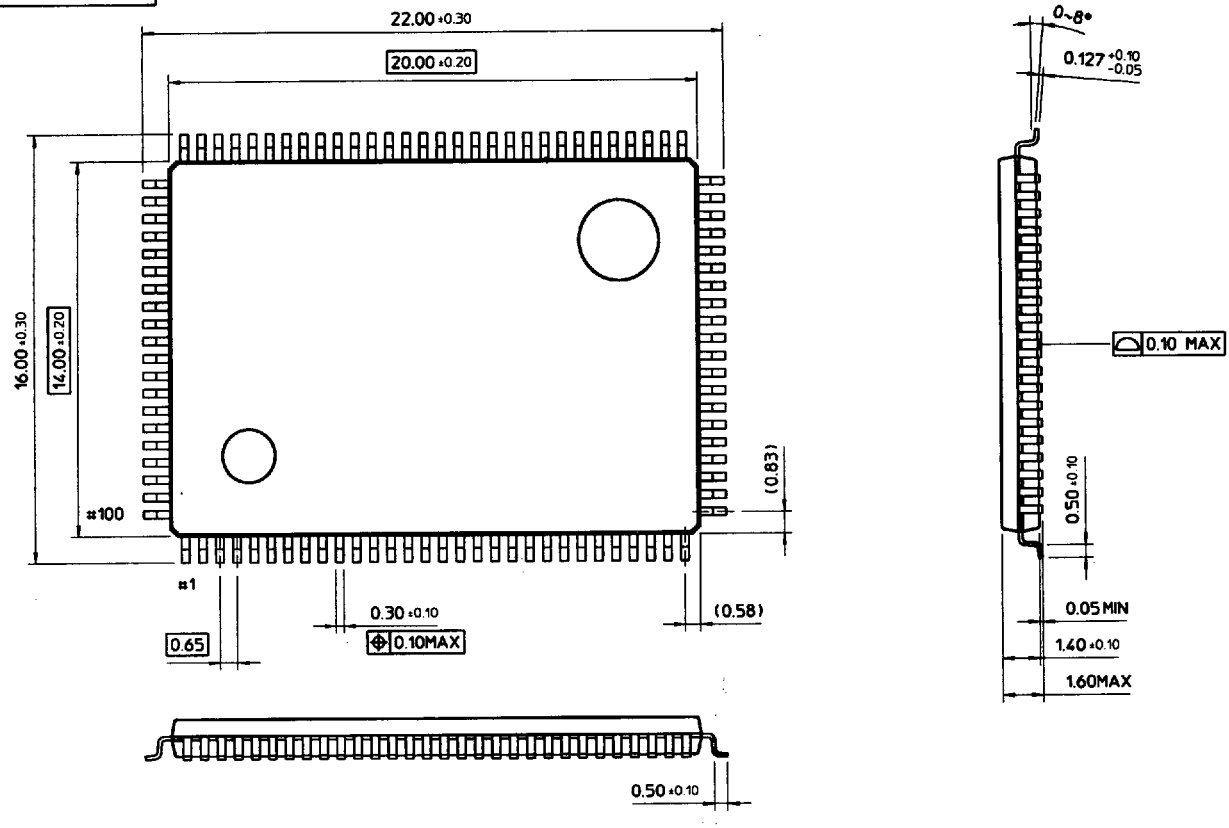

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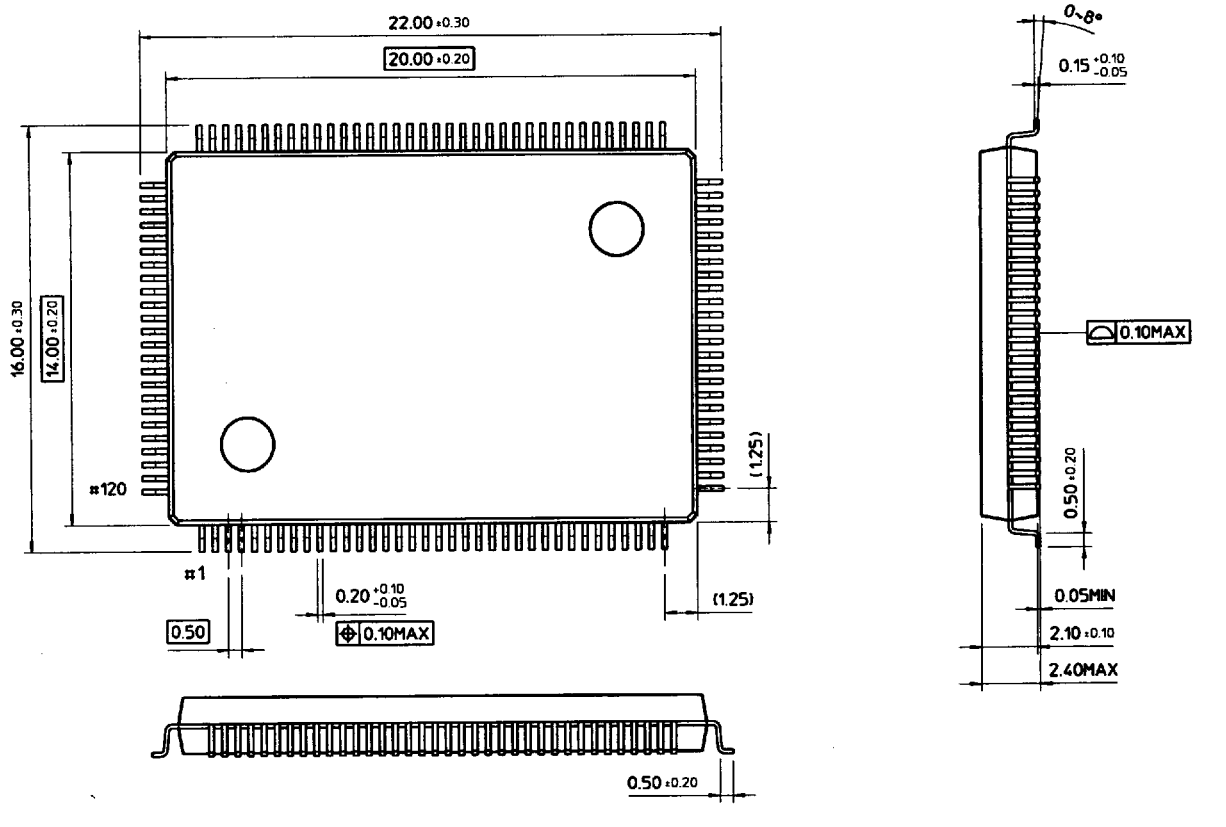

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