

Dual High-Side Switch 40 mΩ

The 33289 is a Dual High Side Switch (DHSS) dedicated for use in automotive applications. It is designed to drive typical inductive loads such as solenoid valves.

This device consists of two independent 40 mΩ $R_{DS(ON)}$ MOSFET channels plus corresponding control circuitry in a surface mount package. The 33289 can be interfaced directly to a microcontroller for input control and monitoring of diagnostic output.

Each switch offers independent protection and diagnosis during overcurrent, overvoltage, and undervoltage conditions, as well as an overtemperature shutdown feature.

A logic low on the Open Load Detect Enable pin (OLDE) minimizes bias current drain by disabling the open load circuitry current source. The device also has a very low quiescent current in standby mode.

FEATURES

- Designed to drive Automotive Inductive loads
- Operating Voltage Range from 6.0 V to 27 V
- Maximum Breakdown Voltage greater than 40 V
- 40 mΩ $R_{DS(ON)}$ at 25°C
- Overtemperature Protection with Hysteresis
- Overcurrent protection
- Under Voltage Shutdown
- Over Voltage Shutdown
- Open Load Detection in Off-State
- Independent Diagnostic Output
- ESD Protection 2.0 kV
- Standby Current less than 5.0 μA at V_{BAT} below 14 V

33289

DUAL HIGH-SIDE SWITCH



**DW SUFFIX)
98ASB42343B
20-PIN SOICW**

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33289DW/R2	-40°C to 125°C	20 SOICW

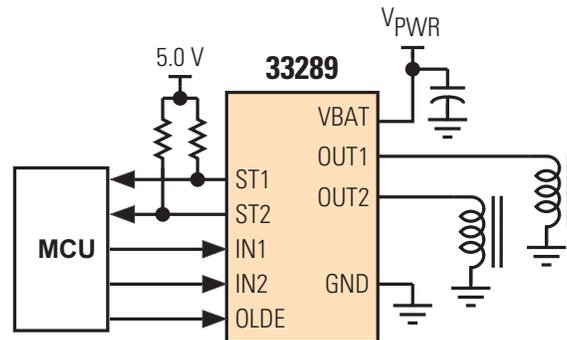


Figure 1. 33289 Simplified Application Diagram

* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

PIN CONNECTIONS

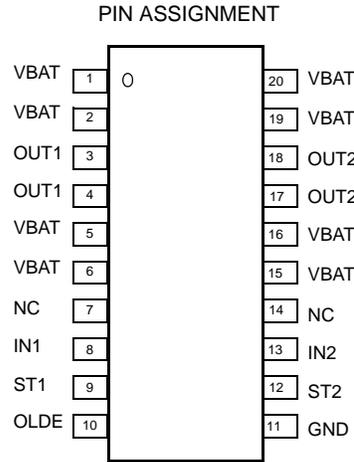


Figure 2. 33289 Pin Connections

Table 1. Pin Function Description

Pin Number	Pin Name	Pin Function	Definition
1, 2, 5, 6, 15, 16, 19, 20	VBAT	Supply Voltage	These are the power supply pins of the device. These pins are directly connected with the lead frame of the package and are tied to the drain of the switching MOSFET. These pins can be directly connected to the battery voltage. In addition to their supply function, these pins participate to the thermal behavior of the device in conducting the heat from the switching MOSFET to the printed circuit board.
3, 4, 18, 17	OUT1 OUT2	OUTPUT Channel 1 OUTPUT Channel 2	Pins 3 and 4 are the output 1 pins. Pins 17 and 18 are the output 2 pins. They are directly connected to the source of the power MOSFET. These pins are used by the control circuitry to sense the device output voltage. The $R_{DS(on)}$ is 40 mΩ max per output at 25°C and will increase to a maximum of 75 mΩ at 150°C junction temperature.
8, 13	IN1 IN2	INPUT Channel 1 INPUT Channel 2	These are the device input pins which directly control their associated outputs. The levels are CMOS compatible. When the input is a logic low, the associated output MOSFET is in the off state. When input is high, the MOSFET is turned on and the load is activated. When both inputs are low, the device is in standby mode and its supply current is reduced. Each input pin has an internal active pull down, so that it will not float if disconnected.
9, 12	ST1 ST2	Status for Channel 1 Status for Channel 2	These pins are the channel 1 and channel 2 fault detection flags. Their internal structure is an open drain architecture with an internal clamp at 6.0 V. An external pull up resistor connected to V_{DD} (5.0 V) is needed. This is an active low output. If the device is in its normal condition the status lines will be high. If open load or other fault occurs, the associated channel status flag will be pulled low. See Functional Truth Table.
10	OLDE	Open Load Detection Enable	This pin is a digital input which enables the open load current diagnostic circuitry. When OLDE is a logic low, the open load circuitry is not powered and the device's bias current draw is at a minimum. If OLDE is a logic high, the open load circuitry is functional at the price of a higher bias current draw. OLDE pin has a pull down resistor.
11	GND	GROUND	This is the GND pin of the device.

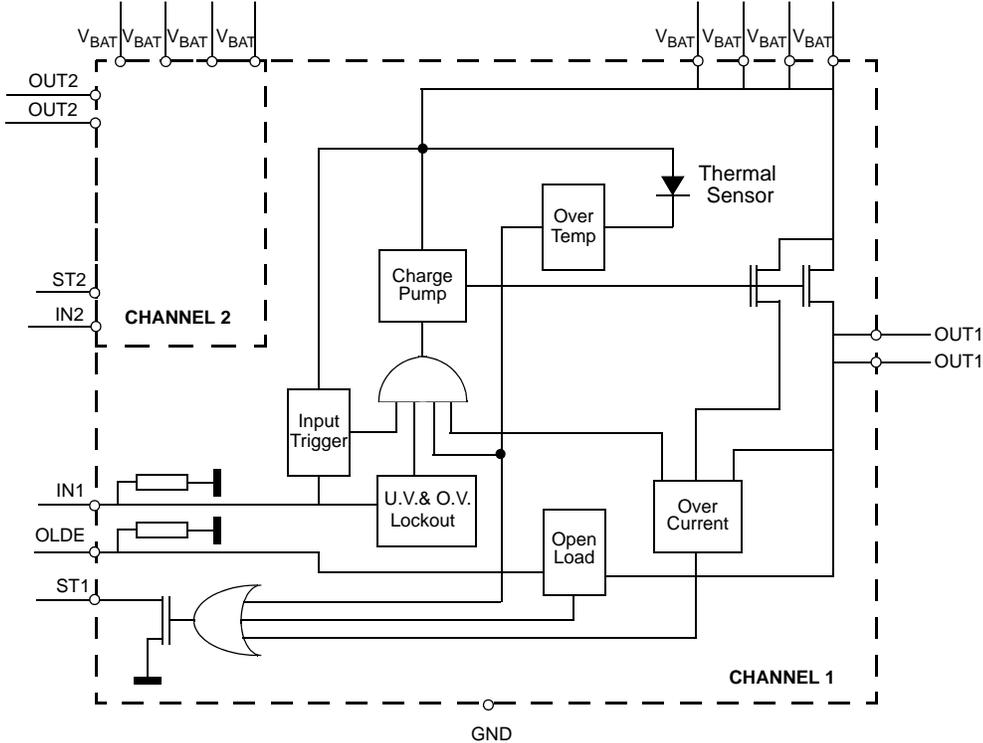


Figure 3. Simplified Internal Block Diagram

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
V _{BAT} and V _{BATC} Voltage: Continuous/Pulse	V _{BAT}	-0.3 to 41	V
OUT1, OUT2 Voltage with Respect to GND: Continuous/Pulse	V _{OUT}	-4.0 to 41	V
OUT1, OUT2 to V _{BTAP} Voltage: Continuous	V _{OUT}	41	V
ST1, ST2 Voltage: Continuous/Pulse	V _{ST}	-0.3 to 7.0	V
IN1, IN2 Voltage: Continuous	V _{IN}	-0.3 to 7.0	V
IN1, IN2, ST1, ST2, OLDE Current	I _{IN}	+/-4.0	mA
ESD all Pins			
Human Body Model ⁽¹⁾	V _{ESD1}	+/-2000	V
Machine Model ⁽¹⁾	V _{ESD2}	+/-200	V
THERMAL RATINGS			
Operating Junction Temperature	T _J	-40 to 150	°C
Storage Temperature	T _{ST}	-55 to 150	°C
Thermal Resistance Junction to Ambient ⁽²⁾	R _{THJA}	70	°C/W
Thermal Resistance Junction to lead: Both Channel on	R _{THJL1}	15	°C/W
Thermal Resistance Junction to lead: One Channel on	R _{THJL2}	15	°C/W
Thermal Resistance Junction to lead: Logic Die	R _{THJL3}	30	°C/W

Notes

- EDS1 testing is performed in accordance with the Human Body Model (Czap = 100 pF, Rzap = 1500 Ω) EDS2 testing is performed in accordance with the Machine Model (Czap = 100 pF, Rzap = 0 Ω)
- With minimum PCB dimensions.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Operating Voltage	V_{BAT}	6.0		V_{OV}	V
Supply Current: Both Channels On $V_{\text{BAT}} = 13.5\text{ V}$; OLDE High	I_{BAT1}		6.0	16	mA
Supply Current: One Channel On $V_{\text{BAT}} = 13.5\text{ V}$; OLDE High	I_{BAT2}		5.0	10	mA
Supply Current: Both Channels Off $V_{\text{BAT}} = 12.6\text{ V}$; OLDE Low, $T_J < 125^\circ\text{C}$	I_{BAT3}			5.0	μA
Supply Current: Any State $V_{\text{BAT}} = 13.5\text{ V}$	$I_{\text{BAT_MAX}}$			30	mA
Output Off state leakage current per channel $V_{\text{BAT}} = 13.5\text{ V}$; IN1, 2, OLDE low, Both output grounded, $T_J < 125^\circ\text{C}$	I_{DSS}		0.1	5.0	μA
Drain-Source On Resistance $V_{\text{BAT}} > 10\text{ V}$, $T_{\text{AMB}} = 25^\circ\text{C}$	R_{DSON1}			40	m Ω
Drain-Source On Resistance $V_{\text{BAT}} > 10\text{ V}$, $T_{\text{AMB}} = 150^\circ\text{C}$	R_{DSON2}			75	m Ω
Negative Inductive Clamp Voltage $I_{\text{OUT}} = 1\text{ A}$	V_{CLAMP}	-4.0		-1.0	V

INPUT CHARACTERISTICS

High Input Voltage (IN1, IN2)	V_{IH}	3.25			V
High Input Voltage (OLDE)	V_{OLDEH}	3.5			V
Low Input Voltage (IN1, IN2, OLDE)	V_{IL}			1.5	V
Logic Input Hysteresis IN1, IN2	V_{HYST}	0.4	0.6	0.8	V
Logic Input Current $V_{\text{IN}} = 1.5\text{ V}$	I_{IN}	3.0			μA
Logic Input Current $V_{\text{IN}} = 3.25\text{ V}$	I_{IN}			32.5	μA
Logic Input Clamp Voltage At $I_{\text{IN}} = 1\text{ mA}$	V_{CLMP}	5.5		7.0	V
Input Capacitance IN1, IN2 $R_{\text{IN}} = 47\text{ k}\Omega$ @ 100 kHz	C_{IN}			80	pF

STATUS CHARACTERISTICS

Status Voltage $I_{\text{ST}} = 1\text{ mA}$; Output in fault	V_{ST}			0.5	V
Status Leakage Current $V_{\text{ST}} = 5\text{ V}$	I_{STLK}			10	μA

Table 3. Static Electrical Characteristics

Characteristics noted under conditions $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Status Pin Capacitance $V_{\text{ST}} = 5\text{ V}$	C_{ST}			80	pF

OVERLOAD PROTECTION CHARACTERISTICS

Overcurrent latchoff threshold $V_{\text{BAT}} = 13.5\text{ V}$	I_{OCT}	4.0		9.0	A
Thermal Shutdown	T_{SHUT}	150	165	175	$^\circ\text{C}$
Thermal Shutdown Hysteresis	T_{HYST}			10	$^\circ\text{C}$
Overvoltage Shutdown Threshold Both IN1, IN2 logic high	V_{OV}	27		38	V
Overvoltage Shutdown Hysteresis Both IN1, IN2 logic high	V_{OVHYST}	0.1		2.0	V
Undervoltage Shutdown Threshold Both IN1, IN2 logic high	V_{UV}	4.75		6.0	V
Undervoltage Shutdown Hysteresis Both IN1, IN2 logic high	V_{UVHYST}	0.3	0.6	1.0	V

OPEN CIRCUIT DETECTION CHARACTERISTICS

Open Load Detect Current $V_{\text{OUT}} = 3.5\text{ V}$, $\text{OLDE} = 4.0\text{ V}$	I_{OL}	200	290	400	μA
Open Load Threshold Voltage	V_{OL}	1.5	2.4	3.5	V
Openload threshold voltage	V_{INOL}	1.5	2.5	3.5	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Description	Symbol	Min	Typ	Max	Unit
OVERLOAD PROTECTION CHARACTERISTICS					
Overcurrent latchoff delay From OverCurrent Treshold achieved to Output Voltage = 10% V_{BAT}	T_{OCTDLY}			30	μs
Overcurrent latchoff status delay From Output Voltage = 10% V_{BAT} to Status Flag <1 V	T_{OCTSTDLY}			50	μs
OPEN CIRCUIT DETECTION CHARACTERISTICS					
Open Load to Status Low Delay Time From $I_N = 1.5$ to Status Flag <1.5 V	T_{OLSTDT}			100	μs
Open Load Detect BlankingTime From $I_N = 1.5$ to Openload circuitry enable	T_{OLDBT}	3.0	10	50	μs
SWITCHING CHARACTERISTICS ⁽³⁾					
Turn-on Slew Rate From 10% to $V_{\text{BAT}} - 3.0\text{ V}$	S_{RPOUT1}	1.0		20	$\text{V}/\mu\text{s}$
Turn-on Slew Rate From $V_{\text{BAT}} - 3.0\text{ V}$ to 90%	S_{RPOUT2}	0.1		3.0	$\text{V}/\mu\text{s}$
Turn-off Slew Rate From 90% to 10%	S_{RNOUT}	1.0		20	$\text{V}/\mu\text{s}$
Turn-on Delay Time From $V_{\text{IN}}/2$ to 10% V_{BAT}	t_{DON}	1.0	2.5	15	μs
Turn-off Delay Time From $V_{\text{IN}}/2$ to 90% V_{BAT}	t_{DOFF}	1.0	5.0	15	μs
Notes					
3. $8\text{ V} < V_{\text{BAT}} < 18\text{ V}$, $R_{\text{LOAD}} = 7\ \Omega$					

TYPICAL APPLICATIONS

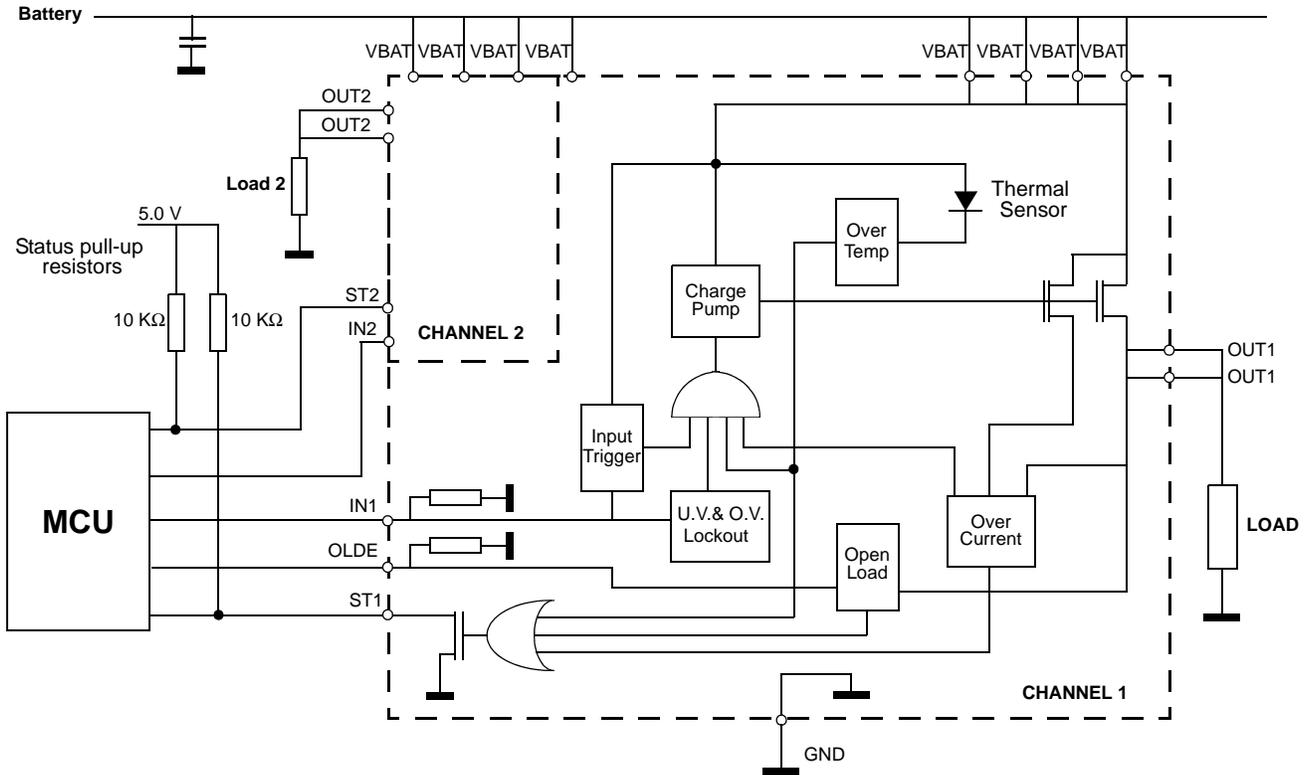


Figure 4. MC33289 Typical Application

Table 5. Functional Truth Table

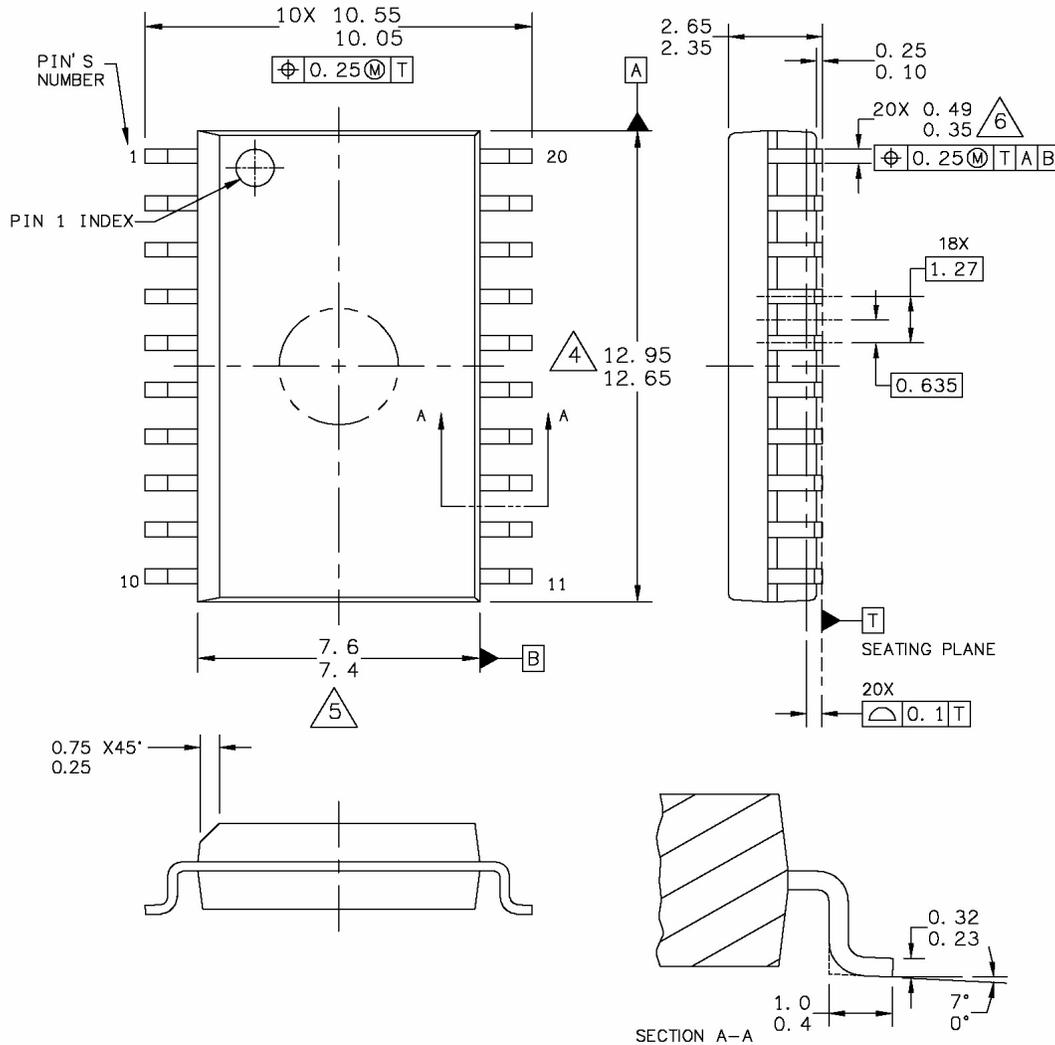
Conditions	IN1	IN2	OUT1	OUT2	ST1	ST2
Normal Operating Conditions	L	L	L	L	H	H
	H	L	H	L	H	H
	L	H	L	H	H	H
	H	H	H	H	H	H
Overtemperature Channel 1	H	X	L	X	L	H
Overtemperature Channel 2	X	H	X	L	H	L
Overtemperature Channel 1/Channel 2	H	H	L	L	L	L
Open Load Channel 1	L	X	H	X	L	H
Open Load Channel 2	X	L	X	H	H	L
Overcurrent Channel 1	H	X	L	X	L	H
Overcurrent Channel 2	X	H	X	L	H	L
Undervoltage Condition	X	X	L	L	H	H
Overvoltage Condition	X	X	L	L	H	H

L = 'Low level'; H = 'High level'; X = 'don't care'

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit www.freescale.com and perform a keyword search using the "98A" listed below



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 20LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42343B	REV: J
	CASE NUMBER: 751D-07	23 MAR 2005
	STANDARD: JEDEC MS-013AC	

DW SUFFIX
20-PIN
PLASTIC PACKAGE
98ASB42343B
ISSUE J

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
4.0	6/2006	<ul style="list-style-type: none">• Implemented Revision History page• Converted to Freescale format• Updated to the prevailing form and style

How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2006. All rights reserved.