

# MSM5416258A

**262,144-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO**

## DESCRIPTION

The MSM5416258A is a 262,144-word × 16-bit dynamic RAM fabricated in Oki's CMOS silicon gate technology. The MSM5416258A achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM5416258A is available in a 44/40-pin plastic TSOP.

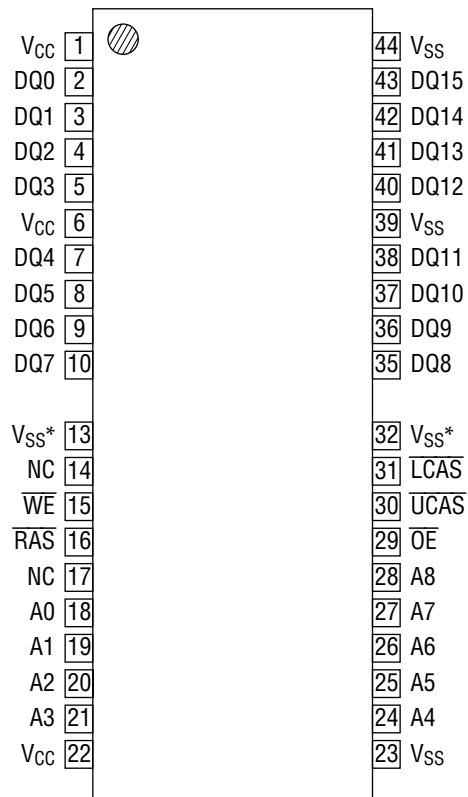
## FEATURES

- 262,144-word × 16-bit configuration
- Single 5.0 V power supply, ±0.5 V tolerance
- Input: TTL compatible
- Output: TTL compatible, 3-state
- Refresh: 512 cycles/8 ms
- Fast page mode with EDO, read modify write capability
- Byte wide control: 2  $\overline{\text{CAS}}$  control
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, hidden refresh,  $\overline{\text{RAS}}$  only refresh capability
- Package :  
44/40-pin 400 mil plastic TSOP (Type II) (TSOPII44/40-P-400-0.80-K) (Product : MSM5416258A-xxTS-K)  
xx indicates speed rank.

## PRODUCT FAMILY

| Family         | Access Time (Max.) |                 |                  |                  | Cycle Time (Min.) |                  | Power Dissipation (Max.) |
|----------------|--------------------|-----------------|------------------|------------------|-------------------|------------------|--------------------------|
|                | t <sub>RAC</sub>   | t <sub>AA</sub> | t <sub>CAC</sub> | t <sub>OEA</sub> | t <sub>RC</sub>   | t <sub>HPC</sub> |                          |
| MSM5416258A-40 | 40 ns              | 22 ns           | 10 ns            | 10 ns            | 80 ns             | 15 ns            | 825 mW                   |
| MSM5416258A-45 | 45 ns              | 24 ns           | 12 ns            | 12 ns            | 90 ns             | 20 ns            | 770 mW                   |

## PIN CONFIGURATION (TOP VIEW)



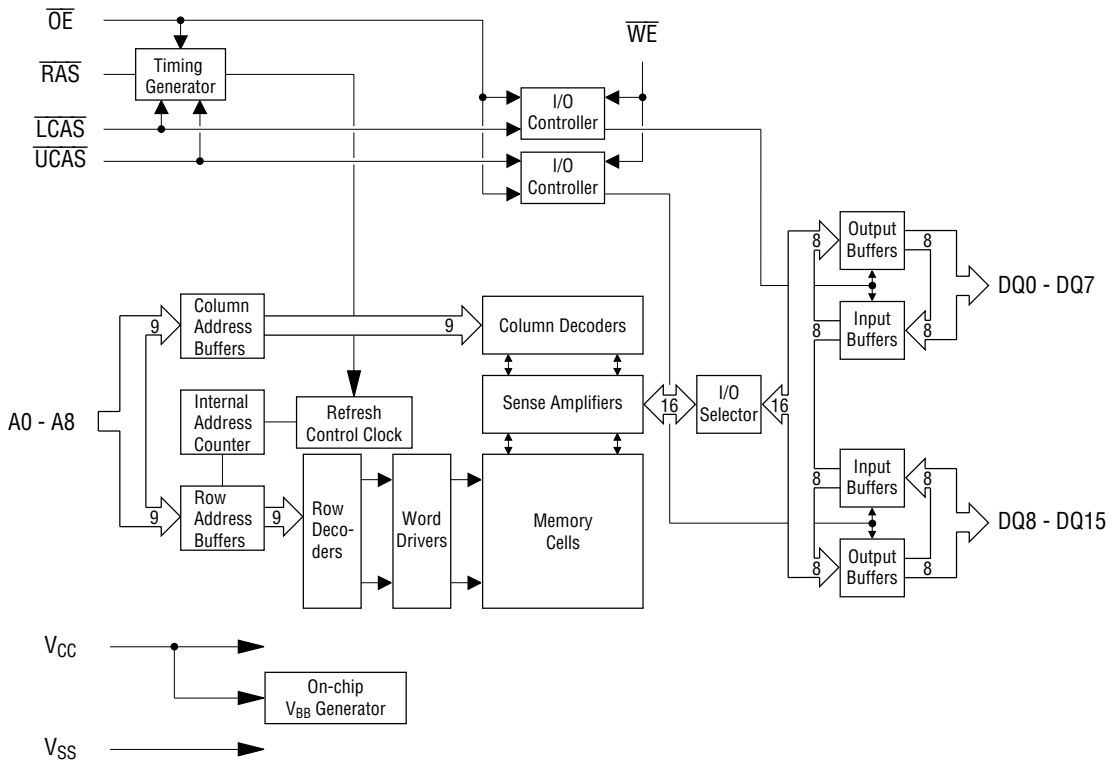
44/40-Pin Plastic TSOP (II)  
(K Type)

| Pin Name   | Function                     |
|--|------------------------------|
| A0 - A8  | Address Input                |
| $\overline{\text{RAS}}$                          | Row Address Strobe           |
| $\overline{\text{LCAS}}, \overline{\text{UCAS}}$ | Column Address Strobe        |
| DQ0 - DQ15                                       | Data - Input / Data - Output |
| $\overline{\text{WE}}$                           | Write Enable                 |
| $\overline{\text{OE}}$                           | Output Enable                |
| V <sub>CC</sub>                                  | Power Supply (5.0 V)         |
| V <sub>SS</sub>                                  | Ground (0 V)                 |
| NC   | No Connection                |
| V <sub>SS</sub> *                                | Ground (0 V)*                |

Note: The same power supply voltage must be provided to every V<sub>CC</sub> pin, and the same GND voltage level must be provided to every V<sub>SS</sub> pin.

\*: For improved signal integrity, it is recommended to connect the V<sub>SS</sub>\* pins, pin 13 and pin 32, to GND: the pins are electrically connected to internal GND.

**BLOCK DIAGRAM**



**FUNCTION TABLE**

| Input Pin |      |      |    |    | DQ Pin           |                  | Function Mode    |
|-----------|------|------|----|----|------------------|------------------|------------------|
| RAS       | LCAS | UCAS | WE | OE | DQ0 - DQ7        | DQ8 - DQ15       |                  |
| H         | *    | *    | *  | *  | High-Z           | High-Z           | Standby          |
| L         | H    | H    | *  | *  | High-Z           | High-Z           | Refresh          |
| L         | L    | H    | H  | L  | D <sub>OUT</sub> | High-Z           | Lower Byte Read  |
| L         | H    | L    | H  | L  | High-Z           | D <sub>OUT</sub> | Upper Byte Read  |
| L         | L    | L    | H  | L  | D <sub>OUT</sub> | D <sub>OUT</sub> | Word Read        |
| L         | L    | H    | L  | H  | D <sub>IN</sub>  | Don't Care       | Lower Byte Write |
| L         | H    | L    | L  | H  | Don't Care       | D <sub>IN</sub>  | Upper Byte Write |
| L         | L    | L    | L  | H  | D <sub>IN</sub>  | D <sub>IN</sub>  | Word Write       |
| L         | L    | L    | H  | H  | High-Z           | High-Z           | —                |

\* : "H" or "L"

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

| Parameter                               | Symbol    | Condition                | Rating      | Unit             |
|---|-----------|--------------------------|-------------|------------------|
| Voltage on Any Pin Relative to $V_{SS}$ | $V_T$     | $T_a = 25^\circ\text{C}$ | -1.0 to 7.0 | V                |
| Short Circuit Output Current            | $I_{OS}$  | $T_a = 25^\circ\text{C}$ | 50          | mA               |
| Power Dissipation                       | $P_D$     | $T_a = 25^\circ\text{C}$ | 1           | W                |
| Operating Temperature                   | $T_{opr}$ | —                        | 0 to 70     | $^\circ\text{C}$ |
| Storage Temperature                     | $T_{stg}$ | —                        | -55 to 150  | $^\circ\text{C}$ |

### Recommended Operating Conditions

(Ta = 0°C to 70°C)

| Parameter            | Symbol   | Min. | Typ. | Max.           | Unit |
|----------------------|----------|------|------|----------------|------|
| Power Supply Voltage | $V_{CC}$ | 4.5  | 5.0  | 5.5            | V    |
|                      | $V_{SS}$ | 0    | 0    | 0              | V    |
| Input High Voltage   | $V_{IH}$ | 2.4  | —    | $V_{CC} + 1.0$ | V    |
| Input Low Voltage    | $V_{IL}$ | -1.0 | —    | 0.8            | V    |

### Capacitance

(V<sub>CC</sub> = 5.0 V ±0.5 V, T<sub>a</sub> = 25°C, f = 1 MHz)

| Parameter                                      | Symbol    | Typ. | Max. | Unit |
|--|-----------|------|------|------|
| Input Capacitance (A0 - A8)                    | $C_{IN1}$ | —    | 5    | pF   |
| Input Capacitance<br>(RAS, LCAS, UCAS, WE, OE) | $C_{IN2}$ | —    | 7    | pF   |
| Input / Output Capacitance<br>(DQ0 - DQ15)     | $C_{I/O}$ | —    | 7    | pF   |

## DC Characteristics

(V<sub>CC</sub> = 5.0 V ±0.5 V, T<sub>a</sub> = 0°C to 70°C)

| Parameter   | Symbol           | Condition   | MSM5416258A<br>-40 |                 | MSM5416258A<br>-45 |                 | Unit | Note |
|---|------------------|---|--------------------|-----------------|--------------------|-----------------|------|------|
|   |                  |   | Min.               | Max.            | Min.               | Max.            |      |      |
| Output High Voltage   | V <sub>OH</sub>  | I <sub>OH</sub> = -2.5 mA   | 2.4                | V <sub>CC</sub> | 2.4                | V <sub>CC</sub> | V    |      |
| Output Low Voltage  | V <sub>OL</sub>  | I <sub>OL</sub> = 2.0 mA  | 0                  | 0.4             | 0                  | 0.4             | V    |      |
| Input Leakage Current                                       | I <sub>LI</sub>  | 0 V ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -10                | 10              | -10                | 10              | μA   |      |
| Output Leakage Current                                      | I <sub>LO</sub>  | DQi Disable<br>0 V ≤ V <sub>O</sub> ≤ 5.5 V   | -10                | 10              | -10                | 10              | μA   |      |
| Average Power<br>Supply Current<br>(Operating)              | I <sub>CC1</sub> | $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ Cycling,<br>t <sub>RC</sub> = Min.                        | —                  | 150             | —                  | 140             | mA   | 1, 2 |
| Power Supply<br>Current (Standby)                           | I <sub>CC2</sub> | $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ = V <sub>IH</sub>   | —                  | 3               | —                  | 3               | mA   | 1    |
| Average Power<br>Supply Current<br>(RAS Only Refresh)       | I <sub>CC3</sub> | $\overline{\text{RAS}}$ = Cycling,<br>$\overline{\text{CAS}}$ = V <sub>IH</sub> ,<br>t <sub>RC</sub> = Min. | —                  | 150             | —                  | 140             | mA   | 1, 2 |
| Average Power<br>Supply Current<br>(Fast Page Mode)         | I <sub>CC4</sub> | $\overline{\text{RAS}}$ = V <sub>IL</sub> ,<br>$\overline{\text{CAS}}$ Cycling,<br>t <sub>HPC</sub> = Min.  | —                  | 130             | —                  | 115             | mA   | 1, 3 |
| Average Power<br>Supply Current<br>(CAS before RAS Refresh) | I <sub>CC5</sub> | $\overline{\text{RAS}}$ = Cycling,<br>$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$                | —                  | 150             | —                  | 140             | mA   | 1, 2 |

- Notes :
1. I<sub>CC</sub> Max. is specified as I<sub>CC</sub> for output open condition.
  2. The address can be changed once or less while  $\overline{\text{RAS}}$  = V<sub>IL</sub>.
  3. The address can be changed once or less while  $\overline{\text{CAS}}$  = V<sub>IH</sub>.

## AC Characteristics (1/2)

(V<sub>CC</sub> = 5.0 V ±0.5 V, T<sub>a</sub> = 0°C to 70°C)

| Parameter  | Symbol            | MSM5416258A<br>-40 |         | MSM5416258A<br>-45 |         | Unit | Note      |
|--|-------------------|--------------------|---------|--------------------|---------|------|-----------|
|  |                   | Min.               | Max.    | Min.               | Max.    |      |           |
| Random Read or Write Cycle Time  | t <sub>RC</sub>   | 80                 | —       | 90                 | —       | ns   |           |
| Read Modify Write Cycle Time   | t <sub>RWC</sub>  | 115                | —       | 130                | —       | ns   |           |
| Fast Page Mode Cycle Time  | t <sub>HPC</sub>  | 15                 | —       | 20                 | —       | ns   |           |
| Fast Page Mode Read Modify Write Cycle Time                              | t <sub>PRWC</sub> | 55                 | —       | 60                 | —       | ns   |           |
| Access Time from $\overline{\text{RAS}}$                                 | t <sub>RAC</sub>  | —                  | 40      | —                  | 45      | ns   | 7, 12, 13 |
| Access Time from $\overline{\text{CAS}}$                                 | t <sub>CAC</sub>  | —                  | 10      | —                  | 12      | ns   | 7, 12     |
| Access Time from Column Address  | t <sub>AA</sub>   | —                  | 22      | —                  | 24      | ns   | 7, 13     |
| Access Time from $\overline{\text{OE}}$                                  | t <sub>OEA</sub>  | —                  | 10      | —                  | 12      | ns   |           |
| Access Time from $\overline{\text{CAS}}$ Precharge                       | t <sub>CPA</sub>  | —                  | 22      | —                  | 24      | ns   | 7, 12     |
| Output Low Impedance Time from $\overline{\text{CAS}}$                   | t <sub>CLZ</sub>  | 0                  | —       | 0                  | —       | ns   |           |
| Data Hold After $\overline{\text{CAS}}$ Low                              | t <sub>COH</sub>  | 3                  | —       | 3                  | —       | ns   | 17        |
| Output Buffer Turn-off Delay Time  | t <sub>OFF</sub>  | 3                  | 8       | 3                  | 8       | ns   | 8         |
| Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$            | t <sub>OEZ</sub>  | 3                  | 8       | 3                  | 8       | ns   | 8         |
| Output Buffer Turn-off Delay Time from $\overline{\text{RAS}}$           | t <sub>REZ</sub>  | 1.5                | 8       | 1.5                | 8       | ns   | 8         |
| Output Buffer Turn-off Delay Time from $\overline{\text{WE}}$            | t <sub>WEZ</sub>  | 3                  | 8       | 3                  | 8       | ns   | 8         |
| Transition Time  | t <sub>T</sub>    | 2                  | 35      | 2                  | 35      | ns   |           |
| Refresh Period   | t <sub>REF</sub>  | —                  | 8       | —                  | 8       | ms   |           |
| $\overline{\text{RAS}}$ Precharge Time                                   | t <sub>RP</sub>   | 30                 | —       | 35                 | —       | ns   |           |
| $\overline{\text{RAS}}$ Pulse Width                                      | t <sub>RAS</sub>  | 40                 | 10,000  | 45                 | 10,000  | ns   |           |
| $\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)                     | t <sub>RASP</sub> | 40                 | 100,000 | 45                 | 100,000 | ns   |           |
| $\overline{\text{RAS}}$ Hold Time  | t <sub>RSH</sub>  | 8                  | —       | 10                 | —       | ns   |           |
| $\overline{\text{RAS}}$ Hold Time Reference to $\overline{\text{OE}}$    | t <sub>ROH</sub>  | 8                  | —       | 8                  | —       | ns   |           |
| $\overline{\text{CAS}}$ Precharge Time                                   | t <sub>CP</sub>   | 5                  | —       | 6                  | —       | ns   |           |
| $\overline{\text{CAS}}$ Pulse Width                                      | t <sub>CAS</sub>  | 6                  | 10,000  | 7                  | 10,000  | ns   |           |
| $\overline{\text{CAS}}$ Hold Time  | t <sub>CSH</sub>  | 35                 | —       | 35                 | —       | ns   |           |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time        | t <sub>CRP</sub>  | 5                  | —       | 5                  | —       | ns   |           |
| $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge | t <sub>RHCP</sub> | 22                 | —       | 24                 | —       | ns   |           |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time            | t <sub>RCD</sub>  | 18                 | 30      | 18                 | 30      | ns   | 12        |
| $\overline{\text{RAS}}$ to Column Address Delay Time                     | t <sub>RAD</sub>  | 13                 | 18      | 13                 | 18      | ns   | 13        |
| Row Address Set-up Time  | t <sub>ASR</sub>  | 0                  | —       | 0                  | —       | ns   |           |
| Row Address Hold Time  | t <sub>RAH</sub>  | 8                  | —       | 8                  | —       | ns   |           |
| Column Address Set-up Time   | t <sub>ASC</sub>  | 0                  | —       | 0                  | —       | ns   |           |
| Column Address Hold Time   | t <sub>CAH</sub>  | 6                  | —       | 6                  | —       | ns   |           |
| Column Address Hold Time from $\overline{\text{RAS}}$                    | t <sub>AR</sub>   | 30                 | —       | 30                 | —       | ns   |           |
| Column Address to $\overline{\text{RAS}}$ Lead Time                      | t <sub>RAL</sub>  | 22                 | —       | 24                 | —       | ns   |           |

## AC Characteristics (2/2)

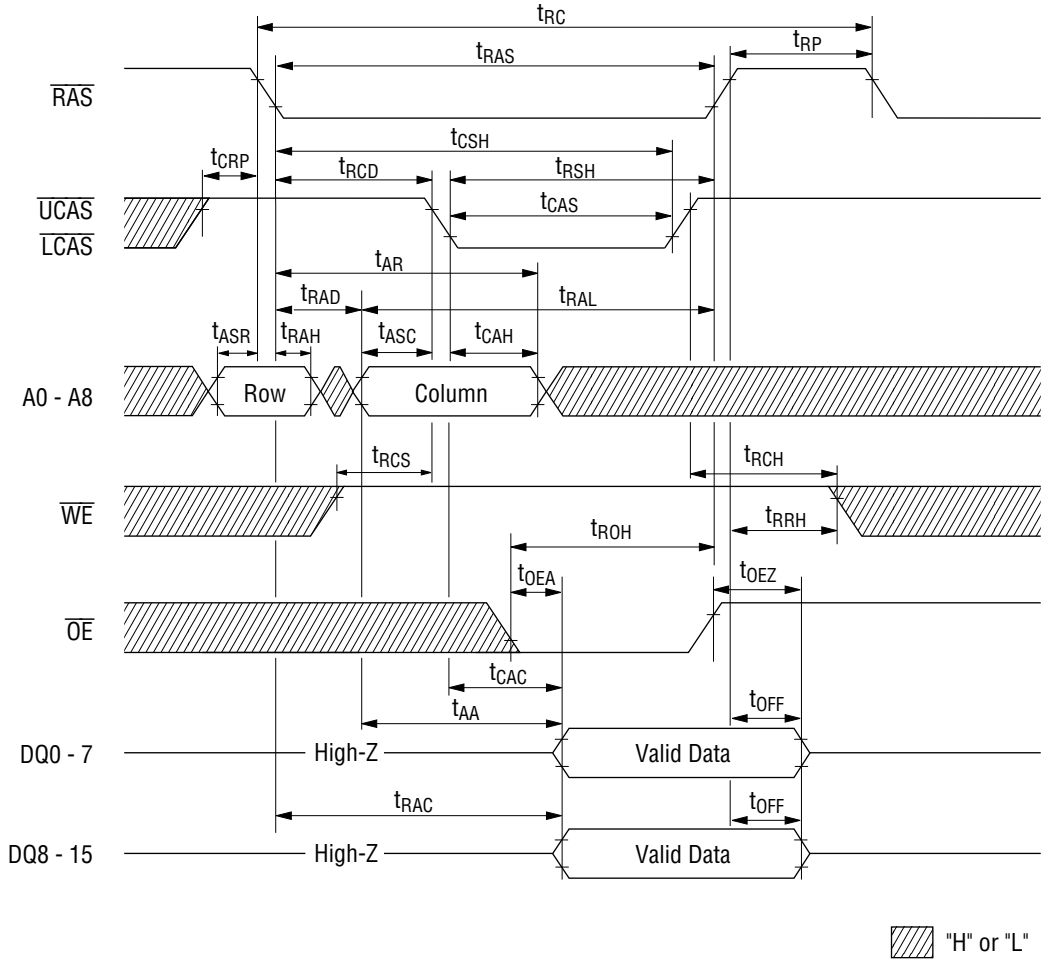
(V<sub>CC</sub> = 5.0 V ±0.5 V, T<sub>a</sub> = 0°C to 70°C)

| Parameter  | Symbol            | MSM5416258A<br>-40 |      | MSM5416258A<br>-45 |      | Unit | Note |
|--|-------------------|--------------------|------|--------------------|------|------|------|
|  |                   | Min.               | Max. | Min.               | Max. |      |      |
| Read Command Set-up Time   | t <sub>RCS</sub>  | 0                  | —    | 0                  | —    | ns   |      |
| Read Command Hold Time   | t <sub>RCH</sub>  | 0                  | —    | 0                  | —    | ns   | 9    |
| Read Command Hold Time<br>Reference to $\overline{\text{RAS}}$   | t <sub>RRH</sub>  | 0                  | —    | 0                  | —    | ns   | 9    |
| $\overline{\text{WE}}$ Pulse Width (DQ Disable)  | t <sub>WEP</sub>  | 10                 | —    | 10                 | —    | ns   |      |
| Write Command Set-up Time  | t <sub>WCS</sub>  | 0                  | —    | 0                  | —    | ns   | 11   |
| Write Command Hold Time  | t <sub>WCH</sub>  | 6                  | —    | 6                  | —    | ns   |      |
| Write Command Pulse Width  | t <sub>WP</sub>   | 6                  | —    | 6                  | —    | ns   |      |
| Write Command Hold Time from $\overline{\text{RAS}}$   | t <sub>WCR</sub>  | 30                 | —    | 30                 | —    | ns   |      |
| $\overline{\text{OE}}$ Command Hold Time   | t <sub>OEH</sub>  | 6                  | —    | 7                  | —    | ns   |      |
| Write Command to $\overline{\text{CAS}}$ Lead Time   | t <sub>CWL</sub>  | 6                  | —    | 7                  | —    | ns   |      |
| Write Command to $\overline{\text{RAS}}$ Lead Time   | t <sub>RWL</sub>  | 8                  | —    | 9                  | —    | ns   |      |
| Data to $\overline{\text{CAS}}$ Delay Time   | t <sub>DZC</sub>  | 0                  | —    | 0                  | —    | ns   |      |
| Data to $\overline{\text{OE}}$ Delay Time  | t <sub>DZO</sub>  | 0                  | —    | 0                  | —    | ns   |      |
| Data-in Set-up Time  | t <sub>DS</sub>   | 0                  | —    | 0                  | —    | ns   | 10   |
| Data-in Hold Time  | t <sub>DH</sub>   | 6                  | —    | 7                  | —    | ns   | 10   |
| Data-in Hold Time referenced to $\overline{\text{RAS}}$  | t <sub>DHR</sub>  | 30                 | —    | 30                 | —    | ns   |      |
| $\overline{\text{OE}}$ to Data-in Delay Time   | t <sub>OEED</sub> | 8                  | —    | 8                  | —    | ns   |      |
| $\overline{\text{OE}}$ "L" to $\overline{\text{CAS}}$ "H" Lead Time  | t <sub>OCH</sub>  | 10                 | —    | 10                 | —    | ns   |      |
| $\overline{\text{CAS}}$ "H" to $\overline{\text{OE}}$ "L" Lead Time  | t <sub>CHO</sub>  | 10                 | —    | 10                 | —    | ns   |      |
| Hi-Z Command Pulse Width   | t <sub>OEP</sub>  | 10                 | —    | 10                 | —    | ns   |      |
| $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time   | t <sub>CWD</sub>  | 22                 | —    | 22                 | —    | ns   | 11   |
| Column Address to $\overline{\text{WE}}$ Delay Time  | t <sub>AWD</sub>  | 32                 | —    | 32                 | —    | ns   | 11   |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time   | t <sub>RWD</sub>  | 50                 | —    | 55                 | —    | ns   | 11   |
| $\overline{\text{CAS}}$ Active Delay Time<br>from $\overline{\text{RAS}}$ Precharge  | t <sub>RPC</sub>  | 0                  | —    | 0                  | —    | ns   |      |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time<br>( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ ) | t <sub>CSR</sub>  | 10                 | —    | 10                 | —    | ns   |      |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time<br>( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )   | t <sub>CHR</sub>  | 10                 | —    | 10                 | —    | ns   |      |

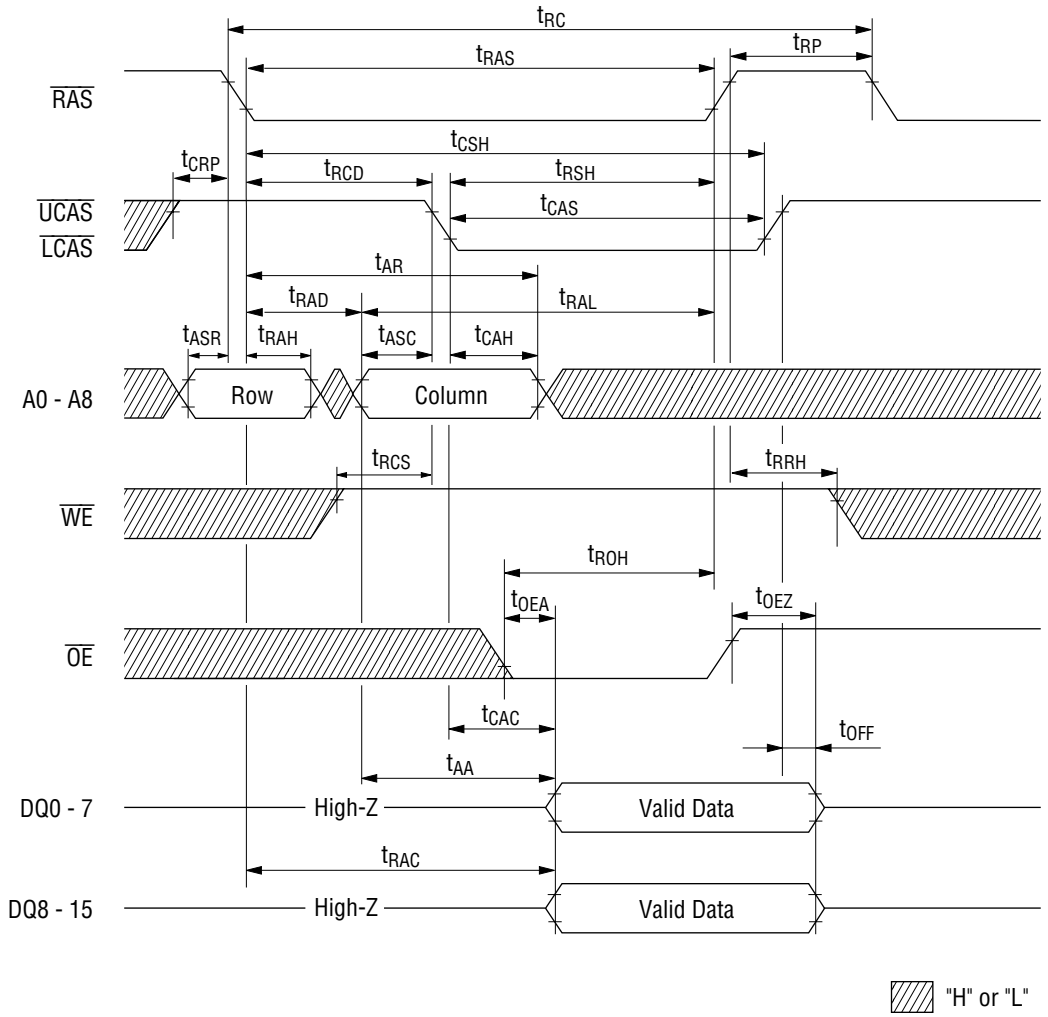
- Notes:
1. All voltages are referenced to  $V_{SS}$ .
  2. This parameter is dependent upon the cycle rate.
  3. This parameter is dependent upon the output loading. Specified values are obtained with the output open.
  4. An initial pause of 200  $\mu$ s is required after power-up, followed by any  $8\overline{RAS}$  cycles. (Example:  $\overline{RAS}$ -only-refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of  $8\overline{CAS}$  before  $\overline{RAS}$  cycles instead of  $8\overline{RAS}$  cycles are required.
  5. The AC characteristics assume  $t_T = 5$  ns.
  6.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  7. Data outputs are measured with a load of 50 pF. DOUT reference levels:  $V_{OH}/V_{OL} = 2.0\text{ V}/1.4\text{ V}$ . Note that  $V_{OL}$  is defined as 1.4 V when  $V_{SS}^*$  pins, pin 13 and pin 32, were open. The data output measurements under  $V_{OH}/V_{OL} = 2.0\text{ V}/0.8\text{ V}$  are guaranteed when  $V_{SS}^*$  pins, pin 13 and pin 32, were connected to GND.
  8.  $t_{REZ}$  (Max.),  $t_{OFF}$  (Max.),  $t_{WEZ}$  (Max.) and  $t_{OEZ}$  (Max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.
  9. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  10. These parameters are referenced to  $\overline{CAS}$  leading edge of early write cycles and to  $\overline{WE}$  leading edge in  $\overline{OE}$ -controlled write cycles and read-modify-write cycles.
  11.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$  (Min.), the cycle is an early write cycle and the data out pins will remain open circuit throughout the entire cycle. If  $t_{RWD} \geq t_{RWD}$  (Min.),  $t_{CWD} \geq t_{CWD}$  (Min.) and  $t_{AWD} \geq t_{AWD}$  (Min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
  12. Operation within the  $t_{RCD}$  (Max.) limit insures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, then access time is controlled by  $t_{CAC}$ .
  13. Operation within the  $t_{RAD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, then access time is controlled by  $t_{AA}$ .
  14. Input levels at the AC testing are 3.0 V/0 V.
  15. Addresses (A0 - A8) may be changed two times or less while  $\overline{RAS} = V_{IL}$ .
  16. Addresses (A0 - A8) may be changed once or less while  $\overline{CAS} = V_{IH}$  and  $\overline{RAS} = V_{IL}$ .
  17. This is guaranteed by design. ( $t_{COH} = t_{CAC}$  - output transition time). This parameter is not 100% tested.
  18. This parameter is dependent upon the number of address transitions. Specified values are measured with a maximum of two transitions per address cycle in Fast Page Mode.

### TIMING WAVEFORM

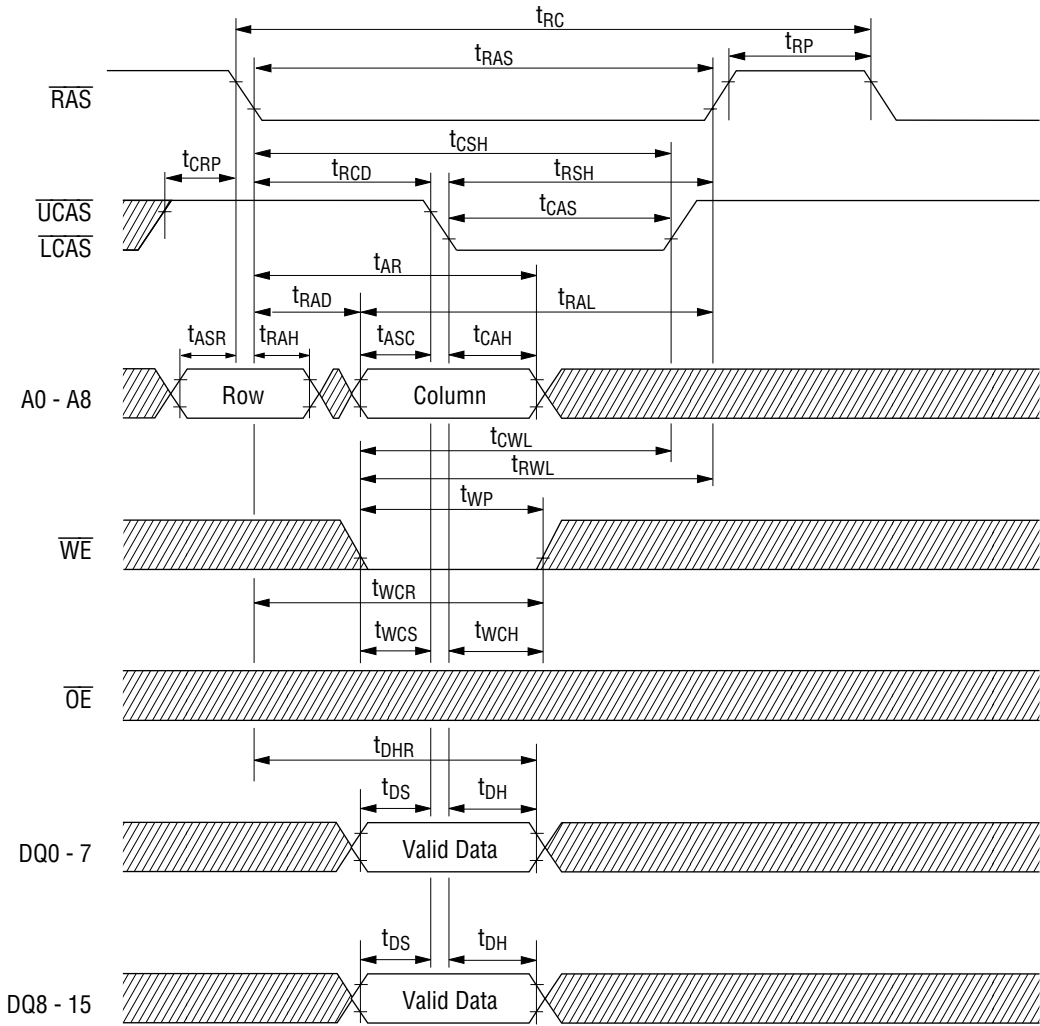
#### Read Cycle ( $\overline{\text{RAS}}$ Output Control)




Read Cycle ( $\overline{\text{CAS}}$  Output Control)

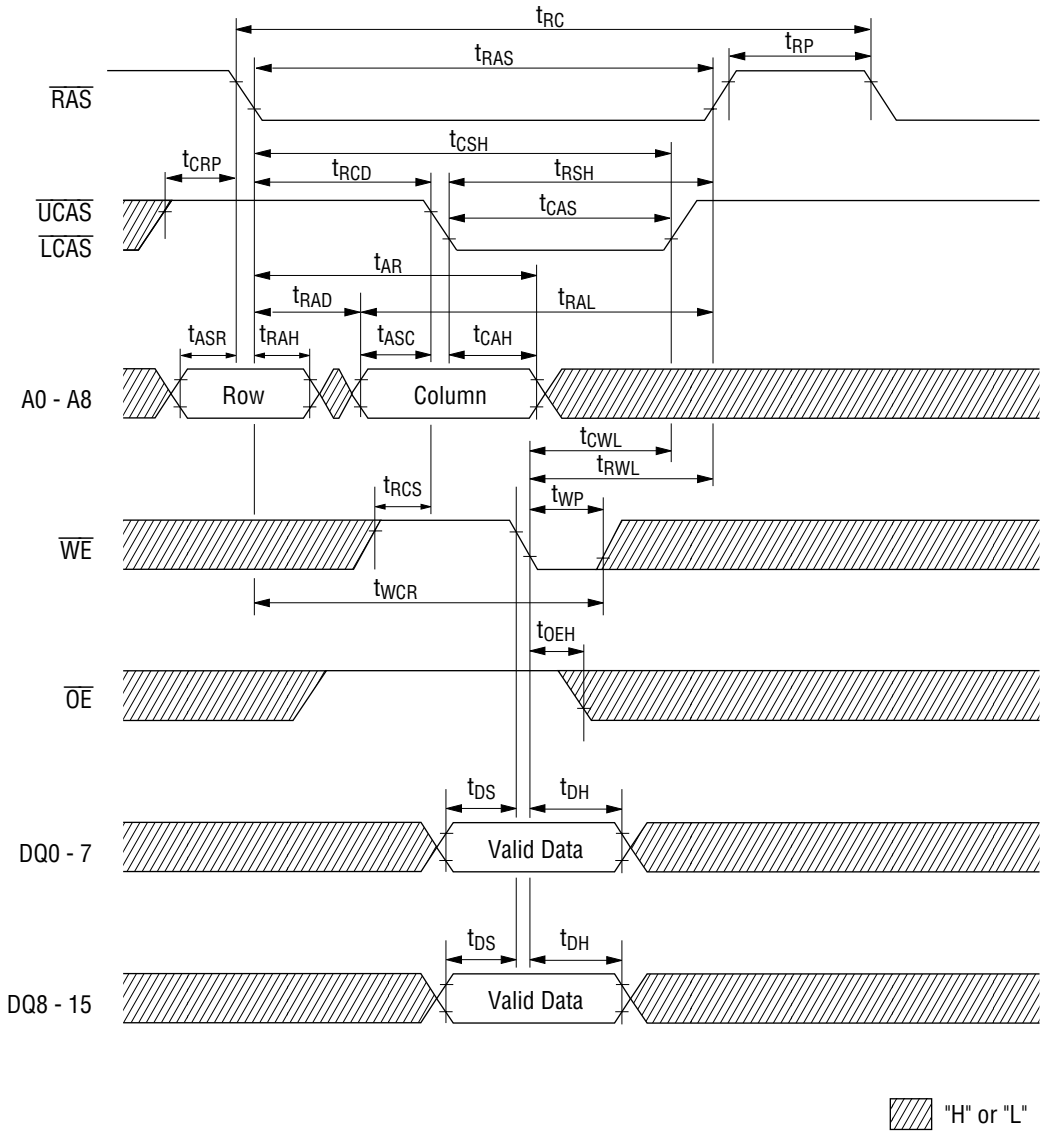


Early Write Cycle ( $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  Active)

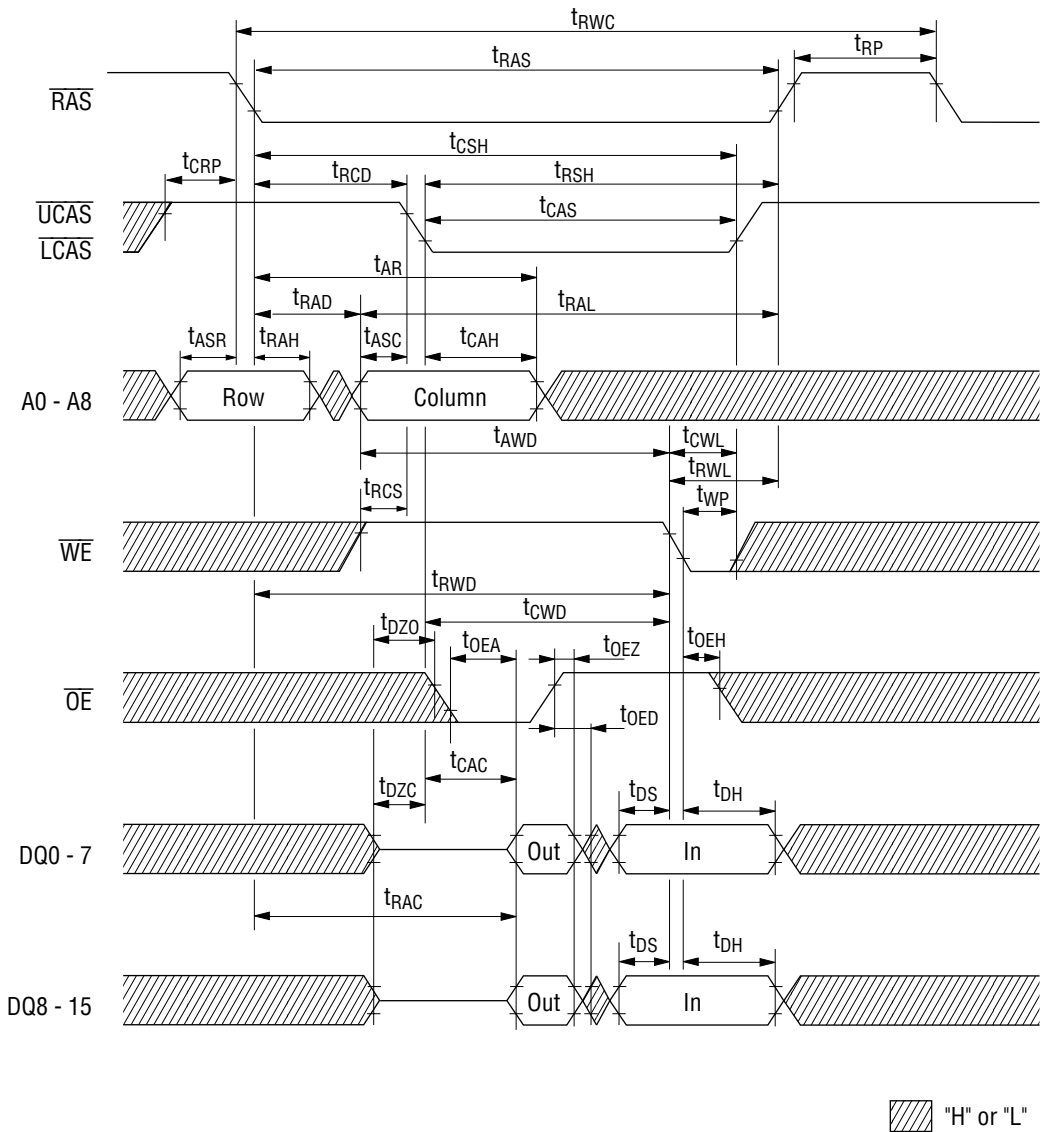


 "H" or "L"

Late Write Cycle ( $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  Active)



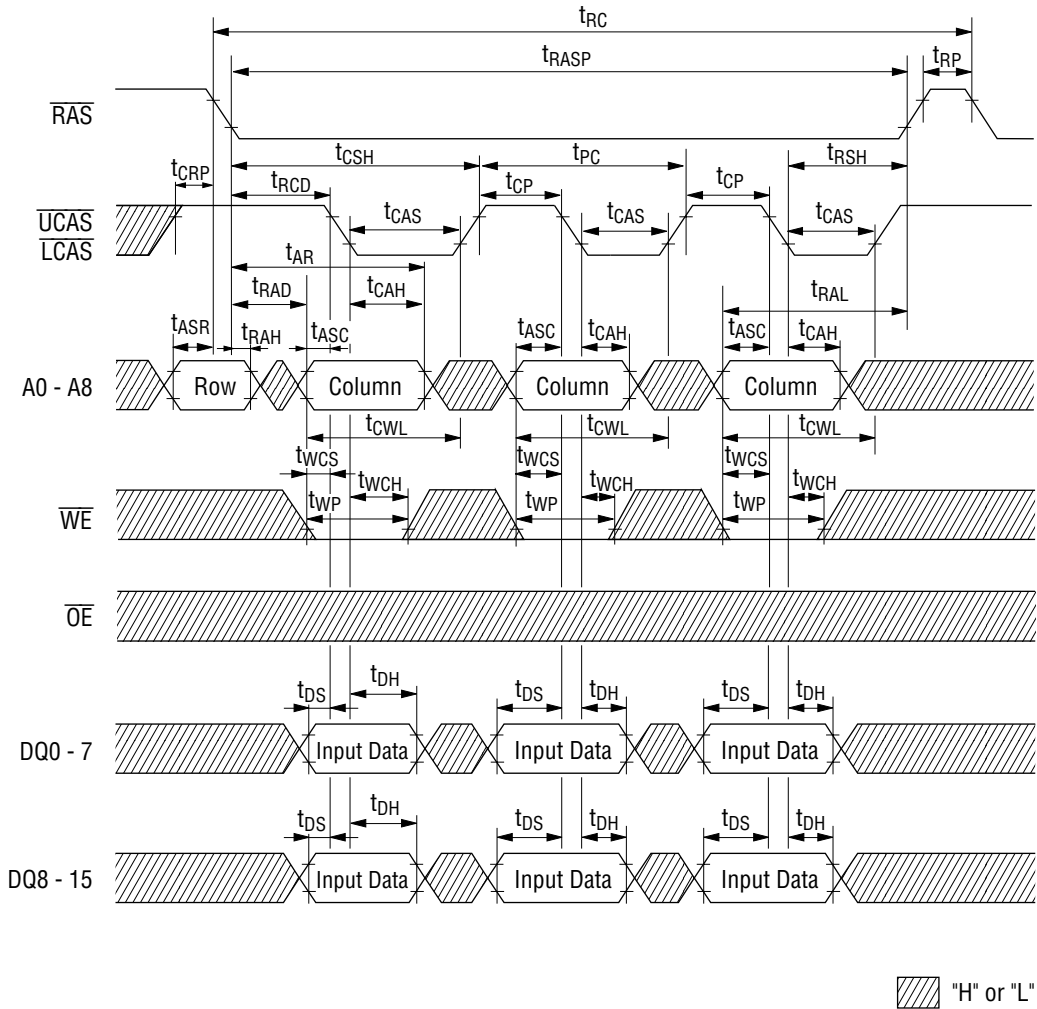
Read Modify Write Cycle ( $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  Active)





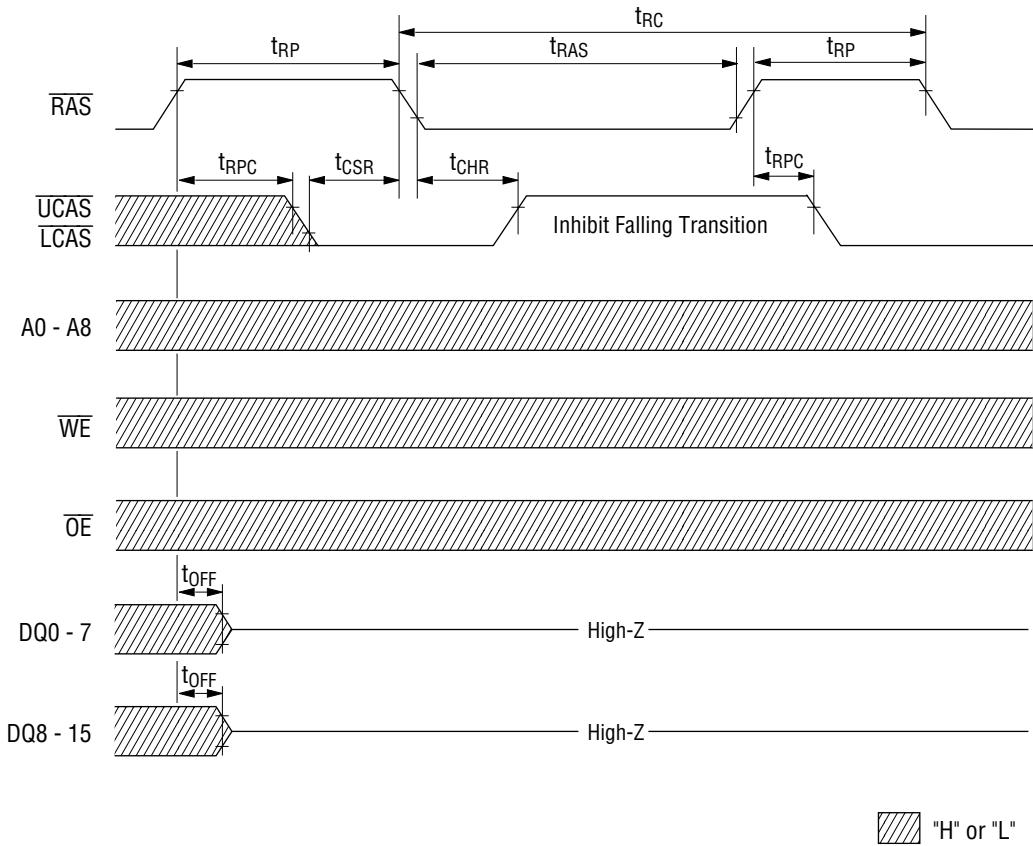


Fast Page Mode Early Write Cycle

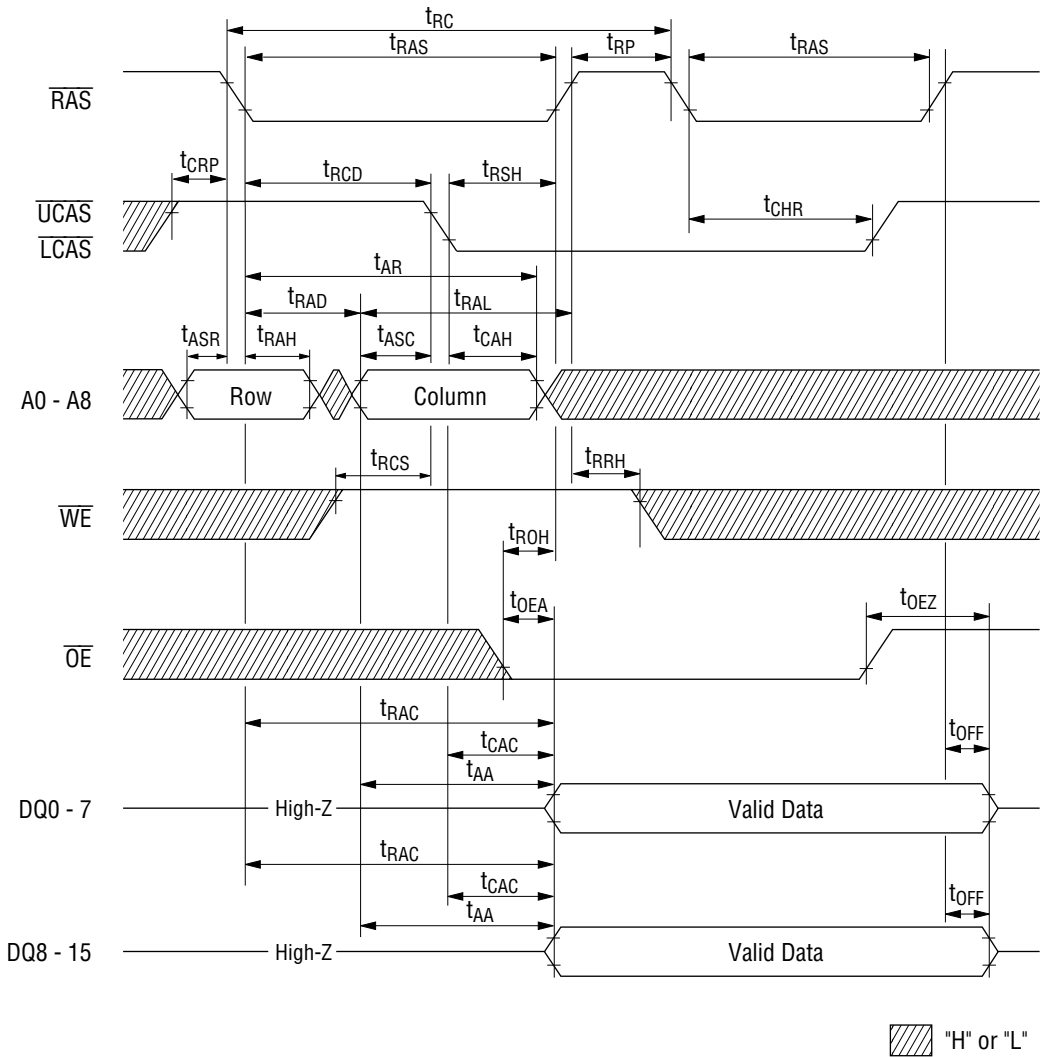




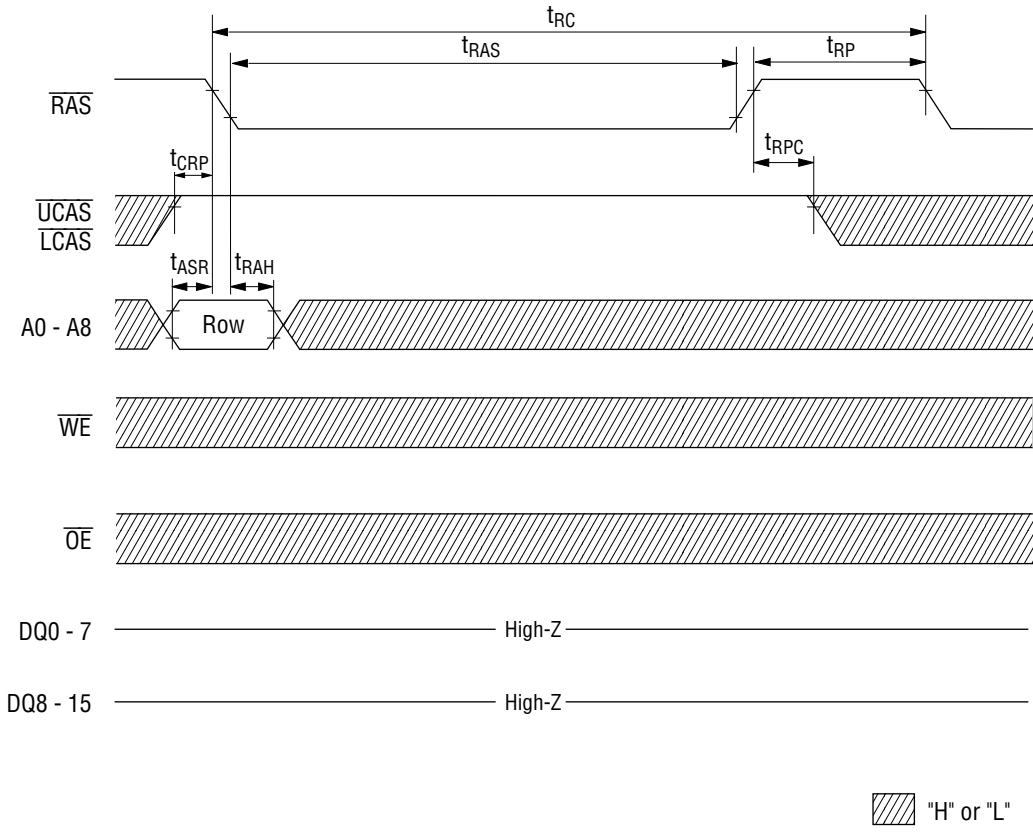
**CAS before RAS Refresh Cycle**



Hidden Refresh Cycle

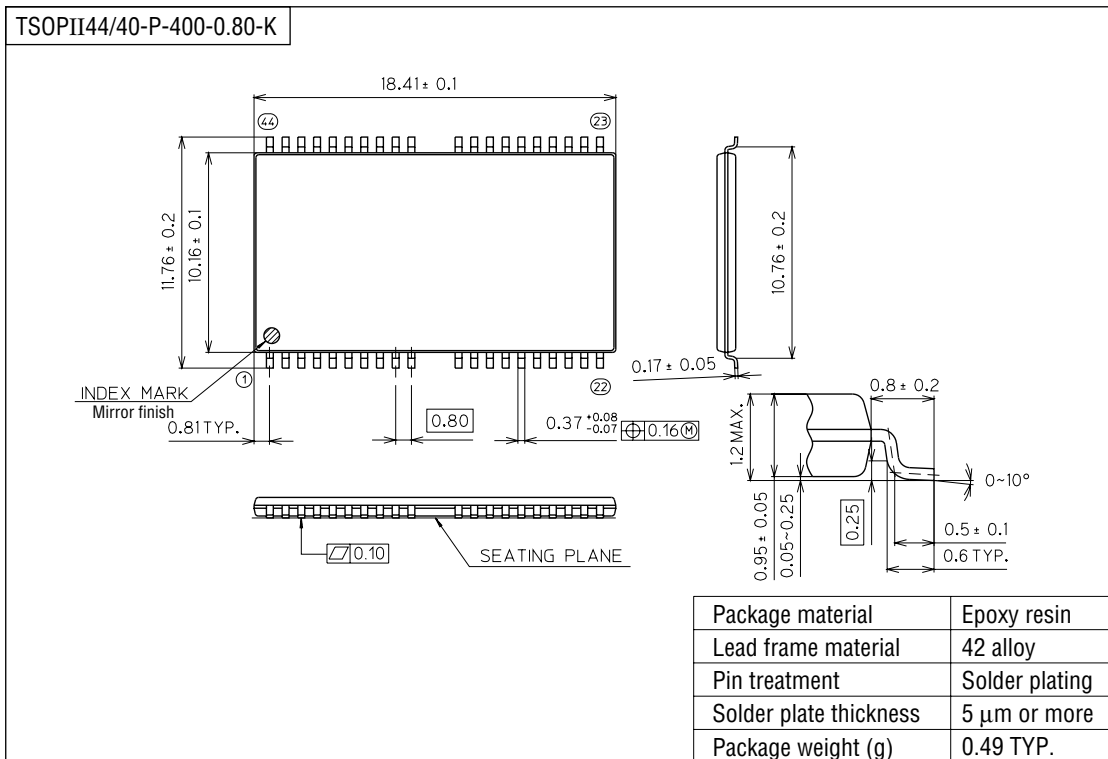


**RAS Only Refresh Cycle**



## PACKAGE DIMENSIONS

(Unit : mm)



## Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

**NOTICE**

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.
2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.
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