OKI Semiconductor

Technical Information

MSM5416258B

262,144-Word x 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM5416258B is a 262,144-word x 16-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM5416258B achieves high integration,high-speed operation,and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM5416258B is available in a 40-pin plastic SOJ.

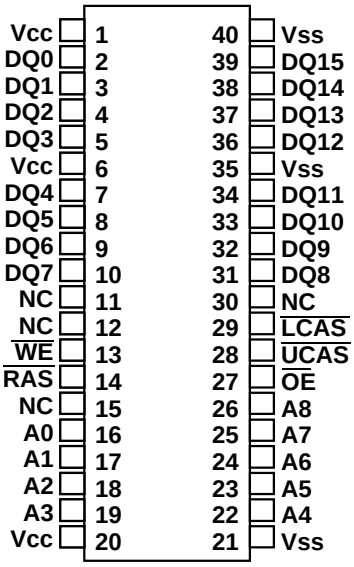
FEATURES

- 262,144-word by 16-bit configuration
- Single 5V power supply, ±10% tolerance
- Input :TTL compatible
- Output :TTL compatible, 3-state
- Refresh : 512 cycles/8ms
- Fast page mode with EDO,read modify write capability
- Byte wide control: 2 CAS control
- CAS before RAS refresh, Hidden refresh, RAS only refresh capability
- Package : 40-Pin 400 mil plastic SOJ (SOJ40-P-400)
  (Product : MSM5416258B-xxJS) xx : indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)		Power Dissipation
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}	t_{RC}	t_{HPC}	
MSM5416258B-28	28ns	15ns	9ns	9ns	48ns	12ns	1485mW
MSM5416258B-30	30ns	16ns	9ns	9ns	55ns	13ns	1458mW
MSM5416258B-35	35ns	19ns	10ns	10ns	60ns	13ns	1430mW

PIN CONFIGURATION (TOP VIEW)



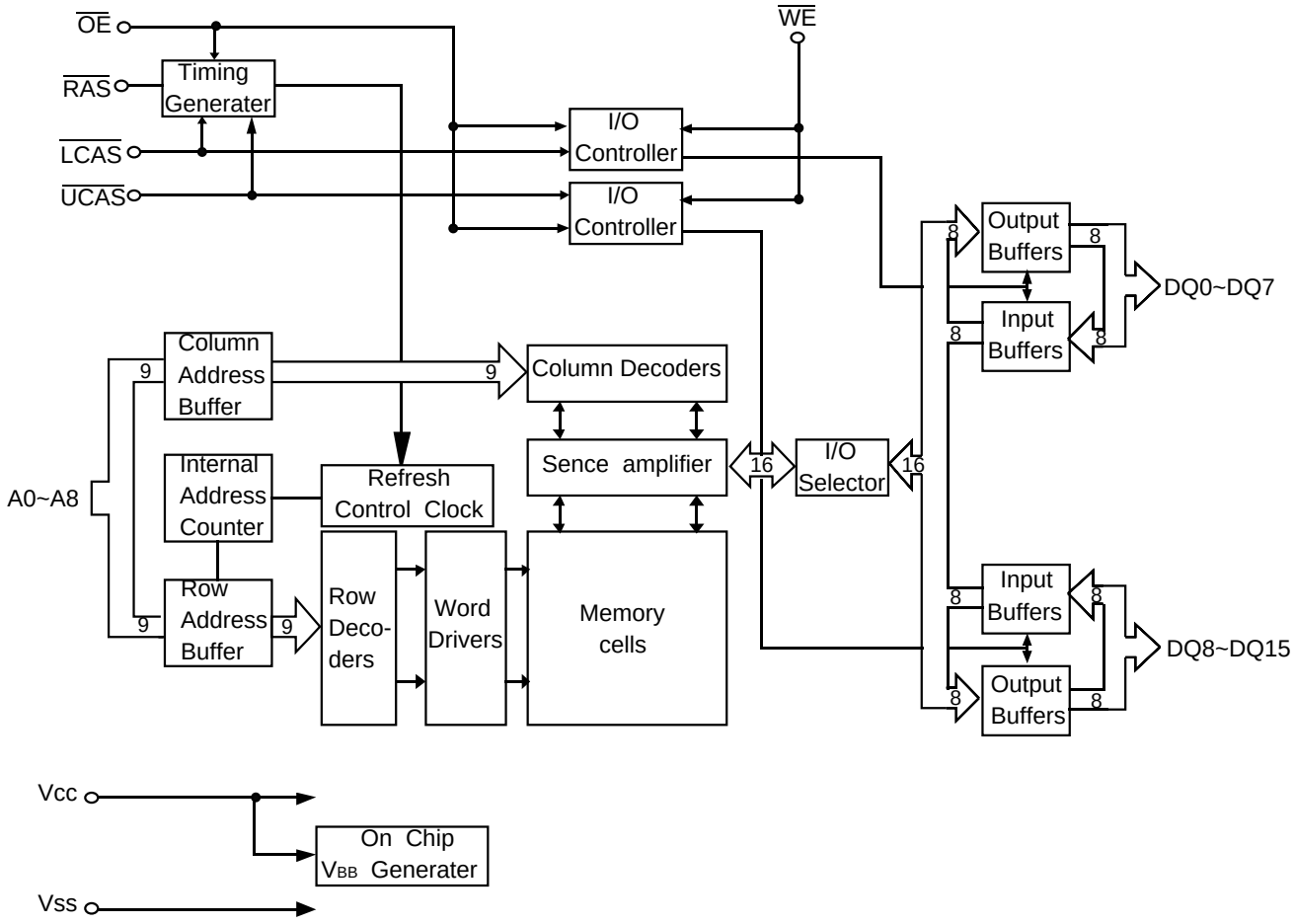
40Pin 400mil SOJ

Pin Names	Function
A0-A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$,$\overline{UCAS}$	Column Address Strobe
DQ0-15	Data-Input/ Data-Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply (+5V)
Vss	Ground (0V)
NC	No Connection

Note1 : The same power supply voltage must be provided to every Vcc pin, and the same GND voltage level must beprovideded to every Vss pin.

REVISION-2 1997.11.10, specification are subject to change without advanced notice.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQPin		Functinal Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ0~DQ7	DQ8~DQ15	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D_{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read
L	L	L	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	H	L	H	D_{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	-

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to Vss	Vt	Ta=25°C	-1.0 ~ +7.0	V
Short circuit output current	Ios	Ta=25°C	50	mA
Power dissipation	P_D	Ta=25°C	1.5	W
Operrating temperrature	Topr	—	0 ~ +70	°C
Storage temperature	Tstg	—	-55 ~ +150	°C

Recommended Operating Conditions

(Ta=0°Cto 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	—	4.5	5.0	5.5	V
	Vss	—	0	0	0	V
Input high voltage	V_{IH}	—	2.4	—	6.5	V
Input low voltage	V_{IL}	—	-1.0	—	0.8	V

Capacitance

(Vcc=5V±10%,Ta=25°C,f=1MHz)

Parameter	Symbol	Conditions	Typ.	Max.	Unit
Input capacitance (A0~A8)	C_{IN1}	—	—	8	pf
Input capacitance ($\overline{RAS}$,$\overline{LCAS}$,$\overline{UCAS}$,$\overline{WE}$,$\overline{OE}$)	C_{IN2}	—	—	8	pf
Input / output capacitance (DQ0~DQ15)	$C_{I/0}$	—	—	9	pf

DC CHARACTERISTICS

(V_{CC}=5V±10%, Ta=0 to 70°C)

Parameter	Symbol	Condition	MSM5416258B-28		MSM5416258B-30		MSM5416258B-35		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH}= - 1.0mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL}= 2.0mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V≤V_{IN}≤Vcc	-10	10	-10	10	-10	10	µA	
Output Leakage Current	I_{LO}	DQi Disable 0V≤V_O≤5.5V	-10	10	-10	10	-10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$,$\overline{CAS}$ Cycling t_{RC}=Min.	-	270	-	265	-	260	mA	1,2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$,$\overline{CAS}$ = V_{IH}	-	3	-	3	-	3	mA	1
Average Power Supply Current ($\overline{RAS}$ only Refresh)	I_{CC3}	$\overline{RAS}$=Cycling $\overline{CAS}$=V_{IH} t_{RC}=Min.	-	270	-	265	-	260	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{CC4}	$\overline{RAS}$=V_{IL} $\overline{CAS}$Cycling t_{HPC}=Min.	-	270	-	265	-	260	mA	1,3
Average Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	I_{CC5}	$\overline{RAS}$=Cycling $\overline{CAS}$ Befor $\overline{RAS}$	-	270	-	265	-	260	mA	1,2

Notes : 1. Icc Max. is specified as Icc for the output open cindition.
2. Address can be changed once or less while $\overline{RAS}$ = VIL.
3. Address can be changed once or less while $\overline{CAS}$ = VIH.

AC CHARACTERISTICS (1/2)

(Vcc =5V±10%, Ta =0~70°C)

Parameter	Symbol	MSM5416258B -28		MSM5416258B -30		MSM5416258B -35		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	48	—	55	—	60	—	ns	
Read/Write cycle time	t_{RMW}	70	—	75	—	85	—	ns	
Hyper page mode cycle time	t_{HPC}	12	—	13	—	13	—	ns	
Fast page mode read/write cycle time	t_{PRMW}	34	—	35	—	45	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	28	—	30	—	35	ns	7,12,13
Access time from $\overline{CAS}$	t_{CAC}	—	9	—	9	—	10	ns	7,12
Access time from column address	t_{AA}	—	15	—	16	—	19	ns	7,13
Access time from $\overline{OE}$	t_{OEA}	—	9	—	9	—	10	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	17	—	18	—	21	ns	7,12
Data hold after $\overline{CAS}$ low	t_{COH}	3	—	3	—	3	—	ns	17
Output buffer turn-off delay time	t_{OFF}	3	7	3	8	3	8	ns	8
$\overline{OE}$ to data output buffer turn-off delay time	t_{OEZ}	3	7	3	8	3	8	ns	8
$\overline{RAS}$ to data output buffer turn-off delay time	t_{REZ}	3	7	3	8	3	8	ns	8
$\overline{WE}$ to data output buffer turn-off delay time	t_{WEZ}	3	7	3	8	3	8	ns	8
Transition time	t_T	2	35	2	35	2	35	ns	
Refresh preiod	t_{REF}	—	8	—	8	—	8	ms	
$\overline{RAS}$ precharge time	t_{RP}	17	—	18	—	20	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	28	10,000	30	10,000	35	10,000	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	28	100,000	30	100,000	35	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	7	—	7	—	8	—	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	t_{ROH}	7	—	7	—	8	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	4	—	4	—	4	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	5	10,000	5	10,000	5	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	22	—	25	—	30	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10	19	11	22	13	26	ns	12
$\overline{RAS}$ to column address delay time	t_{RAD}	8	13	8	15	10	16	ns	
Row address set-up time	t_{ASR}	0	—	0	—	0	—	ns	13
Row address hold time	t_{RAH}	6	—	6	—	7	—	ns	
Column address set-up time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	5	—	5	—	5	—	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	21	—	22	—	25	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	15	—	18	—	20	—	ns	
Read command set-up time	t_{RCS}	0	—	0	—	0	—	ns	9
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	9
$\overline{WE}$ pulse width	t_{WEP}	10	—	10	—	10	—	ns	

AC CHARACTERISTICS (2/2)

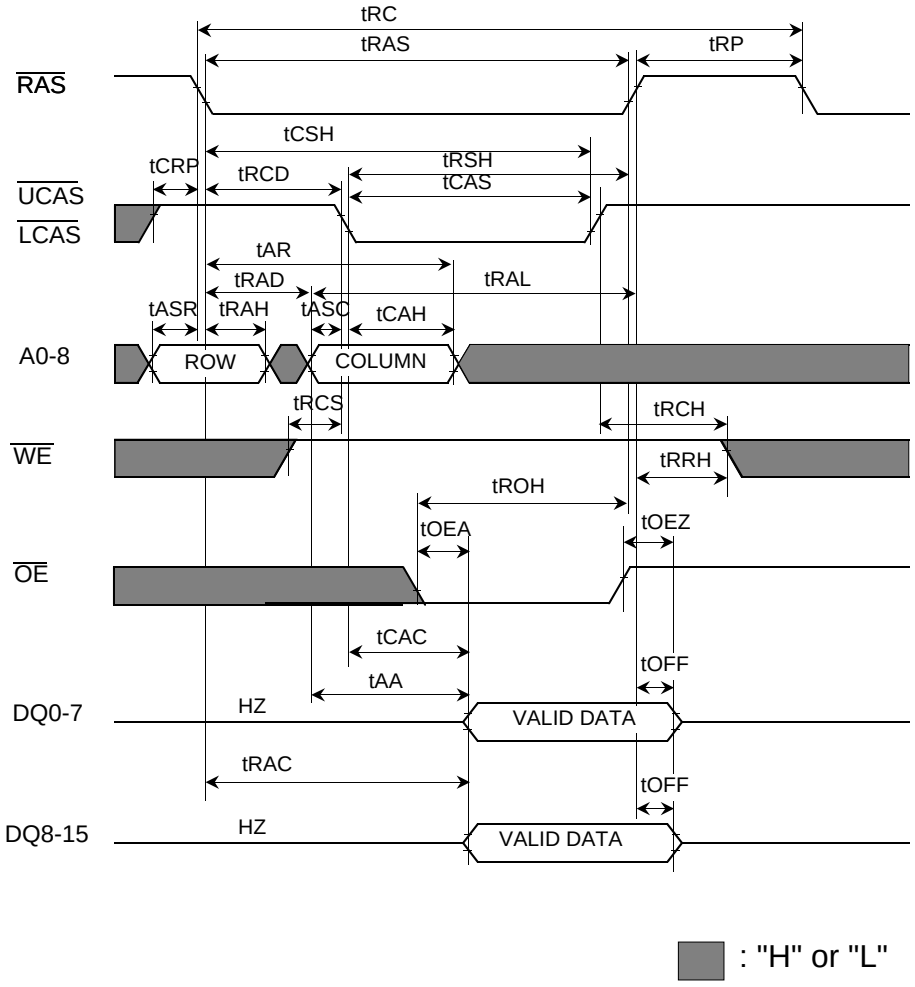
(Vcc=5V±10%, Ta=0~70°C)

Parameter	Symbol	MSM5416258B-28		MSM5416258B-30		MSM5416258B-35		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write command set-up time	t_{WCS}	0	–	0	–	0	–	ns	
Write command hold time	t_{WCH}	5	–	5	–	6	–	ns	
Write command pulse width	t_{WP}	5	–	5	–	6	–	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	21	–	22	–	26	–	ns	
$\overline{OE}$ command hold time	t_{OEH}	5	–	5	–	6	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	5	–	5	–	6	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	7	–	7	–	8	–	ns	
Data to $\overline{CAS}$ delay time	t_{DZC}	0	–	0	–	0	–	ns	
Data to $\overline{OE}$ delay time	t_{DZO}	0	–	0	–	0	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	10
Data-in hold time	t_{DH}	5	–	5	–	6	–	ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	21	–	22	–	26	–	ns	
$\overline{OE}$ to Data-in delay time	t_{OED}	7	–	7	–	8	–	ns	
$\overline{OE}$ "L" to $\overline{CAS}$ "H" lead time	t_{OCH}	5	–	5	–	8	–	ns	
$\overline{CAS}$ "H" to $\overline{OE}$ "L" lead time	t_{CHO}	5	–	5	–	8	–	ns	
Hi-Z command pulse width	t_{OEP}	5	–	6	–	8	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	18	–	18	–	20	–	ns	11
Column address to $\overline{WE}$ delay time	t_{AWD}	24	–	27	–	30	–	ns	11
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	37	–	40	–	45	–	ns	11
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	5	–	6	–	8	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	6	–	6	–	8	–	ns	

Notes:

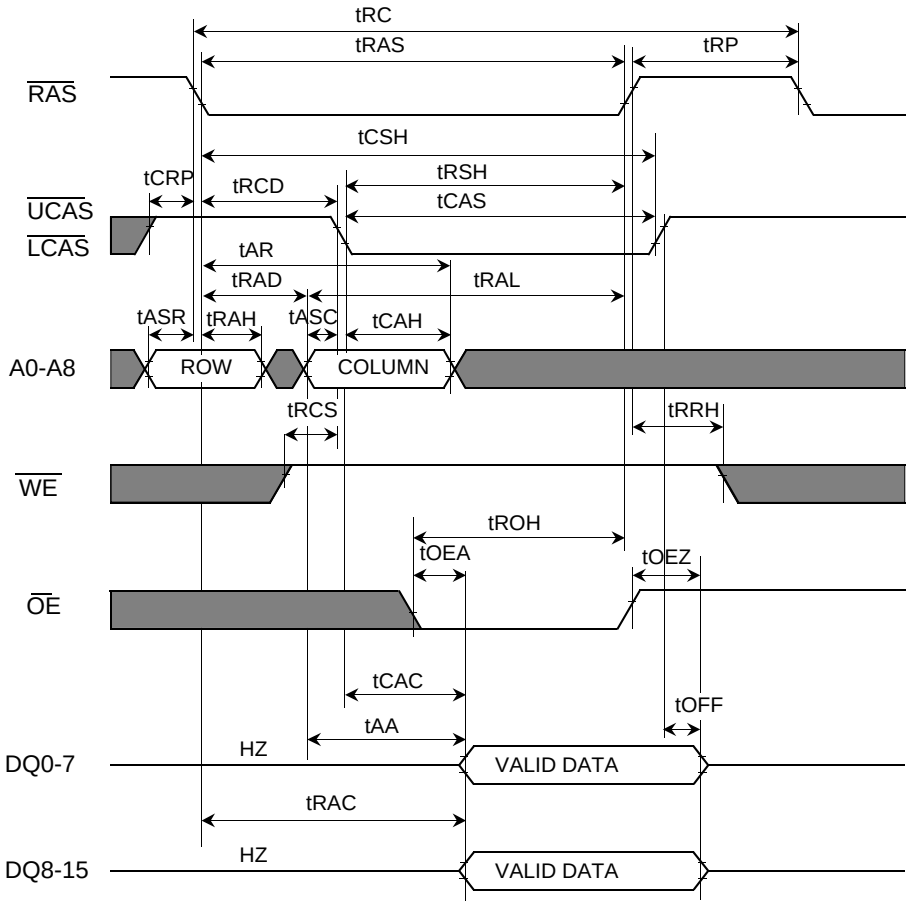
1. All voltages are referenced to Vss.
2. This parameter is dependent upon the cycle rate.
3. This parameter is dependent upon the output loading. Specified values are obtained with the output open.
4. An initial pause of 200μs is required after power-up, followed by any 8$\overline{RAS}$ cycles. (Example: $\overline{RAS}$-only-refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8$\overline{CAS}$ before $\overline{RAS}$ cycles instead of 8$\overline{RAS}$ cycles are required.
5. The AC characteristics assume t_T=5ns.
6. V_{IH} (Min.)and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Data outputs are measured with a load of 30 pF. DOUT reference levels: V_{OH}/V_{OL}=1.8V/1.4V.
8. t_{REZ} (Max.), t_{OFF} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the outputs achieve the open circuit condition and are not referebced to output voltage levels. This parameter is sampled and not 100 % tested.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leadind edge of early write cycles and to $\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycles and read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pins will remain open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (Min.), $t_{CWD} \geq t_{CWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither or the above sets of conditions is satisfied, the condition of the data out is indetermunate.
12. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CDC}.
13. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled by t_{AA}.
14. Input levels at the AC testing are 3.0V/0V.
15. Addresses (A0 - A8) may be changed two times or less while $\overline{RAS}$ =V_{IL}.
16. Addresses (A0 - A8) may be changed once or less while $\overline{CAS}$ =V_{IH} and $\overline{RAS}$ =V_{IL}.
17. This is guaranteed by design. (t_{COH}=t_{CAC} - output transition time). This parameter is not 100 % tested.
18. This parameter is dependent upon the number of address transitions. Specified values are measured with a maximum of two transitions per address cycle in Fast Page Mode.

READ CYCLE ($\overline{RAS}$ output control)



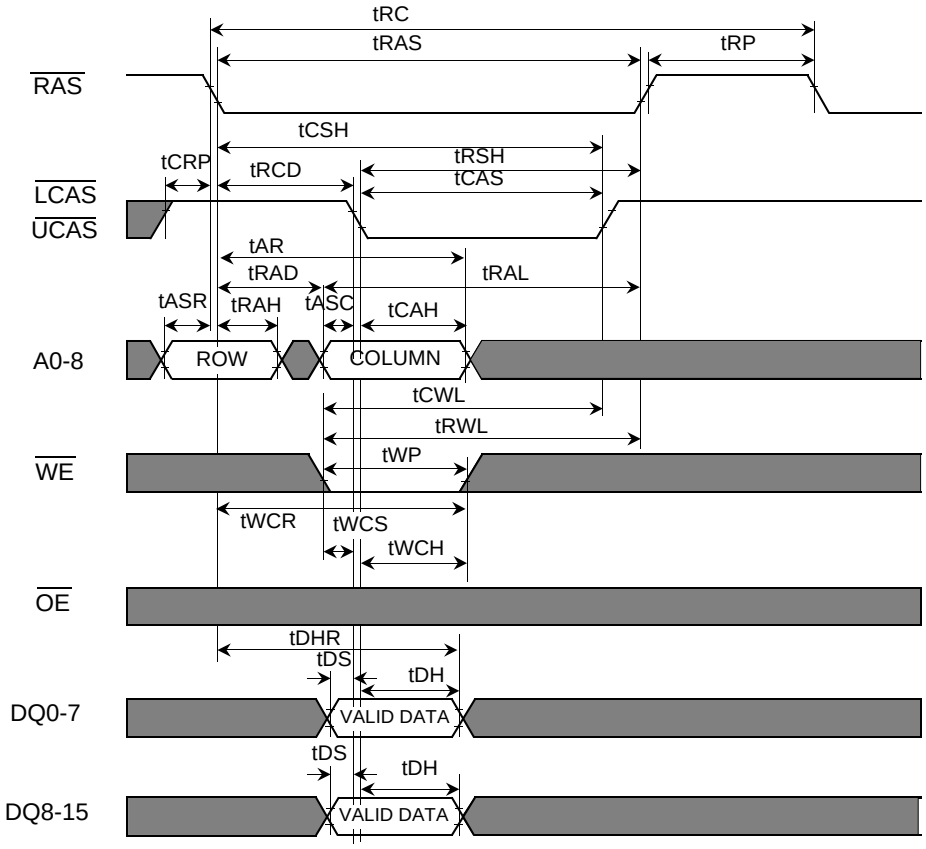
: "H" or "L"

READ CYCLE ($\overline{CAS}$ output control)



: "H" or "L"

EARLY WRITE CYCLE (LCAS and UCAS active)



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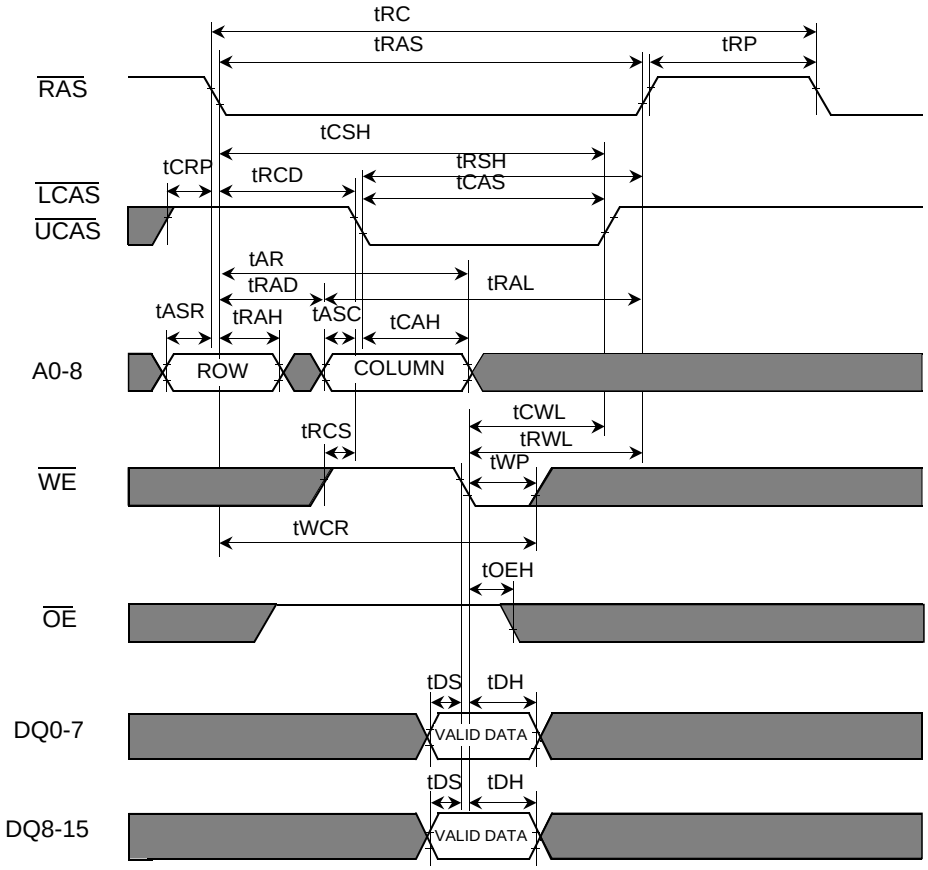
LATE WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)



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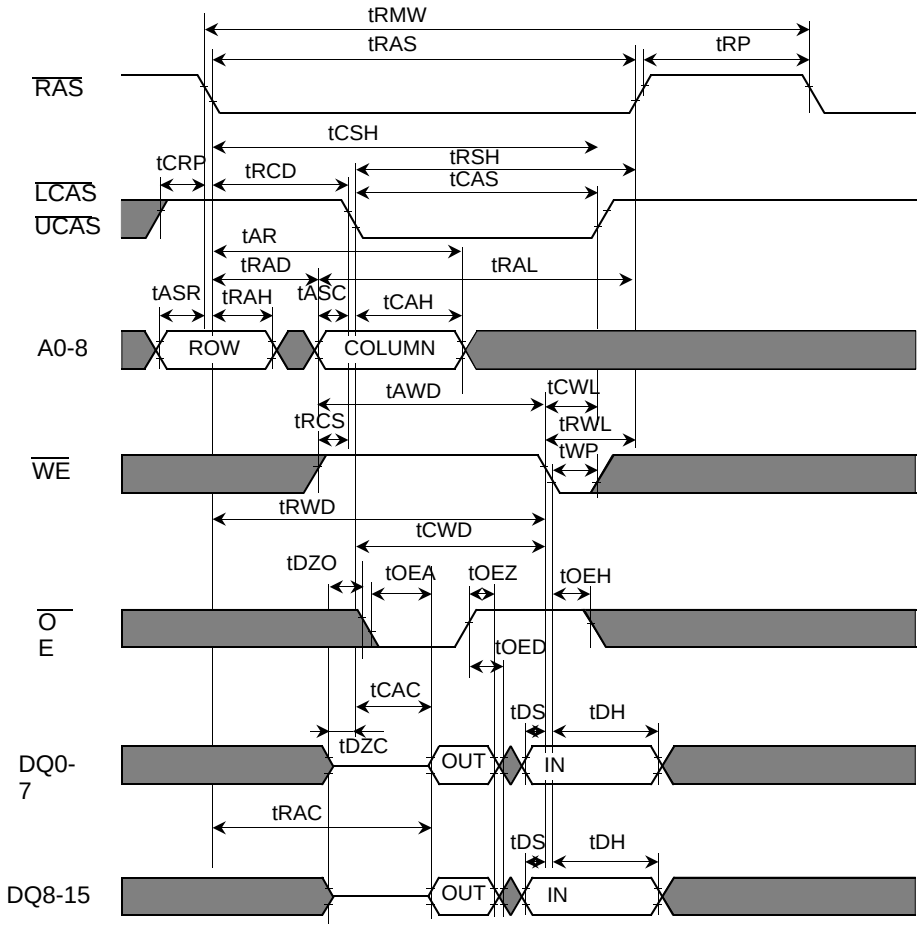
READ MODIFY WRITE CYCLE ($\overline{LCAS}$ and $\overline{UCAS}$ active)



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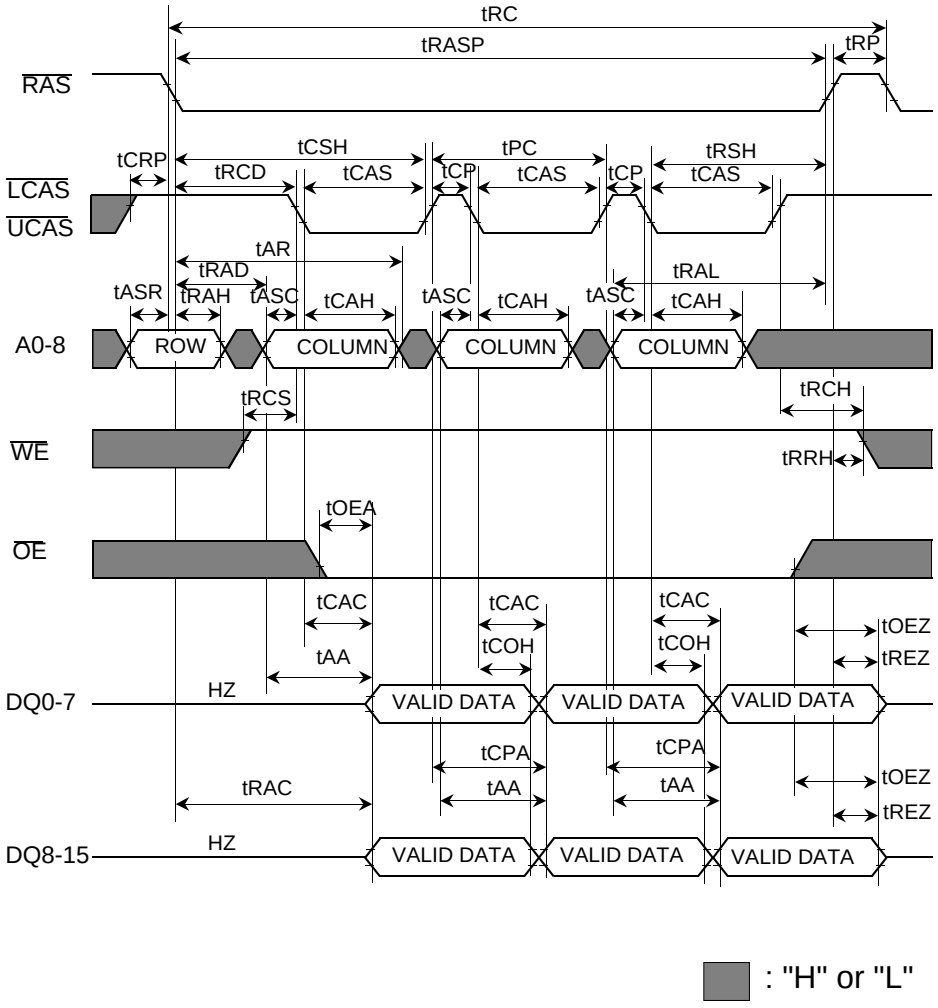
FAST PAGE MODE READ CYCLE with Extended Data Out



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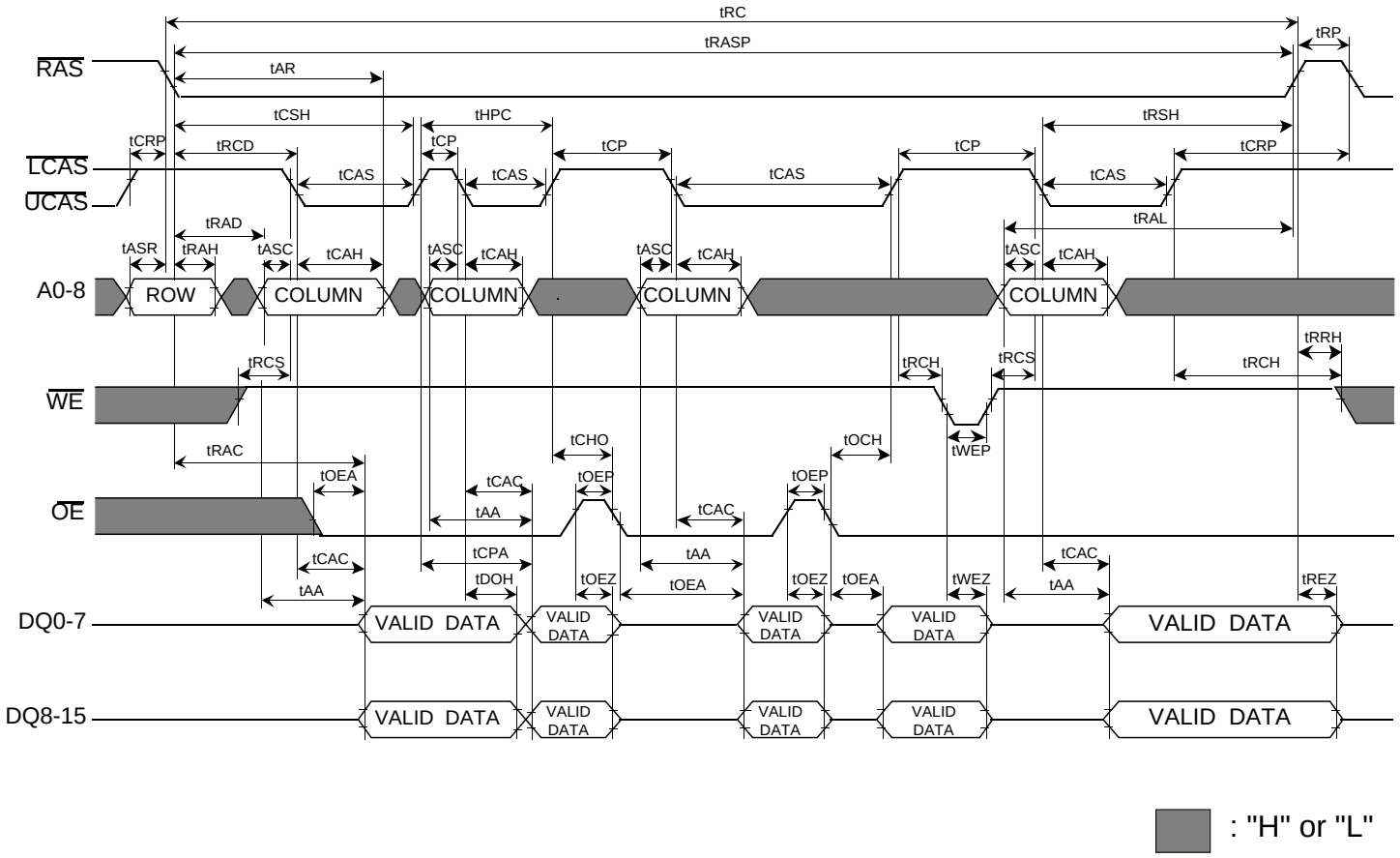
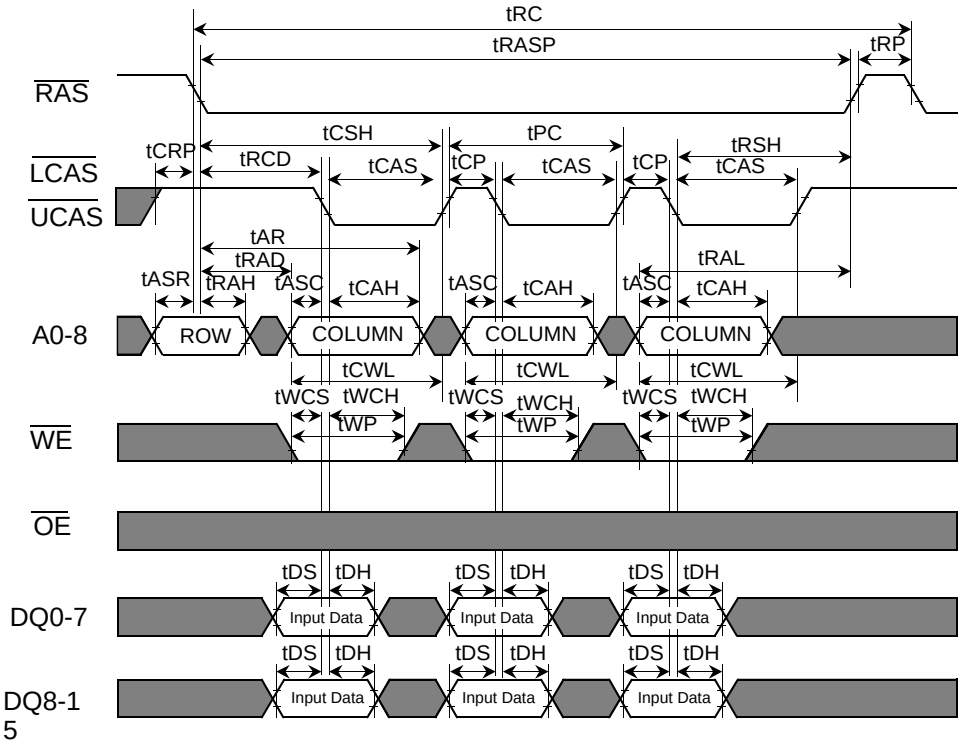
FAST PAGE MODE READ Hi-Z OPERATION

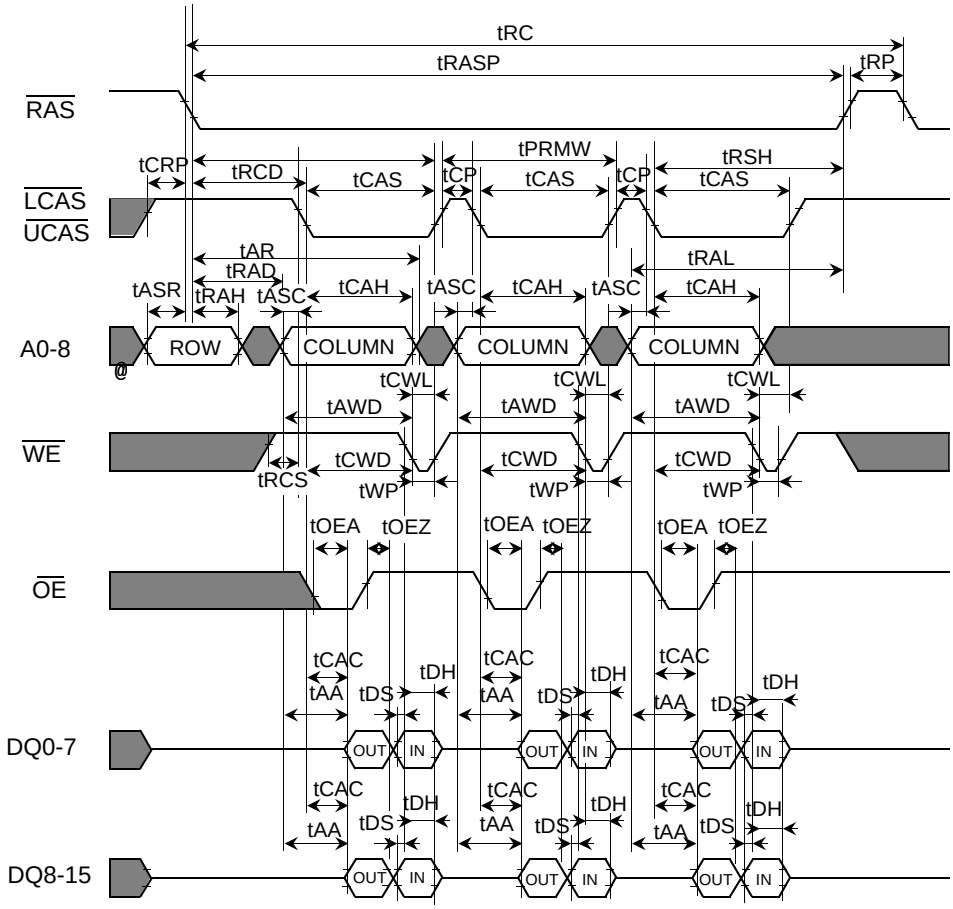


FAST PAGE MODE EARLY WRITE CYCLE



: "H" or "L"

FAST PAGE MODE READ MODIFY WRITE CYCLE



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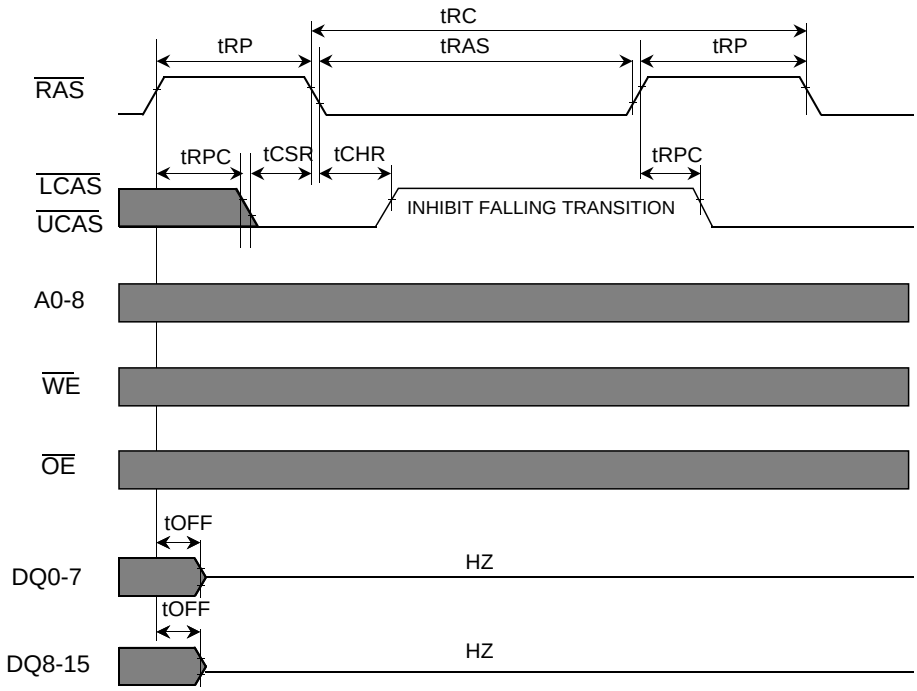
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



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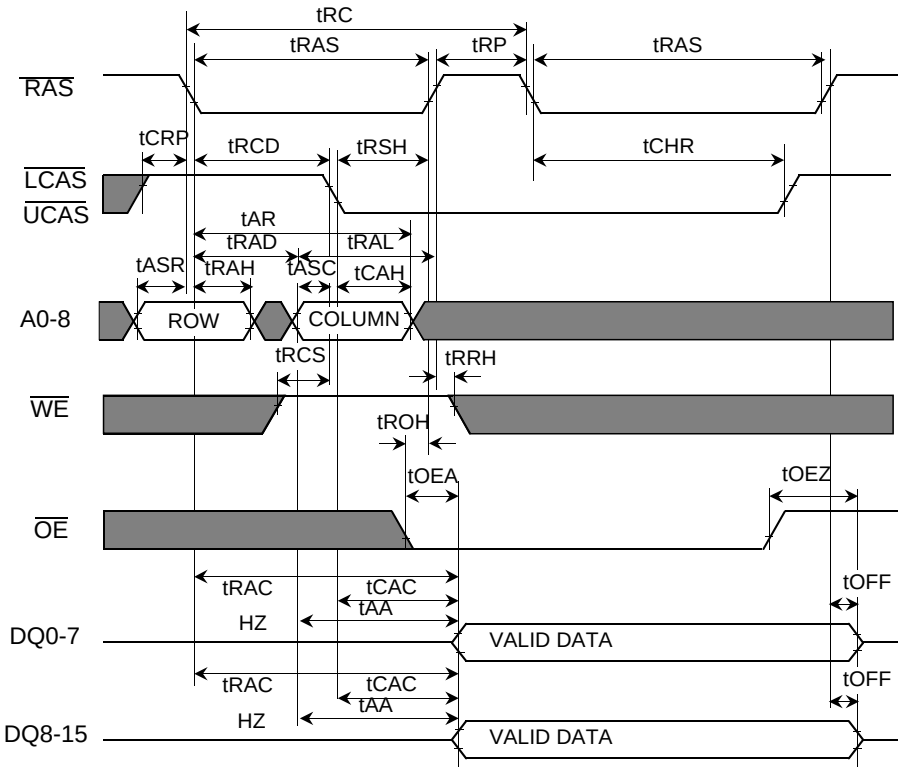
HIDDEN REFRESH CYCLE



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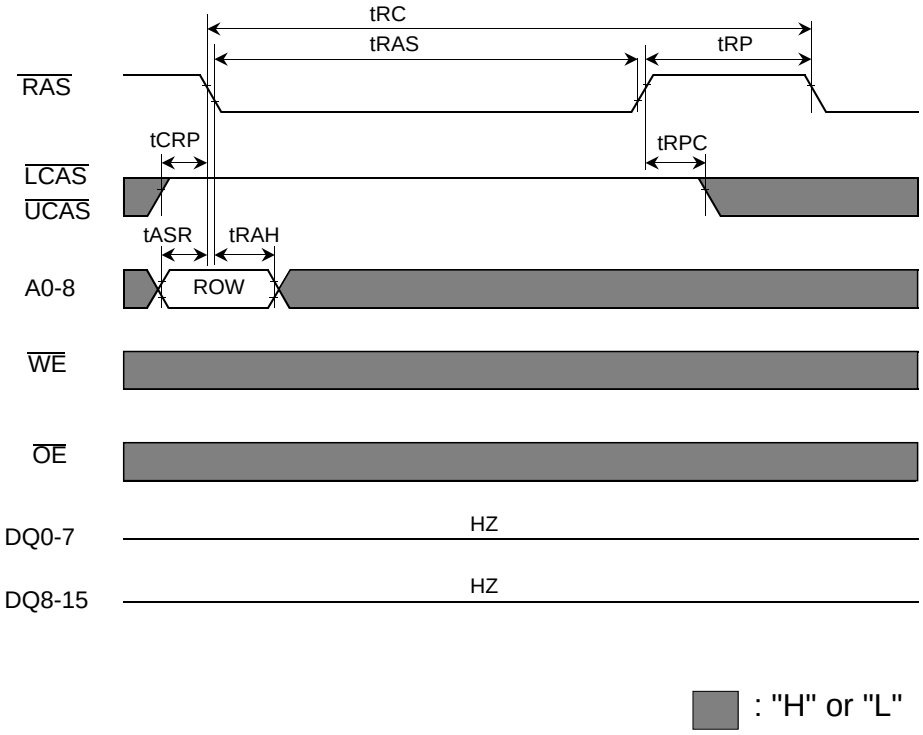
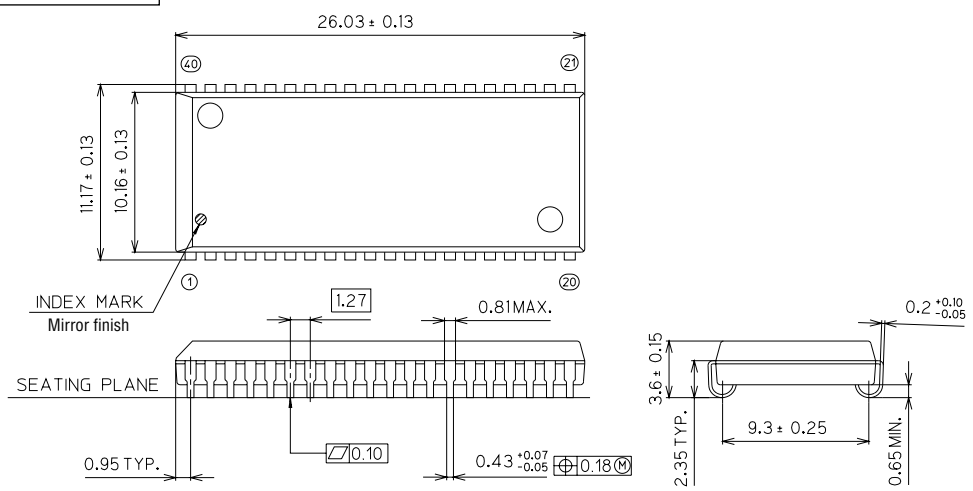
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



PACKAGE OUTLINES AND DIMENSIONS

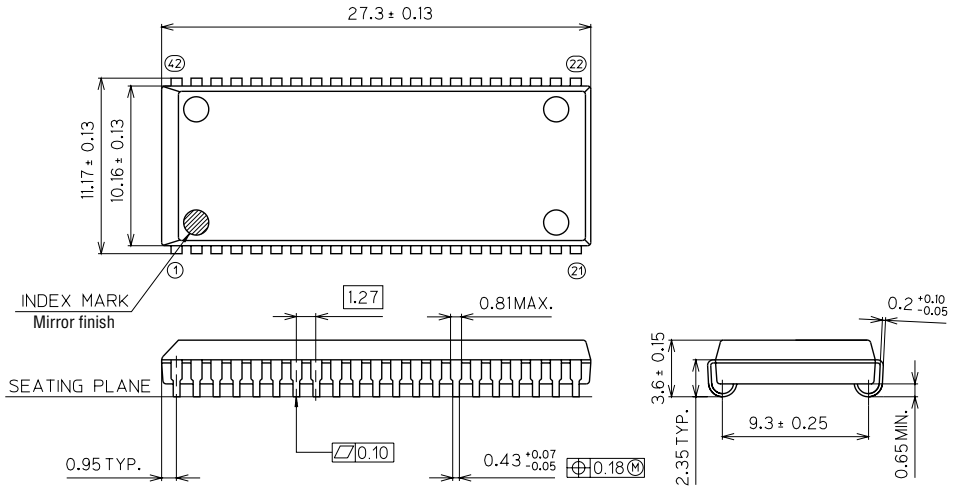
(Unit: mm)

SOJ40-P-400-1.27



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	1.70 TYP.

SOJ42-P-400-1.27



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	1.86 TYP.