OKI Semiconductor

MSM54V12222A

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262,214 Words × 12 Bits FIELD MEMORY

GENERAL DESCRIPTION

The OKI MSM54V12222A is a high performance 3M bits, 256K X 12 bits, Field Memory especially designed for high-speed serial access applications such as HDTVs, conventional NTSC TVs, VTRs, digital movies and Multi-media systems. MSM54V12222A is a FRAM for wide or low end use as general commodity TVs and VTRs, exclusively. MSM54V12222A is not designed for the other use or high end use as medical systems, professional graphics systems require long time picture storage, data storage systems and others. More than two MSM54V12222As can be cascaded directly without any delay devices among the MSM54V12222As. (Cascading of MSM54V12222A provides larger storage depth or a longer delay.)

Each of the 12-bits planes has separate serial write and read ports that employ independent control clocks to support asynchronous read and write operations. Different clock rates are also supported that allow alternate data rates between write and read data streams.

The MSM54V12222A provides high speed FIFO, First-In First-Out, operation without external refreshing: MSM54V12222A refreshes its DRAM storage cells automatically, so that it appears fully static to the users.
Moreover, fully static type memory cells and decoders for serial access enable the serial access operation refresh free, so that serial read and/or write control clock can be halted high or low for any time as long as the power is on. Internal conflicts of any memory access and refreshing operation are prevented by special arbitration logic.

The MSM54V12222A's function is simple like that of a digital delay device whose delay-bit-length is easily set by reset timing. The delay length, number of read delay clocks between write and read, is determined by externally controlled write and read reset timings.

Additional SRAM serial registers, or line buffers, for the initial access of 256X12 bits enable high speed first-bit-access with no clock delay just after the write or read reset timings.

In addition to cascade capability, MSM54V12222A has write mask function or input enable function (IE), and read- data skipping function or output enable function(OE). The differences between write enable (WE) and input enable (IE), and between read enable (RE) and output enable (OE) are that WE and RE can stop serial write/read address increments but IE and OE can not stop the increment when write/read clocking is continuously applied to MSM54V12222A. The input enable (IE) function allows the user to write into selected locations of the memory only, leaving the rest of the memory contents unchanged. This facilitates data processing as "picture in picture" on a TV screen simply.

The MSM54V12222A is similar in operation and functionality to OKI 1M bits Field memory MSM51V4222C and 2M bits Field memory MSM51V8222A. Three MSM51V4222Cs or one MSM51V4222C plus one MSM51V8222A can be replaced simply by one MSM54V12222A.

FEATURES

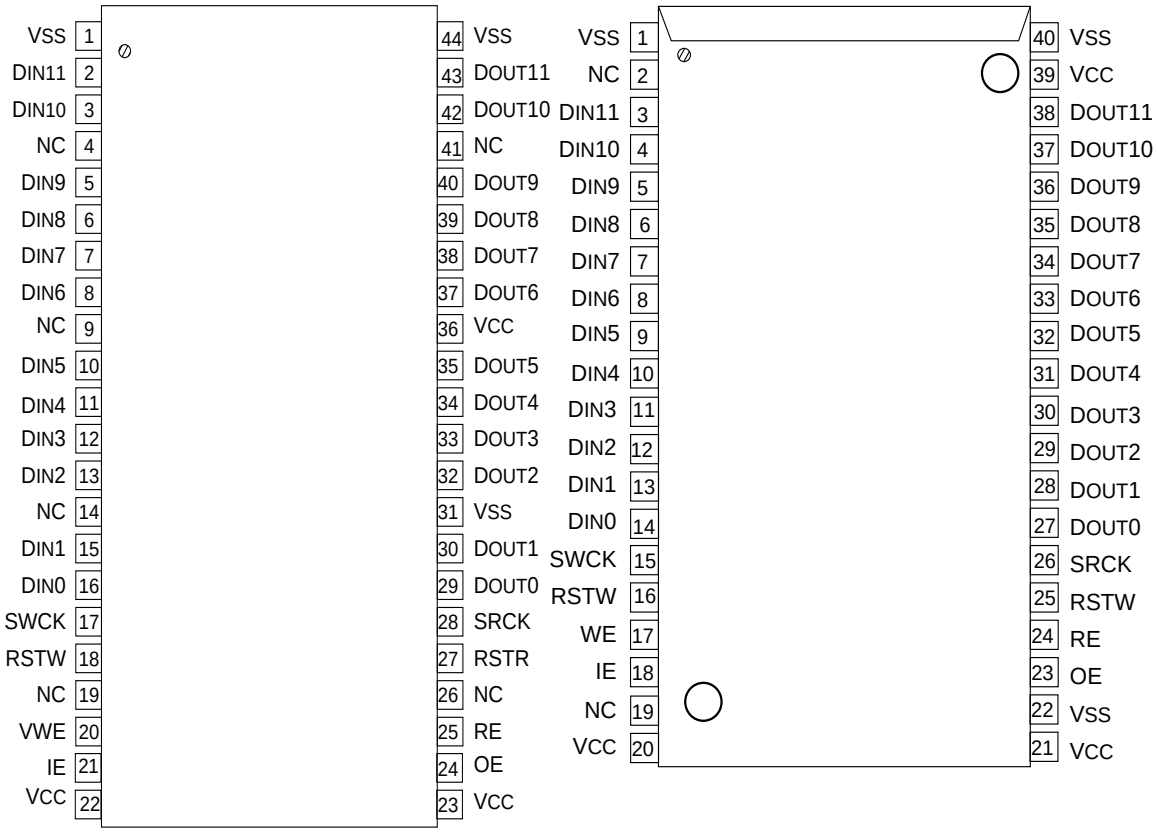
- Signale power supply : 3.3V±0.3V
- 512 Rows X 512 Column X 12 bits
- Fast FIFO (First-In First-Out) Operation
- High Speed Asynchronous Serial Access
- Read/Write Cycle Time 30 ns/40 ns
- Access Time 30 ns/35 ns
- Direct Cascading Capability
- Write Mask Function (Input Enable Control)
- Data Skipping Function (Output Enable Cotrol)
- Self Refresh (No refresh control is required)
- Packageoptions:

  44Pin 400mil plastic TSOP (Type II) (TSOP II 44-P-400-0.80-K) (Product:MSM54V12222A-xxTS-K)
  40Pin 400mil Plastic SOJ (SOJ40-P-400-1.27) (Product:MSM54V12222A-xxJS)
  xx indicates speed rank.

PRODUCT FAMILIES

Family	Access Time (Max.)	Cycle Time (Min.)	Package
MSM54V12222A-30-TS-K	30 ns	30 ns	400 mil 44-pin TSOP (II)
MSM54V12222A-40-TS-K	35 ns	40 ns	
MSM54V12222A-30JS	30 ns	30 ns	400 mil 40-pin SOJ
MSM54V12222A-40JS	35 ns	40 ns	

PIN CONFIGURATION (TOP VIEW)

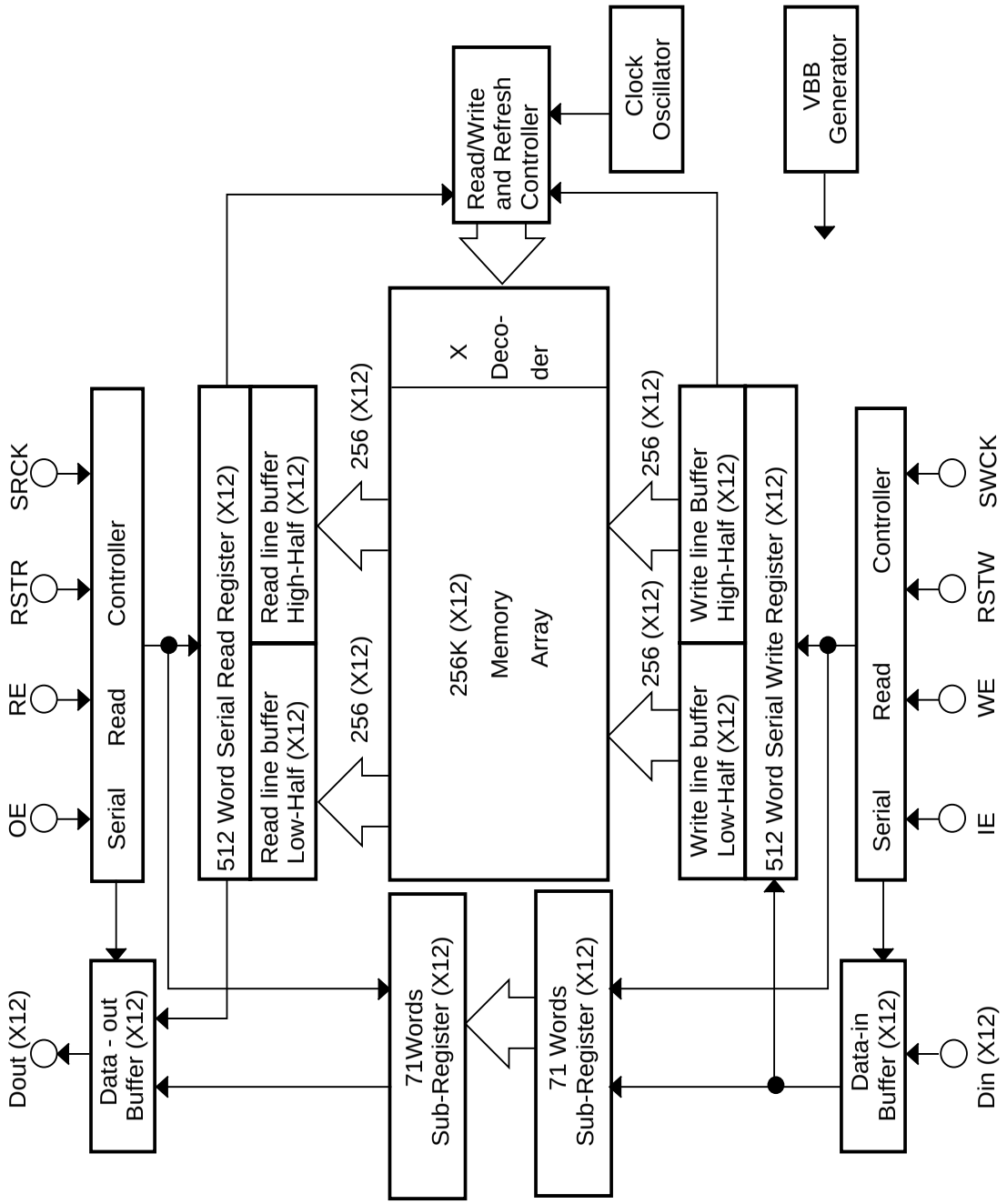


44PIN Plastic TSOP (II)
(K Type)

40PIn Plastick SOJ

Pin Name	Function
SRCK	Serial Read Clock
SWCK	Serial Write Clock
WE	Write Enable
RE	Read Enable
IE	Input Enable
OE	Output Enable
RSTW	Write Reset Clock
RSTR	Read Reset Clock
Din0-11	Data Input
Dout0-11	Data Output
Vcc	Power Supply(3.3V)
Vss	Ground (0V)
NC	No Connection

BLOCK DIAGRAM



OPERATION

Write Operation

The write operation is controlled by tree clocks, SWCK, RSTW, and WE. Write operation is accomplished by cycling SWCK and holding WE high after write address pointer reset operation or RSTW.

Each write operation, which begins after RSTW, must contain at least 80 active write cycles, i.e. SWCK cycles while WE is high. To transfer the last data, which at that time are stored in the serial data registers attached to DRAM array, to the DRAM array, an RSTW operation is required after the last SWCK cycle.

Note that every write timing of MSM54V12222A is delayed by one clock compared wih read timings for easy cascading without any interface delay devices.

Write Reset : RSTW

The first positive transition of SWCK after RSTW going high resets the write address counters to zero. RSTW setup and hold times are referenced to the rising edge of SWCK. Because the write reset function is solely controlled by SWCK rising edge after high level of RSTW, the states of WE and IE are don't care in the write reset cycle.

Before RSTW may be brought high again for a further reset operation, it must have been low for at least two SWCK cycles.

Data Inputs : Din0-11
Write Clock : SWCK

The SWCK latches the input data on chip when WE is high and also increments the internal write address pointer. Data-in setup time, tDS and hold time, tDH, are referenced to the rising edge of SWCK.

Write Enable : WE

WE is used for data write enable/disable control. WE high level enables the input, and WE low level disables the input and holds the internal write address pointer. There are no WE disable time (low) and WE enable time (high) restrictions because MSM54V12222A is fully static operation as long as power is on. Note that WE setup and hold times are referenced to the rising edge of SWCK.

Input Enable : IE

IE is used to enable/disable writing into memory. IE high level enables writing. The internal write address pointer is always incremented by cycling SWCK regardless of IE level. Note that IE setup and hold times are referenced to the rising edge of SWCK.

Read Operation

The read operation is controlled by tree clocks, SRCK, RSTR, and RE. Read operation is accomplished by cycling SRCK and holding RE high after read address pointer reset operation or RSTR. Each read operation, which begins after RSTR, must contain at least 80 active read cycles, i.e. SRCK cycles while RE is high.

Read Reset : RSTR

The first positive transition of SRCK after RSTR going high resets the read address counters to zero. RSTR setup and hold times are referenced to the rising edge of SRCK. Because the read reset function is solely controlled by SRCK rising edge after high level of RSTR, the states of RE and RE are don't care in the read reset cycle.
Before RSTR may be brought high again for a further reset operation, it must have been low for at least *two SRCK cycles.

Data Out : Dout0-11
Read Clock : SRCK

Data is shifted out of the data registers triggered by the rising edge of SRCK when RE is high during a read operation. The SRCK input increments the internal read address pointer when RE is high.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required). Data out is the same polarity as data in. The output becomes valid after the access time interval tAC that begins with the rising edge of SRCK. *There are no output valid time restriction on MSM54V12222A.

Read Enable : RE

The function of RE is gating of the SRCK clock, for incrementing the read pointer. When RE is high before the rising edge of SRCK, the read pointer is incremented. When RE is low, the read pointer is not incremented. RE setup times (tRENS and tRDSS) and RE hold times (tRENH and tRDSH) are referenced to the rising edge of the SRCK clock.

Output Enable : OE

OE is used to enable/disable the outputs. OE high level enables the outputs. The internal read address pointer is always incremented by cycling SRCK regardless of OE level. Note that OE setup and hold times are referenced to the rising edge of SRCK.

Power-up and Initialization

On Powering up, the device is designed to begin proper operation after at least 100 us after VCC has stabilized to a value within the range of recommended operating conditions. After this 100 us stabilization interval, the following initialization sequence must be performed.

Because the read and write address counters are not valid after power-up, a minimum of 80 dummy write operations (SWCK cycles) and read operations (SRCK cycles) must be performed, followed by an RSTW operation and an RSTR operation, to properly initialize the write and the read address pointer. Dummy write cycles/RSTW and dummy read cycles/RSTR may occur simultaneously.

If these dummy read and write operations start while VCC and/or the substrate voltage have not stabilized, it is required to perform an RSTR operation plus a minimum of 80 SRCK cycles plus another RSTR operation, and an RSTW operation plus a minimum of 80 SRCK cycles plus another RSTW operation to properly initialize read and write address pointers.

Old/New Data Access

There must be minimum delay of 600 SWCK cycles between writing into memory and reading out from memory if reading from the first field starts with an RSTR operation, before the start of writing the second field, (before the next RSTW operation), then the data just written in will be read out.

The start of reading out the first field of data may be delayed past the beginning of writing in the second field of data for as many as 70 SWCK cycles. If the RSTR operation for the first field read-out occurs less than 70 SWCK cycles after the RSTW operation for the second field write-in, then the internal buffering of the device assures that the first field will still be read out. The first field of data that is read out while the second field of data is written is called "old data".

In order to read out "new data", i.e., the second field written in, the delay between an RSTW operation and an RSTR operation must be at least 600 SRCK cycles. If the delay between RSTW and RSTR operations is more than 71 but less than 600 cycles, then the data read out will be undetermined. It may be "old data" or "new" data or a combination of old and new data. Such a timing should be avoided.

Cascade Operation

The MSM5412222A has been designed to allow easy cascading of multiple memory devices, in order to obtain a higher storage depth or a longer delay than can be achieved with only one memory device.

ELECTRICAL CHARACTERISTICS

- Absolute Maximum Rating

Parameter	Symbol	Conditions	Rating	Unit
Input Output Voltage	V_T	at Ta = 25°C, Vss	–1.0~4.6	V
Output Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{opr}	—	0~70	°C
Storage Temperature	T_{stg}	—	–55~150	°C

- Recommended /peration Condition

Parameter	Symbol	MIN	TYP	MAX	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Power Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	Vcc	Vcc+0.3	V
Input Low Voltage	V_{IL}	–0.3	0	0.8	V

- DC Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input Leakage Current	I_{LI}	0<Vi<+0.3,Other Pins Tested at V=0V	-10	10	µA
Output Leakage Current	I_{LO}	0<Vo<Vcc	-10	10	µA
Output "H" Level Voltage	V_{OH}	I_{OH}=-1mA	2.4	—	V
Output "L" Level Voltage	V_{OL}	I_{OL}=2mA	—	0.4	V
Operating Current	I_{CC1}	Minimum Cycle Time,Output Open	—	60	mA
Standby Current	I_{CC2}	Input Pin=V_{IH}/V_{IL}	—	3	mA

- Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	MAX	Unit
Input Capacitance (Din, SWCK, SRCK, RSTW, RSTR, WE, RE, IE, OE)	Ci	7	pF
Output Capacitance (Dout)	Co	10	pF

AC CHARACTERISTICS

(Vcc = 3.3V±0.3V, Ta = 0~70°C)

Parameter	Symbol	MSM54V12222A-30		MSM54V12222A-40		Unit
		MIN	MAX	MIN	MAX	
Access Time from SRCK	t_{AC}	—	30	—	35	ns
Dout Hold Time from SRCK	t_{DDCK}	6	—	6	—	ns
Dout Enable Time from SRCK	t_{DECK}	6	30	6	35	ns
SWCK "H" Pulse Width	t_{WSWH}	12	—	17	—	ns
SWCK "L" Pulse Width	t_{WSWL}	12	—	17	—	ns
Input Data Setup Time	t_{DS}	5	—	5	—	ns
Input Data Hold Time	t_{DH}	6	—	6	—	ns
WE Enable Setup Time	t_{WENS}	0	—	0	—	ns
WE Enable Hold Time	t_{WENH}	5	—	5	—	ns
WE Disable Setup Time	t_{WDSS}	0	—	0	—	ns
WE Disable Hold Time	t_{WDSH}	5	—	5	—	ns
IE Enable Setup Time	t_{IENS}	0	—	0	—	ns
IE Enable Hold Time	t_{IENH}	5	—	5	—	ns
IE Disable Setup Time	t_{IDSS}	0	—	0	—	ns
IE Disable Hold Time	t_{IDSH}	5	—	5	—	ns
WE "H" Pulse Width	t_{WWEH}	10	—	10	—	ns
WE "L" Pulse Width	t_{WWEL}	10	—	10	—	ns
IE "H" Pulse Width	t_{WIEH}	10	—	10	—	ns
IE "L" Pulse Width	t_{WIEL}	10	—	10	—	ns
RSTW Setup Time	t_{RSTWS}	0	—	0	—	ns
RSTW Hold Time	t_{RSTWH}	10	—	10	—	ns
SRCK "H" Pulse Width	t_{WSRH}	12	—	17	—	ns
SRCK "L" Pulse Width	t_{WSRL}	12	—	17	—	ns
RE Enable Setup Time	t_{RENS}	0	—	0	—	ns
RE Enable Hold Time	t_{RENH}	5	—	5	—	ns
RE Disable Setup Time	t_{RDSS}	0	—	0	—	ns
RE Disable Hold Time	t_{RDSH}	5	—	5	—	ns
OE Enable Setup Time	t_{OENS}	0	—	0	—	ns
OE Enable Hold Time	t_{OENH}	5	—	5	—	ns
OE Disable Setup Time	t_{ODSS}	0	—	0	—	ns
OE Disable Hold Time	t_{ODSH}	5	—	5	—	ns
RE "H" Puls Width	t_{WREH}	10	—	10	—	ns
RE "L" Puls Width	t_{WREL}	10	—	10	—	ns
OE "H" Puls Width	t_{WOEH}	10	—	10	—	ns
OE "L" Puls Width	t_{WOEL}	10	—	10	—	ns
RSTR Setup Time	t_{RSTRS}	0	—	0	—	ns
RSTR Hold Time	t_{RSTRH}	10	—	10	—	ns
SWCK Cycle Time	t_{SWC}	30	—	40	—	ns
SRCK Cycle Time	t_{SRC}	30	—	40	—	ns
Trandition Time (Rise and Fall)	t_T	3	30	3	30	ns

NOTE

1. Input signal reference levels for the parameter measurement are VIH=3.0V and VIL=0V. The transition time tT is defined to be a transition time that signal transfers between VIH=3.0V and VIL=0V.

2. AC measurements assume tT=3ns.

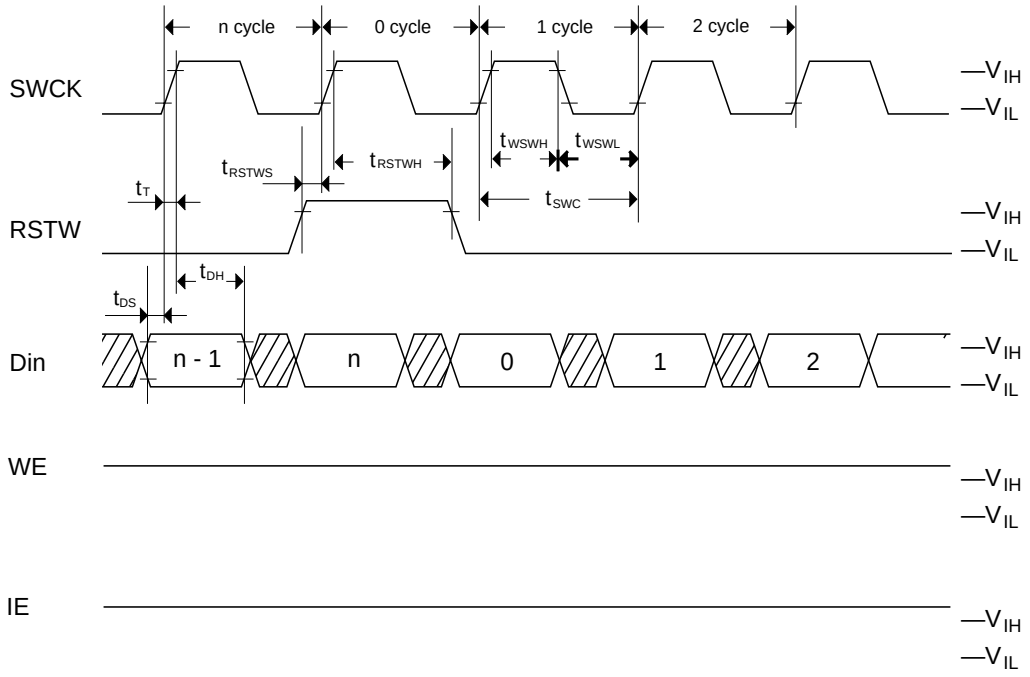
3. Read address must have more than 600 address delay than write address in every cycle when asynchronous read/write is performed.

4. Read must have more than 600 address delay than write in order to read the data written in a current series of write cycle which has been started last write reset cycle : this is called "new data read".
When read has less than 70 address delay than write, the read data are the data written in a previous series of write cycle which had been written before last write reset cycle: this is called "old data read".

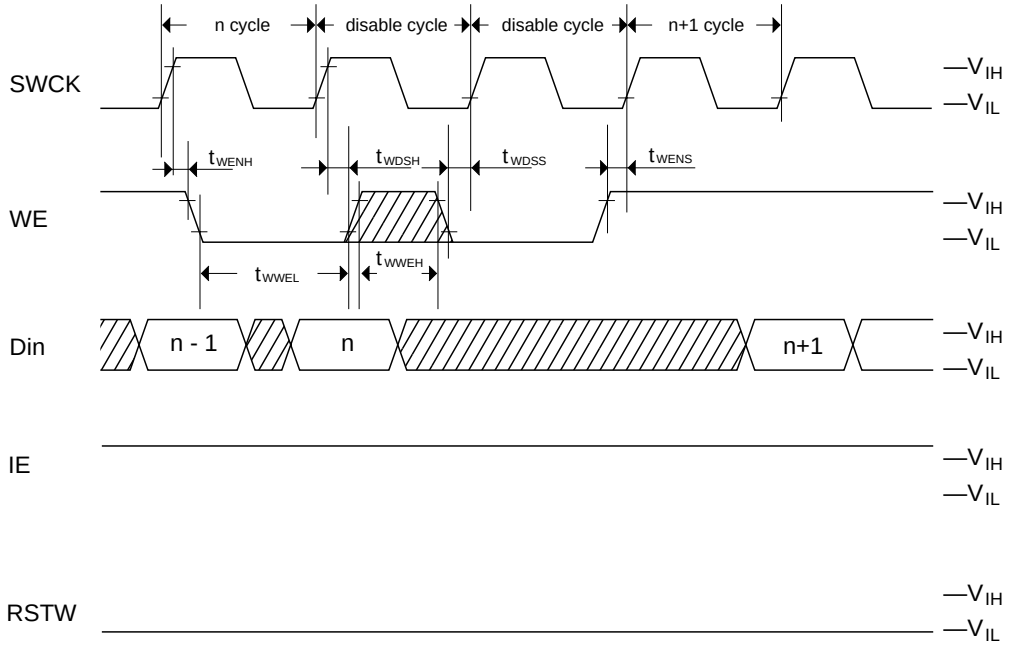
5. When the read address delay is between more than 71 and less than 599, read data will be undetermined. However, normal write is achieved in this address condition.

6. Outputs are measured with a load equivalent to 1 TTL load and 30pF.
Output reference levels are VOH=2.0V and VOL=0.8V.

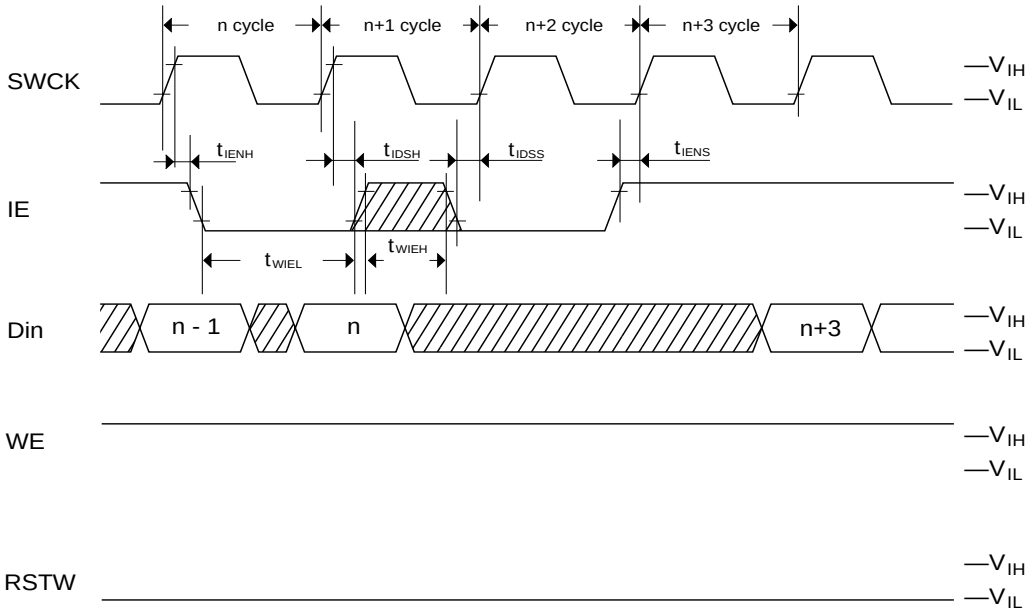
WRITE CYCLE TIMING (Write Reset)



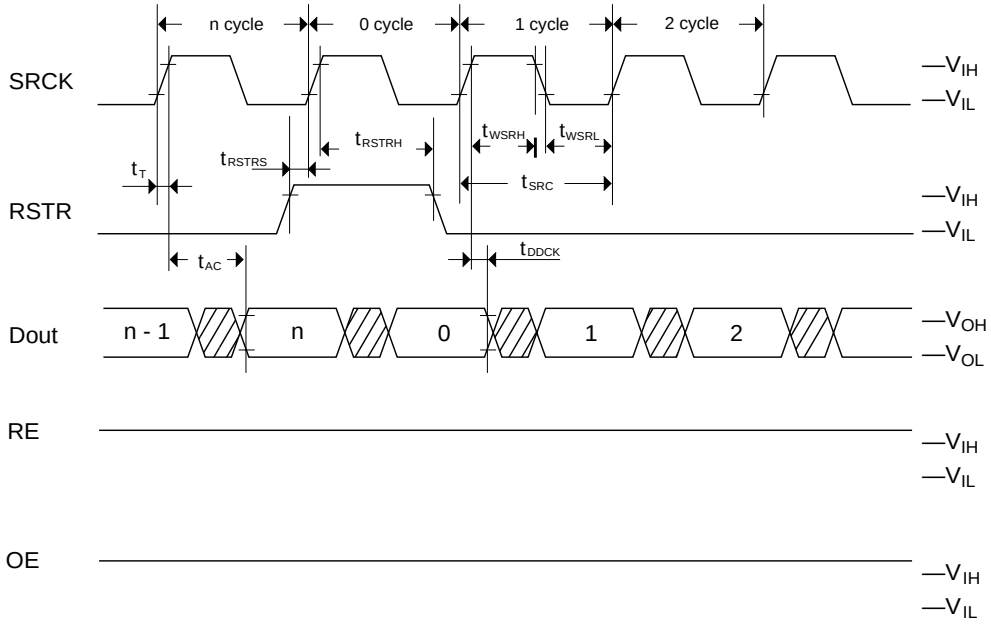
WRITE CYCLE TIMING (Write Enable)



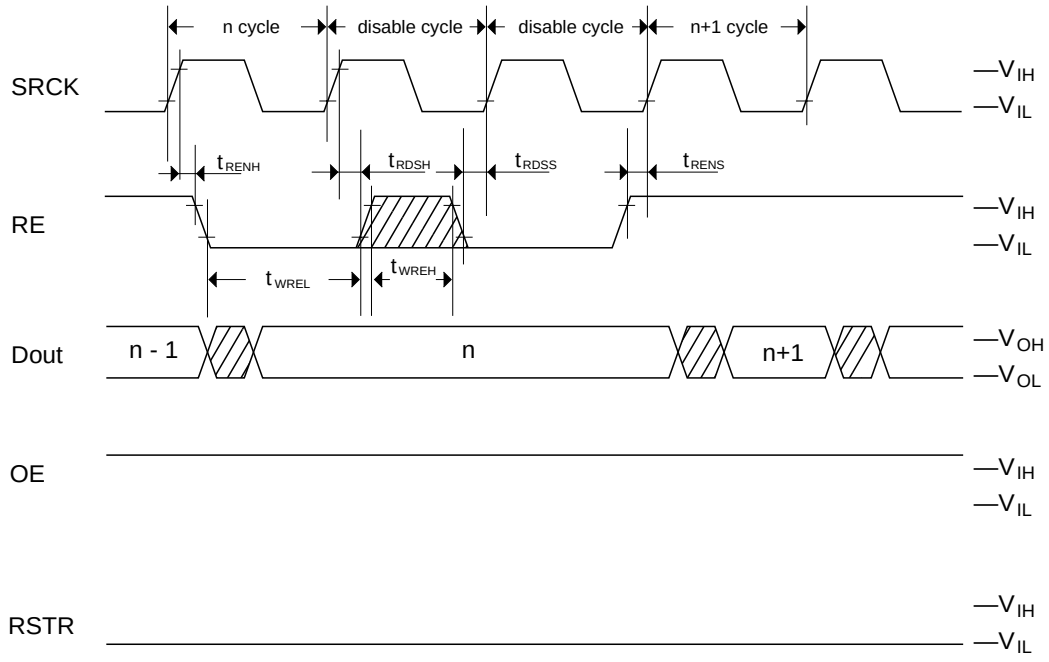
WRITE CYCLE TIMING (Input Enable)



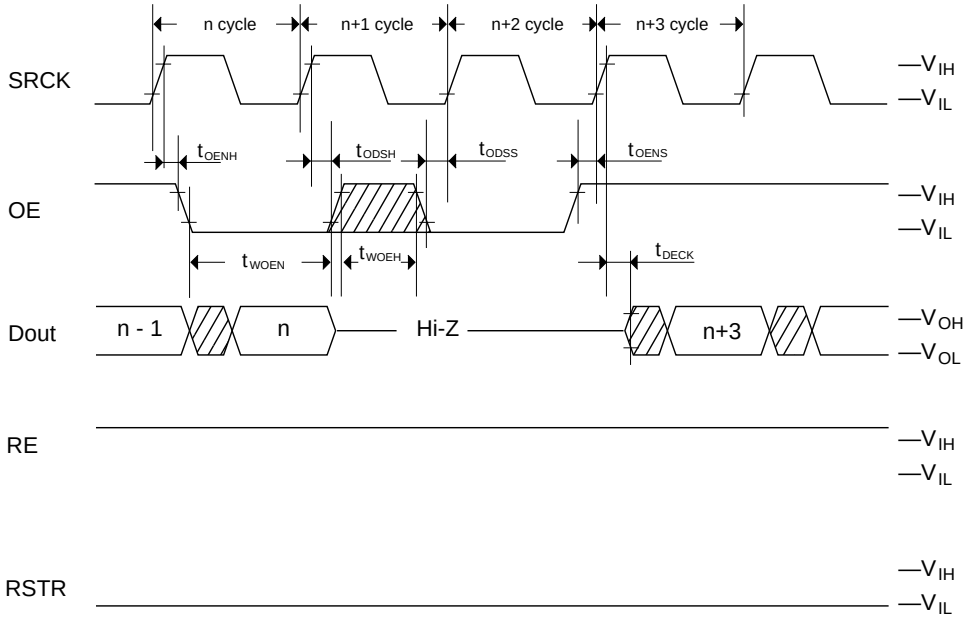
READ CYCLE TIMING (Read Reset)



READ CYCLE TIMING (Read Enable)



READ CYCLE TIMING (Output Enable)



NOTICE

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