PRELIMINARY

OKI Semiconductor

REVISION-2 1996.11.2

MSM54V16258A/SL

262,144-Word x 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM54V16258A/SL is a 262,144-word x 16-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM54V16258A/SL achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM54V16258A/SL is available in a 40-pin plastic SOJ or 44/40-pin plastic TSOP.
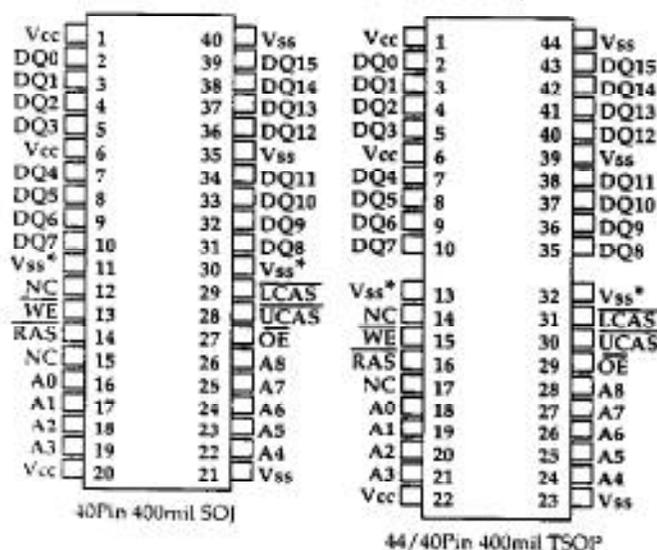
FEATURES

*   262,144-word × 16-bit configuration
*   Single 3.3V power supply, ±0.3V tolerance
*   Input   : LVTTL compatible, low input capacitance
*   Output : LVTTL compatible, 3-state
*   Refresh : 512 cycles/8ms
*   Fast page mode with EDO, read modify write capability
*   Byte wide control: 2 $\overline{CAS}$ control
* $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$ only refresh capability
* $\overline{CAS}$ before $\overline{RAS}$ self-refresh capability (SL version)
*   Package options:
    40-Pin 400 mil plastic SOJ   (SOJ40-P-400)   (Product : MSM54V16258A/SL-xxJS)
    44/40-Pin 400 mil plastic TSOP (TSOP44/40-P-400/0.8-K) (Product : MSM54V16258A/SL-xxTS-K)
    xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)		Power Dissipation
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}	t_{RC}	t_{HPC}	
MSM54V16258A/SL-40	40ns	22ns	10ns	10ns	80ns	15ns	504mW
MSM54V16258A/SL-45	45ns	24ns	12ns	12ns	90ns	17ns	450mW

PIN CONFIGURATION (TOP VIEW)

40Pin 400mil SOJ

Vcc	1	40	Vss
DQ0	2	39	DQ15
DQ1	3	38	DQ14
DQ2	4	37	DQ13
DQ3	5	36	DQ12
Vcc	6	35	Vss
DQ4	7	34	DQ11
DQ5	8	33	DQ10
DQ6	9	32	DQ9
DQ7	10	31	DQ8
Vss*	11	30	Vss*
NC	12	29	$\overline{LCAS}$
$\overline{WE}$	13	28	$\overline{UCAS}$
$\overline{RAS}$	14	27	$\overline{OE}$
NC	15	26	A8
A0	16	25	A7
A1	17	24	A6
A2	18	23	A5
A3	19	22	A4
Vcc	20	21	Vss

44/40Pin 400mil TSOP

Vcc	1	44	Vss
DQ0	2	43	DQ15
DQ1	3	42	DQ14
DQ2	4	41	DQ13
DQ3	5	40	DQ12
Vcc	6	39	Vss
DQ4	7	38	DQ11
DQ5	8	37	DQ10
DQ6	9	36	DQ9
DQ7	10	35	DQ8
Vss*	13	32	Vss*
NC	14	31	$\overline{LCAS}$
$\overline{WE}$	15	30	$\overline{UCAS}$
$\overline{RAS}$	16	29	$\overline{OE}$
NC	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
Vcc	22	23	Vss

| Pin Names	Function
A0-A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$, $\overline{UCAS}$	Column Address Strobe
DQ0-15	Data-Input/ Data-Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply (3.3V)
Vss	Ground (0V)
NC	No Connection
Vss*	Ground (0V) : see Note2

Note1 :
The same power supply voltage must be provided to every Vcc pin, and the same GND voltage level must be provided to every Vss pin.

Note2 :
For improved signal integrity, it is recommended to connect the Vss* pins, pin 11 and 31(SOJ) or pin 13 and 32(TSOP) to GND : the pins are electrically connected to internal GND.

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BLOCK DIAGRAM
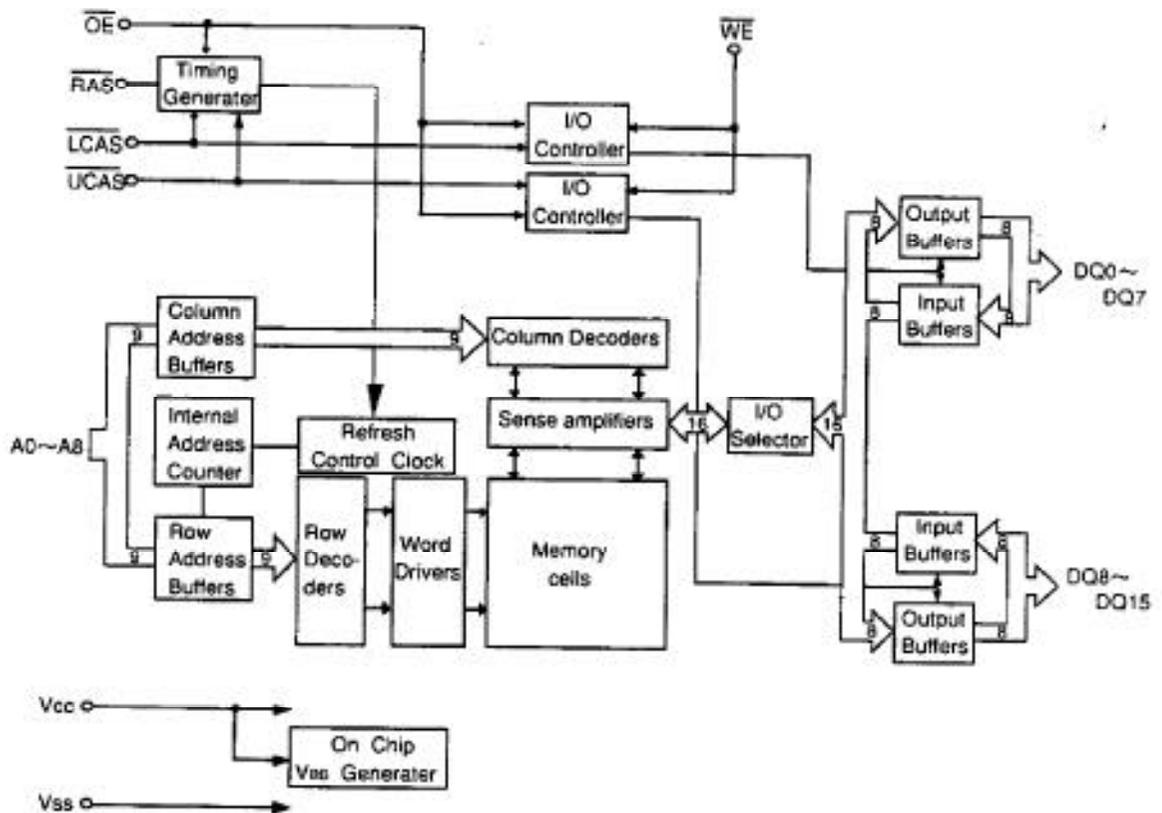
FUNCTION TABLE

Input Pin					DQ Pin		Functinal Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ0~DQ7	DQ8~DQ15	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	Dout	Upper Byte Read
L	L	L	H	L	Dout	Dout	Word Read
L	L	H	L	H	Din	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	Din	Upper Byte Write
L	L	L	L	H	Din	Din	Word Write
L	L	L	H	H	High-Z	High-Z	—

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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to Vss	Vt	Ta=25°C	-0.5~+4.6	V
Short circuit output current	Ios	Ta=25°C	50	mA
Power dissipation	Pb	Ta=25°C	1	W
Operrating temperature	Topr	—	0~+70	°C
Storage temperature	Tstg	—	-55~+150	°C

Recommended Operating Conditions

(Ta=0°C to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	—	3.0	3.3	3.6	V
	Vss	—	0	0	0	V
Input high voltage	VIH	—	2.0	—	Vcc+0.3	V
Input low voltage	VIL	—	-0.3	—	0.8	V

Capacitance

(Vcc=3.3V±0.3V,Ta=25°C,f=1MHz)

Parameter	Symbol	Conditions	Typ.	Max.	Unit
Input capacitance (A0~A8)	CIN1	—	—	8	pf
Input capacitance ($\overline{RAS}$,$\overline{LCAS}$,$\overline{UCAS}$,$\overline{WE}$,$\overline{OE}$)	CIN2	—	—	8	of
Input / output capacitance (DQ0~DQ15)	CIO	—	—	9	pf

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AC CHARACTERISTICS (1/2)

(Vcc = 3.3V ± 0.3V, Ta = 0~70℃)

Parameter	Symbol	MSM54V16258A /SL-40		MSM54V16258A /SL-45		Unit	Note
		MIN	MAX	MIN	MAX		
Random read or write cycle time	tRC	80	—	90	—	ns	
Read/Write cycle time	tRMW	115	—	130	—	ns	
Hyper page mode cycle time	tHPC	15	—	17	—	ns	
Fast page mode read/write cycle time	tPRMW	55	—	60	—	ns	
Access time from RAS	tRAC	—	40	—	45	ns	7,12,13
Access time from CAS	tCAC	—	10	—	12	ns	7,12
Access time from column address	tAA	—	22	—	24	ns	7,13
Access time from OE	tOEA	—	10	—	12	ns	
Access time from CAS precharge	tCPA	—	24	—	27	ns	7,12
Data hold after CAS low	tDOH	3	—	3	—	ns	17
Output buffer turn-off delay time	tOFF	3	8	3	8	ns	8
OE to data output buffer turn-off delay time	tOEZ	3	8	3	8	ns	8
RAS to data output buffer turn-off delay time	tREZ	3	8	3	8	ns	8
WE to data output buffer turn-off delay time	tWEZ	3	8	3	8	ns	8
Transition time	tT	2	35	2	35	ns	
Refresh preiod	tREF	—	8	—	8	ms	
RAS precharge time	tRP	30	—	35	—	ns	
RAS pulse width	tRAS	40	10,000	45	10,000	ns	
RAS pulse width (Fast page mode)	tRASP	40	100,000	45	100,000	ns	
RAS hold time	tRSH	8	—	10	—	ns	
RAS hold time reference to OE	tROH	8	—	8	—	ns	
CAS precharge time	tCP	5	—	6	—	ns	
CAS pulse width	tCAS	6	10,000	7	10,000	ns	
CAS hold time	tCSH	40	—	45	—	ns	
CAS to RAS precharge time	tCRP	5	—	5	—	ns	
RAS to CAS delay time	tRCD	18	30	18	33	ns	12
RAS to column address delay time	tRAD	13	18	13	21	ns	
Row address set-up time	tASR	0	—	0	—	ns	13
Row address hold time	tRAH	8	—	8	—	ns	
Column address set-up time	tASC	0	—	0	—	ns	
Column address hold time	tCAH	5	—	6	—	ns	
Column address hold time from RAS	tAR	30	—	30	—	ns	
Column address to RAS lead time	tRAL	22	—	24	—	ns	
Read command set-up time	tRCS	0	—	0	—	ns	9
Read command hold time	tRCH	0	—	0	—	ns	
Read command hold time reference to RAS	tRRH	0	—	0	—	ns	9
WE pulse width	tWEP	10	—	10	—	ns	

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AC CHARACTERISTICS (2/2)

(Vcc = 3.3V ± 0.3V, Ta = 0~70°C)

| Parameter	Symbol	MSM54V16258A /SL-40		MSM54V16258A /SL-45		Unit	Note
		MIN	MAX	MIN	MAX		
Write command set-up time	twcs	0	—	0	—	ns	
Write command hold time	twch	7	—	8	—	ns	
Write command pulse width	twp	7	—	8	—	ns	
Write command hold time from RAS	twcr	30	—	30	—	ns	
OE command hold time	tceh	7	—	8	—	ns	
Write command to CAS lead time	tcwl	7	—	8	—	ns	
Write command to RAS lead time	trwl	10	—	12	—	ns	
Data to CAS delay time	tdzc	0	—	0	—	ns	
Data to OE delay time	tdzo	0	—	0	—	ns	
Data-in set-up time	tds	0	—	0	—	ns	10
Data-in hold time	tdh	6	—	7	—	ns	10
Data-in hold time referenced to RAS	tdhr	20	—	20	—	ns	
OE to Data-in delay time	tced	8	—	8	—	ns	
OE "L" to CAS "H" lead time	toch	10	—	10	—	ns	
CAS "H" to OE "L" lead time	tcho	10	—	10	—	ns	
Hi-Z command pulse width	toep	10	—	10	—	ns	
CAS to WE delay time	tcwd	28	—	30	—	ns	11
Column address to WE delay time	tawd	38	—	40	—	ns	11
RAS to WE delay time	trwd	60	—	65	—	ns	11
CAS active delay time from RAS precharge	trpc	0	—	0	—	ns	
RAS to CAS set-up time (CAS before RAS)	tcsr	10	—	10	—	ns	
RAS to CAS hold time (CAS before RAS)	tchr	10	—	10	—	ns	
RAS Pulse Width (CAS before RAS Self-Refresh)	TRASS	100	—	100	—	ns	
RAS Precharge Time (CAS before RAS Self-Refresh)	trps	100	—	100	—	ns	
CAS Hold Time (CAS before RAS Self-Refresh)	tchs	-40	—	-40	—	ns	

Notes:

1. All voltages are referenced to Vss.
2. This parameter is dependent upon the cycle rate.
3. This parameter is dependent upon the output loading. Specified values are obtained with the output open.
4. An initial pause of 200 μ s is required after power-up, followed by any 8 $\overline{RAS}$ cycles. (Example: $\overline{RAS}$-only-refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles instead of 8 $\overline{RAS}$ cycles are required.
5. The AC characteristics assume $t_r = 5ns$.
6. V_{IH}(Min.)and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Data outputs are measured with a load of 50 pF. DOUT reference levels: $V_{OH}/V_{OL} = 2.0$ V/1.4V. Note that V_{OL} is defined as 1.4V when Vss* pins, pin 11 and pin 30, were open. The data output measurements under $V_{OH}/V_{OL} = 2.0V/0.8V$ are guaranteed when Vss* pins, pin 11 and 30(SOJ) or pin 13 and 32(TSOP) were connected to GND.
8. t_{REZ} (Max.), t_{OFF} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels. This parameter is sampled and not 100 % tested.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycles and read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pins will remain open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (Min.), $t_{CWD} \geq t_{CWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither or the above sets of conditions is satisfied, the condition of the data out is indeterminate.
12. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CAC}.
13. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled by t_{AA}.
14. Input levels at the AC testing are 3.0V/0V.
15. Addresses (A0 - A8) may be changed two times or less while $\overline{RAS} = V_{IL}$.
16. Addresses (A0 - A8) may be changed once or less while $\overline{CAS} = V_{IH}$ and $\overline{RAS} = V_{IL}$.
17. This is guaranteed by design. ($t_{COH} = t_{CAC}$ - output transition time). This parameter is not 100 % tested.
18. This parameter is dependent upon the number of address transitions. Specified values are measured with a maximum of two transitions per address cycle in Fast Page Mode.
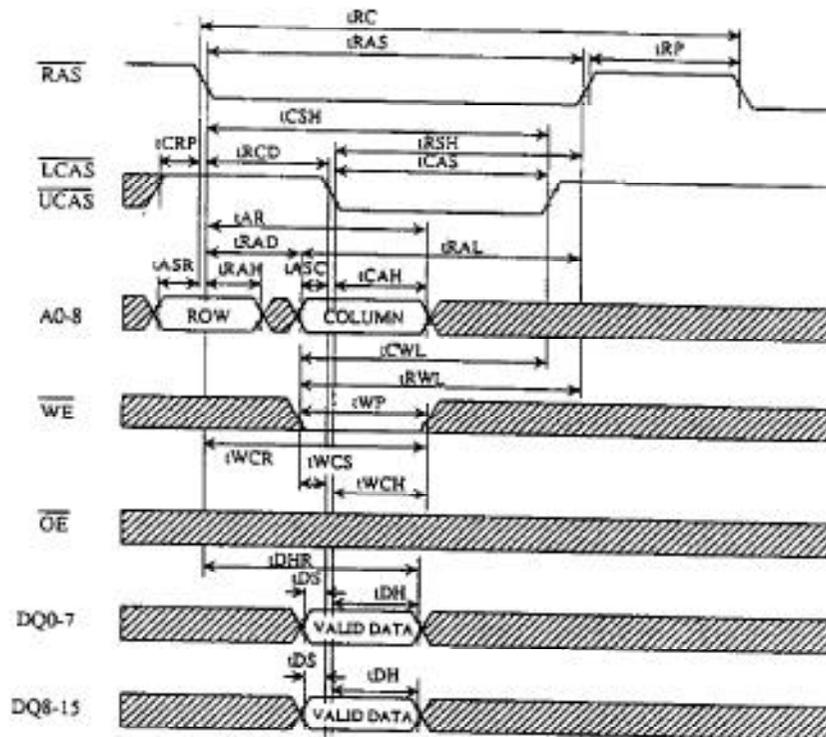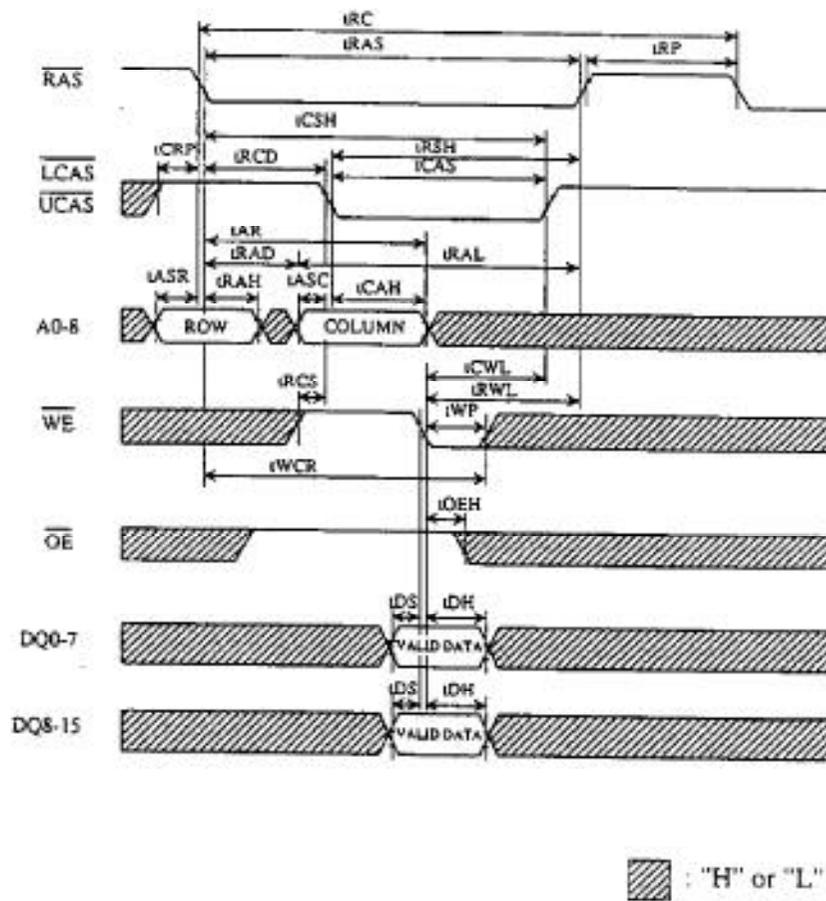
READ CYCLE ($\overline{RAS}$ output control)
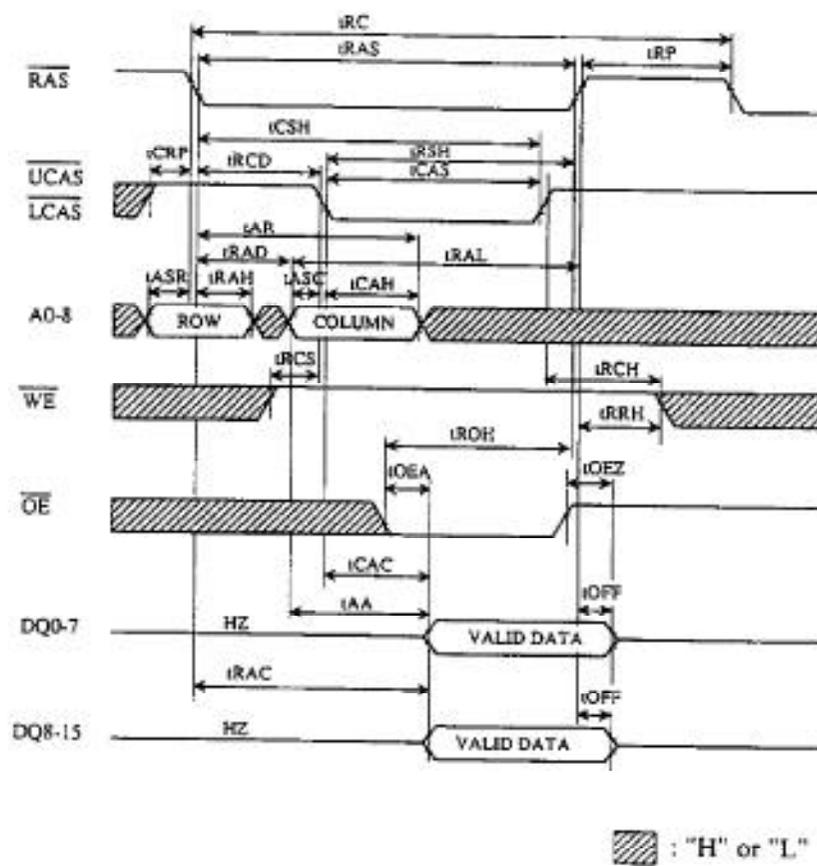
▨ : "H" or "L"

READ CYCLE ($\overline{CAS}$ output control)
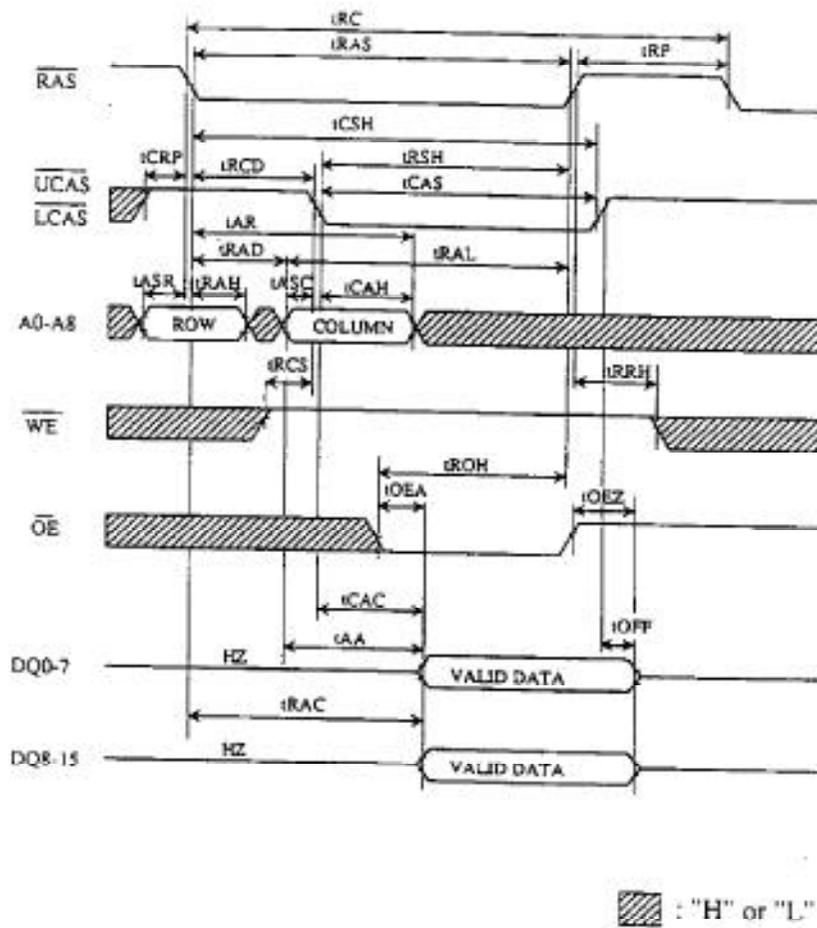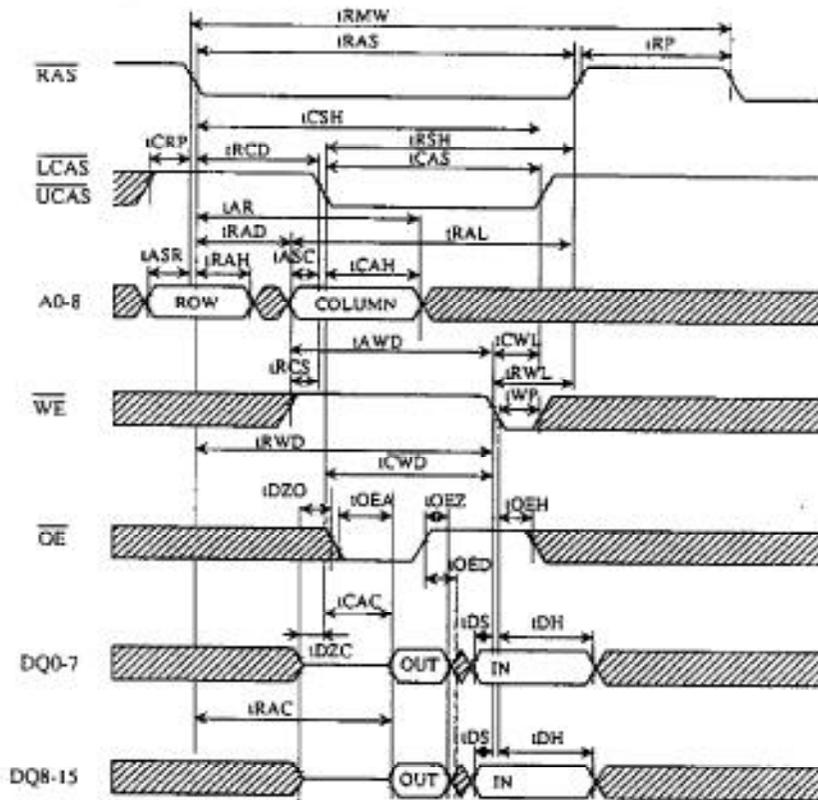

: "H" or "L"

EARLY WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)

: "H" or "L"

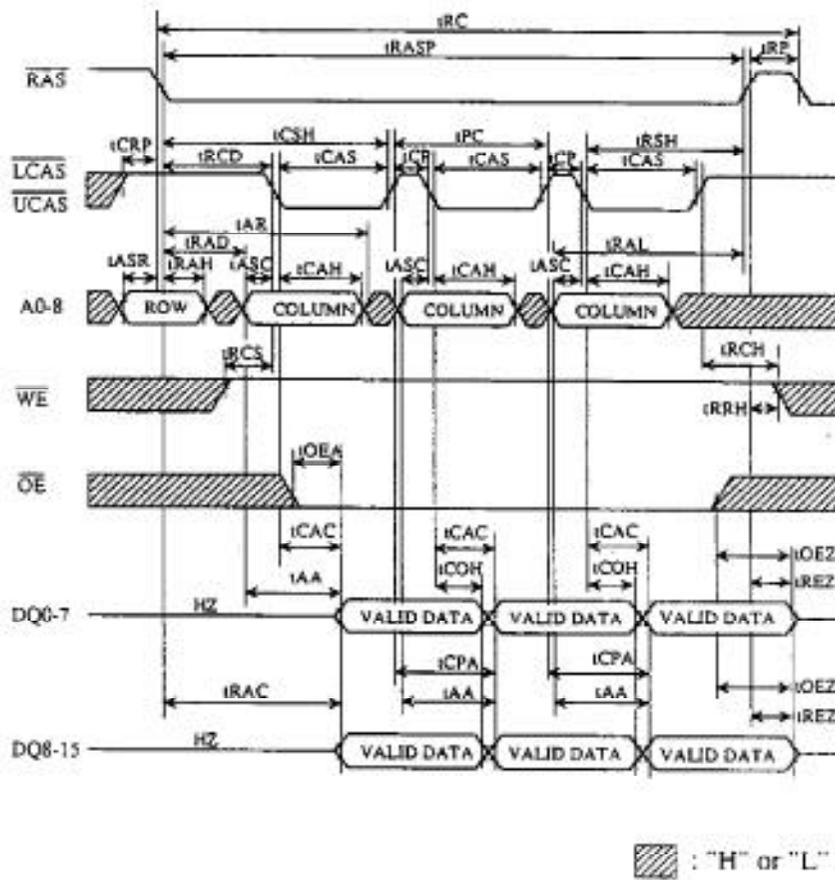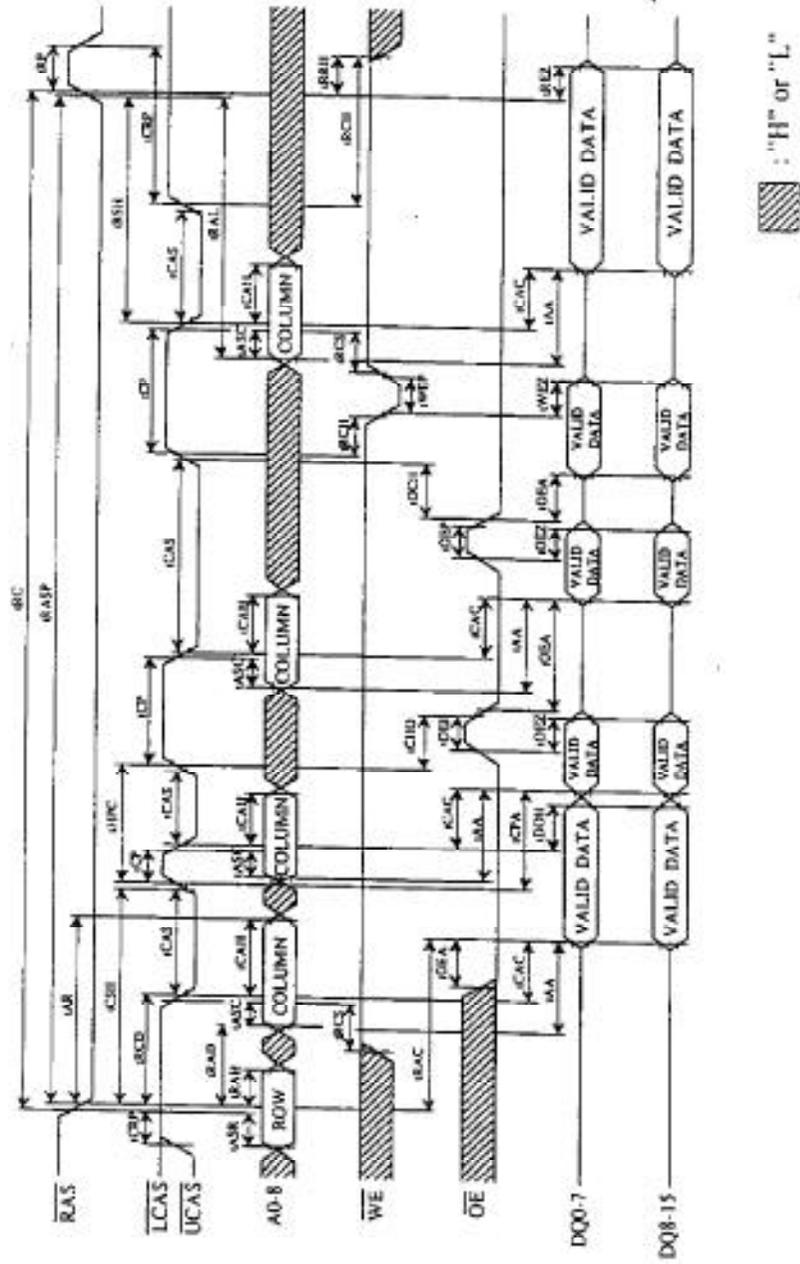# LATE WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)
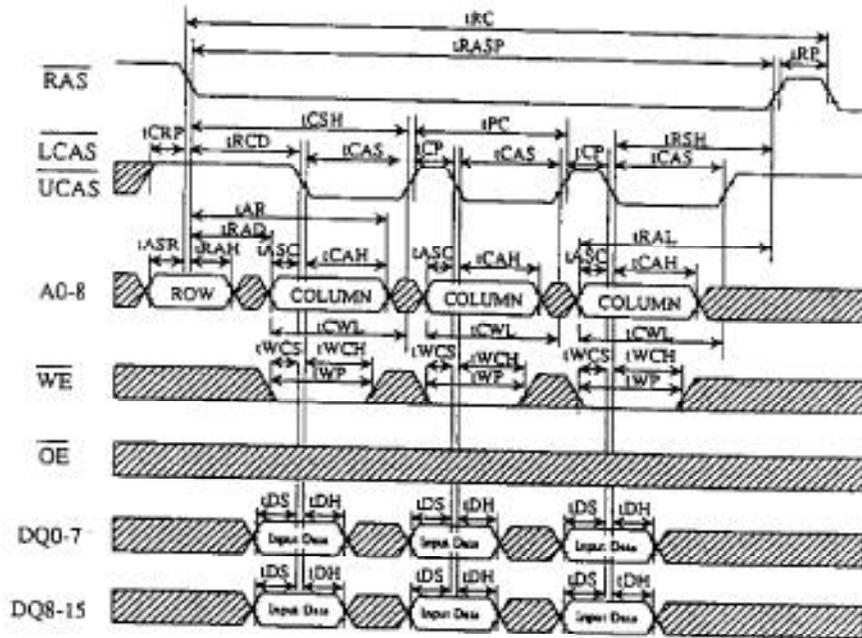

☐ : "H" or "L"

READ MODIFY WRITE CYCLE ($\overline{LCAS}$ and $\overline{UCAS}$ active)

� : "H" or "L"

FAST PAGE MODE READ CYCLE with Extended Data Out
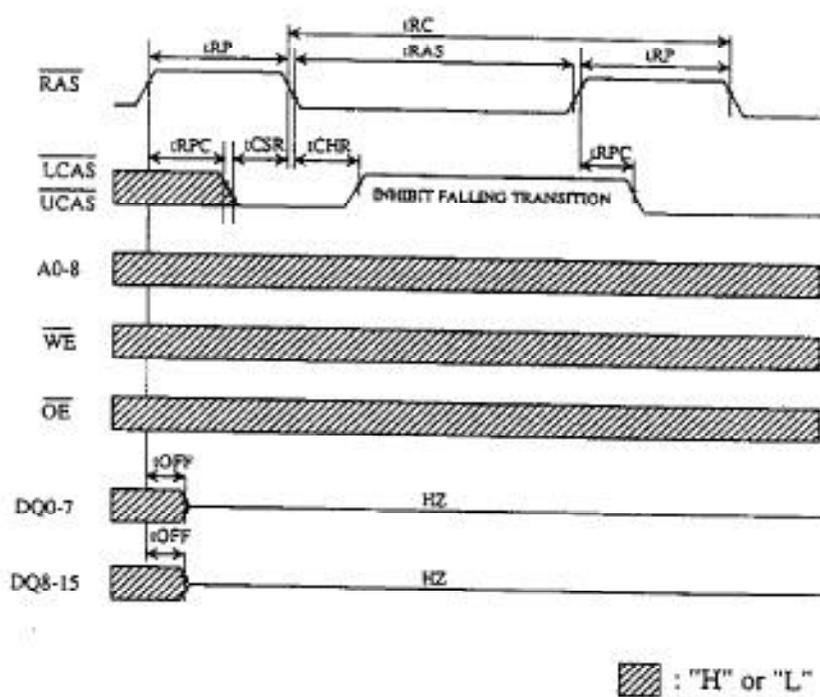

▨ : "H" or "L"

FAST PAGE MODE READ Hi-Z OPERATION

: "H" or "L"

FAST PAGE MODE EARLY WRITE CYCLE

: "H" or "L"

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FAST PAGE MODE READ MODIFY WRITE CYCLE

: "H" or "L"

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

: "H" or "L"

HIDDEN REFRESH CYCLE

▨ : "H" or "L"
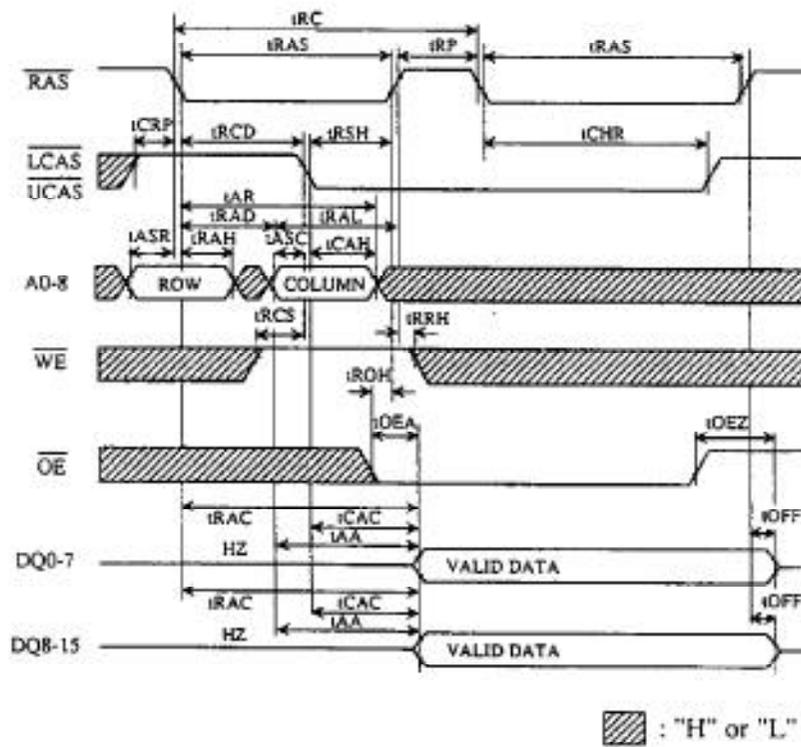
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ SELFREFRESH CYCLE

: "H" or "L"