Solid State Devices, Inc.
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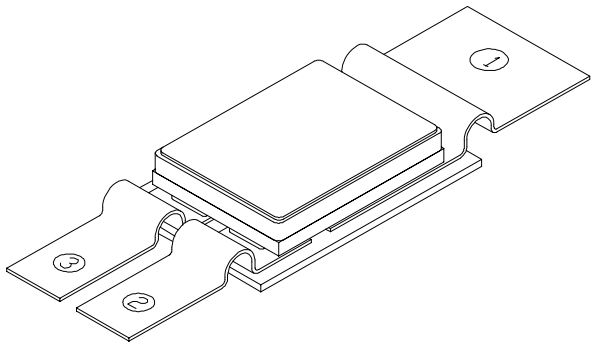
SFF25P20S2I series

DESIGNER'S DATA SHEET

25 AMP / 200 Volts
125 mΩ
P-Channel MOSFET

SMD 2 isolated



NOTE: SEE DASH# DEFINITION TABLE FOR AVAILABLE LEAD FORMING CONFIGURATION

Features:

- polySi gate cell structure
- Low ON-resistance
- UIS (unclamped inductive switching) rated
- Hermetically Sealed, Isolated Package
- Low package inductance
- Stress relief provided by flexible leads – several options available
- Improved ($R_{DS(ON)}$ Q_G) figure of merit
- TX, TXV, S Level screening available

Maximum Ratings		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	-200	V
Gate – Source Voltage		V_{GS}	±20	V
Max. Continuous Drain Current	@ T_C = 25ºC	I_{D1}	25	A
Max. Instantaneous Drain Current (Tj limited)	@ T_C = 25ºC	I_{D3}	95	A
Max. Avalanche current		I_{AR}	25	A
Repetitive Avalanche Energy		E_{AR}	30	mJ
Total Power Dissipation	@ T_C = 25ºC	P_D	250	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	ºC
Maximum Thermal Resistance	Junction to Case	$R_{\theta JC}$	0.5	ºC/W

Electrical Characteristics (@25ºC, unless otherwise specified)		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	V_{GS} = 0V, I_D = 250µA	BV_{DSS}	200	—	—	V
Drain to Source On State Resistance	V_{GS} = 10V, I_D = 12A, Tj= 25ºC V_{GS} = 10V, I_D = 25A, Tj= 25ºC	$R_{DS(on)}$	— —	110 125	120 —	mΩ
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	$V_{GS(th)}$	3.0	—	5.0	V
Gate to Source Leakage	V_{GS} = ±20V	I_{GSS}	—	—	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 160V, V_{GS} = 0V, T_j = 25ºC V_{DS} = 160V, V_{GS} = 0V, T_j = 125ºC	I_{DSS}	— —	— —	25 1	µA mA

NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0009A DOC

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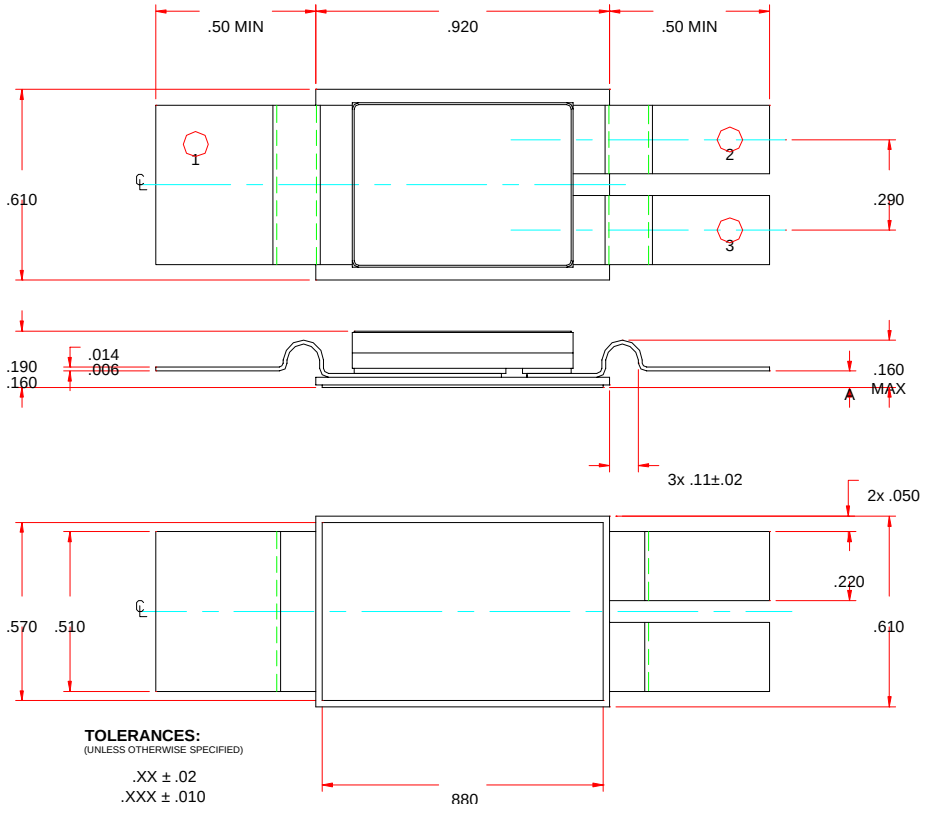
Electrical Characteristics (@25°C, unless otherwise specified)		Symbol	Min	Typ	Max	Units
Forward Transconductance	V_{DS} = 10V, I_D = 24A, T_j = 25°C	g_{fs}	5	12	—	Mho
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	V_{GS} = 10V V_{DS} = 100V I_D = 12A	Q_g Q_{gs} Q_{gd}	— — —	150 35 70	— — —	nC
Turn on Delay Time **Rise Time** **Turn off Delay Time** **Fall Time**	V_{GS} = 10V V_{DS} = 100V I_D = 12A R_G = 4.7Ω	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	35 30 70 30	— — — —	nsec
Diode Forward Voltage	I_F = 25A, V_{GS} = 0V	V_{SD}	—	2.0	3.0	V
Diode Reverse Recovery Time **Peak Reverse Recovery Current** **Reverse Recovery Charge**	I_F = 24A, di/dt = 100A/usec	t_{rr}	—	250	—	nsec
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	V_{GS} = 0V V_{DS} = 25V f = 1 MHz	C_{iss} C_{oss} C_{rss}	— — —	4200 1200 350	— — —	pF

NOTES: Pulse Test: Pulse Width = 300µsec, Duty Cycle = 2%.



LEAD FORMING CONFIGURATIONS			
SMD2I dash#	**-01**	**-02**	**-03**
A	0.062”	0.000”	0.097”

PIN ASSIGNMENT (Standard)			
Package	**Drain**	**Source**	**Gate**
SMD2I	Pin 1	Pin 2	Pin 3