

SFF75N06-28

SOLID STATE DEVICES, INC.

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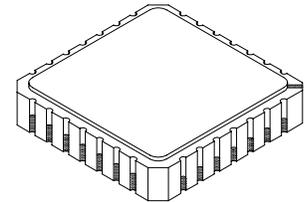
DESIGNER'S DATA SHEET

FEATURES:

- Rugged construction with poly silicon gate
- Low RDS (on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input transfer capacitance for easy paralleling
- Hermetically sealed surface mount package
- TX, TXV and Space Level screening available

30 AMP ^{1/}
60 VOLTS
25mΩ
N-CHANNEL
POWER MOSFET

28 PIN CLCC



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V _{DS}	100	Volts
Drain to Gate Voltage (R _{GS} = 1.0 mΩ)	V _{DG}	60	Volts
Gate to Source Voltage	V _{GS}	±20	Volts
Continuous Drain Current @ TC = 25°C	I _D	30	Amps
Operating and Storage Temperature	T _{op} & T _{stg}	-55 to +150	°C
Thermal Resistance, Junction to Case (All Four)	R _{θJC}	3.5	°C/W
Total Device Dissipation @ TC = 25°C	P _D	35	Watts

PACKAGE OUTLINE: 28 PIN CLCC

PIN OUT:

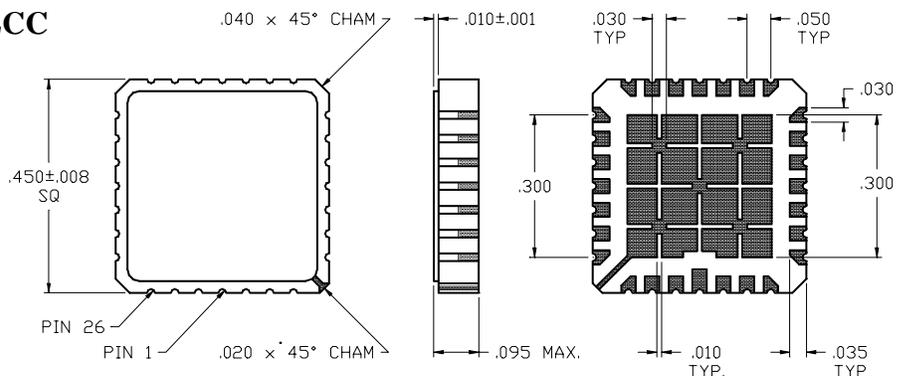
SOURCE: 1, 15 - 28

DRAIN: 5 - 11

GATE: 2, 3, 13, 14

NOTE:

All drain/source pins must be connected on the PC board in order to maximize current carrying capability and to minimize RDS (on)



**ELECTRICAL CHARACTERISTICS @ T_J = 25°C (Unless Otherwise Specified)**

RATING	SYMBOL	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage (V _{GS} = 0 V, I _D = 250μA)	B_VDSS	60	-	-	V
Drain to Source ON State Resistance ^{2/} (V _{GS} = 10 V)	R_{DS(on)}	60% of Rated I _D , T _C = 25°C Rated I _D , T _C = 25°C 60% of Rated I _D , T _C = 150°C	- 23 25 27	25 27 -	mΩ
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250μA)	V_{GS(th)}	2	-	4	V
Forward Transconductance (V _{DS} > I _{D(on)} x R _{DS(on)} Max, I _{DS} = 60% rated I _D)	g_{fs}	15	35	-	S(Ω)
Zero Gate Voltage Drain Current (V _{DS} = 80% rated V _{DS} , V _{GS} = 0 V, T _A = 25°C) (V _{DS} = 80% rated V _{DS} , V _{GS} = 0 V, T _A = 125°C)	I_{DSS}	- -	- -	10 100	μA
Gate to Source Leakage Forward Gate to Source Leakage Reverse	At rated V _{GS}	I_{GSS}	- -	- -	100 100 nA
Total Gate Charge Gate to Source Charge Gate to Drain Charge	V _{GS} = 10 Volts 50% rated V _{DS} Rated I _D	Q_g Q_{gs} Q_{gd}	- - -	83 13 40	100 20 55 nC
Turn on Delay Time Rise Time Turn off DELAY Time Fall Time	V _{DD} = 50% rated V _{DS} rated I _D R _G = 6.2 Ω	t_{d(on)} t_r t_{d(off)} t_f	- - - -	20 35 65 40	40 70 130 80 nsec
Diode Forward Voltage (I _S = rated I _D , V _{GS} = 0V, T _J = 25°C)		V_{SD}	-	1.47	1.6 V
Diode Reverse Recovery Time Reverse Recovery Charge	T _J = 25°C I _F = 10A di/dt = 100A/μsec	t_{rr}	-	70	150 nsec
Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{GS} = 0 Volts V _{DS} = 25 Volts f = 1 MHz	C_{iss} C_{oss} C_{rss}	- - -	2600 700 260	2900 1100 275 pF

For thermal derating curves and other characteristic curves please contact SSDI Marketing Department.

NOTES:

1/ Die Rating: 75Amps.

2/ All package pins of the same terminations (Drain/Source/Gate) must be connected together to minimize R_{DS(on)} and maximize current carrying capability.