



**Solid State Devices, Inc.**

14830 Valley View Blvd \* La Mirada, Ca 90638

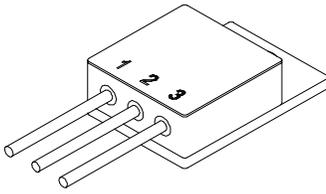
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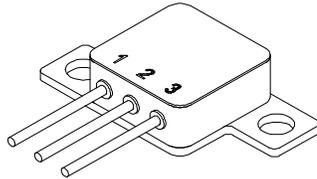
**DESIGNER'S DATA SHEET**

**TO-254, TO254Z**

**Note 1: maximum current limited by package configuration**



TO-254 (SFF85N10M)



TO-254Z (SFF85N10Z)

**SFF80N10M  
SFF80N10Z**

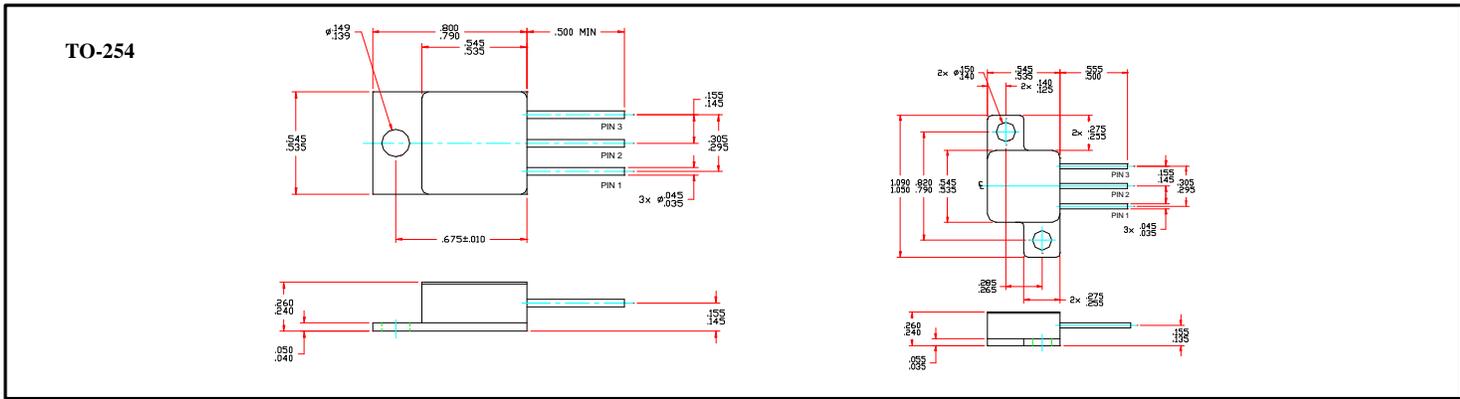
**55 AMP (note 1) /100 Volts  
12 mO**

**N-Channel Trench Gate MOSFET**

**Features:**

- Trench gate technology for high cell density
- Lowest ON-resistance in the industry
- Enhanced operating temperature range
- Hermetically Sealed, Isolated Power Package
- Low Total Gate Charge
- Fast Switching
- Enhanced replacement for IRM150
- TX, TXV, S-Level screening available
- Improved ( $R_{DS(ON)}$   $Q_G$ ) figure of merit

Maximum Ratings		Symbol	Value	Units
Drain - Source Voltage		$V_{DSS}$	100	V
Gate - Source Voltage		$V_{GS}$	$\pm 20$	V
Max. Continuous Drain Current (package limited)	@ $T_C = 25^\circ C$	$I_{D1}$	55 (note 1)	A
	@ $T_C = 125^\circ C$	$I_{D2}$	55 (note 1)	A
Max. Instantaneous Drain Current ( $T_j$ limited)	@ $T_C = 25^\circ C$	$I_{D3}$	110	A
	@ $T_C = 125^\circ C$	$I_{D4}$	70	A
Max. Avalanche current	@ $L = 0.1$ mH	$I_{AR}$	75	A
Repetitive Avalanche Energy	@ $L = 0.1$ mH	$E_{AR}$	280	mJ
Total Power Dissipation	@ $T_C = 25^\circ C$	$P_D$	250	W
Operating & Storage Temperature		$T_{OP}$ & $T_{STG}$	-55 to +200	$^\circ C$
Maximum Thermal Resistance	Junction to Case	$R_{\theta JC}$	0.7 (typ 0.55)	$^\circ C/W$



**NOTE:** All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

**DATA SHEET #: FT0019A**

**DOC**


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# SFF80N10M

# SFF80N10Z

Electrical Characteristics <sup>4/</sup>		Symbol	Min	Typ	Max	Units
<b>Drain to Source Breakdown Voltage</b>	$V_{GS} = 0V, I_D = 250\mu A$	$BV_{DSS}$	100	—	—	V
<b>Drain to Source On State Resistance</b>	$V_{GS} = 10V, I_D = 30A, T_j = 25^\circ C$ $V_{GS} = 10V, I_D = 30A, T_j = 125^\circ C$ $V_{GS} = 10V, I_D = 30A, T_j = 200^\circ C$ $V_{GS} = 10V, I_D = 85A, T_j = 25^\circ C$	$R_{DS(on)}$	—	9.5 16 22 10	12.0 — — —	mΩ
<b>Gate Threshold Voltage</b>	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(th)}$	2.0	—	4.0	V
<b>Gate to Source Leakage</b>	$V_{GS} = \pm 20V$	$I_{GSS}$	—	—	±100	nA
<b>Zero Gate Voltage Drain Current</b>	$V_{DS} = 80V, V_{GS} = 0V, T_j = 25^\circ C$ $V_{DS} = 80V, V_{GS} = 0V, T_j = 125^\circ C$ $V_{DS} = 80V, V_{GS} = 0V, T_j = 200^\circ C$	$I_{DSS}$	—	—	1 50 10	μA μA mA
<b>Forward Transconductance</b>	$V_{DS} = 15V, I_D = 30A, T_j = 25^\circ C$	$g_{fs}$	23	—	—	Mho
<b>Total Gate Charge</b>	$V_{GS} = 10V$	$Q_g$	—	140	220	nC
<b>Gate to Source Charge</b>	$V_{DS} = 50V$	$Q_{gs}$	—	40	—	
<b>Gate to Drain Charge</b>	$I_D = 85A$	$Q_{gd}$	—	40	—	
<b>Turn on Delay Time</b>	$V_{GS} = 10V$	$t_{d(on)}$	—	25	35	nsec
<b>Rise Time</b>	$V_{DS} = 50V$	$t_r$	—	115	185	
<b>Turn off Delay Time</b>	$I_D = 85A$	$t_{d(off)}$	—	75	110	
<b>Fall Time</b>	$R_G = 2.5\Omega$	$t_f$	—	110	160	
<b>Diode Forward Voltage</b>	$I_F = 50A, V_{GS} = 0V$	$V_{SD}$	—	1.0	1.5	V
<b>Diode Reverse Recovery Time</b>	$I_F = 50A, di/dt = 100A/\mu sec$	$t_{rr}$	—	70	150	nsec
<b>Peak Reverse Recovery Current</b>		$I_{RM(rec)}$	—	5.5	10	A
<b>Reverse Recovery Charge</b>		$Q_{rr}$	—	0.2	0.35	μC
<b>Input Capacitance</b>	$V_{GS} = 0V$	$C_{iss}$	—	8700	—	pF
<b>Output Capacitance</b>	$V_{DS} = 25V$	$C_{oss}$	—	750	—	
<b>Reverse Transfer Capacitance</b>	$f = 1 MHz$	$C_{rss}$	—	450	—	

**NOTES:**

\* Pulse Test: Pulse Width = 300μsec, Duty Cycle = 2%.

1/ For Ordering Information, Price, and Availability Contact Factory.

2/ Screening per MIL-PRF-19500.

3/ For Package Outlines Contact Factory.

4/ Unless Otherwise Specified, All Electrical Characteristics @25°C.

**Available Part Numbers:**

Consult Factory

**PIN ASSIGNMENT (Standard)**

Package	Drain	Source	Gate
TO254	Pin 1	Pin 2	Pin 3
TO254Z	Pin 1	Pin 2	Pin 3

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