

1. GENERAL DESCRIPTION

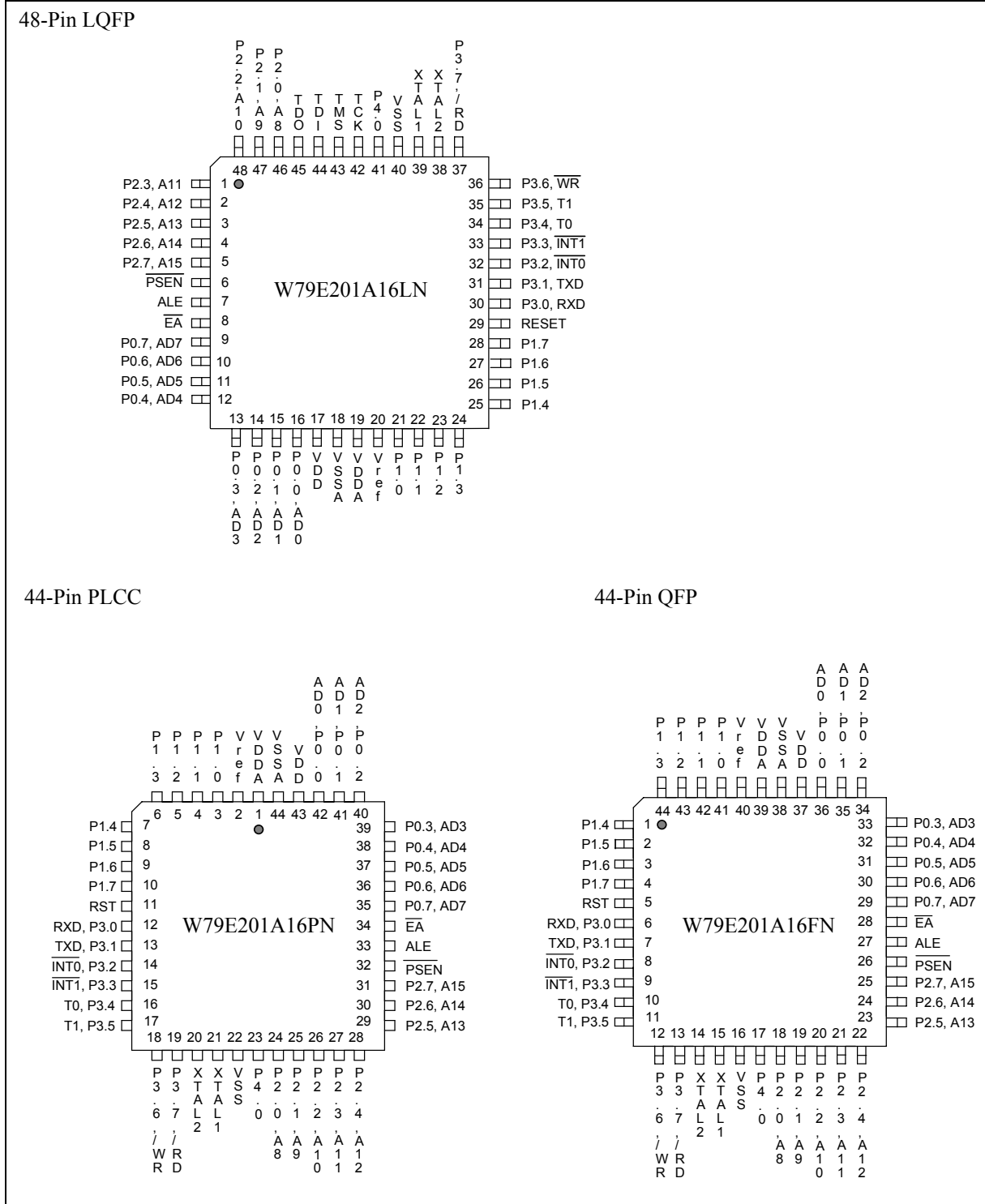
The W79E201 is a fast 8051 compatible microcontroller with a redesigned processor core without wasted clock and memory cycles. The W79E201 contains In-System Programmable (ISP) 16 KB AP Flash EPROM; 4KB LD Flash EPROM for loader program; a 256 bytes of RAM; one 8-bit digital or analog input port (Port 1); three 8-bit bi-directional and bit-addressable I/O ports; an 1-bit port P4.0 for external ISP reboot used; three 16-bit timer/counters; one serial ports. These peripherals are supported by 8 sources two-level interrupt capability. To facilitate programming and verification, the FLASH EPROM inside the W79E201 allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security. The W79E201 is added 10-bit ADC with an 8 channel analog input with digital input port. Furthermore, the W79E201A16LN, packaged in 48-pin LQFP, supports the in circuit emulation (ICE) function with JTAG interface to the development tool. The W79E201 executes every 8051 instruction faster than the original 8051 for the same crystal speed. Typically, the instruction executing time of W79E201 is 1.5 to 3 times faster than that of traditional 8051, depending on the type of instruction. In general, the overall performance is about 2.5 times better than the original for the same crystal speed. Giving the same throughput with lower clock speed, power consumption has been improved. Consequently, the W79E201 is a fully static CMOS design; it can also be operated at a lower crystal clock.

2. FEATURES

- Fully static design 8-bit Turbo 51 CMOS microcontroller up to 16MHz
- 16K bytes of in-system-programmable Flash EPROM (AP Flash EPROM)
- 4KB Auxiliary Flash EPROM for loader program (LD Flash EPROM)
- 256 bytes of on-chip RAM
- Instruction-set compatible with MSC-51
- On-chip debug function with JTGA interface to development tool
- Three 8-bit bi-directional ports
- Three 16-bit timer/counters
- 8 interrupt source with two levels of priority
- One enhanced full duplex serial port with framing error detection and automatic address recognition
- Port 0 internal pull-up resistor optional
- Programmable Watchdog Timer
- 6 channel PWM
- Software programmable access cycle to external RAM/peripherals
- 10-bits ADC with 8 channel analog input or digital input port (At least 8-bits resolution guaranteed)
- Packages:
 - PLCC 44: W79E201A16PN
 - QFP 44: W79E201A16FN
 - LQFP 48: W79E201A16LN



3. PIN CONFIGURATION





4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
\overline{EA}	I H	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be present on the bus if \overline{EA} pin is high and the program counter is within 16KB area. Otherwise they will be present on the bus.
\overline{PSEN}	O H	PROGRAM STORE ENABLE: \overline{PSEN} enables the external ROM data onto the Port 0 address/data bus during fetch and MOVC operations. When internal ROM access is performed, no \overline{PSEN} strobe signal outputs from this pin.
ALE	O H	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0.
RST	I L	RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1.
VSS	P	Digital GROUND: Ground potential
VDD	P	Digital POWER SUPPLY: Supply voltage for operation.
AVDD	P	Analog POWER SUPPLY: Supply analog voltage for operation.
AVSS	P	GROUND: Analog Ground potential
Vref	P	Vref: Analog reference input maximum voltage for ADC
P0.0–P0.7	I/O D(H)	PORT 0: Port 0 is an open-drain bi-directional I/O port with internal pull-up resistor option that is enabled by setting bit 0 of P0R(8Fh) to logic high. This port also provides a multiplexed low order address/data bus during accesses to external memory.
P1.0–P1.7	I	PORT 1: Port 1 is an input port. Or with an 8-bit analog input port for ADC0-ADC7(8 analog input channels) used.
P2.0–P2.7	I/O	PORT 2: Port 2 is a bi-directional I/O port with internal weakly pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0–P3.7	I/O	PORT 3: Port 2 is a bi-directional I/O port with internal weakly pull-ups. Function is the same as that of the standard 8052.
P4.0	I/O	PORT 4: A bi-directional I/O port with internal with weakly pull-ups
TCK	I L	TCK: JTAG test clock
TMS	I H	TMS: JTAG Test Mode select
TDI	I H	TDI: JTAG Test Data In
TDO	O	TDO: JTAG Test Data Out

* Note: **TYPE** P: Power, I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain.



6. FUNCTIONAL DESCRIPTION

The W79E201 is not pin compatible with 8052 but the instruction set is compatible. It includes the resources of the standard 8052 such as three 8-bit I/O Ports, one 8-bit digital or analog input port, three 16-bit timer/counters, one full duplex serial port and interrupt sources.

The W79E201 features a faster running and better performance 8-bit CPU with a redesigned core processor without wasted clock and memory cycles. It improves the performance not just by running at high frequency but also by reducing the machine cycle duration from the standard 8052 period of twelve clocks to four clock cycles for the majority of instructions. This improves performance by an average of 1.5 to 3 times. It can also adjust the duration of the MOVX instruction (access to off-chip data memory) between two machine cycles and nine machine cycles. This flexibility allows the W79E201 to work efficiently with both fast and slow RAMs and peripheral devices.

The W79E201 is an 8052 compatible device that gives the user the features of the original 8052 device, but with improved speed and power consumption characteristics. It has the same instruction set as the 8051 family. While the original 8051 family was designed to operate at 12 clock periods per machine cycle, the W79E201 operates at a much reduced clock rate of only 4 clock periods per machine cycle. This naturally speeds up the execution of instructions. Consequently, the W79E201 can run at a higher speed as compared to the original 8052, even if the same crystal is used. Since the W79E201 is a fully static CMOS design, it can also be operated at a lower crystal clock, giving the same throughput in terms of instruction execution, yet reducing the power consumption.

The 4 clocks per machine cycle feature in the W79E201 is responsible for a three-fold increase in execution speed. The W79E201 has all the standard features of the 8052, and has a few extra peripherals and features as well.

I/O Ports

The W79E201 has one 8-bit digital or analog input port, Three 8-bit I/O ports and one extra 1-bit port at P4.0. Port 0 can be used as an Address/Data bus when external program is running or external memory/device is accessed by MOVC or MOVX instruction. In these cases, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as a general I/O port with open-drain circuit. Port 2 is used chiefly as the upper 8-bits of the Address bus when port 0 is used as an address/data bus. It also has strong pull-ups and pull-downs when it serves as an address bus. Port 1 is only input port which can be selected to 8-channel analog input pins of ADC. Port 3 act as I/O ports with alternate functions. Port 4.0 serves as a general purpose I/O port as Port 3.

Serial I/O

The W79E201 has one enhanced serial port that is functionally similar to the serial port of the original 8052 family. However the serial port on the W79E201 can operate in different modes in order to obtain timing similarity as well. The serial port has the enhanced features of Automatic Address recognition and Frame Error detection.

Timers

The W79E201 has three 16-bit timers that are functionally similar to the timers of the 8052 family. When used as timers, they can be set to run at either 4 clocks or 12 clocks per count, thus providing the user with the option of operating in a mode that emulates the timing of the original 8052. The W79E201 has an additional feature, the watchdog timer. This timer is used as a System Monitor or as a very long time period timer.



Interrupts

The Interrupt structure in the W79E201 is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased. The W79E201 provides 8 interrupt resources with two priority levels, including 2 external interrupt sources, 3 timer interrupts, 1 serial I/O interrupt, 1 ADC interrupt and 1 watch dog timer interrupt.

Power Management

Like the standard 80C52, the W79E201 also has IDLE and POWER DOWN modes of operation. In the POWER DOWN mode, all of the clocks of peripheral are stopped and the chip operation is completely stopped. This is the lowest power consumption state.

7. MEMORY ORGANIZATION

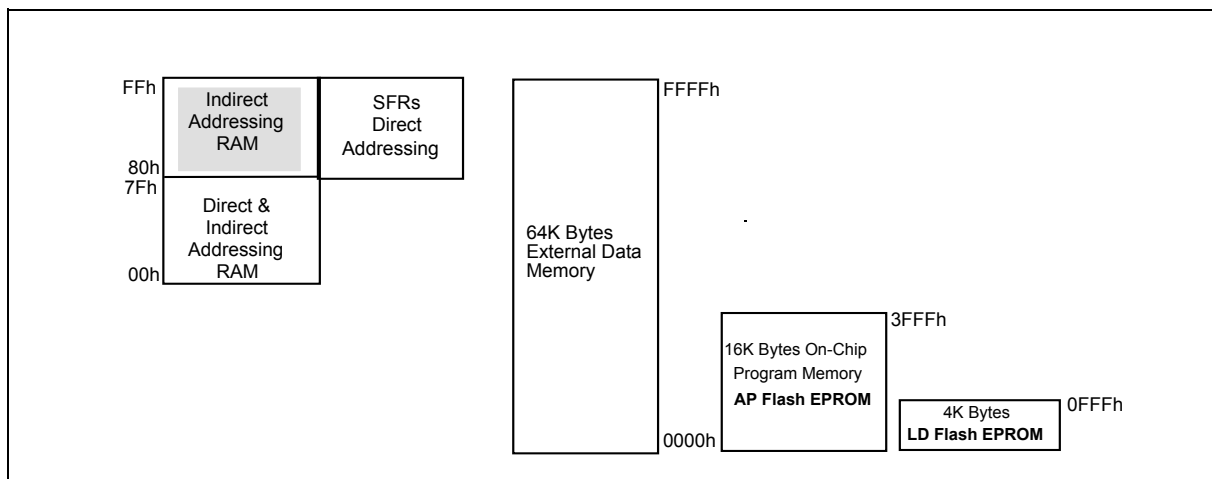
The W79E201 separates the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

Program Memory

The Program Memory on the standard 8052 can only be addressed to 64 Kbytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region. There is an auxiliary 4KB Flash EPROM bank (LD Flash EPROM) resided user loader program for In-System Programming (ISP). The AP Flash EPROM allows serial or parallel download according to user loader program in LD Flash EPROM.

Data Memory

The W79E201 can access up to 64Kbytes of external Data Memory. This memory region is accessed by the MOVX instructions. Any MOVX directed to the space between 0000H and FFFFH goes to the expanded bus on Port 0 and 2. This is the default condition. In addition, the W79E201 has the standard 256 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 256 bytes, it can be used only when data contents are small.



Memory Map



Special Function Registers

The W79E201 uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes.

The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where one wishes to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W79E201 contains all the SFRs present in the standard 8052. However, some additional SFRs have been added. In some cases unused bits in the original 8052 have been given new functions. The list of SFRs is as follows. The table is condensed with eight locations per row. Empty locations indicate that there are no registers at these addresses. When a bit or register is not implemented, it will read high.

Table 1. Special Function Register Location Table

F8	EIP							
F0	B							
E8	EIE							
E0	ACC	ADCCON	ADCH		ADCCEN			
D8	WDCON	PWMP	PWM0	PWM1	PWMCON 1	PWM2	PWM3	
D0	PSW							
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON 2	PWM4
C0				PWM5	PMR	Status		TA
B8	IP	SADEN						
B0	P3							
A8	IE	SADDR			SFRAL	SFRAH	SFRFD	SFRCN
A0	P2					P4		
98	SCON	SBUF						CHPCON
90	P1							
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	P0R
80	P0	SP	DPL	DPH				PCON

Note: The SFRs in the column with dark borders are bit-addressable.



Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0

Address: 80h

Port 0 is an open-drain bi-directional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory.

Stack Pointer

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP

Address: 81h

The Stack Pointer stores the Scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

Data Pointer Low

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL

Address: 82h

This is the low byte of the standard 8052 16-bit data pointer.

Data Pointer High

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH

Address: 83h

This is the high byte of the standard 8052 16-bit data pointer.

Power Control

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON

Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 acts as per the standard 8052 function. 1: Framing Error Detection Enable, then and SCON.7 indicates a Frame Error and acts as the FE flag.
5	-	Reserve



Continued

BIT	NAME	FUNCTION
4	-	Reserve
3	GF1	General purpose user flag.
2	GF0	General purpose user flag.
1	PD	1: Setting this bit causes the Chip to go into the POWER DOWN mode. In this mode all the clocks are stopped and program execution is frozen.
0	IDL	1: Setting this bit causes the Chip to go into the IDLE mode. In this mode the clocks to the CPU are stopped, so program execution is frozen. But the clock to the serial port, ADC, timer and interrupt blocks is not stopped, and these blocks continue operating.

Timer Control

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON

Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 run control: This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 run control: This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.
2	IT1	Interrupt 1 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.
0	IT0	Interrupt 0 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.



Timer Mode Control

Bit:	7	6	5	4	3	2	1	0
	GATE	C/T	M1	M0	GATE	C/T	M1	M0

Mnemonic: TMOD

Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter x is enabled only while $\overline{\text{INTx}}$ pin is high and TRx control bit is set. When cleared, Timer x is enabled whenever TRx control bit is set.
6	C/T	Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the Tx pin.
5	M1	Mode Select bit.
4	M0	Mode Select bit.
3	GATE	Gating control: When this bit is set, Timer/counter x is enabled only while $\overline{\text{INTx}}$ pin is high and TRx control bit is set. When cleared, Timer x is enabled whenever TRx control bit is set.
2	C/T	Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the Tx pin.
1	M1	Mode Select bit.
0	M0	Mode Select bit.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bits with 5-bit prescale.
0	1	Mode 1: 18-bits, no prescale.
1	0	Mode 2: 8-bits with auto-reload from THx
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits. (Timer 1) Timer/counter is stopped.

Timer 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0

Address: 8Ah

TL0.7–0: Timer 0 LSB



Timer 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1

Address: 8Bh

TL1.7–0: Timer 1 LSB

Timer 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0

Address: 8Ch

TH0.7–0: Timer 0 MSB

Timer 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1

Address: 8Dh

TH1.7–0: Timer 1 MSB

Clock Control

Bit:	7	6	5	4	3	2	1	0
	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0

Mnemonic: CKCON

Address: 8Eh

BIT	NAME	FUNCTION
7	WD1	Watchdog timer mode select bit 1: These bits determine the time-out period for the watchdog timer. In all four time-out options the reset time-out is 512 clocks more than the interrupt time-out period.
6	WD0	Watchdog timer mode select bit 0: These bits determine the time-out period for the watchdog timer. In all four time-out options the reset time-out is 512 clocks more than the interrupt time-out period.
5	T2M	Timer 2 clock select: When T2M is set to 1, timer 2 uses a divide by 4 clock, and when set to 0 it uses a divide by 12 clock.

Continued

BIT	NAME	FUNCTION
4	T1M	Timer 1 clock select: When T1M is set to 1, timer 1 uses a divide by 4 clock, and when set to 0 it uses a divide by 12 clock.
3	T0M	Timer 0 clock select: When T0M is set to 1, timer 0 uses a divide by 4 clock, and When set to 0 it uses a divide by 12 clock.
2	MD2	Stretch MOVX select bit 2: These three bits are used to select the stretch value for the MOVX instruction. Using a variable MOVX length enables the user to access slower external memory devices or peripherals without the need for external circuits. The \overline{RD} or \overline{WR} strobe will be stretched by the selected interval. When accessing the on-chip SRAM, the MOVX instruction is always in 2 machine cycles regardless of the stretch setting. By default, the stretch has value of 1. If the user needs faster accessing, then a stretch value of 0 should be selected.
1	MD1	Stretch MOVX select bit 1: These three bits are used to select the stretch value for the MOVX instruction. Using a variable MOVX length enables the user to access slower external memory devices or peripherals without the need for external circuits. The \overline{RD} or \overline{WR} strobe will be stretched by the selected interval. When accessing the on-chip SRAM, the MOVX instruction is always in 2 machine cycles regardless of the stretch setting. By default, the stretch has value of 1. If the user needs faster accessing, then a stretch value of 0 should be selected.
0	MD0	Stretch MOVX select bit 0: These three bits are used to select the stretch value for the MOVX instruction. Using a variable MOVX length enables the user to access slower external memory devices or peripherals without the need for external circuits. The \overline{RD} or \overline{WR} strobe will be stretched by the selected interval. When accessing the on-chip SRAM, the MOVX instruction is always in 2 machine cycles regardless of the stretch setting. By default, the stretch has value of 1. If the user needs faster accessing, then a stretch value of 0 should be selected.

WD1	WD0	INTERRUPT TIME-OUT	RESET TIME-OUT
0	0	2^{17}	$2^{17} + 512$
0	1	2^{20}	$2^{20} + 512$
1	0	2^{23}	$2^{23} + 512$
1	1	2^{26}	$2^{26} + 512$

MD2	MD1	MD0	STRETCH VALUE	MOVX DURATION
0	0	0	0	2 machine cycles
0	0	1	1	3 machine cycles (<i>Default</i>)
0	1	0	2	4 machine cycles
0	1	1	3	5 machine cycles
1	0	0	4	6 machine cycles
1	0	1	5	7 machine cycles
1	1	0	6	8 machine cycles
1	1	1	7	9 machine cycles

Port 0 pull-up resistor

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P0UP

Mnemonic: P0R

Address: 8Fh

BIT	NAME	FUNCTION
7~1	-	Reserved
0	P0UP	Port 0 Pull-up resistor 0: No Pull-up resistor 1: Pull-up resistor(~10KΩ)

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1

Address: 90h

P1.7~0: General purpose digital input port or analog input port, AD0~AD7. By the digital input port, most instructions will read the port pins in case of a port read access, however in case of read instructions, the port latch is read. The alternate functions are described below:

BIT	NAME	FUNCTION
1	P1.1	T2 : External Input for Timer/Counter 2
0	P1.0	T2EX : Timer/Counter 2 Capture/Reload Trigger



Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON

Address: 98h

BIT	NAME	FUNCTION																									
7	SM0/FE	Serial port, Mode 0 bit or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.																									
6	SM1	Serial port Mode bit 1: <table border="1"> <thead> <tr> <th>Mode: SM0</th> <th>SM1</th> <th>Description</th> <th>Length</th> <th>Baud rate</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0 Synchronous</td> <td>8</td> <td>4/12 Tclk</td> </tr> <tr> <td>1</td> <td>0</td> <td>1 Asynchronous</td> <td>10</td> <td>Variable</td> </tr> <tr> <td>2</td> <td>1</td> <td>0 Asynchronous</td> <td>11</td> <td>64/32 Tclk</td> </tr> <tr> <td>3</td> <td>1</td> <td>1 Asynchronous</td> <td>11</td> <td>Variable</td> </tr> </tbody> </table>	Mode: SM0	SM1	Description	Length	Baud rate	0	0	0 Synchronous	8	4/12 Tclk	1	0	1 Asynchronous	10	Variable	2	1	0 Asynchronous	11	64/32 Tclk	3	1	1 Asynchronous	11	Variable
Mode: SM0	SM1	Description	Length	Baud rate																							
0	0	0 Synchronous	8	4/12 Tclk																							
1	0	1 Asynchronous	10	Variable																							
2	1	0 Asynchronous	11	64/32 Tclk																							
3	1	1 Asynchronous	11	Variable																							
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052.																									
4	REN	Receive enable: When set to 1 serial reception is enabled, otherwise reception is disabled.																									
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.																									
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.																									
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.																									
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.																									

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF

Address: 99h



BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive register, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

ISP Control Register

Bit:	7	6	5	4	3	2	1	0
	SWRST/ REBOOT	-	LDAP	-	-	-	FBOOTSL	FPROGEN

Mnemonic: CHPCON

Address: 9Fh

BIT	NAME	FUNCTION
7	SWRST/ REBOOT	Set this bit to launch a whole device reset that is same as asserting high to RST pin, micro controller will be back to initial state and clear this bit automatically. To read this bit, its alternate function to indicate the ISP hardware reboot mode is invoking when reading it in high.
6	-	Reserved
5	LDAP	This bit is Read Only. High: device is executing the program in LD Flash EPROM Low: device is executing the program in AP Flash EPROM.
4	-	Reserved
3	-	Reserved
2	-	Reserved
1	FBOOTSL	Loader program residence selection. Set to high to route the device fetching code from LD Flash EPROM.
0	FPROGEN	In System Programming Mode Enable. Set this bit to launch the ISP mode. Device will operate ISP procedures, such as Erase, Program and Read operations, according to correlative SFRs settings. During ISP mode, device achieves ISP operations by the way of IDLE state. In the other words, device is not indeed in IDLE mode is set bit PCON.1 while ISP is enabled. Clear this bit to disable ISP mode, device get back to normal operation including IDLE state.

Port 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2

Address: A0h

P2.7-0: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.



Port 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P4.0

Mnemonic: P4

Address: A5h

P4.0: When B3 of security bits is set to logical 0, the P4.0 as reboot pin.

When B3 of security bits is set to logical 1, the P4.0 as I/O pin.

Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE

Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/disable all interrupts.
6	EADC	Enable ADC interrupt.
5	ET2	Enable Timer 2 interrupt.
4	ES	Enable Serial Port interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

Slave Address

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR

Address: A9h

BIT	NAME	FUNCTION
7~0	SADDR	The SADDR should be programmed to the given or broadcast address for serial port to which the slave processor is designated.

ISP Address Low Byte

Bit:	7	6	5	4	3	2	1	0
	SFRAL.7	SFRAL.6	SFRAL.5	SFRAL.4	SFRAL.3	SFRAL.2	SFRAL.1	SFRAL.0

Mnemonic: SFRAL

Address: ACh

Low byte destination address is for In System Programming operations. SFRAH and SFRAL address are specific ROM bytes for erasure, programming or read.



ISP Address High Byte

Bit:	7	6	5	4	3	2	1	0
	SFRAH.7	SFRAH.6	SFRAH.5	SFRAH.4	SFRAH.3	SFRAH.2	SFRAH.1	SFRAH.0

Mnemonic: SFRAH

Address: ADh

High byte destination address is for In System Programming operations. SFRAH and SFRAL address are specific ROM bytes for erasure, programming or read.

ISP Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SFRFD.7	SFRFD.6	SFRFD.5	SFRFD.4	SFRFD.3	SFRFD.2	SFRFD.1	SFRFD.0

Mnemonic: SFRFD

Address: AEh

In ISP mode, read/write a specific byte ROM content must go through SFRFD register.

ISP Operation Modes

Bit:	7	6	5	4	3	2	1	0
	-	WFWIN	OEN	CEN	CTRL3	CTRL2	CTRL1	CTRL0

Mnemonic: SFRCN

Address: AFh

BIT	NAME	FUNCTION
7	-	Reserve
6	WFWIN	On-chip Flash EPROM bank select for in-system programming. 0: 16K bytes Flash EPROM bank is selected as destination for re-programming. 1: 4K bytes Flash EPROM bank is selected as destination for re-programming.
5	OEN	Flash EPROM output is enabled.
4	CEN	Flash EPROM chip is enabled.
3~0	CTRL[3:0]	The flash control signals

ISP MODE	WFWIN	NOE	NCE	CTRL<3:0>	SFRAH, SFRAL	SFRFD
Erase 4KB LD FLASH PROM	1	1	0	0010	X	X
Erase 16K AP FLASH EPROM	0	1	0	0010	X	X
Program 4KB LD FLASH EPROM	1	1	0	0001	Address in	Data in
Program 16KBAP FLASH EPROM	0	1	0	0001	Address in	Data in
Read 4KB LD FLASH EPROM	1	0	0	0000	Address in	Data out
Read 16KB AP FLASH EPROM	0	0	0	0000	Address in	Data out



Port 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3

Address: B0h

P3.7-0: General purpose I/O port. Each pin also has an alternate input or output function. There alternate functions are described below table.

BIT	NAME	FUNCTION
7	P3.7	Strobe for read from external RAM
6	P3.6	\overline{WR} Strobe for write to external RAM
5	P3.5	T1 Timer/counter 1 external count input
4	P3.4	T0 Timer/counter 0 external count input
3	P3.3	$\overline{INT1}$ External interrupt 1
2	P3.2	$\overline{INT0}$ External interrupt 0
1	P3.1	TxD Serial port 0 output
0	P3.0	RxD Serial port 0 input

Interrupt Priority

Bit:	7	6	5	4	3	2	1	0
	-	PADC	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP

Address: B8h

BIT	NAME	FUNCTION
7	-	This bit is un-implemented and will read high.
6	PADC	1: To set interrupt priority of ADC is highest priority level.
5	PT2	1: To set interrupt priority of Timer 2 is highest priority level.
4	PS	1: To set interrupt priority of Serial port 0 is highest priority level.
3	PT1	1: To set interrupt priority of Serial port 0 is highest priority level.
2	PX1	1: To set interrupt priority of External interrupt 1 is highest priority level.
1	PT0	1: To set interrupt priority of Timer 0 is highest priority level.
0	PX0	1: To set interrupt priority of External interrupt 0 is highest priority level.



Slave Address Mask Enable

Bit:	7	6	5	4	3	2	1	0
	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0

Mnemonic: SADEN

Address: B9h

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature of the Serial port 0. When a bit in the SADEN is set to 1, the same bit location in SADDR will be compared with the incoming serial data. When SADEN is 0, then the bit becomes a "don't care" in the comparison. This register enables the Automatic Address Recognition feature of the Serial port 0. When all the bits of SADEN are 0, interrupt will occur for any incoming address.

PWM 5 Register

Bit:	7	6	5	4	3	2	1	0
	PWM5.7	PWM5.6	PWM5.5	PWM5.4	PWM5.3	PWM5.2	PWM5.1	PWM5.0

Mnemonic: PWM 5

Address: C3h

Power Management Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ALE-OFF	-	-

Mnemonic: PMR

Address: C4h

BIT	NAME	FUNCTION
7~3	-	Reserved.
2	ALE-OFF	This bit disables the expression of the ALE signal on the device pin during all on-board program and data memory accesses. External memory accesses will automatically enable ALE independent of ALE-OFF. 0: ALE expression is enabled. 1: ALE expression is disabled and keep in logic high state.
1~0	-	Reserved.

Status Register

Bit:	7	6	5	4	3	2	1	0
	-	HIP	LIP	-	-	-	SPTA0	SPRA0

Mnemonic: STATUS

Address: C5h

BIT	NAME	FUNCTION
7	-	Reserved.
6	HIP	High Priority Interrupt Status. When set, it indicates that software is servicing a high priority interrupt. This bit will be cleared when the program executes the corresponding RETI instruction.
5	LIP	Low Priority Interrupt Status. When set, it indicates that software is servicing a low priority interrupt. This bit will be cleared when the program executes the corresponding RETI instruction.
4	-	Reserved.
3	-	Reserved.
2	-	Reserved.
1	SPTA0	Serial Port 0 Transmit Activity. This bit is set during serial port is currently transmitting data. It is cleared when TI bit is set by hardware.
0	SPRA0	Serial Port 0 Receive Activity. This bit is set during serial port is currently receiving a data. It is cleared when RI bit is set by hardware.

Timed Access

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA

Address: C7h

TA: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

Timer 2 Control

Bit:	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$\overline{C/T2}$	$\overline{CP/RL2}$

Mnemonic: T2CON

Address: C8h

BIT	NAME	FUNCTION
7	TF2	Timer 2 overflow flag: This bit is set when Timer 2 overflows. It is also set when the count is equal to the capture register in down count mode. It can be set only if RCLK and TCLK are both 0. It is cleared only by software. Software can also set or clear this bit.
6	EXF2	Timer 2 External Flag: A negative transition on the T2EX pin (P1.1) or timer 2 underflow/overflow will cause this flag to set based on the CP/RL2, EXEN2 and DCEN bits. If set by a negative transition, this flag must be cleared by software. Setting this bit in software or detection of a negative transition on T2EX pin will force a timer interrupt if enabled.
5	RCLK	Receive clock Flag: This bit determines the serial port time-base when receiving data in serial modes 1 or 3. If it is 0, then timer 1 overflow is used for baud rate generation, else timer 2 overflow is used. Setting this bit forces timer 2 in baud rate generator mode.
4	TCLK	Transmit clock Flag: This bit determines the serial port time-base when transmitting data in mode 1 and 3. If it is set to 0, the timer 1 overflow is used to generate the baud rate clock, else timer 2 overflow is used. Setting this bit forces timer 2 in baud rate generator mode.
3	EXEN2	Timer 2 External Enable: This bit enables the capture/reload function on the T2EX pin if Timer 2 is not generating baud clocks for the serial port. If this bit is 0, then the T2EX pin will be ignored, else a negative transition detected on the T2EX pin will result in capture or reload.
2	TR2	Timer 2 Run Control: This bit enables/disables the operation of timer 2. halting this will preserve the current count in TH2, TL2.
1	$\overline{C/T2}$	Counter/Timer select: This bit determines whether timer 2 will function as a timer or a counter. Independent of this bit, the timer will run at 2 clocks per tick when used in baud rate generator mode. If it is set to 0, then timer 2 operates as a timer at a speed depending on T2M bit (CKCON.5), else, it will count negative edges on T2 pin.
0	$\overline{CP/RL2}$	Capture/Reload Select: This bit determines whether the capture or reload function will be used for timer 2. If either RCLK or TCLK is set, this bit will not function and the timer will function in an auto-reload mode following each overflow. If the bit is 0 then auto-reload will occur when timer 2 overflows or a falling edge is detected on T2EX if EXEN2 = 1. If this bit is 1, then timer 2 captures will occur when a falling edge is detected on T2EX if EXEN2 = 1.



Timed 2 Mode Control

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	T2CR	-	-	DCEN

Mnemonic: T2MOD

Address: C9h

BIT	NAME	FUNCTION
7~4	-	Reserved.
3	T2CR	Timer 2 Capture Reset. In the Timer 2 Capture Mode this bit enables/disables hardware automatically reset Timer 2 while the value in TL2 and TH2 have been transferred into the capture register.
2~1	-	Reserved.
0	DCEN	Down Count Enable: This bit, in conjunction with the T2EX pin, controls the direction that timer 2 counts in 16-bit auto-reload mode.

Timer 2 Capture LSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L

Address: CAh

RCAP2L: This register is used to capture the TL2 value when a timer 2 is configured in capture mode. RCAP2L is also used as the LSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

Timer 2 Capture MSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H

Address: CBh

RCAP2H: This register is used to capture the TH2 value when a timer 2 is configured in capture mode.

RCAP2H is also used as the MSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

Timer 2 LSB

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2

Address: CCh

TL2: Timer 2 LSB



Timer 2 MSB

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2

Address: CDh

TH2: Timer 2 MSB

PWM 4~5 Control Register 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM5OE	PWM4OE	ENPWM5	ENPWM4

Mnemonic: PWMCON2

Address: CEh

BIT	NAME	FUNCTION
7~4	-	Reserved.
3	PWM5OE	Output enable for PWM5 0: Disable PWM5 Output. 1: Enable PWM5 Output.
2	PWM4OE	Output enable for PWM4 0: Disable PWM4 Output. 1: Enable PWM4 Output.
1	ENPWM5	Enable PWM5 0: Disable PWM5. 1: Enable PWM5.
0	ENPWM4	Enable PWM4 0: Disable PWM4. 1: Enable PWM4.

PWM 4 Register

Bit:	7	6	5	4	3	2	1	0
	PWM4.7	PWM4.6	PWM4.5	PWM4.4	PWM4.3	PWM4.2	PWM4.1	PWM4.0

Mnemonic: PWM 4

Address: CFh

Program Status Word

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW

Address: D0h



BIT	NAME	FUNCTION
7	CY	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	User flag 0: The General purpose flag that can be set or cleared by the user.
4	RS1	Register bank select bits:
3	RS0	Register bank select bits:
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1: The General purpose flag that can be set or cleared by the user by software.
0	P	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

RS.1-0: Register bank select bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

Watchdog Control

Bit:	7	6	5	4	3	2	1	0
	-	POR	-	-	WDIF	WTRF	EWT	RWT

Mnemonic: WDCON

Address: D8h

BIT	NAME	FUNCTION
7	-	Reserved.
6	POR	Power-on reset flag. Hardware will set this flag on a power up condition. This flag can be read or written by software. A write by software is the only way to clear this bit once it is set.
5	-	Reserved.
4	-	Reserved.
3	WDIF	Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software.
2	WTRF	Watchdog Timer Reset Flag. Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWT = 0, the watchdog timer will have no affect on this bit.



1	EWT	Enable Watchdog timer Reset. Setting this bit will enable the Watchdog timer Reset function.
0	RWT	Reset Watchdog Timer. This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWT before time-out will cause an interrupt, if EWDI (EIE.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWT is set. This bit is self-clearing by hardware.

The WDCON SFR is set to a 0x0x0xx0b on an external reset. WTRF is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF is not altered by an external reset. POR is set to 1 by a power-on reset. EWT is set to 0 on a Power-on reset and unaffected by other resets.

All the bits in this SFR have unrestricted read access. POR, EWT, WDIF and RWT require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

```

TA          EG    C7H
WDCON      REG   D8H
CKCON      REG   8EH
MOV        TA, #AAH
MOV        TA, #55H
SETB      WDCON.0          ; Reset watchdog timer
ORL       CKCON, #11000000B ; Select 26 bits watchdog timer
MOV        TA, #AAH
MOV        TA, #55H
ORL       WDCON, #00000010B ; Enable watchdog
    
```

PWM Prescale Register

Bit:	7	6	5	4	3	2	1	0
	PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0

Mnemonic: PWMP

Address: D9h

PWM 0 Register

Bit:	7	6	5	4	3	2	1	0
	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0

Mnemonic: PWM0

Address: DAh

PWM 1 Register

Bit:	7	6	5	4	3	2	1	0
	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0

Mnemonic: PWM1

Address: DBh



PWM 0~3 Control Register 1

Bit:	7	6	5	4	3	2	1	0
	PWM3OE	PWM2OE	ENPWM3	ENPWM2	PWM1OE	PWM0OE	ENPWM1	ENPWM0

Mnemonic: PWMCON1

Address: DCh

BIT	NAME	FUNCTION
7	PWM3OE	Output enable for PWM3 0: Disable PWM3 Output. 1: Enable PWM3 Output.
6	PWM2OE	Output enable for PWM2 0: Disable PWM2 Output. 1: Enable PWM2 Output.
5	ENPWM3	Enable PWM3 0: Disable PWM3. 1: Enable PWM3.
4	ENPWM2	Enable PWM2 0: Disable PWM2. 1: Enable PWM2.
3	PWM1OE	Output enable for PWM1 0: Disable PWM1 Output. 1: Enable PWM1 Output.
2	PWM0OE	Output enable for PWM0 0: Disable PWM0 Output. 1: Enable PWM0 Output.
1	ENPWM1	Enable PWM1 0: Disable PWM1. 1: Enable PWM1.
0	ENPWM0	Enable PWM0 0: Disable PWM0. 1: Enable PWM0.

PWM 2 Register

Bit:	7	6	5	4	3	2	1	0
	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0

Mnemonic: PWM2

Address: DDh

PWM 3 Register

Bit:	7	6	5	4	3	2	1	0
	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0

Mnemonic: PWM3

Address: DEh



Accumulator

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC

Address: E0h

ACC.7-0: The A (or ACC) register is the standard 8052 accumulator.

ADC Control Register

Bit:	7	6	5	4	3	2	1	0
	ADC.1	ADC.0	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0

Mnemonic: ADCCON

Address: E1h

BIT	NAME	FUNCTION															
7	ADC.1	Bit 1 of ADC result.															
6	ADC.0	Bit 0 of ADC result.															
5	ADCEX	Enable external start of conversion by STADC 0 = Conversion can be started by software only (by setting ADCS) 1 = Conversion can be started by software or externally pin P2.0 (by a rising edge on STADC)															
4	ADCI	ADC Interrupt flag: This ADCI flag is set when an A/D conversion result is ready to be read. An interrupt is invoked if it is enabled. The flag may be cleared by the interrupt service routine. While this flag is set, the ADC can not start a new conversion. ADCI can not set by software.															
3	ADCS	<p>ADC Start and Status: setting this bit starts an A/D conversion. It may be set by software or by the external STADC signal. The ADC logic ensures that this signal is HIGH while the ADC is busy. On completion of the conversion, ADCS is reset immediately after the interrupt flag has been set. ADCS can not be reset by software. A new conversion may not be started while either ADCS or ADCI is high.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr> <th style="width: 15%;">ADCI</th> <th style="width: 15%;">ADCS</th> <th style="width: 70%;">ADC Status</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td>ADC not busy; a conversion can be started</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td>ADC busy; start of a new conversion is blocked</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td>Conversion completed; start of a new conversion requires ADCI=0</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td>Conversion completed; start of a new conversion requires ADCI=0</td> </tr> </tbody> </table> <p>If ADCI is cleared by software while ADCS is set at the same time, a new A/D conversion with the same channel number may be started. But it is recommended to reset ADCI before ADCS is set.</p>	ADCI	ADCS	ADC Status	0	0	ADC not busy; a conversion can be started	0	1	ADC busy; start of a new conversion is blocked	1	0	Conversion completed; start of a new conversion requires ADCI=0	1	1	Conversion completed; start of a new conversion requires ADCI=0
ADCI	ADCS	ADC Status															
0	0	ADC not busy; a conversion can be started															
0	1	ADC busy; start of a new conversion is blocked															
1	0	Conversion completed; start of a new conversion requires ADCI=0															
1	1	Conversion completed; start of a new conversion requires ADCI=0															
2	AADR2	See the below table.															
1	AADR1	See the below table.															
0	AADR0	See the below table.															



AADR2~AADR0: The ADC analog input channel select bits: This binary coded address selects one of eight analogue port bits of ADC input converter. It can only be changed when ADCl and ADCS are both LOW.

AADR2	AADR1	AADR0	Selected Analog Channel
0	0	0	ADC0
0	0	1	ADC1
0	1	0	ADC2
0	1	1	ADC3
1	0	0	ADC4
1	0	1	ADC5
1	1	0	ADC6
1	1	1	ADC7

ADC Conversion Result Register

Bit:	7	6	5	4	3	2	1	0
	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2

Mnemonic: ADCH

Address: E2h

BIT	NAME	FUNCTION
7	ADC.9	Bit 9 of ADC result.
6	ADC.8	Bit 8 of ADC result.
5	ADC.7	Bit 7 of ADC result.
4	ADC.6	Bit 6 of ADC result.
3	ADC.5	Bit 5 of ADC result.
2	ADC.4	Bit 4 of ADC result.
1	ADC.3	Bit 3 of ADC result.
0	ADC.2	Bit 2 of ADC result.

ADC Conversion Enable Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	nADCEN

Mnemonic: ADCCEN

Address: E4h

nADCEN: Enable ADC Function: The default is "1" that disables ADC analog circuit. Clear this bit to enable ADC analog circuit.



Extended Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	-	-	-	EWDI	-	-	-	-

Mnemonic: EIE

Address: E8h

BIT	NAME	FUNCTION
7~5	-	Reserved, will read high
4	EWDI	Enable Watchdog timer interrupt
3~0	-	Reserved, will read high

B Register

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B

Address: F0h

B.7-0: The B register is the standard 8052 register that serves as a second accumulator.

Extended Interrupt Priority

Bit:	7	6	5	4	3	2	1	0
	-	-	-	PWDI	-	-	-	-

Mnemonic: EIP

Address: F8h

BIT	NAME	FUNCTION
7~5	-	Reserved.
4	PWDI	Watchdog Timer Interrupt Priority.
3~0	-	Reserved.



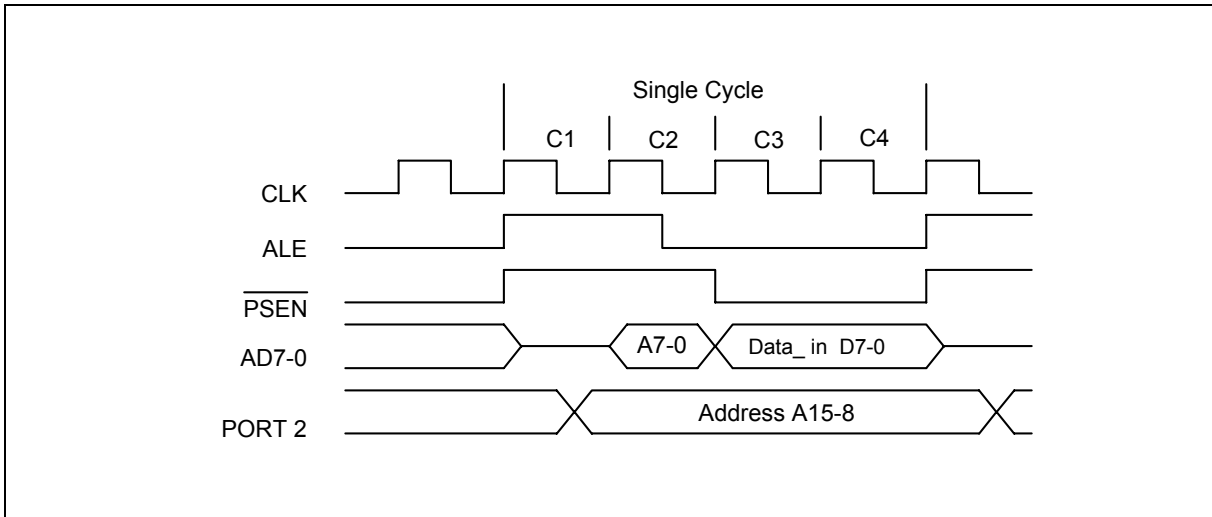
8. INSTRUCTION

The W79E201 executes all the instructions of the standard 8032 family. The operation of these instructions, their effect on the flag bits and the status bits is exactly the same. However, timing of these instructions is different. The reason for this is two fold. Firstly, in the W79E201, each machine cycle consists of 4 clock periods, while in the standard 8032 it consists of 12 clock periods. Also, in the W79E201 there is only one fetch per machine cycle i.e. 4 clocks per fetch, while in the standard 8032 there can be two fetches per machine cycle, which works out to 6 clocks per fetch.

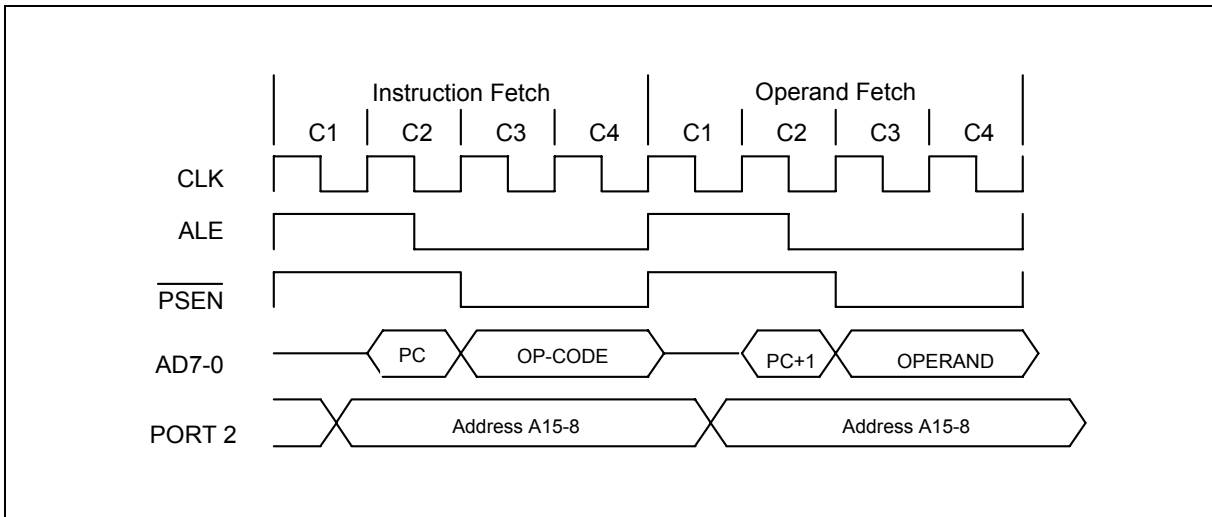
The advantage the W79E201 has is that since there is only one fetch per machine cycle, the number of machine cycles in most cases is equal to the number of operands that the instruction has. In case of jumps and calls there will be an additional cycle that will be needed to calculate the new address. But overall the W79E201 reduces the number of dummy fetches and wasted cycles, thereby improving efficiency as compared to the standard 8032.

8.1 Instruction Timing

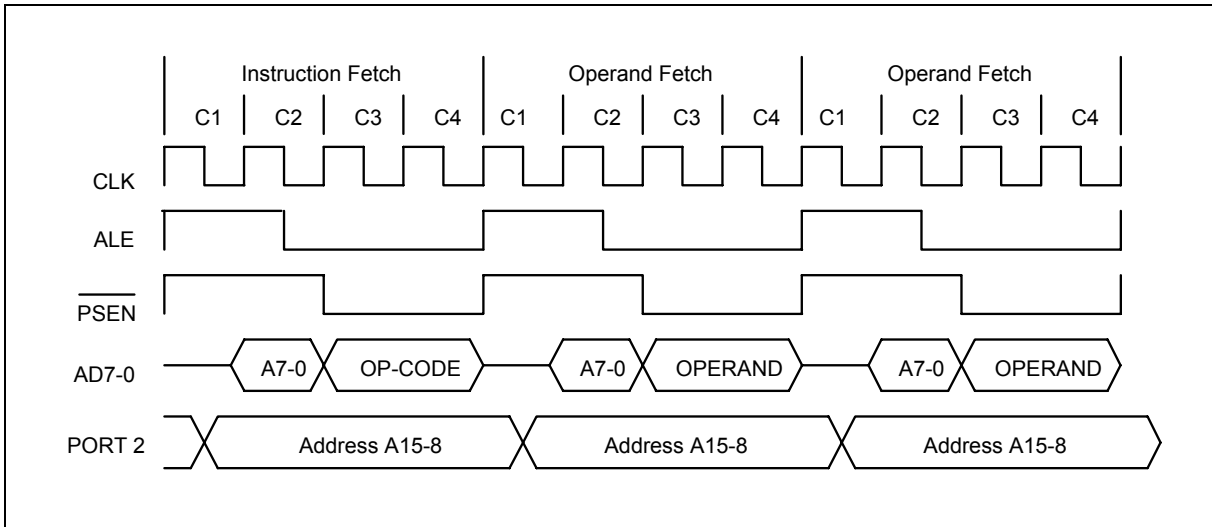
The instruction timing for the W79E201 is an important aspect, especially for those users who wish to use software instructions to generate timing delays. Also, it provides the user with an insight into the timing differences between the W79E201 and the standard 8032. In the W79E201 each machine cycle is four clock periods long. Each clock period is designated a state. Thus each machine cycle is made up of four states, C1, C2 C3 and C4, in that order. Due to the reduced time for each instruction execution, both the clock edges are used for internal timing. Hence it is important that the duty cycle of the clock be as close to 50% as possible to avoid timing conflicts. As mentioned earlier, the W79E201 does one op-code fetch per machine cycle. Therefore, in most of the instructions, the number of machine cycles needed to execute the instruction is equal to the number of bytes in the instruction. Of the 256 available op-codes, 128 of them are single cycle instructions. Thus more than half of all op-codes in the W79E201 are executed in just four clock periods. Most of the two-cycle instructions are those that have two byte instruction codes. However there are some instructions that have only one byte instructions, yet they are two cycle instructions. One instruction which is of importance is the MOVX instruction. In the standard 8032, the MOVX instruction is always two machine cycles long. However in the W79E201, the user has a facility to stretch the duration of this instruction from 2 machine cycles to 9 machine cycles. The RD and WR strobe lines are also proportionately elongated. This gives the user flexibility in accessing both fast and slow peripherals without the use of external circuitry and with minimum software overhead. The rest of the instructions are either three, four or five machine cycle instructions. Note that in the W79E201, based on the number of machine cycles, there are five different types, while in the standard 8032 there are only three. However, in the W79E201 each machine cycle is made of only 4 clock periods compared to the 12 clock periods for the standard 8032. Therefore, even though the number of categories has increased, each instruction is at least 1.5 to 3 times faster than the standard 8032 in terms of clock periods.



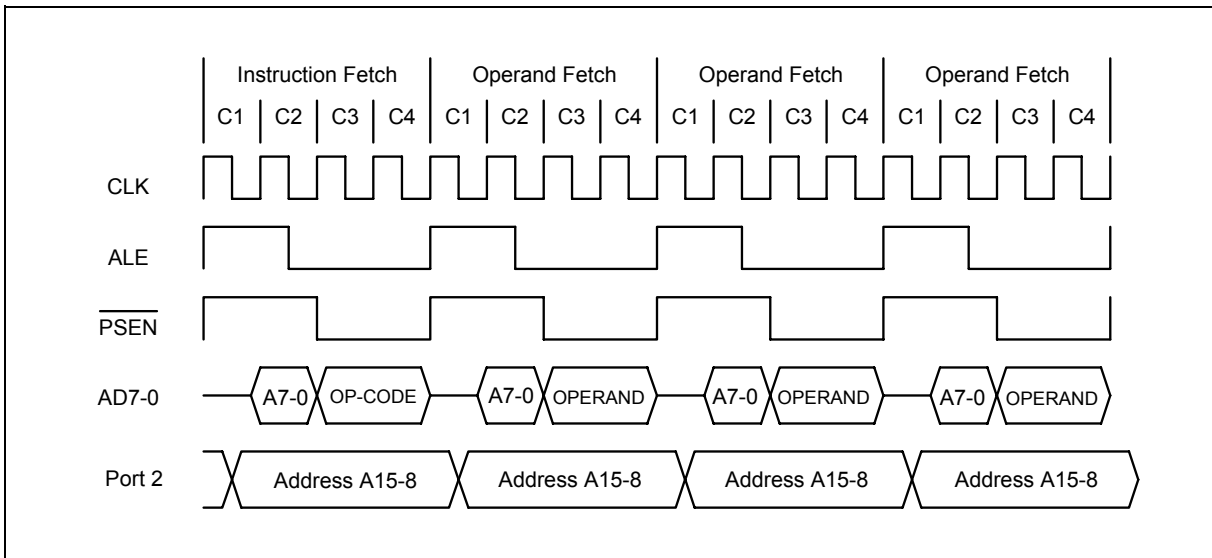
Single Cycle Instruction Timing



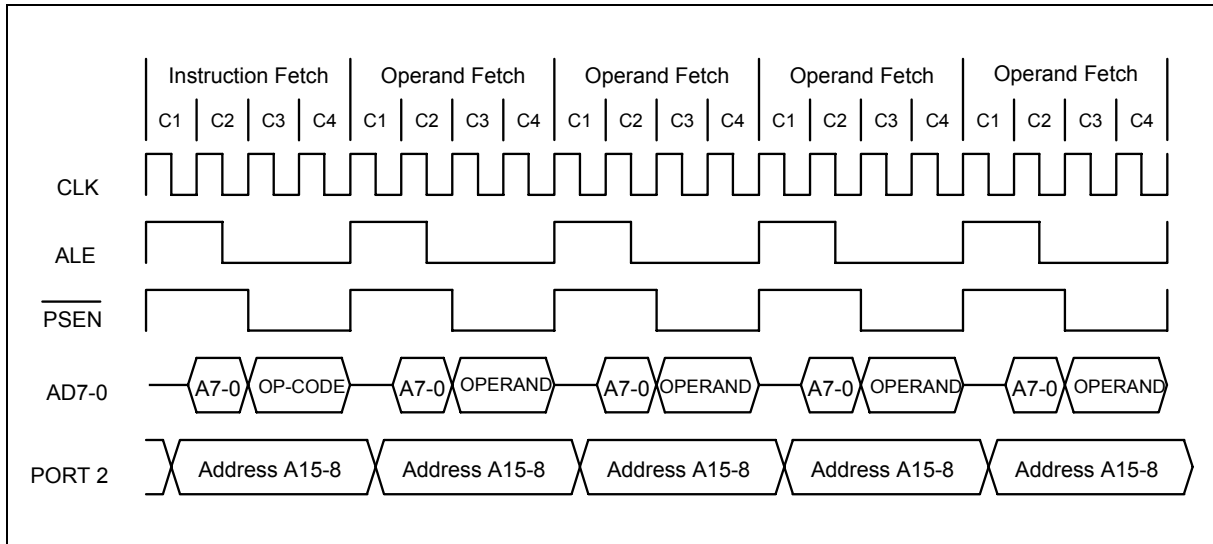
Two Cycle Instruction Timing



Three Cycle Instruction Timing



Four Cycle Instruction Timing



Five Cycle Instruction Timing

8.1.1 External Data Memory Access Timing

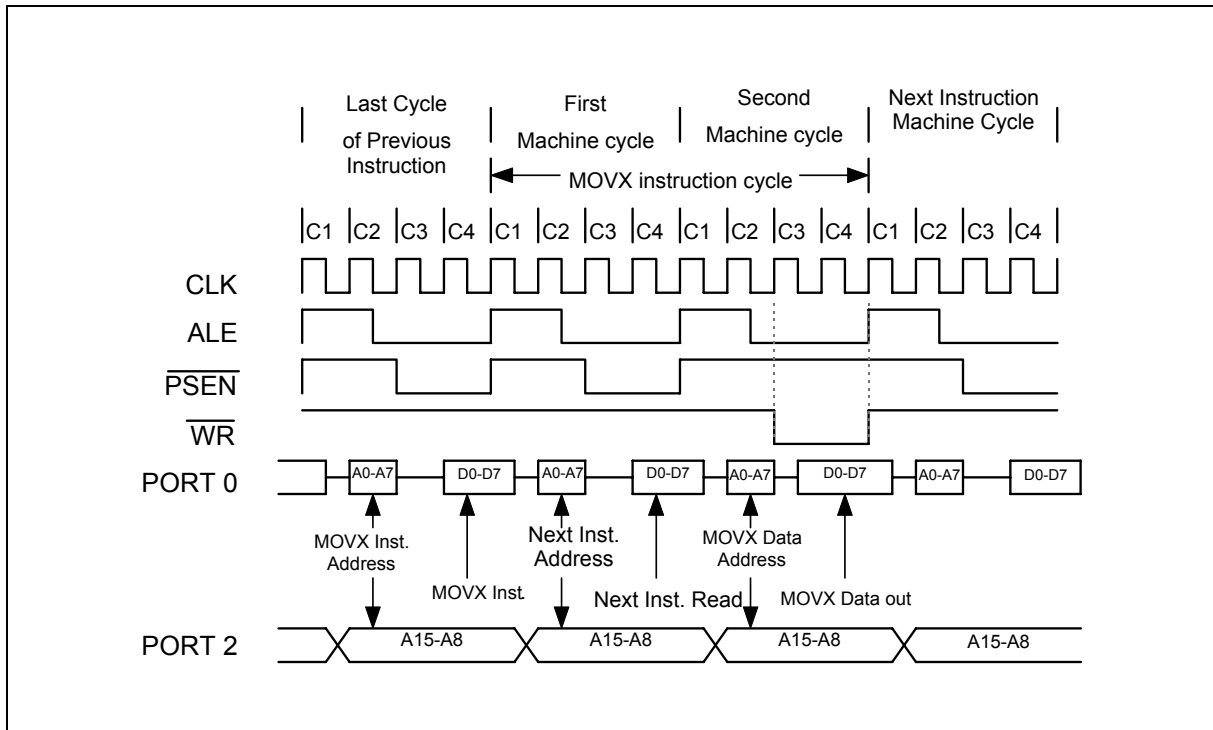
The timing for the MOVX instruction is another feature of the W79E201. In the standard 8032, the MOVX instruction has a fixed execution time of 2 machine cycles. However in the W79E201, the duration of the access can be varied by the user.

The instruction starts off as a normal op-code fetch of 4 clocks. In the next machine cycle, the W79E201 puts out the address of the external Data Memory and the actual access occurs here. The user can change the duration of this access time by setting the STRETCH value. The Clock Control SFR (CKCON) has three bits that control the stretch value. These three bits are M2-0 (bits 2-0 of CKCON). These three bits give the user 8 different access time options. The stretch can be varied from 0 to 7, resulting in MOVX instructions that last from 2 to 9 machine cycles in length. Note that the stretching of the instruction only results in the elongation of the MOVX instruction, as if the state of the CPU was held for the desired period. There is no effect on any other instruction or its timing. By default, the Stretch value is set at 1, giving a MOVX instruction of 3 machine cycles. If desired by the user the stretch value can be set to 0 to give the fastest MOVX instruction of only 2 machine cycles.

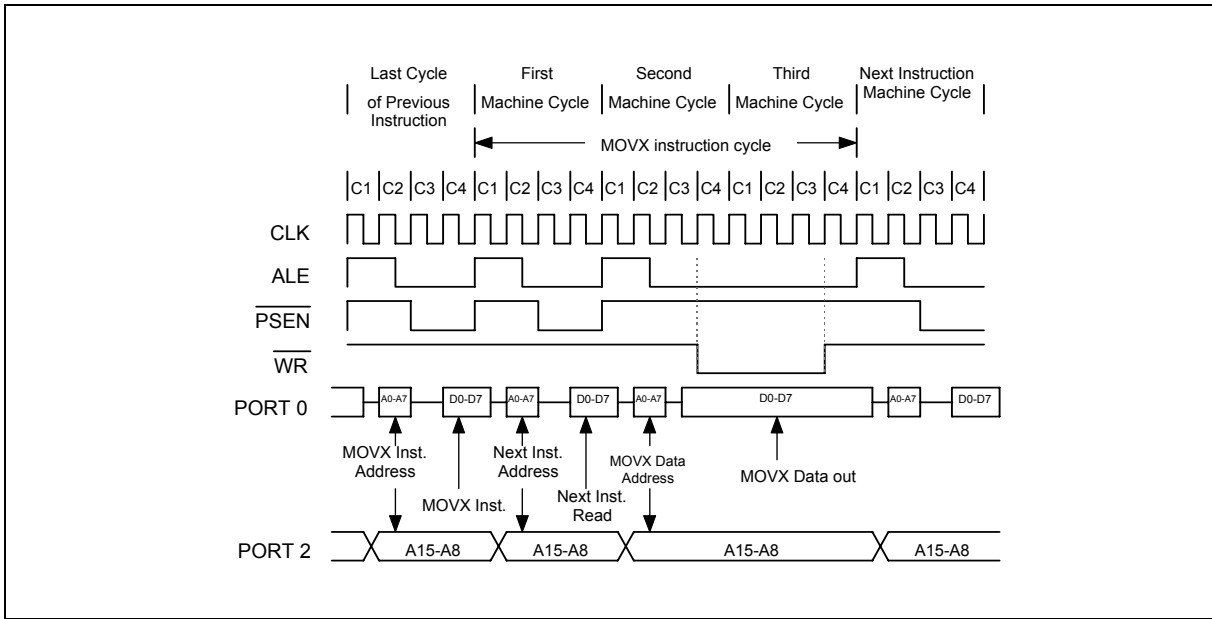


Table 4. Data Memory Cycle Stretch Values

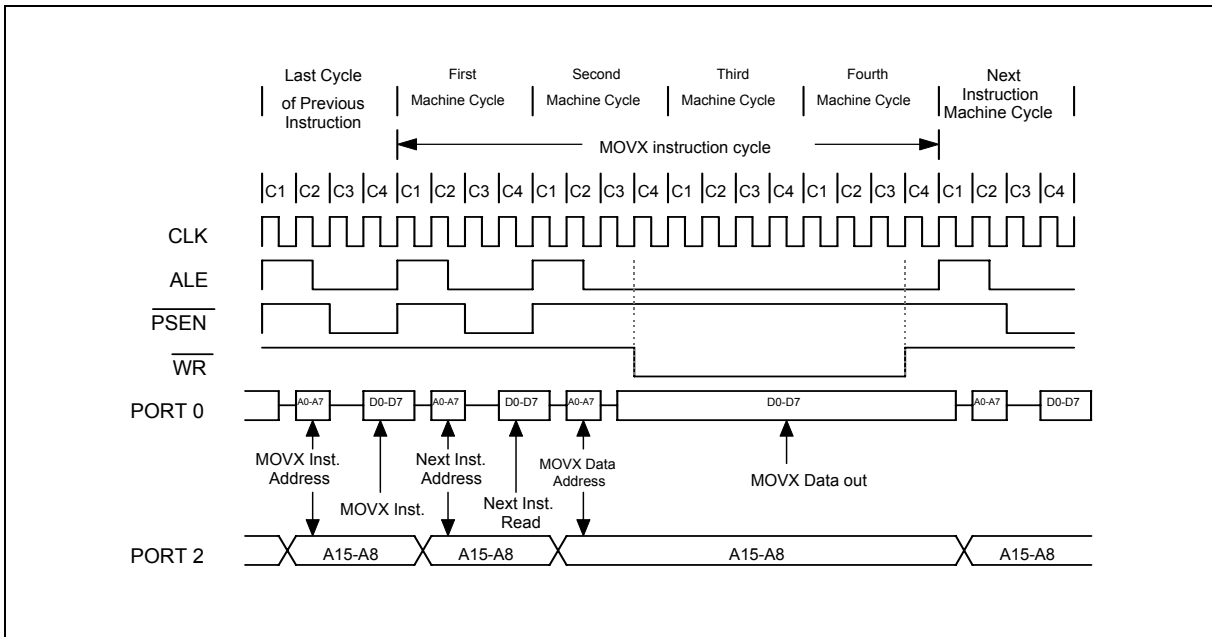
M2	M1	M0	MACHINE CYCLES	RD OR WR STROBE WIDTH IN CLOCKS	RD OR WR STROBE WIDTH @ 25 MHZ	RD OR WR STROBE WIDTH @ 40 MHZ
0	0	0	2	2	80 nS	50 nS
0	0	1	3 (default)	4	160 nS	100 nS
0	1	0	4	8	320 nS	200 nS
0	1	1	5	12	480 nS	300 nS
1	0	0	6	16	640 nS	400 nS
1	0	1	7	20	800 nS	500 nS
1	1	0	8	24	960 nS	600 nS
1	1	1	9	28	1120 nS	700 nS



Data Memory Write with Stretch Value = 0



Data Memory Write with Stretch Value = 1



Data Memory Write with Stretch Value = 2



9. POWER MANAGEMENT

The W79E201 has several features that help the user to control the power consumption of the device. The power saving features is basically the POWER DOWN mode and the IDLE mode of operation.

Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The ALE and PSEN pins are held high during the Idle state. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle mode.

The Idle mode can also be exited by activating the reset. The device can be put into reset either by applying a high on the external RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the W79E201 is exiting from an Idle mode with a reset, the instruction following the one which put the device into Idle mode is not executed. So there is no danger of unexpected writes.

Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. In this state the ALE and PSEN pins are pulled low. The port pins output the values held by their respective SFRs.

The W79E201 will exit the Power Down mode with a reset or by an external interrupt pin enabled as level detect. An external reset can be used to exit the Power down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode.

The W79E201 can be woken from the Power Down mode by forcing an external interrupt pin activated, provided the corresponding interrupt is enabled, while the global enable(EA) bit is set and the external input has been set to a level detect mode. If these conditions are met, then the low level on the external pin re-starts the oscillator. Then device executes the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after the one which put the device into Power Down mode and continues from there.


Table 5. Status of external pins during Idle and Power Down

MODE	PROGRAM MEMORY	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Reset Conditions

The user has several hardware related options for placing the W79E201 into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software. There are two ways of putting the device into reset state. They are External reset and Watchdog reset.

External Reset

The device continuously samples the RST pin at state C4 of every machine cycle. Therefore the RST pin must be held for at least 2 machine cycles to ensure detection of a valid RST high. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain so as long as RST is 1. Even after RST is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h. There is no flag associated with the external reset condition. However since the other two reset sources have flags, the external reset can be considered as the default reset if those two flags are cleared.

The software must clear the POR flag after reading it, otherwise it will not be possible to correctly determine future reset sources. If the power fails, i.e. falls below V_{rst} , then the device will once again go into reset state. When the power returns to the proper operating levels, the device will again perform a power on reset delay and set the POR flag.

Watchdog Timer Reset

The Watchdog timer is a free running timer with programmable time-out intervals. The user can clear the watchdog timer at any time, causing it to restart the count. When the time-out interval is reached an interrupt flag is set. If the Watchdog reset is enabled and the watchdog timer is not cleared, then 512 clocks from the flag being set, the watchdog timer will generate a reset. This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h.

Reset State

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the V_{DD} falls below approximately 2V, as this is the minimum voltage level required for the RAM to operate normally. Therefore after a first time power on reset the



RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost.

After a reset most SFRs are cleared. Interrupts and Timers are disabled. The Watchdog timer is disabled if the reset source was a POR. The ports SFRs have FFh written into them which puts the port pins in a high state. Port 0 floats as it does not have on-chip pull-ups.

Table 6. SFR Reset Value

SFR NAME	RESET VALUE	SFR NAME	RESET VALUE
P0	11111111b	EIP	xxx00000b
SP	00000111b	IP	x0000000b
DPL	00000000b	SADEN	00000000b
DPH	00000000b	PMR	xxxxx0xxb
PCON	00xx0000b	STATUT2	000x0000b
TCON	00000000b	T2CON	00000000b
TMOD	00000000b	T2MOD	00000x00b
TL0	00000000b	RCAP2L	00000000b
TL1	00000000b	RCAP2H	00000000b
TH0	00000000b	TL2	00000000b
TH1	00000000b	TH2	00000000b
CKCON	00000001b	PSW	00000000b
P1	11111111b	WDCON	0x0x0xx0b
SCON	00000000b	PWMP	00000000b
SBUF	xxxxxxxxb	PWMCON1	00000000b
P2	11111111b	PWM0	00000000b
P0R	00000000b	PWM1	00000000b
P4	Xxxxxx1b	PWM2	00000000b
IE	00000000b	PWM3	00000000b
SADDR	00000000b	ACC	00000000b
CHPCON	00000000b	ADCCON	xxxxx000b
SFRAL	00000000b	ADCH	xxxxxxxxb
SFRAH	00000000b	ADCCEN	xxxxxxxx1b
SFRFD	11111111b	PWMCON2	00000000b
SFRCN	00111111b	PWM4	00000000b
P3	11111111b	EIE	xxx00000b
PWM5	00000000b	B	00000000b

The WDCON SFR bits are Set/Cleared in reset condition depending on the source of the reset.

	External reset	Watchdog reset	Power on reset
WDCON	0x0x0xx0b	0x0x01x0b	01000000b

The POR bit WDCON.6 is set only by the power on reset. The WTRF bit WDCON.2 is set when the Watchdog timer causes a reset. A power on reset will also clear this bit. The EWT bit WDCON.1 is



cleared by power on resets. This disables the Watchdog timer resets. A watchdog or external reset does not affect the EWT bit.

10. INTERRUPTS

The W79E201 has a two priority level interrupt structure with 8 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

Interrupt Sources

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be either edge triggered or level triggered, depending on bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Timer 2 interrupt is generated by a logical OR of the TF2 and the EXF2 flags. These flags are set by overflow or capture/reload events in the timer 2 operation. The hardware does not clear these flags when a timer 2 interrupt is executed. Software has to resolve the cause of the interrupt between TF2 and EXF2 and clear the appropriate flag.

The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE.4, then an interrupt will occur.

All the bits that generate interrupts can be set or reset by hardware, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all the interrupts.

Priority Level Structure

There are two priority levels for the interrupts, highest, high and low. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown below; the interrupts are numbered starting from the highest priority to the lowest.


Table 7. Priority structure of interrupts

SOURCE	FLAG	VECTOR ADDRESS	PRIORITY LEVEL
External Interrupt 0	IE0	0003h	1(highest)
ADC Interrupt	ADCI	006Bh	2
Timer 0 Overflow	TF0	000Bh	3
External Interrupt 1	IE1	0013h	4
Timer 1 Overflow	TF1	001Bh	5
Serial Port	RI + TI	0023h	6
Timer 2 Overflow	TF2 + EXF2	002Bh	7
Watchdog Timer	WDIF	0063h	8 (lowest)

11. PROGRAMMABLE TIMERS/COUNTERS

The W79E201 has three 16-bit programmable timer/counters and one programmable Watchdog timer. The Watchdog timer is operationally quite different from the other two timers.

11.1 Timer/Counters 0 & 1

The Timer/Counters 0/1 have two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "C/T" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

Time-Base Selection

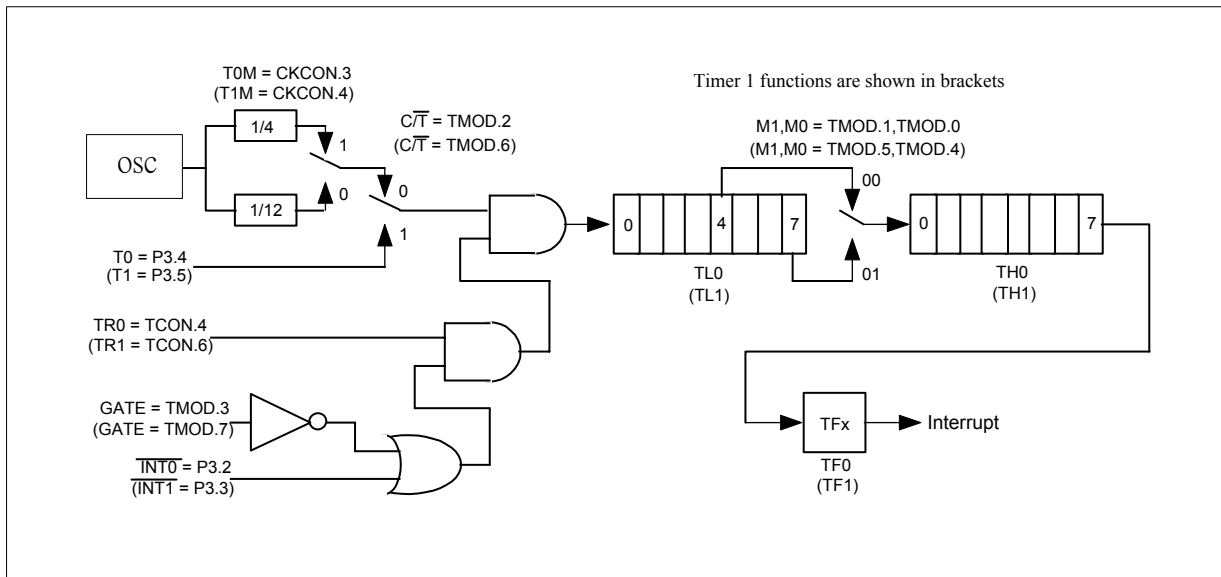
The W79E201 gives the user two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on the W79E201 and the standard 8051 can be matched. This is the default mode of operation of the W79E201 timers. The user also has the option to count in the turbo mode, where the

timers will increment at the rate of 1/4 clock speed. This will straight-away increase the counting speed three times. This selection is done by the T0M and T1M bits in CKCON SFR. A reset sets these bits to 0, and the timers then operate in the standard 8051 mode. The user should set these bits to 1 if the timers are to operate in turbo mode.

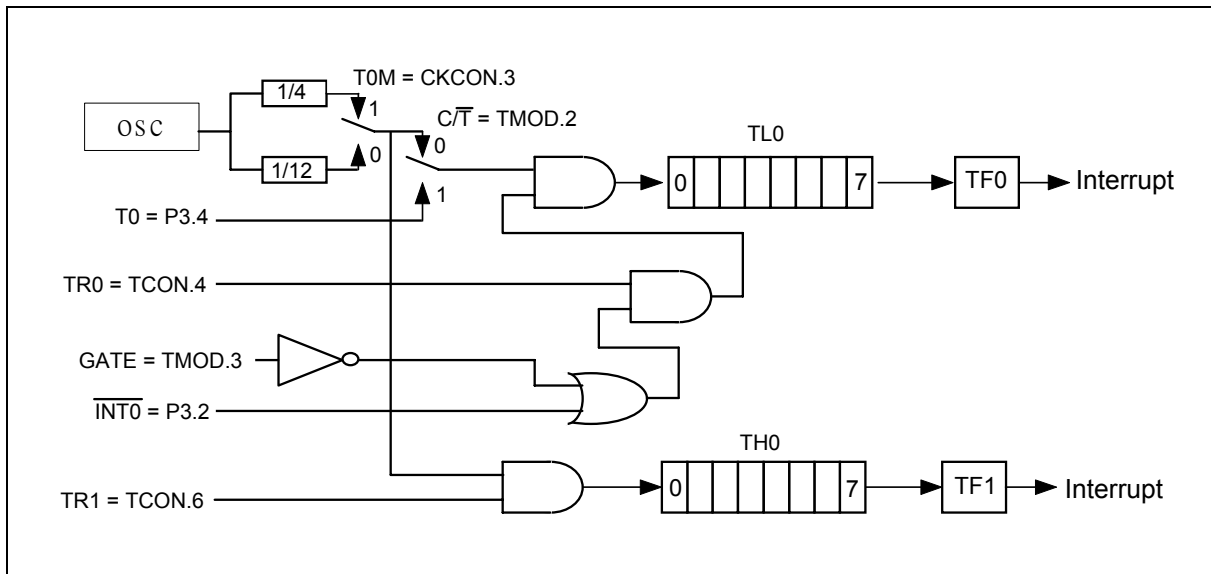
Mode 0

In Mode 0, the timer/counters act as a 8 bit counter with a 5 bit, divide by 32 pre-scale. In this mode we have a 13 bit timer/counter. The 13 bit counter consists of 8 bits of THx and 5 lower bits of TLx. The upper 3 bits of TLx are ignored.

The negative edge of the clock is increments the count in the TLx register. When the fifth bit in TLx moves from 1 to 0, then the count in the THx register is incremented. When the count in THx is moving from FFh to 00h, then the overflow flag \overline{TFx} in TCON SFR is set. The counted input is enabled only if TRx is set and either GATE = 0 or $\overline{INTx} = 1$. When $\overline{C/T}$ is set to 0, then it will count clock cycles, and if $\overline{C/T}$ is set to 1, then it will count 1 to 0 transitions on T0 (P3.4) for timer 0 and T1 (P3.5) for timer 1. When the 13 bit count reaches 1FFFh the next count will cause it to roll-over to 0000h. The timer overflow flag \overline{TFx} of the relevant timer is set and if enabled an interrupts will occur. Note that when used as a timer, the time-base may be either clock cycles/12 or clock cycles/4 as selected by the bits TxM of the CKCON SFR.



Timer/Counter Mode 0 & Mode 1



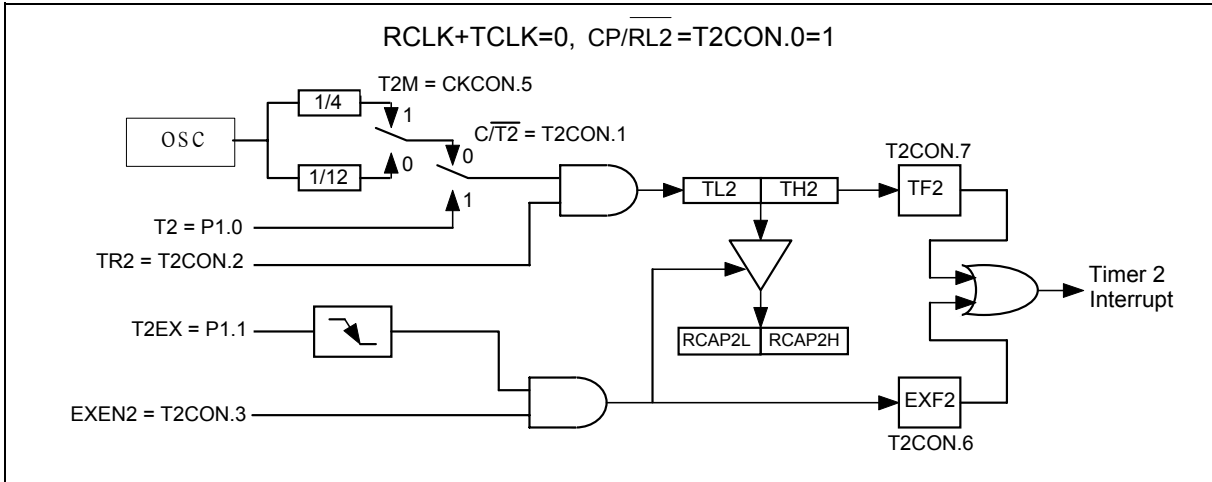
Timer/Counter 0 Mode 3

11.2 Timer/Counter 2

Timer/Counter 2 is a 16 bit up/down counter which is configured by the T2MOD register and controlled by the T2CON register. Timer/Counter 2 is equipped with a capture/reload capability. As with the Timer 0 and Timer 1 counters, there exists considerable flexibility in selecting and controlling the clock, and in defining the operating mode. The clock source for Timer/Counter 2 may be selected for either the external T2 pin ($C/\overline{T2} = 1$) or the crystal oscillator, which is divided by 12 or 4 ($C/\overline{T2} = 0$). The clock is then enabled when TR2 is a 1, and disabled when TR2 is a 0.

Capture Mode

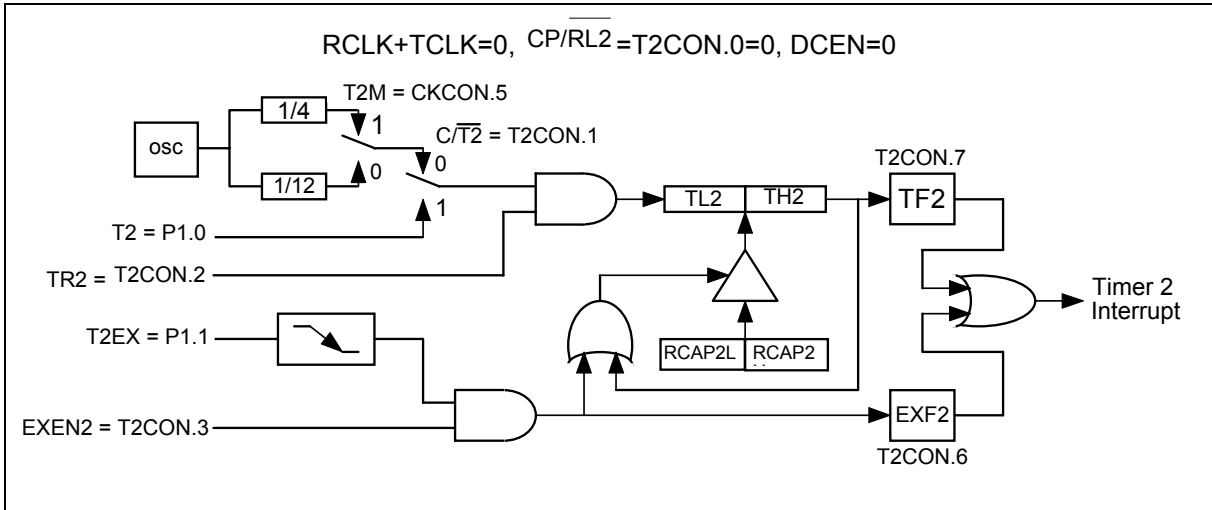
The capture mode is enabled by setting the $\overline{CP/RL2}$ bit in the T2CON register to a 1. In the capture mode, Timer/Counter 2 serves as a 16 bit up counter. When the counter rolls over from FFFFh to 0000h, the TF2 bit is set, which will generate an interrupt request. If the EXEN2 bit is set, then a negative transition of T2EX pin will cause the value in the TL2 and TH2 register to be captured by the RCAP2L and RCAP2H registers. This action also causes the EXF2 bit in T2CON to be set, which will also generate an interrupt. Setting the T2CR bit (T2MOD.3), the W79E201 allows hardware to reset timer 2 automatically after the value of TL2 and TH2 have been captured.



16-Bit Capture Mode

Auto-reload Mode, Counting up

The auto-reload mode as an up counter is enabled by clearing the $\overline{CP/RL2}$ bit in the T2CON register and clearing the DCEN bit in T2MOD register. In this mode, Timer/Counter 2 is a 16 bit up counter. When the counter rolls over from FFFFh, a reload is generated that causes the contents of the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers. The reload action also sets the TF2 bit. If the EXEN2 bit is set, then a negative transition of T2EX pin will also cause a reload. This action also sets the EXF2 bit in T2CON.

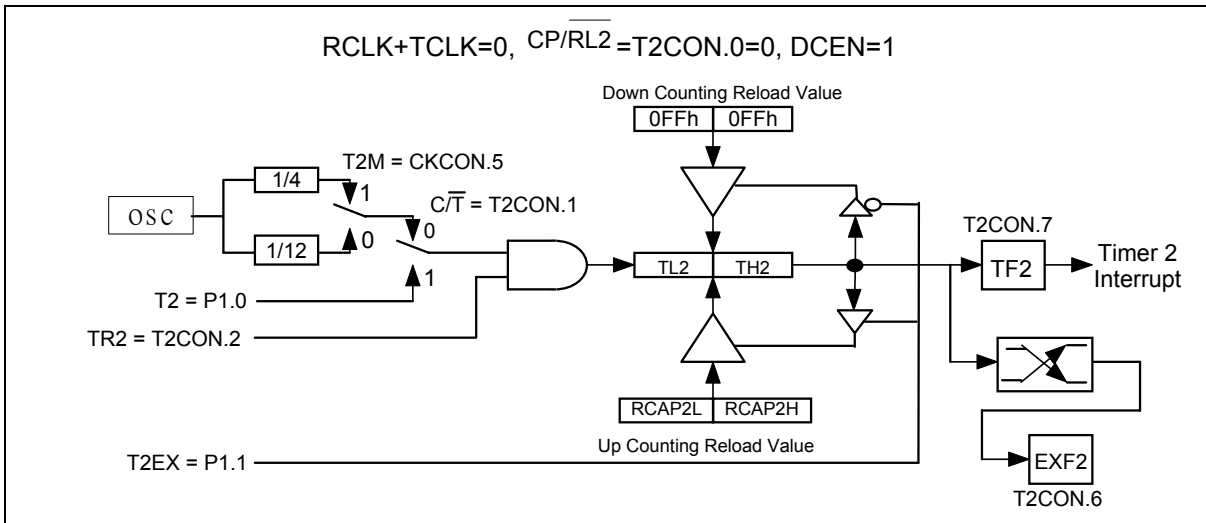


16-Bit Auto-reload Mode, Counting Up



Auto-reload Mode, Counting Up/Down

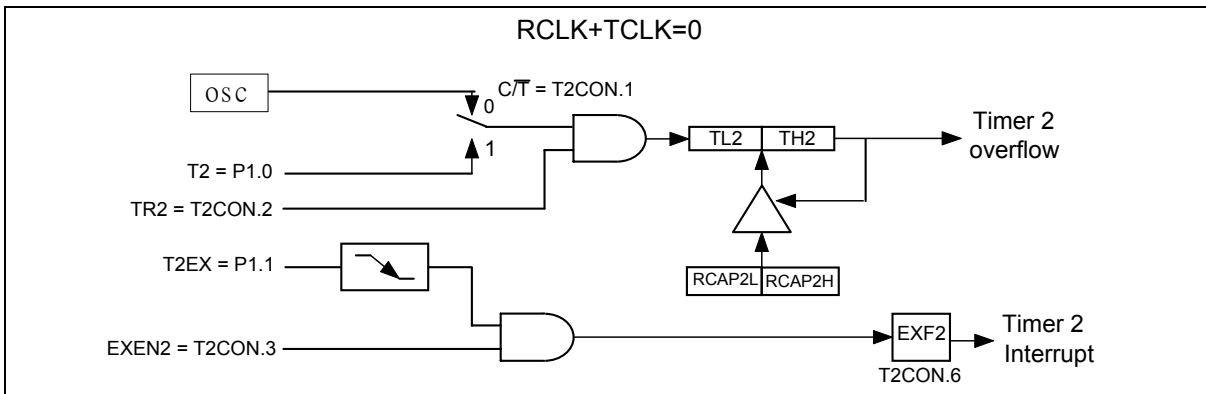
Timer/Counter 2 will be in auto-reload mode as an up/down counter if $\overline{CP/RL2}$ bit in T2CON is cleared and the DCEN bit in T2MOD is set. In this mode, Timer/Counter 2 is an up/down counter whose direction is controlled by the T2EX pin. A 1 on this pin cause the counter to count up. An overflow while counting up will cause the counter to be reloaded with the contents of the capture registers. The next down count following the case where the contents of Timer/Counter equal the capture registers will load an FFFFh into Timer/Counter 2. In either event a reload will set the TF2 bit. A reload will also toggle the EXF2 bit. However, the EXF2 bit can not generate an interrupt while in this mode.



16-Bit Auto-reload Up/Down Counter

Baud Rate Generator Mode

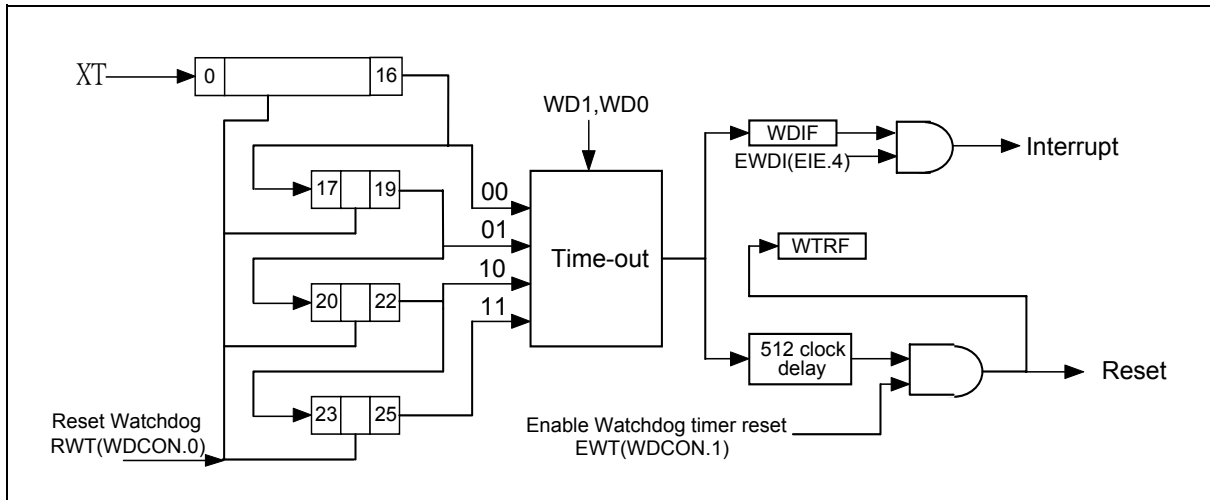
The baud rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. While in the baud rate generator mode, Timer/Counter 2 is a 16 bit counter with auto reload when the count rolls over from FFFFh. However, rolling-over does not set the TF2 bit. If EXEN2 bit is set, then a negative transition of the T2EX pin will set EXF2 bit in the T2CON register and cause an interrupt request.



Baud Rate Generator Mode

12. WATCHDOG TIMER

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the user's software.



Watchdog Timer

The Watchdog timer should first be restarted by using RWT. This ensures that the timer starts from a known state. The RWT bit is used to restart the watchdog timer. This bit is self clearing, i.e. after writing a 1 to this bit the software will automatically clear it. The watchdog timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (CKCON.7 and CKCON.6). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the watchdog timer waits for an additional 512 clock cycles. If the Watchdog Reset EWT (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no RWT, a system reset due to Watchdog timer will occur. This will last for two machine cycles, and the Watchdog timer reset flag WTRF (WDCON.2) will be set. This indicates to the software that the watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the RWT allows software to restart the timer. The Watchdog timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the watchdog timer which will allow the code to run without any watchdog timer interrupts. Now the watchdog timer reset is enabled and the watchdog interrupt may be disabled. If



any errant code is executed now, then the reset watchdog timer instructions will not be executed at the required instants and watchdog reset will occur.

The watchdog time-out selection will result in different time-out values depending on the clock speed. The reset, when enabled, it will occur 512 clocks after the time-out had occurred.

Table 9. Time-out values for the Watchdog timer

WD1	WD0	Watchdog Interval	Number of Clocks	Time @ 1.8432 MHz	Time @ 10 MHz	Time @ 25 MHz
0	0	2^{17}	131072	71.11 mS	13.11 mS	5.24 mS
0	1	2^{20}	1048576	568.89 mS	104.86 mS	41.94 mS
1	0	2^{23}	8388608	4551.11 mS	838.86 mS	335.54 mS
1	1	2^{26}	67108864	36408.88 mS	6710.89 mS	2684.35 mS

The Watchdog timer will be disabled by a power-on/fail reset. The Watchdog timer reset does not disable the watchdog timer, but will restart it. In general, software should restart the timer to put it into a known state.

The control bits that support the Watchdog timer are discussed below.

Watchdog Control

BIT	NAME	FUNCTION
7	-	Reserved.
6	POR	Power-on reset flag. Hardware will set this flag on a power up condition. This flag can be read or written by software. A write by software is the only way to clear this bit once it is set.
5	-	Reserved.
4	-	Reserved.
3	WDIF	Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software.
2	WTRF	Watchdog Timer Reset Flag. Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWT = 0, the watchdog timer will have no effect on this bit.
1	EWT	Enable Watchdog timer Reset. Setting this bit will enable the Watchdog timer Reset function.
0	RWT	Reset Watchdog Timer. This bit helps in putting the watchdog timer into a known state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWT before time-out will cause an interrupt, if EWDI (EIE.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWT is set. This bit is self-clearing by hardware.



Clock Control

WD1, WD0: CKCON.7, CKCON.6 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the watchdog timer. The reset time is 512 clocks longer than the interrupt time-out value.

The default Watchdog time-out is 2^{17} clocks, which is the shortest time-out period. The EWT, WDIF and RWT bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the watchdog timer. Please refer as below demo program.

```

    org    63h
    mov    TA,#AAH
    mov    TA,#55H
    clr    WDIF
    jnb    execute_reset_flag,bypass_reset    ; Test if CPU need to reset.
    jmp    $                                  ; Wait to reset
bypass_reset:
    mov    TA,#AAH
    mov    TA,#55H
    setb   RWT
    reti

    org    300h
start:
    mov    ckcon,#01h    ; select 2 ^ 17 timer
;   mov    ckcon,#61h    ; select 2 ^ 20 timer
;   mov    ckcon,#81h    ; select 2 ^ 23 timer
;   mov    ckcon,#c1h    ; select 2 ^ 26 timer
    mov    TA,#aah
    mov    TA,#55h
    mov    WDCON,#00000011B
    setb   EWDI
    setb   ea
    jmp    $              ; wait time out

```



13. SERIAL PORT

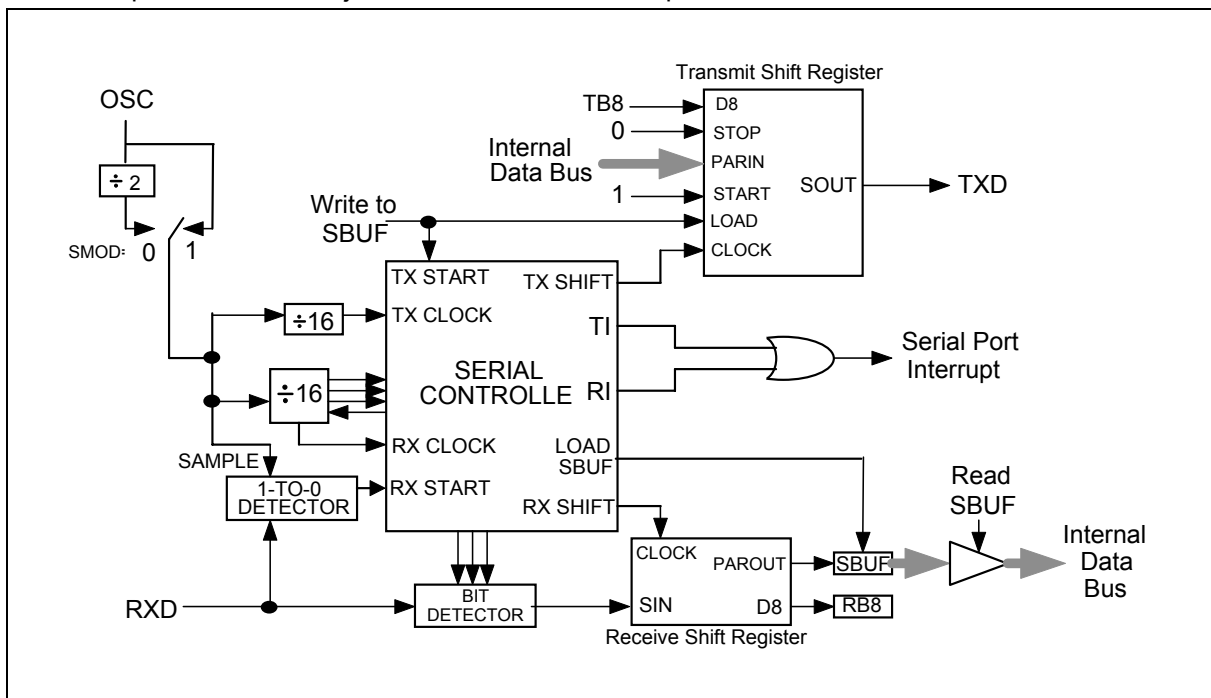
Serial port in the W79E201 is a full duplex port. The W79E201 provides the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial ports are capable of synchronous as well as asynchronous communication. In Synchronous mode the W79E201 generates the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receive buffer register. The serial port can operate in four different modes as described below.

Mode 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the W79E201 whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is Transmitted/Received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This baud rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and the W79E201.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of the W79E201 and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

divide by 16 Counter, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 Counter after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 Counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 Counter. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.



Serial Port Mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

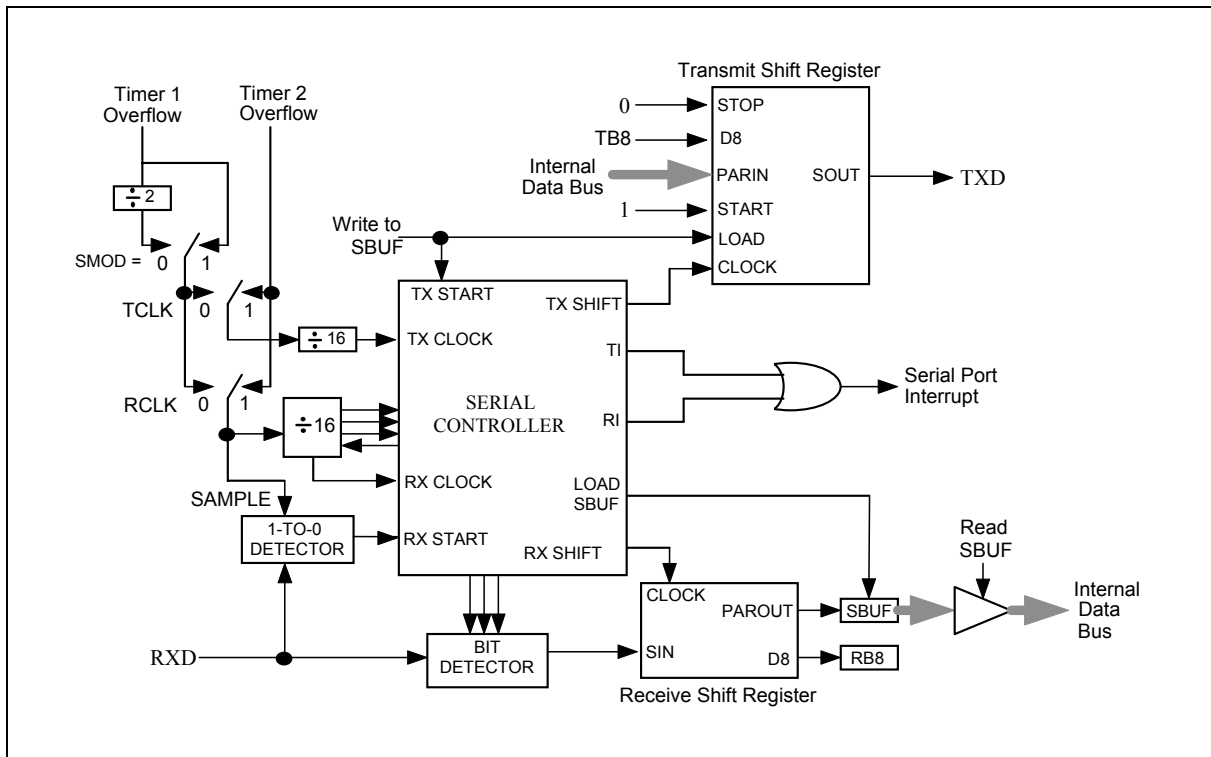
1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

Mode 3



This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.



Serial Port Mode 3

Table 10. Serial Ports Modes

SM1	SM0	Mode	Type	Baud Clock	Frame Size	Start Bit	Stop Bit	9th bit Function
0	0	0	Synch.	4 or 12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1 or 2	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1



13.1 Framing Error Detection

A Frame Error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically the frame error is due to noise and contention on the serial communication line. The W79E201 has the facility to detect such framing errors and set a flag which can be checked by software.

The Frame Error FE(FE_1) bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, in the W79E201 it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is indicated in SM0/FE. When SMOD0 is set to 0, then the SM0 flag is indicated in SM0/FE.

The FE bit is set to 1 by hardware but must be cleared by software. Note that SMOD0 must be 1 while reading or writing to FE. If FE is set, then any following frames received without any error will not clear the FE flag. The clearing has to be done by software.

13.2 Multiprocessor Communications

Multiprocessor communications makes use of the 9th data bit in modes 2 and 3. In the W79E201, the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address, and greatly simplifies the software programmer task.

In the multiprocessor communication mode, the address bytes are distinguished from the data bytes by transmitting the address with the 9th bit set high. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they will be interrupted only by the reception of a address byte. The Automatic address recognition feature ensures that only the addressed slave will be interrupted. The address comparison is done in hardware not software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave will be interrupted on the reception of every single complete frame of data. The unaddressed slaves will be unaffected, as they will be still waiting for their address. In Mode 1, the 9th bit is the stop bit, which is 1 in case of a valid frame. If SM2 is 1, then RI is set only if a valid frame is received and the received byte matches the Given or Broadcast address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

SADDR 1010 0100

SADEN 1111 1010

Given 1010 0x0x



Slave 2:

SADDR 1010 0111

SADEN 1111 1001

Given 1010 0xx1

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is a don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly the bit 1 position is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 3 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical ORing of the SADDR and SADEN SFRs. The zeros in the result are defined as don't cares. In most cases the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN SFRs are located at address A9h and B9h respectively. On reset, these two SFRs are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXX XXXX (i.e. all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled.



14. PULSE WIDTH MODULATED OUTPUTS (PWM)

There are six pulse width modulated output channels to generate pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler PWMP, which supplies the clock for the counter. The prescaler and counter are common to both PWM channels. The 8-bit counter counts modular 255 (0 ~ 254). The value of the 8-bit counter compared to the contents of six registers: PWM0, PWM1, PWM2, PWM3, PWM4 and PWM5. Provided the contents of either these registers is greater than the counter value, the corresponding PWM0, PWM1, PWM2, PWM3, PWM4 or PWM5 output is set HIGH. If the contents of these registers are equal to, or less than the counter value, the output will be LOW. The pulse-width-ratio is defined by the contents of the registers PWM0, PWM1, PWM2, PWM3, PWM4 and PWM5. The pulse-width-ratio is in the range of 0 to 1 and may be programmed in increments of 1/255. ENPWM0, ENPWM1, ENPWM2, ENPWM3, ENPWM4 and ENPWM5 bit will enable or disable PWM output.

Buffered PWM outputs may be used to drive DC motors. The rotation speed of the motor would be proportional to the contents of PWM0/1/2/3/4/5. The repetition frequency F_{pwm} at the PWM0/1/2/3/4/5 output is given by:

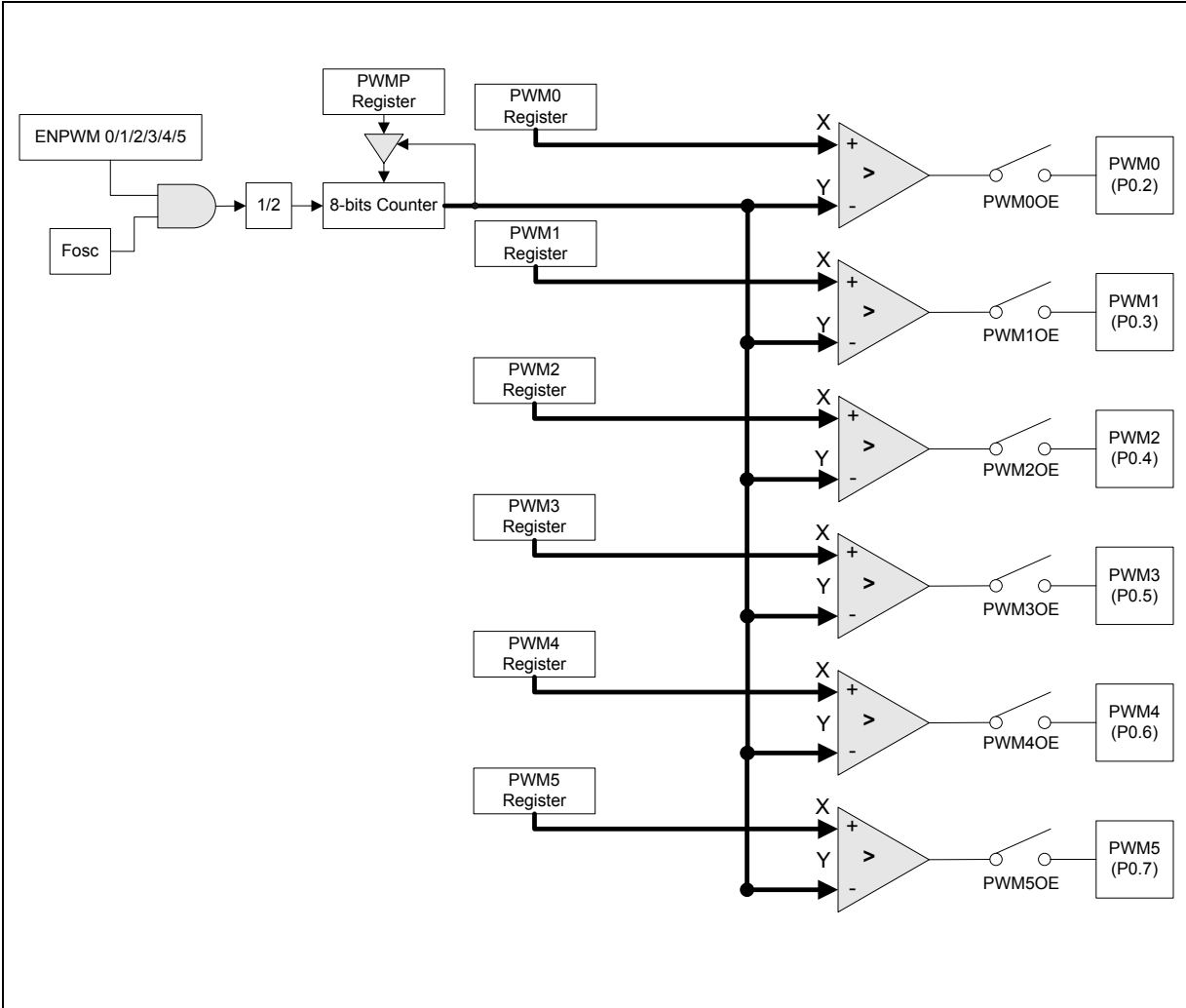
$$F_{pwm} = \frac{F_{osc}}{2 \times (1 + PWMP) \times 255}$$

$$\text{Prescaler division factor} = PWM + 1$$

$$\text{PWMn high/low ratio of PWMn} = \frac{(PWMn)}{255 - (PWMn)}$$

This gives a repetition frequency range of 123 Hz to 31.4K Hz ($f_{osc} = 16\text{M Hz}$). By loading the PWM registers with either 00H or FFH, the PWM channels will output a constant HIGH or LOW level, respectively. Since the 8-bit counter counts modulo 255, it can never actually reach the value of the PWM registers when they are loaded with FFH.

When a compare register (PWM0, PWM1, PWM2, PWM3, PWM4, PWM5) is loaded with a new value, the associated output updated immediately. It does not have to wait until the end of the current counter period. There is weakly pulled high on PWM output.



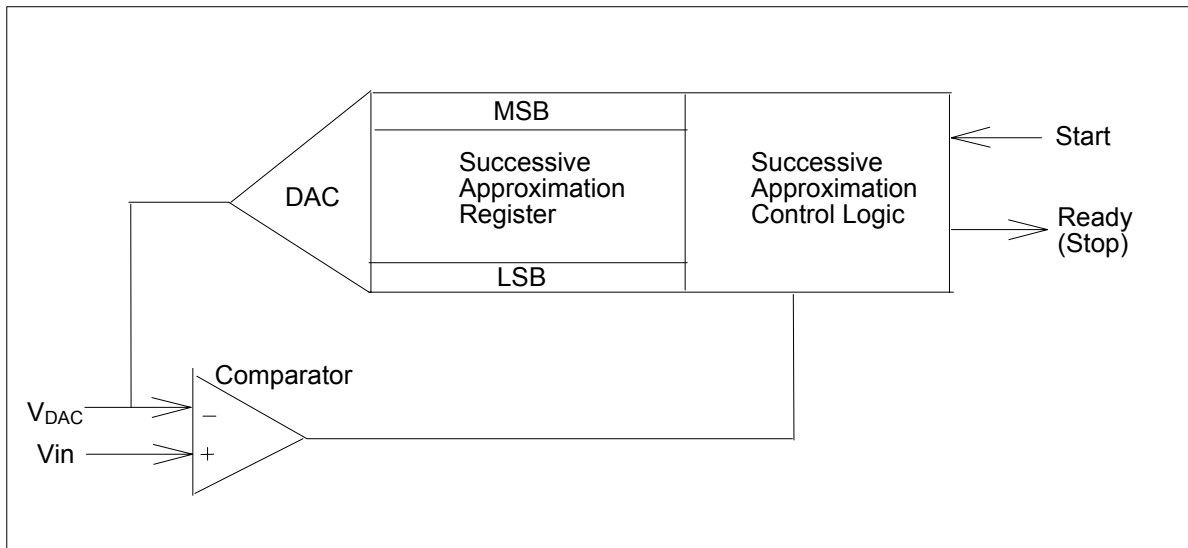
PWM block diagram

15. ANALOG-TO-DIGITAL CONVERTER

The ADC contains a DAC which converts the contents of a successive approximation register to a voltage (V_{DAC}) which is compared to the analog input voltage (V_{in}). The output of the comparator is fed to the successive approximation control logic which controls the successive approximation register. A conversion is initiated by setting ADCS in the ADCCON register. ADCS can be set by software only or by either hardware (P2.0) or software.

Before used ADC circuit, it must enabled by ADCCEN. The software only start mode is selected when control bit ADCCON.5 (ADEX) =0. A conversion is then started by setting control bit ADCCON.3 (ADCS) The hardware or software start mode is selected when ADCCON.5 =1, and a conversion may be started by setting ADCCON.3 as above or by applying a rising edge to external pin STADC. When a conversion is started by applying a rising edge, a low level must be applied to STADC for at least one machine cycle followed by a high level for at least one machine cycle.

The low-to-high transition of STADC is recognized at the end of a machine cycle, and the conversion commences at the beginning of the next cycle.



Successive Approximation ADC

The end of the 10-bit conversion is flagged by control bit ADCCON.4 (ADCI). The upper 8 bits of the result are held in special function register ADCH, and the two remaining bits are held in ADCCON.7 (ADC.1) and ADCCON.6 (ADC.0). The user may ignore the two least significant bits in ADCCON and use the ADC as an 8-bit converter (8 upper bits in ADCH). In any event, the total actual conversion time is 50 machine cycles. ADC will be set and the ADCS status flag will be reset 50 cycles after the ADCS is set.



Control bits ADCCON.0, ADCCON.1 and ADCCON.2 are used to control an analog multiplexer which selects one of eight analog channels. An ADC conversion in progress is unaffected by an external or software ADC start. The result of a completed conversion remains unaffected provided ADCI = logic 1; a new ADC conversion already in progress is aborted when the idle or power down mode is entered. The result of a completed conversion (ADCI = logic 1) remains unaffected when entering the idle mode.

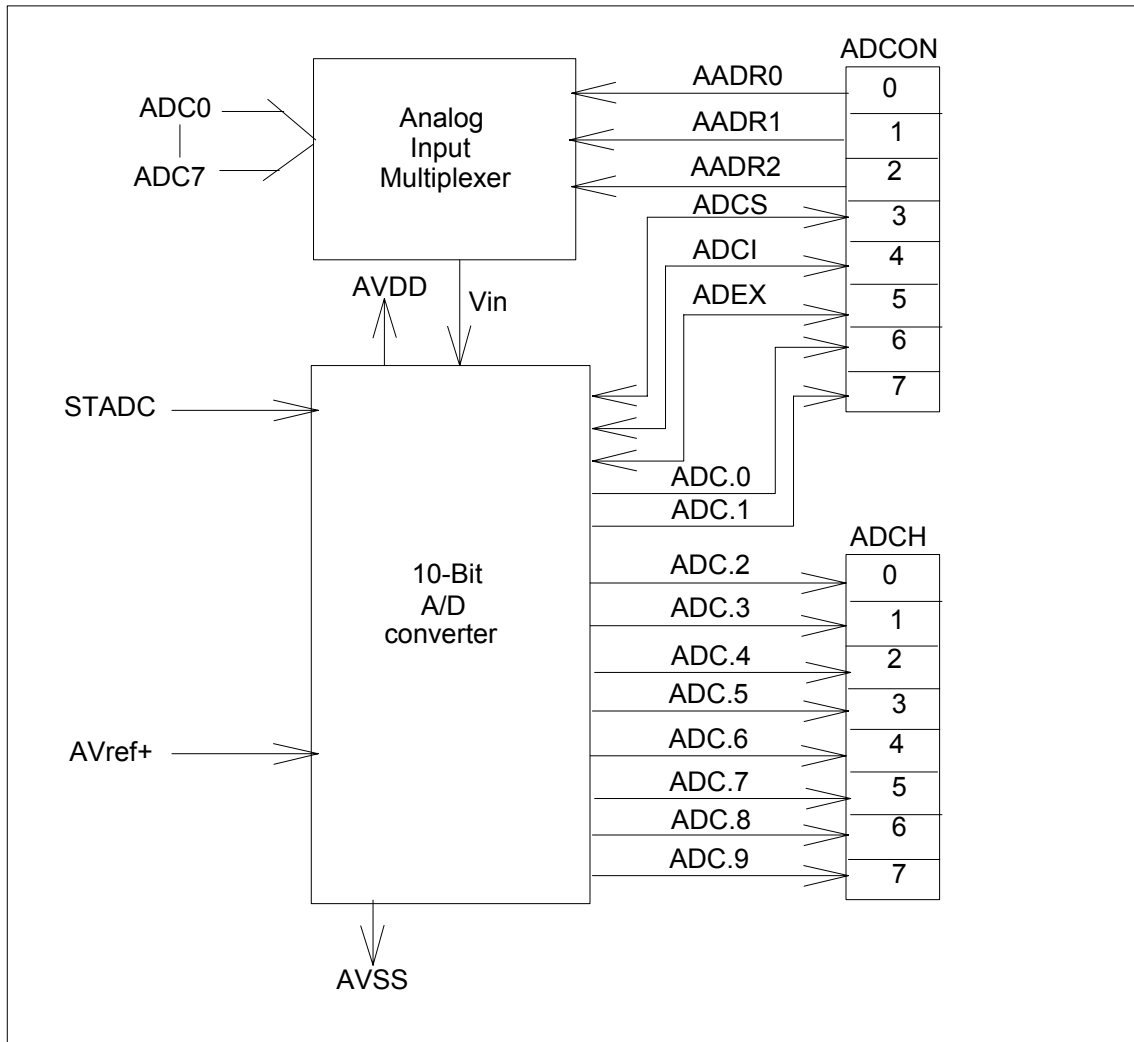
ADC Resolution and Analog Supply:

The ADC has its own supply pins (AVDD and AVSS) and one pins (Vref+) connected to each end of the DAC's resistance-ladder. The ladder has 1023 equally spaced taps, separated by a resistance of "R". The first tap is located 0.5XR above AVSS, and the last tap is located 0.5XR below Vref+. This gives a total ladder resistance of 1024XR. This structure ensures that the DAC is monotonic and results in a symmetrical quantization error.

For input voltages between AVSS and [(Vref+) + 1/2 LSB], the 10-bit result of an A/D conversion will be 00 0000 0000 b = 000H. For input voltages between [(Vref+) – 3/2 LSB] and Vref+, the result of a conversion will be 11 1111 1111B = 3FFH. AVref+ and AVSS may be between AVDD + 0.2V and AVSS – 0.2 V. Avref+ should be positive with respect to AVSS, and the input voltage (Vin) should be between AVref+ and AVSS.

The result can always be calculated from the following formula:

$$\text{Result} = 1024 \times \frac{V_{in}}{AV_{ref+}}$$



ADC Functional block Diagram



16. TIMED ACCESS PROTECTION

The W79E201 has several new features, like the Watchdog timer, on-chip ROM size adjustment, wait state control signal and Power on/fail reset flag, which are crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the W79E201 has a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access (TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```

    TA    REG    0C7h          ; Define new register TA, located at 0C7h
        MOV    TA, #0AAh
        MOV    TA, #055h
  
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Accessing are shown below.

Example 1: Valid access

```

    MOV    TA, #0AAh          3 M/C ; Note: M/C = Machine Cycles
    MOV    TA, #055h          3 M/C
    MOV    WDCON, #00h        3 M/C
  
```

Example 2: Valid access

```

    MOV    TA, #0AAh          3 M/C
    MOV    TA, #055h          3 M/C
    NOP                                1 M/C
    SETB   EWT                  2 M/C
  
```

Example 3: Valid access

```

    MOV    TA, #0Aah          3 M/C
    MOV    TA, #055h          3 M/C
    ORL    WDCON, #00000010B 3M/C
  
```

Example 4: Invalid access

```

    MOV    TA, #0AAh          3 M/C
    MOV    TA, #055h          3 M/C
  
```



```

NOP                1 M/C
NOP                1 M/C
CLR  POR          2 M/C
    
```

Example 5: Invalid Access

```

MOV  TA, #0AAh    3 M/C
NOP                1 M/C
MOV  TA, #055h    3 M/C
SETB EWT          2 M/C
    
```

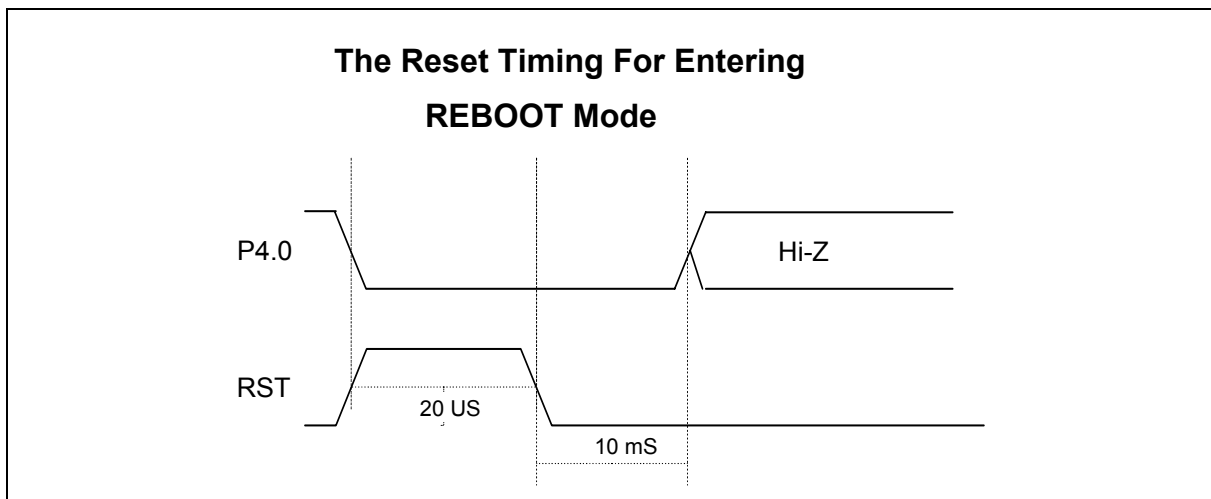
In the first two examples, the writing to the protected bits is done before the 3 machine cycle window closes. In Example 3, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 4, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window is not opened at all, and the write to the protected bit fails.

17. H/W REBOOT MODE (BOOT FROM 4K BYTES OF LD FLASH EPROM)

The W79E201 boots from AP Flash EPROM program (16K bytes) by default at the external reset. On some occasions, user can force W79E201 to boot from the LD Flash EPROM program (4K bytes) at the external reset. The set for this special mode is as follow. It is necessary to add 10K resistor on P4.0 pins.

Reboot Mode

OPTION BITS	RST	P4.0	MODE
Bit3 L	H	L	REBOOT



Notes:

- 1: In application system design, user must take care the P4.0, ALE, /EA and /PSEN pin value at reset to avoid W79E201 entering the programming mode or REBOOT mode in normal operation.

18. IN-SYSTEM PROGRAMMING

18.1 The Loader Program Locates at LD Flash EPROM Memory

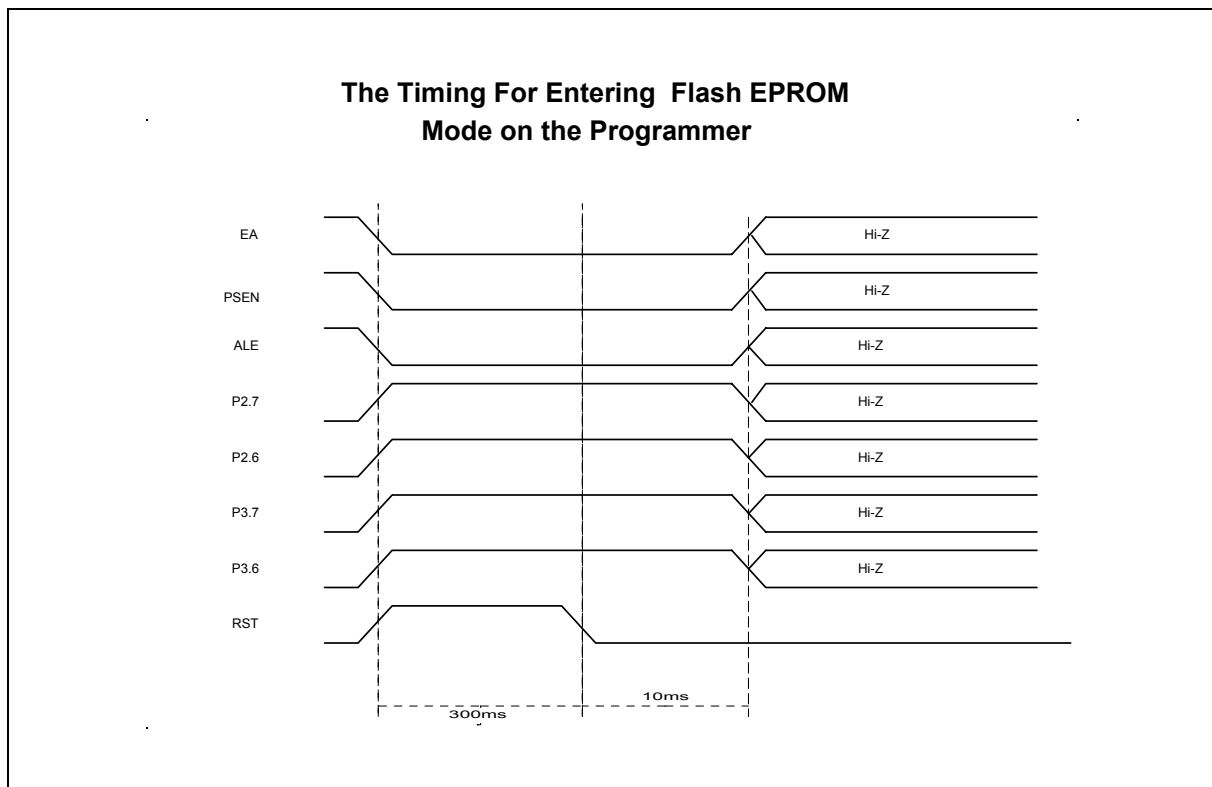
CPU is Free Run at AP Flash EPROM memory. CHPCON register had been set #03H value before CPU has entered idle state. CPU will switch to LD Flash EPROM memory and execute a reset action. H/W reboot mode will switch to LD Flash EPROM memory, too. Set SFRCN register where it locates at user's loader program to update AP Flash EPROM memory. Set a SWRESET (CHPCON=#83H) to switch back AP Flash EPROM after CPU has updated AP Flash EPROM program. CPU will restart to run program from reset state.

18.2 The Loader Program Locates at AP Flash EPROM Memory

CPU is Free Run at AP Flash EPROM memory. CHPCON register had been set #01H value before CPU has entered idle state. Set SFRCN register to update LD Flash EPROM program. CPU will continue to run user's AP Flash EPROM program after CPU has updated program. Please refer demonstrative code to understand other detail description.

19. H/W WRITER MODE

This mode is for the writer to write / read Flash EPROM operation. A general user may not enter this mode.





20. SECURITY BITS

Using device programmer, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below. The W79E201 has Special Setting Register which can be accessed by device programmer. The register can only be accessed from the Flash EPROM operation mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation.

Reserved	B3	B2	B1	B0	Security Bits
----------	----	----	----	----	----------------------

B3: 0 -> Enable H/W reboot with P4.0
 B2: 0 -> Encryption
 B1: 0 -> MOVC Inhibited
 B0: 0 -> Data out lock
 Default 1 for each bit.

B0: Lock bit

This bit is used to protect the customer's program code in the W79E201. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and Special Setting Registers can not be accessed again.

B1: MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

B2: Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.

B3: H/W Reboot with P4.0

If this bit is set to logic 0, enable to reboot 4k LD Flash EPROM mode while RST =H and P4.0 = L state. CPU will start from LD Flash EPROM to update the user's program



21. THE PERFORMANCE CHARACTERISTIC OF ADC

OFFSET ERROR

The offset error is the deviation between ideal transfer value and actual transfer value.

GAIN ERROR

The gain error is the difference between the slope of ideal transfer curve and the slope of actual transfer curve.

DIFFERENTIAL NONLINEARITY (DNL)

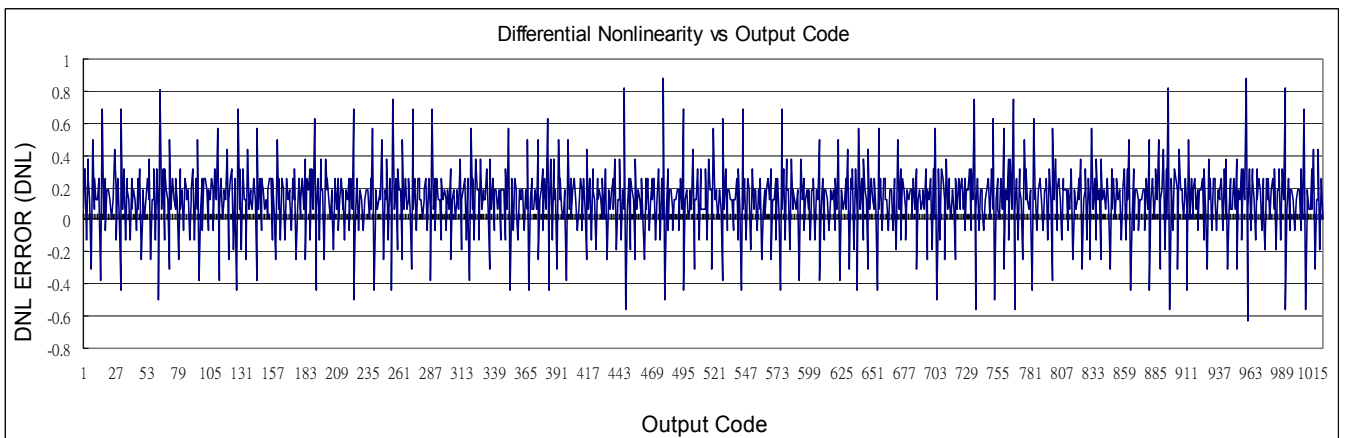
The differential non-linearity is the difference between the actual step width and ideal step width. The ideal step width is 1 LSB. The characteristic of DNL is as below figure.

INTEGRAL NONLINEARITY (INL)

The integral non-linearity is the deviation of a code from actual straight line. The deviation of each code is measured from middle of this code. The characteristic of INL is as below figure.

21.1 The Differential Nonlinearity VS Output code

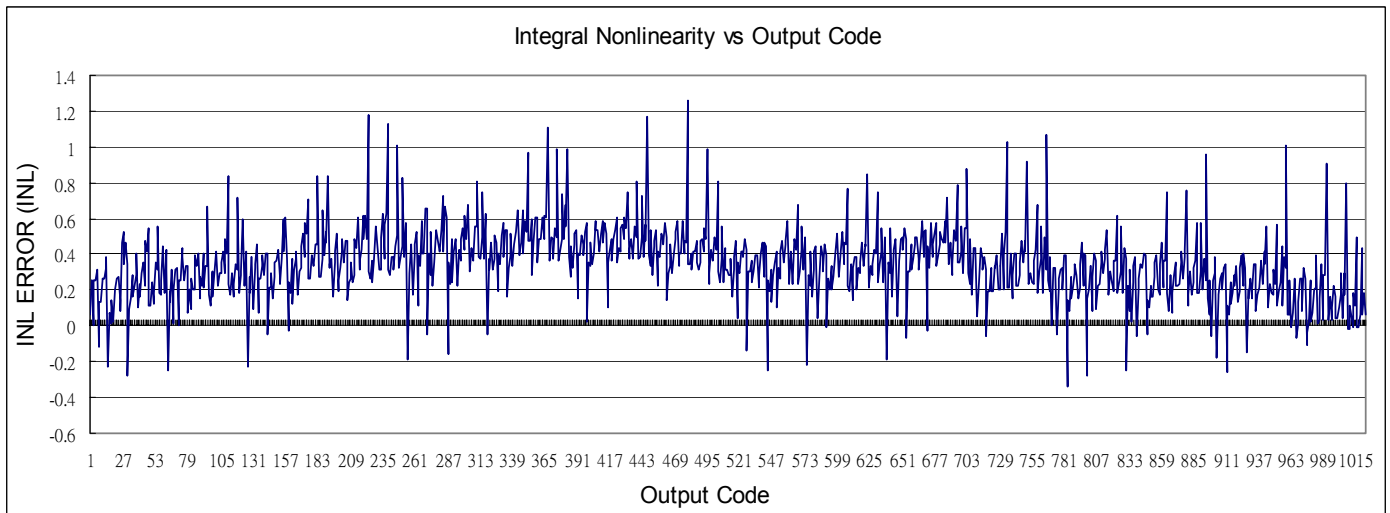
$V_{DD} - V_{SS} = 5V \pm 10\%$, $AV_{DD} - V_{SS} = 5V$, $V_{ref} = 5V$, $T_A = 25^\circ C$, $F_{osc} = 16\text{ MHz}$





21.2 The Integral Nonlinearity VS Output code

$V_{DD} - V_{SS} = 5V \pm 10\%$, $AV_{DD} - V_{SS} = 5V$, $V_{ref} = 5V$, $T_A = 25^\circ C$, $F_{osc} = 16\text{ MHz}$



22. THE EMBEDDED ICE WITH JTAG INTERFACE

The W79E201A16LN is packaged in 48-pins LQFP with the function of in-circuit emulation (ICE). The embedded ICE provides the below functions.

Eight breakpoints to detect program counter

Two enhanced watch breakpoints that can hold program by observing CPU access to data memory and Flash ROM

Read/Write data memory when program holds

Write application code to Flash ROM



23. ELECTRICAL CHARACTERISTICS

23.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITION	RATING	UNIT	
	DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+7.0	V
	Input Voltage	V_{IN}	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
	Operating Temperature	T_A	0	+70	°C
	Storage Temperature	T_{st}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

23.2 DC Characteristics

($V_{DD} - V_{SS} = 5V \pm 10\%$, $T_A = 25^\circ\text{C}$, $F_{osc} = 16\text{ MHz}$, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	4.5	5.5	V	
Operating Current	I_{DD}	-	30	mA	No load $V_{DD} = RST = 5.5V$
Idle Current	I_{IDLE}	-	24	mA	Idle mode $V_{DD} = 5.5V$
Power Down Current	I_{PWDN}	-	10	μA	Power-down mode $V_{DD} = 5.5V$
Input Current P1, P2, P3	I_{IN1}	-50	+10	μA	$V_{DD} = 5.5V$ $V_{IN} = 0V$ or V_{DD}
Input Current RST ^[*1]	I_{IN2}	-10	+120	μA	$V_{DD} = 5.5V$ $0 < V_{IN} < V_{DD}$
Input Leakage Current P0, \overline{EA}	I_{LK}	-10	+10	μA	$V_{DD} = 5.5V$ $0V < V_{IN} < V_{DD}$
Logic 1 to 0 Transition Current P1, P2, P3	I_{TL} ^[*4]	-500	-200	μA	$V_{DD} = 5.5V$ $V_{IN} = 2.0V$
Input Low Voltage P0, P1, P2, P3, \overline{EA}	V_{IL1}	0	0.8	V	$V_{DD} = 4.5V$
Input Low Voltage RST ^[*1]	V_{IL2}	0	0.8	V	$V_{DD} = 4.5V$



DC Characteristics, continued

PARAMETER	SYMBOL	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Input Low Voltage XTAL1 ^[*3]	V_{IL3}	0	0.8	V	$V_{DD} = 4.5V$
Input High Voltage P0, P1, P2, P3, \overline{EA}	V_{IH1}	2.4	$V_{DD} + 0.2$	V	$V_{DD} = 5.5V$
Input High Voltage RST	V_{IH2}	3.5	$V_{DD} + 0.2$	V	$V_{DD} = 5.5V$
Input High Voltage XTAL1 ^[*3]	V_{IH3}	3.5	$V_{DD} + 0.2$	V	$V_{DD} = 5.5V$
Sink current P1, P3	I_{SK1}	4	10	mA	$V_{DD} = 4.5V$ $V_S = 0.45V$
Sink current P0, P2, ALE, \overline{PSEN}	I_{SK2}	8	12	mA	$V_{DD} = 4.5V$ $V_{OL} = 0.45V$
Source current P1, P3	I_{SR1}	-180	-360	μA	$V_{DD} = 4.5V$ $V_{OL} = 2.4V$
Source current P0, P2, ALE, \overline{PSEN}	I_{SR2}	-10	-14	mA	$V_{DD} = 4.5V$ $V_{OL} = 2.4V$
Output Low Voltage P1, P3	V_{OL1}	-	0.45	V	$V_{DD} = 4.5V$ $I_{OL} = +6 \text{ mA}$
Output Low Voltage P0, P2, ALE, \overline{PSEN} ^[*2]	V_{OL2}	-	0.45	V	$V_{DD} = 4.5V$ $I_{OL} = +10 \text{ mA}$
Output High Voltage P1, P3	V_{OH1}	2.4	-	V	$V_{DD} = 4.5V$ $I_{OH} = -180 \mu A$
Output High Voltage P0, P2, ALE, \overline{PSEN} ^[*2]	V_{OH2}	2.4	-	V	$V_{DD} = 4.5V$ $I_{OH} = -10 \text{ mA}$

Notes:

- *1. RST pin is a Schmitt trigger input.
- *2. P0, ALE and \overline{PSEN} are tested in the external access mode.
- *3. XTAL1 is a CMOS input.
- *4. Pins of P1, P2, P3 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} approximates to 2V.

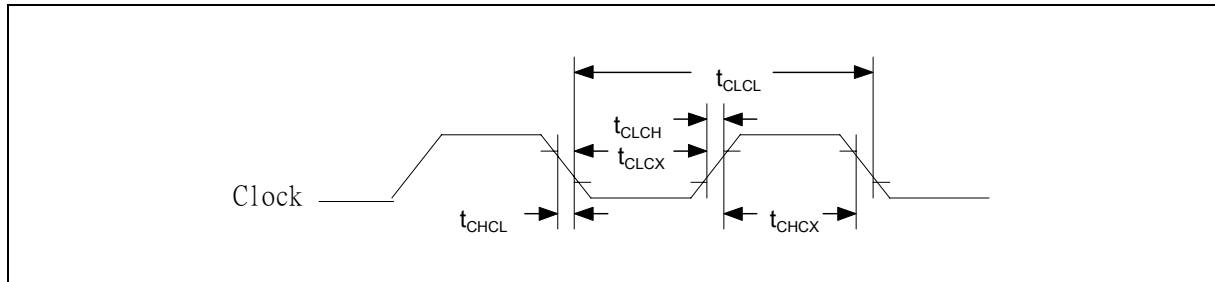


23.3 ADC DC Electrical Characteristics

($AV_{DD} - AV_{SS} = 5V \pm 10\%$, $T_A = 25^\circ C$, $F_{osc} = 16MHz$, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Analog input	AVin	AVSS-0.2	AVDD+0.2	V	
Reference voltage	AVref	-	AVDD+0.2	V	
Resistance between AVref and AVSS	Rref	10	50	KΩ	When ADC is enabled
Conversion time	t _c		52t _{MC}	μs	t _{MC} is machine cycle
Offset error	Ofe	-2	+2	LSB	
Gain error	Ge	-0.4	+0.4	%	
Differential non-linearity	DNL	-1	+1	LSB	
Integral non-linearity	INL	-2	+2	LSB	

23.4 AC Characteristics



Note: Duty cycle is 50%.

External Clock Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t _{CHCX}	12	-	-	nS	
Clock Low Time	t _{CLCX}	12	-	-	nS	
Clock Rise Time	t _{CLCH}	-	-	10	nS	
Clock Fall Time	t _{CHCL}	-	-	10	nS	

23.4.1 AC Specification

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	16	MHz
ALE Pulse Width	t_{LHLL}	$1.5t_{CLCL} - 5$		nS
Address Valid to ALE Low	t_{AVLL}	$0.5t_{CLCL} - 5$		nS
Address Hold After ALE Low	t_{LLAX1}	$0.5t_{CLCL} - 5$		nS
Address Hold After ALE Low for MOVX Write	t_{LLAX2}	$0.5t_{CLCL} - 5$		nS
ALE Low to Valid Instruction In	t_{LLIV}		$2.5t_{CLCL} - 20$	nS
ALE Low to PSEN Low	t_{LLPL}	$0.5t_{CLCL} - 5$		nS
\overline{PSEN} Pulse Width	t_{PLPH}	$2.0t_{CLCL} - 5$		nS
\overline{PSEN} Low to Valid Instruction In	t_{PLIV}		$2.0t_{CLCL} - 20$	nS
Input Instruction Hold After PSEN	t_{PXIX}	0		nS
Input Instruction Float After PSEN	t_{PXIZ}		$t_{CLCL} - 5$	nS
Port 0 Address to Valid Instr. In	t_{AVIV1}		$3.0t_{CLCL} - 20$	nS
Port 2 Address to Valid Instr. In	t_{AVIV2}		$3.5t_{CLCL} - 20$	nS
\overline{PSEN} Low to Address Float	t_{PLAZ}	0		nS
Data Hold After Read	t_{RHDX}	0		nS
Data Float After Read	t_{RHDZ}		$t_{CLCL} - 5$	nS
\overline{RD} Low to Address Float	t_{RLAZ}		$0.5t_{CLCL} - 5$	nS

23.4.2 MOVX Characteristics Using Stretch Memory Cycle

PARAMETER	SYM.	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS	STRECH
Data Access ALE Pulse Width	t_{LLHL2}	$1.5t_{CLCL} - 5$ $2.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS} > 0$
Address Hold After ALE Low for MOVX write	t_{LLAX2}	$0.5t_{CLCL} - 5$		nS	
\overline{RD} Pulse Width	t_{RLRH}	$2.0t_{CLCL} - 5$ $t_{MCS} - 10$		nS	$t_{MCS} = 0$ $t_{MCS} > 0$
\overline{WR} Pulse Width	t_{WLWH}	$2.0t_{CLCL} - 5$ $t_{MCS} - 10$		nS	$t_{MCS} = 0$ $t_{MCS} > 0$
\overline{RD} Low to Valid Data In	t_{RLDV}		$2.0t_{CLCL} - 20$ $t_{MCS} - 20$	nS	$t_{MCS} = 0$ $t_{MCS} > 0$
Data Hold after Read	t_{RHDX}	0		nS	
Data Float after Read	t_{RHDZ}		$t_{CLCL} - 5$ $2.0t_{CLCL} - 5$	nS	$t_{MCS} = 0$ $t_{MCS} > 0$
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL} - 5$ $t_{MCS} + 2t_{CLCL} - 40$	nS	$t_{MCS} = 0$ $t_{MCS} > 0$
Port 0 Address to Valid Data In	t_{AVDV1}		$3.0t_{CLCL} - 20$ $2.0t_{CLCL} - 5$	nS	$t_{MCS} = 0$ $t_{MCS} > 0$
ALE Low to \overline{RD} or \overline{WR} Low	t_{LLWL}	$0.5t_{CLCL} - 5$ $1.5t_{CLCL} - 5$	$0.5t_{CLCL} + 5$ $1.5t_{CLCL} + 5$	nS	$t_{MCS} = 0$ $t_{MCS} > 0$
Port 0 Address to \overline{RD} or \overline{WR} Low	t_{AVWL}	$t_{CLCL} - 5$ $2.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS} > 0$
Port 2 Address to \overline{RD} or \overline{WR} Low	t_{AVWL2}	$1.5t_{CLCL} - 5$ $2.5t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS} > 0$
Data Valid to WR Transition	t_{QVWX}	-5 $1.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS} > 0$
Data Hold after Write	t_{WHQX}	$t_{CLCL} - 5$ $2.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS} > 0$
\overline{RD} Low to Address Float	t_{RLAZ}		$0.5t_{CLCL} - 5$	nS	
\overline{RD} or WR high to ALE high	t_{WHLH}	0 $1.0t_{CLCL} - 5$	10 $1.0t_{CLCL} + 5$	nS	$t_{MCS} = 0$ $t_{MCS} > 0$



Note: The t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the time period of the t_{MCS} for each selection of the Stretch value.

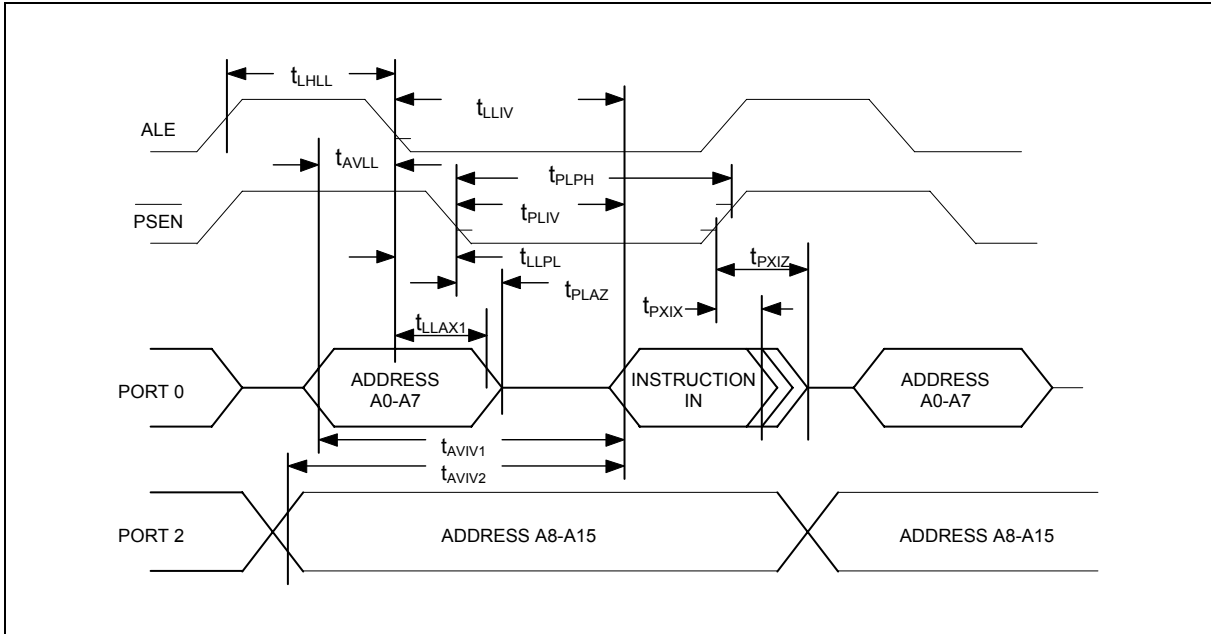
M2	M1	M0	MOVX Cycles	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

Explanation of Logics Symbols

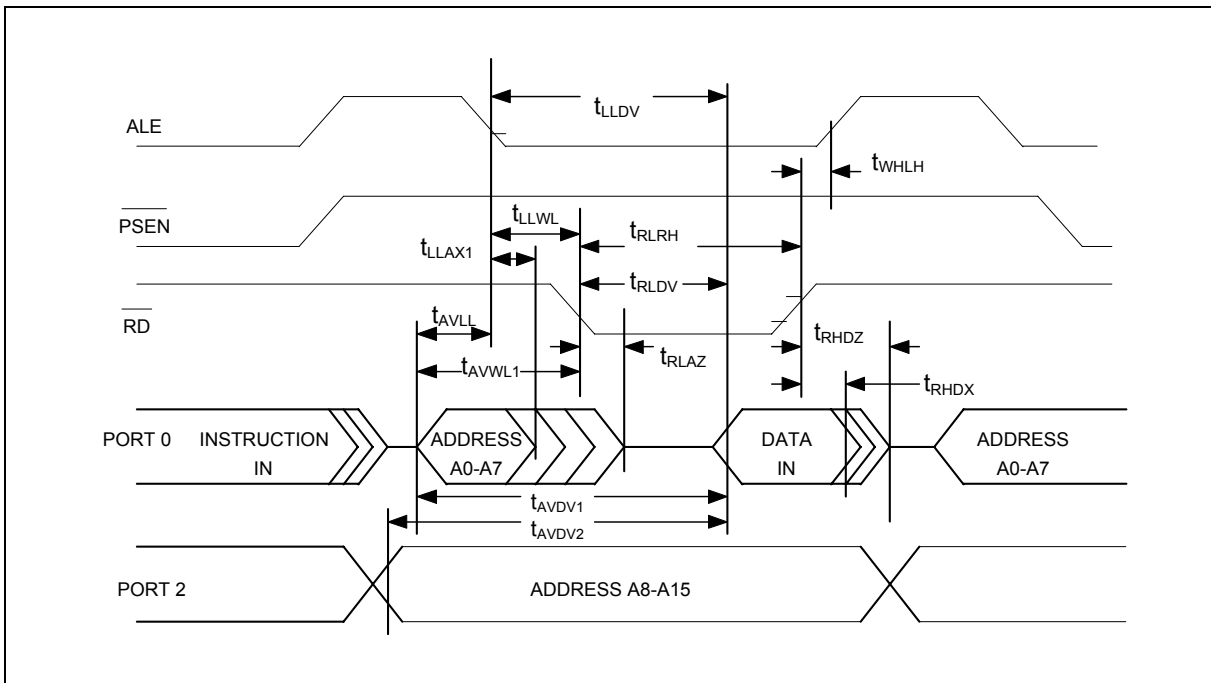
In order to maintain compatibility with the original 8051 family, this device specifies the same parameter for each device, using the same symbols. The explanation of the symbols is as follows.

t	Time	A	Address
C	Clock	D	Input Data
H	Logic level high	L	Logic level low
I	Instruction	P	\overline{PSEN}
Q	Output Data	R	\overline{RD} signal
V	Valid	W	\overline{WR} signal
X	No longer a valid state	Z	Tri-state

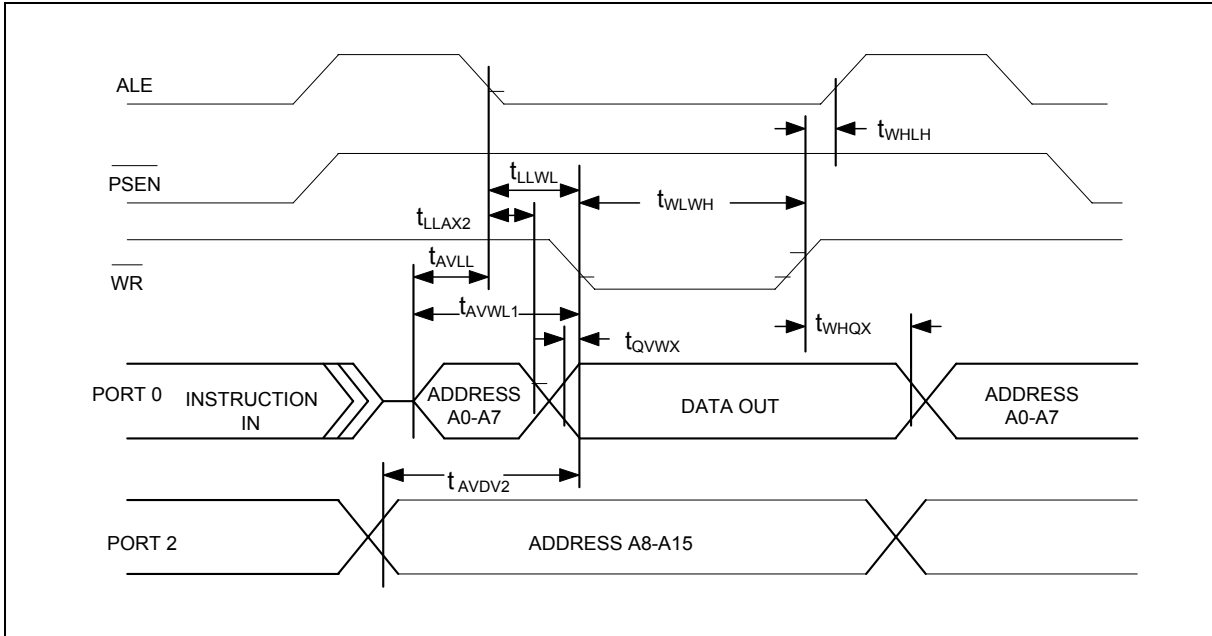
23.4.3 Program Memory Read Cycle



23.4.4 Data Memory Read Cycle



23.4.5 Data Memory Write Cycle



Expanded External Data Memory and Oscillator

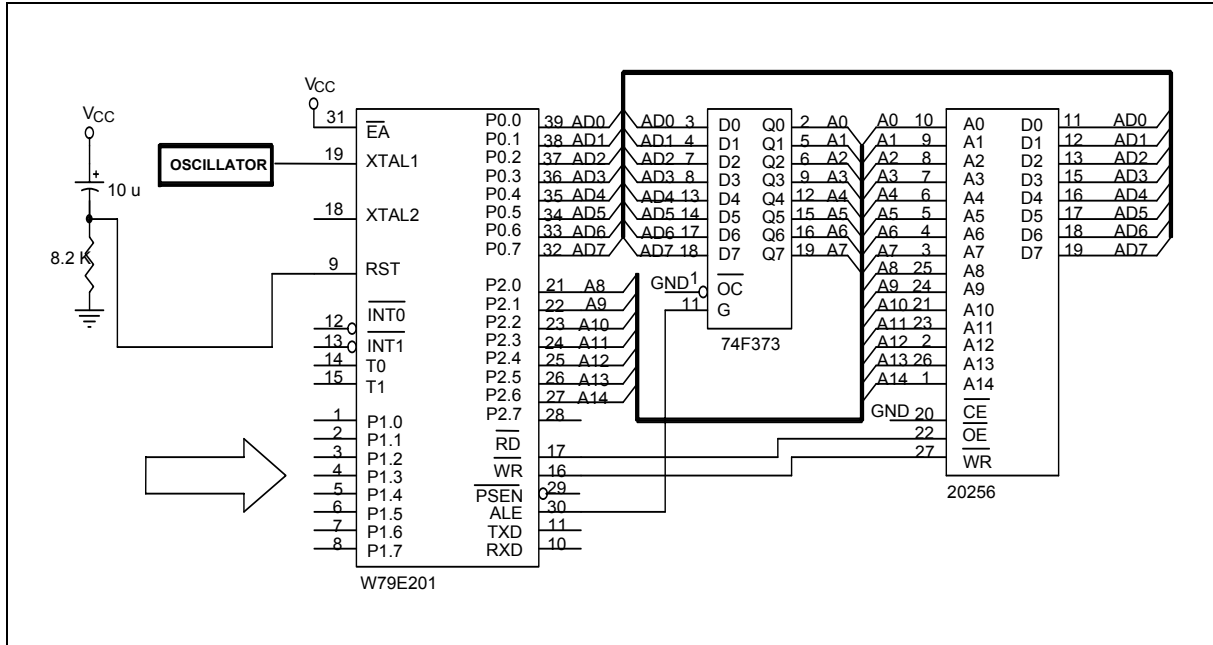
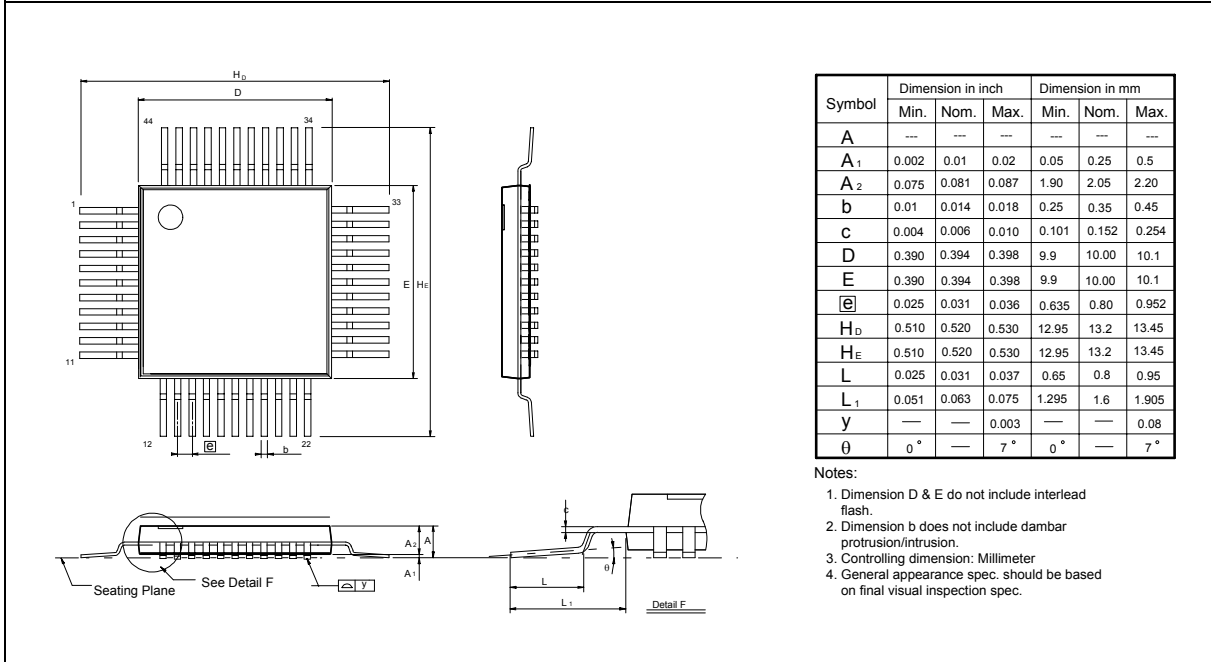


Figure B

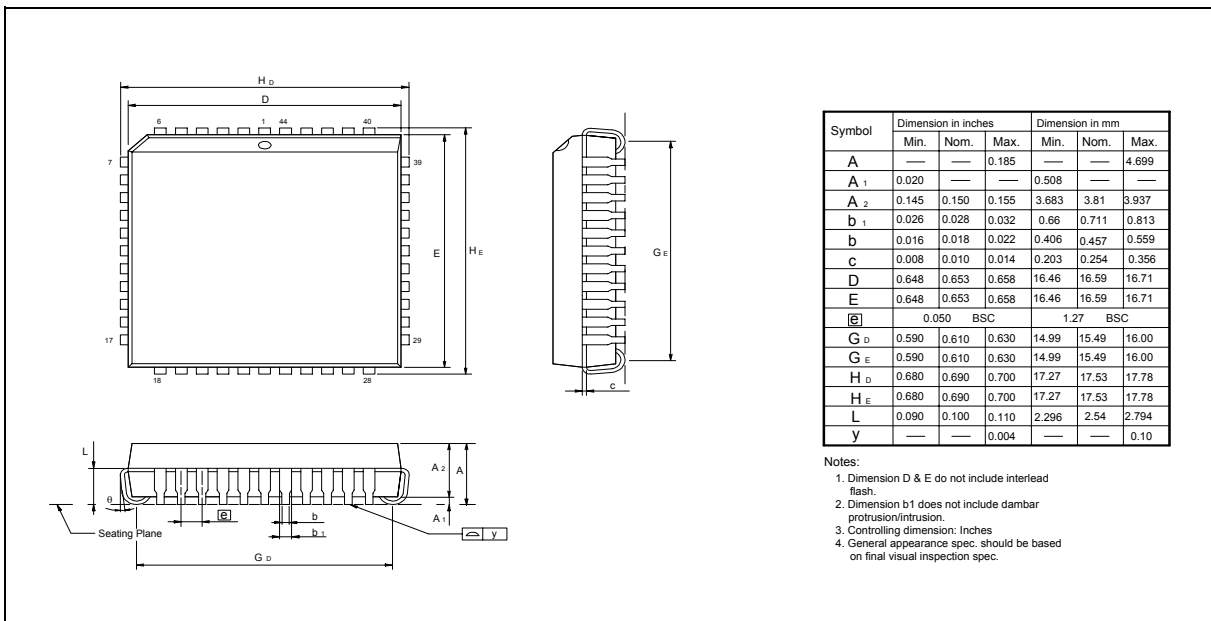


25. PACKAGE DIMENSIONS

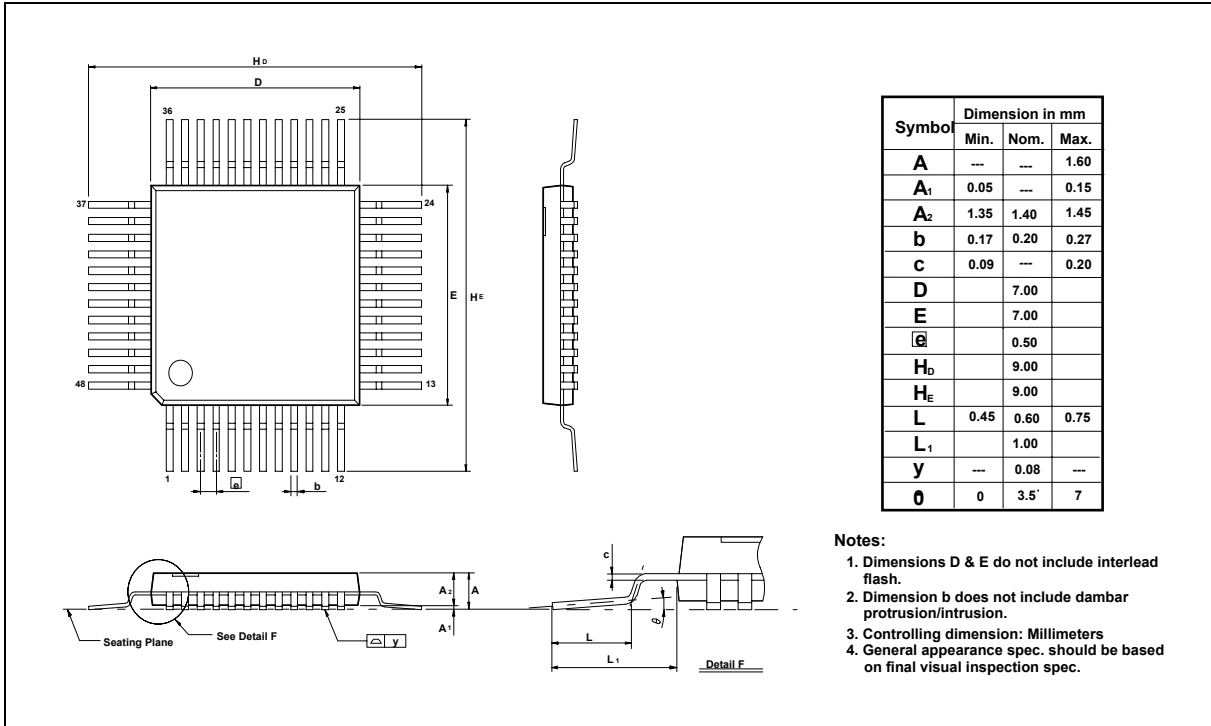
44-pin QFP



44-pin PLCC



48-pin LQFP





26. APPLICATION NOTE

In-system Programming Software Examples

This application note illustrates the in-system programmability of the Winbond W79E201 Flash EPROM microcontroller. In this example, microcontroller will boot from 16 KB AP Flash EPROM and waiting for a key to enter in-system programming mode for re-programming the contents of 16 KB AP Flash EPROM. While entering in-system programming mode, microcontroller executes the loader program in 4KB LD Flash EPROM. The loader program erases the 16 KB AP Flash EPROM then reads the new code data from external SRAM buffer (or through other interfaces) to update the 16KB AP Flash EPROM.

If the customer uses the reboot mode to update his program, please enable this b3 of security bit from the writer. Please refer security bits for detail description

EXAMPLE 1:

```

*****
;
;* Example of 64K AP Flash EPROM program: Program will scan the P1.0. if P1.0 = 0, enters in-system
;* programming mode for updating the content of AP Flash EPROM code else executes the current ROM code.
;* XTAL = 24 MHz
*****
;
        .chip 8052
        .RAMCHK OFF
        .symbols

CHPCON    EQU        9FH
TA        EQU        C7H
SFRAL     EQU        ACH
SFRAH     EQU        ADH
SFRFD     EQU        AEH
SFRCN     EQU        AFH

        ORG    0H
        LJMP  100H        ; JUMP TO MAIN PROGRAM
*****
;* TIMER0 SERVICE VECTOR ORG = 000BH
*****
        ORG    00BH
        CLR   TR0        ; TR0 = 0, STOP TIMER0
        MOV   TL0,R6
        MOV   TH0,R7
        RETI

```



```

*****
;
;* 64K AP Flash EPROM MAIN PROGRAM
*****
;
                ORG    100H

MAIN_64K:
    MOV    A,P1            ; SCAN P1.0
    ANL    A,#01H
    CJNE   A,#01H,PROGRAM_64K ; IF P1.0 = 0, ENTER IN-SYSTEM PROGRAMMING MODE
    JMP    NORMAL_MODE

PROGRAM_64:
    MOV    TA, #AAH        ; CHPCON register is written protect by TA register.
    MOV    TA, #55H
    MOV    CHPCON, #03H    ; CHPCON = 03H, ENTER IN-SYSTEM PROGRAMMING MODE
    MOV    SFRCN, #0H
    MOV    TCON, #00H      ; TR = 0 TIMER0 STOP
    MOV    IP, #00H        ; IP = 00H
    MOV    IE, #82H        ; TIMER0 INTERRUPT ENABLE FOR WAKE-UP FROM IDLE MODE
    MOV    R6, #F0H        ; TL0 = F0H
    MOV    R7, #FFH        ; TH0 = FFH
    MOV    TL0, R6
    MOV    TH0, R7
    MOV    TMOD, #01H      ; TMOD = 01H, SET TIMER0 A 16-BIT TIMER
    MOV    TCON, #10H      ; TCON = 10H, TR0 = 1,GO
    MOV    PCON, #01H      ; ENTER IDLE MODE FOR LAUNCHING THE IN-SYSTEM

PROGRAMMING
*****
;
;* Normal mode 64KB AP Flash EPROM program: depending user's application
*****
;
NORMAL_MODE:
    .
    ; User's application program
    .
    .
    .

```

**EXAMPLE 2:**

```

*****
;
;* Example of 4KB LD Flash EPROM program: This loader program will erase the 64KB AP Flash EPROM first,
;* then reads the new code from external SRAM and program them into 64KB AP Flash EPROM.
;* XTAL = 24 MHz
*****
;
                .chip 8052
                .RAMCHK OFF
                .symbols

CHPCON        EQU            9FH
TA            EQU            C7H
SFRAL         EQU            ACH
SFRAH         EQU            ADH
SFRFD         EQU            AEH
SFRCN         EQU            AFH

                ORG    000H
                LJMP   100H          ; JUMP TO MAIN PROGRAM
*****
;
;* 1. TIMER0 SERVICE VECTOR ORG = 0BH
*****
;
ORG 000BH
                CLR    TR0          ; TR0 = 0, STOP TIMER0
                MOV    TL0, R6
                MOV    TH0, R7
                RETI

*****
;
;* 4KB LD Flash EPROM MAIN PROGRAM
*****
;
                ORG    100H
MAIN_4K:
                MOV    TA,#AAH
                MOV    TA,#55H
                MOV    CHPCON,#03H ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
                MOV    SFRCN,#0H
                MOV    TCON,#00H   ; TCON = 00H, TR = 0 TIMER0 STOP
                MOV    TMOD,#01H   ; TMOD = 01H, SET TIMER0 A 16BIT TIMER

```



```

MOV IP,#00H ; IP = 00H
MOV IE,#82H ; IE = 82H, TIMER0 INTERRUPT ENABLED
MOV R6,#F0H
MOV R7,#FFH
MOV TL0,R6
MOV TH0,R7
MOV TCON,#10H ; TCON = 10H, TR0 = 1, GO
MOV PCON,#01H ; ENTER IDLE MODE
UPDATE_64K:
MOV TCON,#00H ; TCON = 00H , TR = 0 TIM0 STOP
MOV IP,#00H ; IP = 00H
MOV IE,#82H ; IE = 82H, TIMER0 INTERRUPT ENABLED
MOV TMOD,#01H ; TMOD = 01H, MODE1
MOV R6,#D0H ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 ms
;DEPENDING ON USER'S SYSTEM CLOCK RATE.

MOV R7,#8AH
MOV TL0,R6
MOV TH0,R7
ERASE_P_4K:
MOV SFRCN,#22H ; SFRCN = 22H, ERASE 64K AP Flash EPROM
MOV TCON,#10H ; TCON = 10H, TR0 = 1,GO
MOV PCON,#01H ; ENTER IDLE MODE (FOR ERASE OPERATION)
,*****
,* BLANK CHECK
,*****
MOV SFRCN,#0H ; SFRCN = 00H, READ 64KB AP Flash EPROM
MOV SFRAH,#0H ; START ADDRESS = 0H
MOV SFRAL,#0H
MOV R6,#FDH ; SET TIMER FOR READ OPERATION, ABOUT 1.5 μS.
MOV R7,#FFH
MOV TL0,R6
MOV TH0,R7
blank_check_loop:
SETB TR0 ; enable TIMER 0
MOV PCON,#01H ; enter idle mode
MOV A,SFRFD ; read one byte
CJNE A,#FFH,blank_check_error
INC SFRAL ; next address
MOV A,SFRAL

```



```

JNZ    blank_check_loop
INC    SFRAH
MOV    A,SFRAH
CJNE  A,#0H,blank_check_loop ; end address = FFFFH
JMP    PROGRAM_64KROM

blank_check_error:
JMP    $

;*****
;
;* RE-PROGRAMMING 64KB AP Flash EPROM BANK
;*****
PROGRAM_64KROM:
MOV    R2,#00H          ; Target low byte address
MOV    R1,#00H          ; TARGET HIGH BYTE ADDRESS
MOV    DPTR,#0H
MOV    SFRAH,R1         ; SFRAH, Target high address
MOV    SFRCN,#21H       ; SFRCN = 21H, PROGRAM 16K AP Flash EPROM
MOV    R6,#9CH          ; SET TIMER FOR PROGRAMMING, ABOUT 50 μS.
MOV    R7,#FFH
MOV    TL0,R6
MOV    TH0,R7

PROG_D_64K:
MOV    SFRAL,R2         ; SFRAL = LOW BYTE ADDRESS
CALL   GET_BYTE_FROM_PC_TO_ACC ; tHIs prOGRAM IS BASED ON USER'S CIRCUIT.
MOV    @DPTR,A          ; SAVE DATA INTO SRAM TO VERIFY CODE.
MOV    SFRFD,A          ; SFRFD = data IN
MOV    TCON,#10H        ; TCON = 10H, TR0 = 1,GO
MOV    PCON,#01H        ; ENTER IDLE MODE (PRORGAMMING)
INC    DPTR
INC    R2
CJNE  R2,#0H,PROG_D_64K
INC    R1
MOV    SFRAH,R1
CJNE  R1,#0H,PROG_D_64K

;*****
;
;* VERIFY 16KB AP Flash EPROM BANK
;*****

MOV    R4,#03H          ; ERROR COUNTER
MOV    R6,#FDH          ; SET TIMER FOR READ VERIFY, ABOUT 1.5 μS.

```



```

MOV    R7,#FFH
MOV    TL0,R6
MOV    TH0,R7
MOV    DPTR,#0H      ; The start address of sample code
MOV    R2,#0H        ; Target low byte address
MOV    R1,#0H        ; Target high byte address
MOV    SFRAH,R1      ; SFRAH, Target high address
MOV    SFRCN,#00H    ; SFRCN = 00H, Read AP Flash EPROM
READ_VERIFY_64K:
MOV    SFRAL,R2      ; SFRAL = LOW ADDRESS
MOV    TCON,#10H     ; TCON = 10H, TR0 = 1,GO
MOV    PCON,#01H
INC    R2
MOVX   A,@DPTR
INC    DPTR
CJNE   A,SFRFD,ERROR_64K
CJNE   R2,#0H,READ_VERIFY_64K
INC    R1
MOV    SFRAH,R1
CJNE   R1,#0H,READ_VERIFY_64K
,*****
,* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
,*****
MOV    TA,#AAH
MOV    TA,#55H
MOV    CHPCON,#83H   ; SOFTWARE RESET. CPU will restart from AP Flash EPROM
ERROR_64K:
DJNZ   R4,UPDATE_64K ; IF ERROR OCCURS, REPEAT 3 TIMES.
                        ; IN-SYST PROGRAMMING FAIL, USER'S PROCESS TO DEAL
                        WITH IT.
.
.
.

```



27. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	November 9, 2004	-	Initial Issued
A2	December 16, 2004	58 / 60	1. To add PWM Function Description 2. To add ADC Function Description



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