NN514400A / NN514400B series
Fast Page Mode CMOS 1M × 4bit Dynamic RAM

NPNX

DESCRIPTION

The NN514400A/B series is a high performance CMOS Dynamic Random Access Memory organized as 1,048,576 words by 4 bit. The NN514400A/B series is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN514400A/B series features a high speed page mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

The outputs are tri-stated by $\overline{CAS}$ which, in essence, acts as an output enable independent of $\overline{RAS}$ with very fast $\overline{CAS}$ to output access time.

Refresh is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 1,024 address combinations of A0 to A9 during a 16 ms period.

Multiplexed address inputs permit The NN514400A/B series to be packaged in a standard 26-pin plastic SOJ, 26 pin TSOP TYPE II. The package sizes provide high system bit densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ±10% tolerance and direct inter-

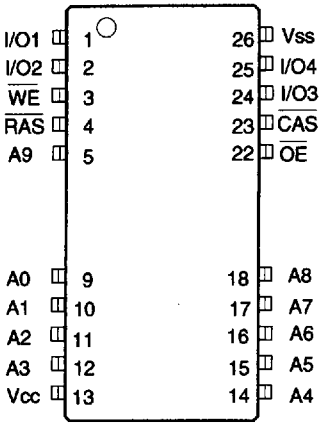
FEATURES

- 1,048,576 × 4 bit Organization
- Single 5V ±10% Power Supply
- Performance Ranges

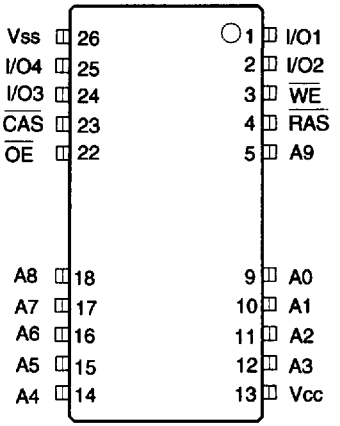
Parameter	-45	-50	-60	-70
Max. $\overline{RAS}$ Access Time (t_{RAC})	45ns	50ns	60ns	70ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	13ns	13ns	15ns	20ns
Max. Column Address Access Time (t_{AA})	25ns	27ns	30ns	35ns
Min. Read/Write Cycle Time (t_{RC})	80ns	90ns	110ns	130ns

- Fast Page Mode Operation
- Low Power Operation
  Low Standby Current (CMOS level inputs)
  – Standard 1mA
  – L version 50μA
- 1,024 Refresh Cycles
  – Standard distributed across 16ms
  – L version distributed across 128ms
- Self Refresh Mode
  (L version)
- All inputs/Outputs and Clocks
  fully TTL and CMOS compatible
- Refresh Modes
  $\overline{RAS}$ only
  $\overline{CAS}$ before $\overline{RAS}$
  Hidden Refresh
- ×8 bit Test Mode
- High Reliability Packages
  Plastic 26pin SOJ (P26/20SJ-2A)
  Plastic 26pin TSOP TYPE II (P26/20TP-2A)

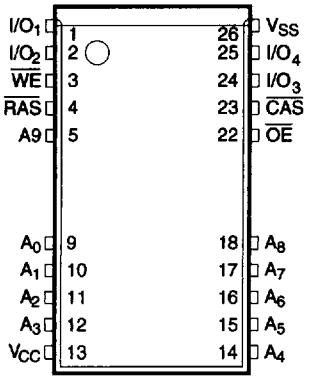
PIN CONFIGURATION (TOP VIEW)



26/20-pin TSOP TYPE (II)
Normal Bend (300 mil)
P26/20TP-2A



26/20-pin TSOP TYPE (II)
Reverse Bend (300 mil)
P26/20TP-2A-R

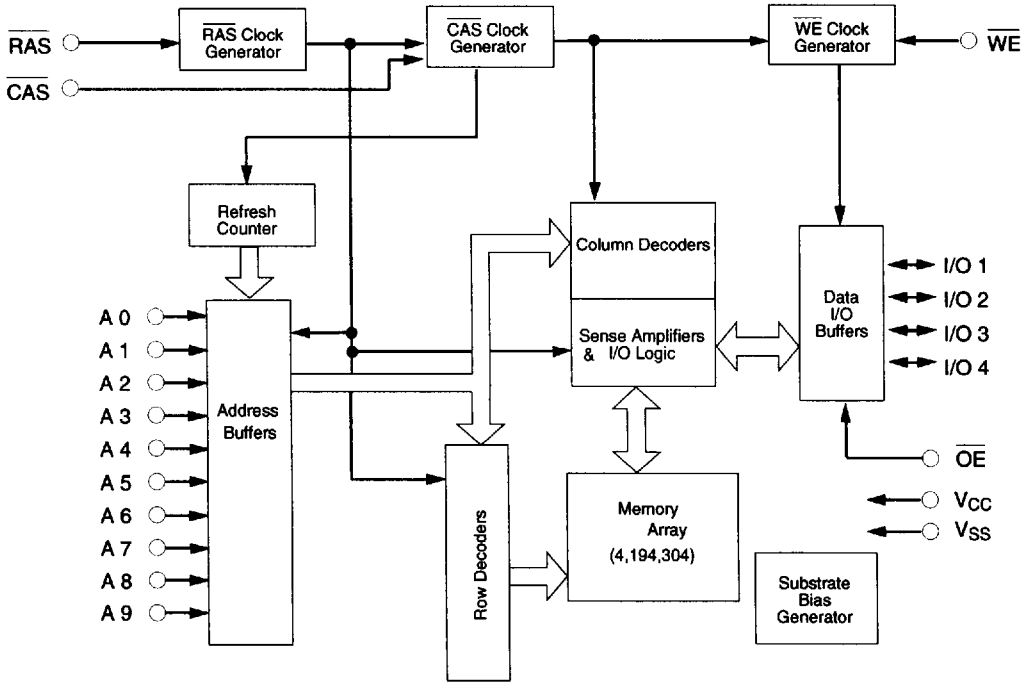


26/20-pin SOJ (300mil)
P26/20SJ-2A

PIN NAMES

A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{OE}$	Output Enable
I/O1~I/O4	Data-in / Data-out
$\overline{WE}$	Write Enable
V_{CC}	+5V Supply
V_{SS}	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	Vin, Vout	−1 to 7	V
Voltage on Vcc Relative to V_{SS}	V_{CC}	−1 to 7	V
Storage Temperature (Plastic)	Tstg	−55 to +125	°C
Power Dissipation	Pd	1.0	W
Ambient Operating Temperature	Ta	0 to + 70	°C
Short Circuit Output Current	Iout	50	mA

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage, All Inputs	2.4	—	6.5	V
V_{IL}	Input Low Voltage, All Inputs	−1.0	—	0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS} unless otherwise specified.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%)

(NN514400A)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I_{CC1}	Operating Current	-45		130	mA	t_{RC} = t_{RC} (min.)	1, 2
		-50		120	mA	$\overline{RAS}$, $\overline{CAS}$, Address cycling	
		-60		110	mA		
		-70		100	mA		
I_{CC2}	Standby Current			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V)	
				2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}	
	Standby Current (L version)			50	µA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	
I_{CC3}	Refresh Current ($\overline{RAS}$ only refresh)	-45		130	mA	t_{RC} = t_{RC} (min.)	1
		-50		120	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}	
		-60		110	mA		
		-70		100	mA		
I_{CC4}	Fast Page Mode Current	-45		75	mA	t_{PC} = t_{PC} (min.)	1,2
		-50		70	mA	$\overline{RAS}$ = V_{IL}	
		-60		60	mA	$\overline{CAS}$, Address cycling	
		-70		50	mA		
I_{CC5}	Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	-45		130	mA	t_{RC} = t_{RC} (min.)	1
		-50		120	mA	$\overline{RAS}$, $\overline{CAS}$ cycling	
		-60		110	mA		
		-70		100	mA		
I_{CC6}	Refresh Current (NN514400L/AL/BL: $\overline{CAS}$ before $\overline{RAS}$ refresh)			150	µA	1024 cycles / 128ms t_{RAS} ≤ 200ns, $\overline{WE}$ ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	
I_{CC7}	Self Refresh Mode Current			100	µA	$\overline{RAS}$ =$\overline{CAS}$ ≤ (V_{SS} + 0.2V) All other input high levels are (V_{CC} - 0.2V) or input low levels are (V_{SS} + 0.2V)	
$\|I_{L1}\|$	Input Leakage Current (Any input pin)		-10	10	µA	0V ≤ V_{IH} ≤ 5.5V, Others = 0V	
$\|I_{LO}\|$	Output Leakage Current (For high impedance state)		-10	10	µA	$\overline{RAS}$ ≥ V_{IH}(min.), $\overline{CAS}$ ≥ V_{IH}(min.) 0V ≤ V_{OUT} ≤ 5.5V	
V_{OH}	Output High Voltage		2.4		V	I_{OH} = –5.0 mA	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	

Notes: 1. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN1}	Address(A0 ~ A9)	—	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$,$\overline{OE}$	—	5	pF
C_{OUT}	I/O1,I/O2,I/O3,I/O4	—	7	pF

DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%) (NN514400B)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I_{CC1}	Operating Current	-45		100	mA	t_{RC} = t_{RC} (min.)	1, 2
		-50		90	mA	$\overline{RAS}$, $\overline{CAS}$, Address cycling	
		-60		80	mA		
		-70		70	mA		
I_{CC2}	Standby Current			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V)	
				2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}	
	Standby Current (L version)			150	µA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	
I_{CC3}	Refresh Current ($\overline{RAS}$ only refresh)	-45		100	mA	t_{RC} = t_{RC} (min.)	1
		-50		90	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}	
		-60		80	mA		
		-70		70	mA		
I_{CC4}	Fast Page Mode Current	-45		70	mA	t_{PC} = t_{PC} (min.)	1,2
		-50		60	mA	$\overline{RAS}$ = V_{IL}	
		-60		50	mA	$\overline{CAS}$, Address cycling	
		-70		40	mA		
I_{CC5}	Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	-45		100	mA	t_{RC} = t_{RC} (min.)	1
		-50		90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling	
		-60		80	mA		
		-70		70	mA		
I_{CC6}	Refresh Current (NN514400BL: $\overline{CAS}$ before $\overline{RAS}$ refresh)			200	µA	1024 cycles / 128ms t_{RAS} ≤ 200ns, $\overline{WE}$ ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	
I_{CC7}	Self Refresh Mode Current			200	µA	$\overline{RAS}$ =$\overline{CAS}$ ≤ (V_{SS} + 0.2V) All other input high levels are (V_{CC} - 0.2V) or input low levels are (V_{SS} + 0.2V)	16
$\|I_{LI}\|$	Input Leakage Current (Any input pin)		-10	10	µA	0V ≤ V_{IH} ≤ 5.5V, Others = 0V	
$\|I_{LO}\|$	Output Leakage Current (For high impedance state)		-10	10	µA	$\overline{RAS}$ ≥ V_{IH}(min.), $\overline{CAS}$ ≥ V_{IH}(min.) 0V ≤ V_{OUT} ≤ 5.5V	
V_{OH}	Output High Voltage		2.4		V	I_{OH} = -5.0 mA	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	

Notes: 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN1}	Address(A0 ~ A9)	—	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$,$\overline{OE}$	—	5	pF
C_{OUT}	I/O1,I/O2,I/O3,I/O4	—	7	pF

A.C. OPERATING CONDITIONS (0 °C≤Ta≤70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (NOTES 3, 4, 5)

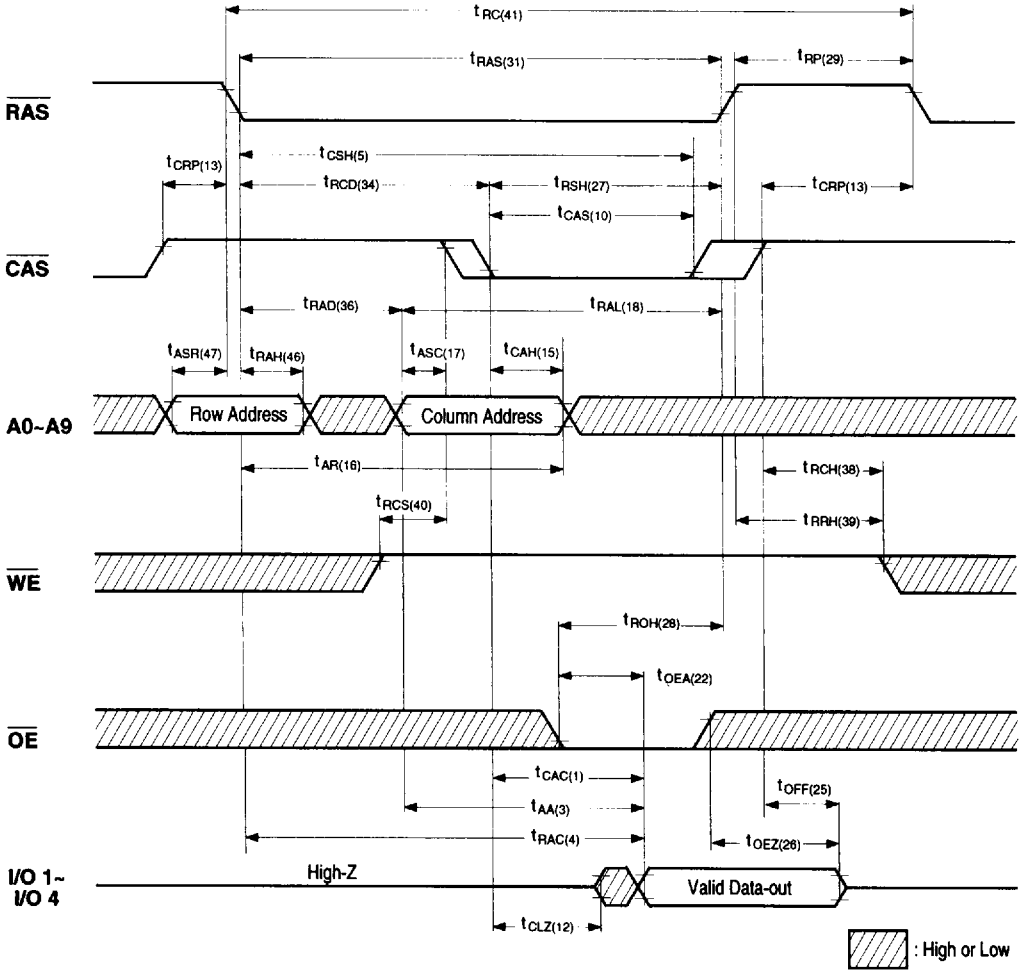
NO.	NOTES		PARAMETER	-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	13	—	13	—	15	—	20	ns	6,13
2	t_{CH2QV}	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	30	—	32	—	35	—	40	ns	13,14
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	25	—	27	—	30	—	35	ns	7,13
4	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	—	45	—	50	—	60	—	70	ns	6,7
5	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	45	—	50	—	60	—	70	—	ns	
6	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	10	—	10	—	ns	
7	t_{RL1CX}	t_{CHS}	$\overline{CAS}$ Precharge Time (Self Refresh Mode)	-50	—	-50	—	-50	—	-50	—	ns	
8	t_{CH2CL2}	t_{CPN}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	10	—	10	—	ns	
9	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	5	—	5	—	5	—	5	—	ns	14
10	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	13	100K	13	100K	15	100K	20	100K	ns	
11	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	5	—	5	—	5	—	5	—	ns	
12	t_{CL1QX}	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	35	—	35	—	35	—	50	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	10	—	10	—	15	—	15	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	30	—	35	—	40	—	40	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	ns	14
18	t_{AVRH1}	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	22	—	24	—	30	—	35	—	ns	
19	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	48	—	50	—	50	—	65	—	ns	11
20	t_{CL1DX} / t_{WL1DX}	t_{DH}	Data Hold Time — NN514400A	10	—	10	—	10	—	10	—	ns	12
			Data Hold Time — NN514400B	10	—	10	—	10	—	15	—		
21	t_{DVCL2} / t_{DVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	0	—	ns	12
22	t_{OL1QV}	t_{OEA}	$\overline{OE}$ Access Time	—	13	—	13	—	15	—	20	ns	
23	t_{WL1OL2}	t_{OEH}	$\overline{OE}$ Command Hold Time	13	—	13	—	15	—	20	—	ns	
24	t_{CH2QV}	t_{OED}	$\overline{OE}$ to Data Delay Time	7	—	8	—	10	—	10	—	ns	
25	t_{CH2QZ}	t_{OFF}	Output Buffer Turn-off Delay Time	0	13	0	13	0	15	0	20	ns	10
26	t_{OH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{OE}$	0	10	0	10	0	15	0	15	ns	
27	t_{CL1RH1}	t_{RSH}	$\overline{RAS}$ Hold Time	13	—	13	—	15	—	20	—	ns	
28	t_{OL1RH1}	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	8	—	8	—	10	—	10	—	ns	
29	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	25	—	25	—	30	—	40	—	ns	
30	t_{RH2RL2}	t_{RPS}	$\overline{RAS}$ Precharge Time (Self Refresh Mode)	80	—	90	—	110	—	130	—	ns	
31	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	45	100K	50	100K	60	100K	70	100K	ns	
32	t_{RL1RH1}	t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	45	100K	50	100K	60	100K	70	100K	ns	
33	t_{RL1RH1}	t_{RASS}	$\overline{RAS}$ Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	300	—	µs	
34	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	13	30	13	35	13	45	13	50	ns	6
35	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to CAS Precharge Time	10	—	10	—	10	—	10	—	ns	
36	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	11	20	11	23	11	30	11	35	ns	
37	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	62	—	68	—	80	—	100	—	ns	11
38	t_{CH2WL2}	t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	0	—	ns	9

NO.	SYMBOL		PARAMETER		-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
39	t_{RH2WL2}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$		5	—	5	—	5	—	5	—	ns	9
40	t_{WH2CL2}	t_{RCS}	Read Command Setup Time		0	—	0	—	0	—	0	—	ns	
41	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time		80	—	90	—	110	—	130	—	ns	
42	t_{CL2CL2}	t_{PC}	Read or Write Cycle Time (Fast Page Mode)		30	—	33	—	40	—	45	—	ns	13,14
43	t_{RL2RL2}	t_{RMW}	Read-Modify-Write Cycle Time	NN514400A	120	—	125	—	135	—	185	—	ns	
				NN514400B	120	—	125	—	135	—	165	—		
44	t_{CL2CL2}	t_{PRMW}	Read-Modify-Write Cycle Time (Fast Page Mode)		57	—	57	—	66	—	100	—	ns	13,14
45	t_{REF}	t_{REF}	Refresh Period		—	16	—	16	—	16	—	16	ms	15
46	t_{RL1AX}	t_{RAH}	Row Address Hold Time		8	—	8	—	8	—	8	—	ns	
47	t_{AVRL2}	t_{ASR}	Row Address Setup Time		0	—	0	—	0	—	0	—	ns	
48	t_T	t_T	Transition Time (Rise and Fall)		2	50	2	50	2	50	2	50	ns	4,5
49	t_{CL1WH1}	t_{WCH}	Write Command Hold Time		8	—	8	—	10	—	15	—	ns	
50	t_{WL1WH1}	t_{WP}	Write Command Pulse Width		8	—	8	—	10	—	15	—	ns	
51	t_{WL1CL2}	t_{WCS}	Write Command Setup Time		0	—	0	—	0	—	0	—	ns	11
52	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time		13	—	13	—	15	—	20	—	ns	
53	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time		13	—	13	—	15	—	20	—	ns	
54	t_{WL1RL2}	t_{WSR}	Write Command Setup Time (Test Mode)		10	—	10	—	10	—	10	—	ns	
55	t_{RL1WH1}	t_{WHR}	Write Command Hold Time (Test Mode)		10	—	10	—	10	—	10	—	ns	
56	t_{WH2RL2}	t_{WRP}	WE to RAS Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)		10	—	10	—	10	—	10	—	ns	
57	t_{RL1WH2}	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)		10	—	10	—	10	—	10	—	ns	

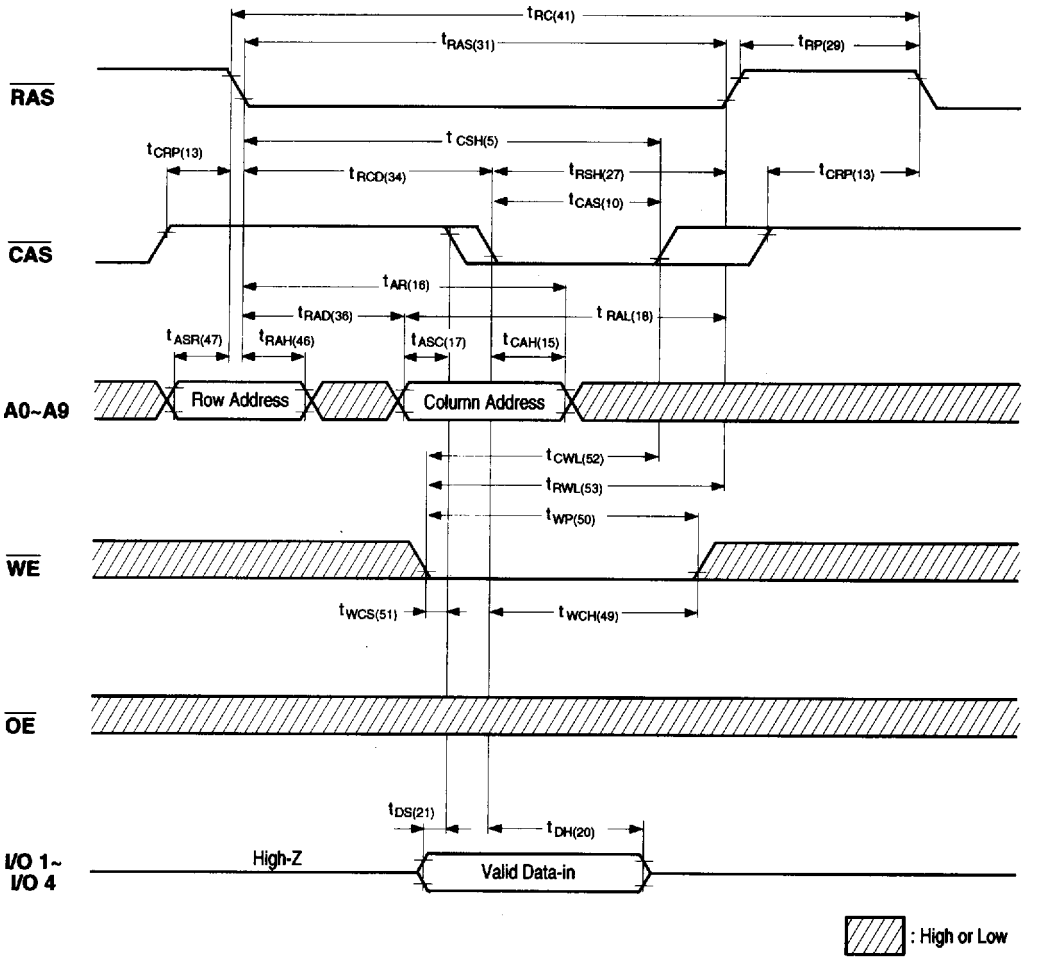
Notes:

3. Eight Initialization Cycles are required following a 200μs pause after Power Up. These Initialization Cycles may consist of any combination of the following : $\overline{RAS}$ only refresh Cycles, Read Cycles, Write Cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh Cycles.
4. AC measurements assume t_T=3ns. All AC parameters are measured with V_{IL}(min.)≥V_{SS} and V_{IH}(max.)≤V_{CC} and with a load equivalent to two TTL loads and 100pF.
5. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
7. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
8. Assumes three state test load (5pF and a 220 ohm to 1.3V Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{OFF}(max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS}≥t_{WCS}(min.) , the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If t_{RWD}≥t_{RWD}(min.), t_{CWD}≥t_{CWD}(min.) and t_{AWD}≥t_{AWD}(min.), the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
13. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{CPA}.
14. t_{ASC}≥t_{CP} to achieve t_{PC}(min.) and t_{CPA}(max.) values.
15. t_{REF}=128msec for Long Refresh version (L version).

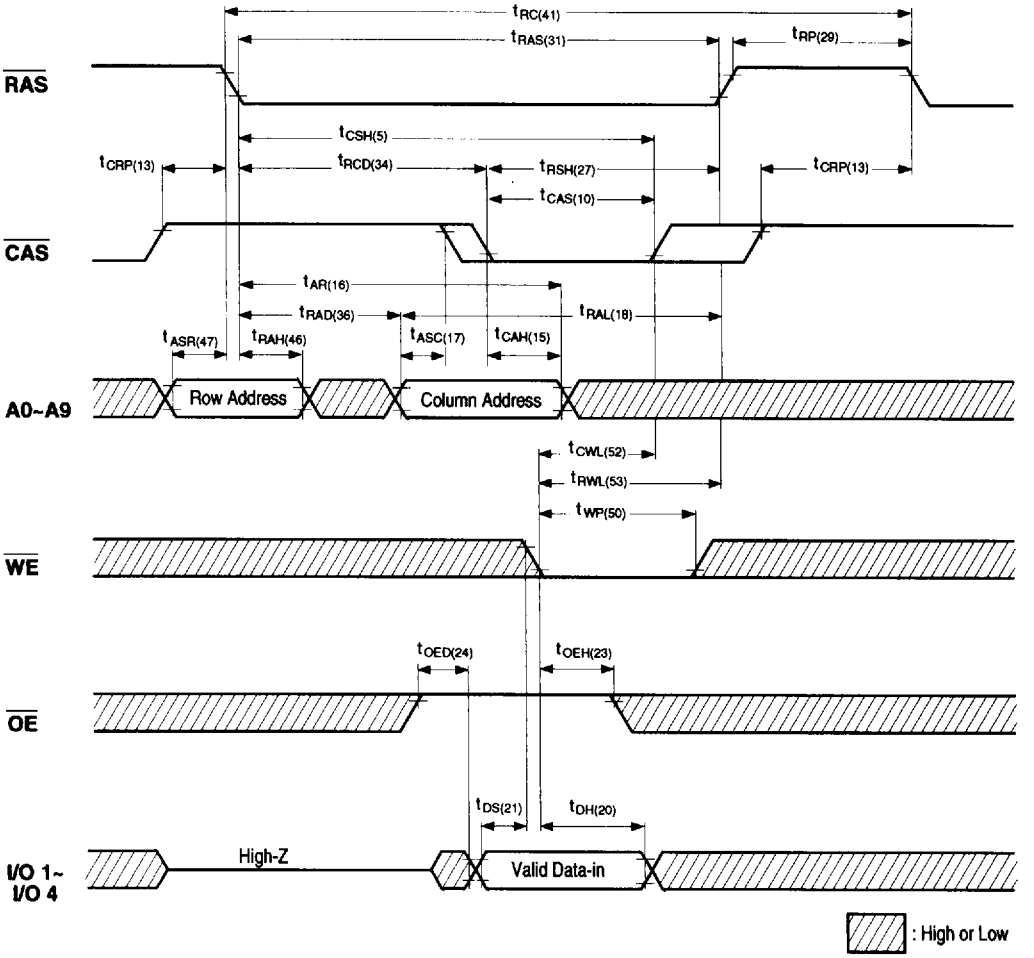
READ CYCLE



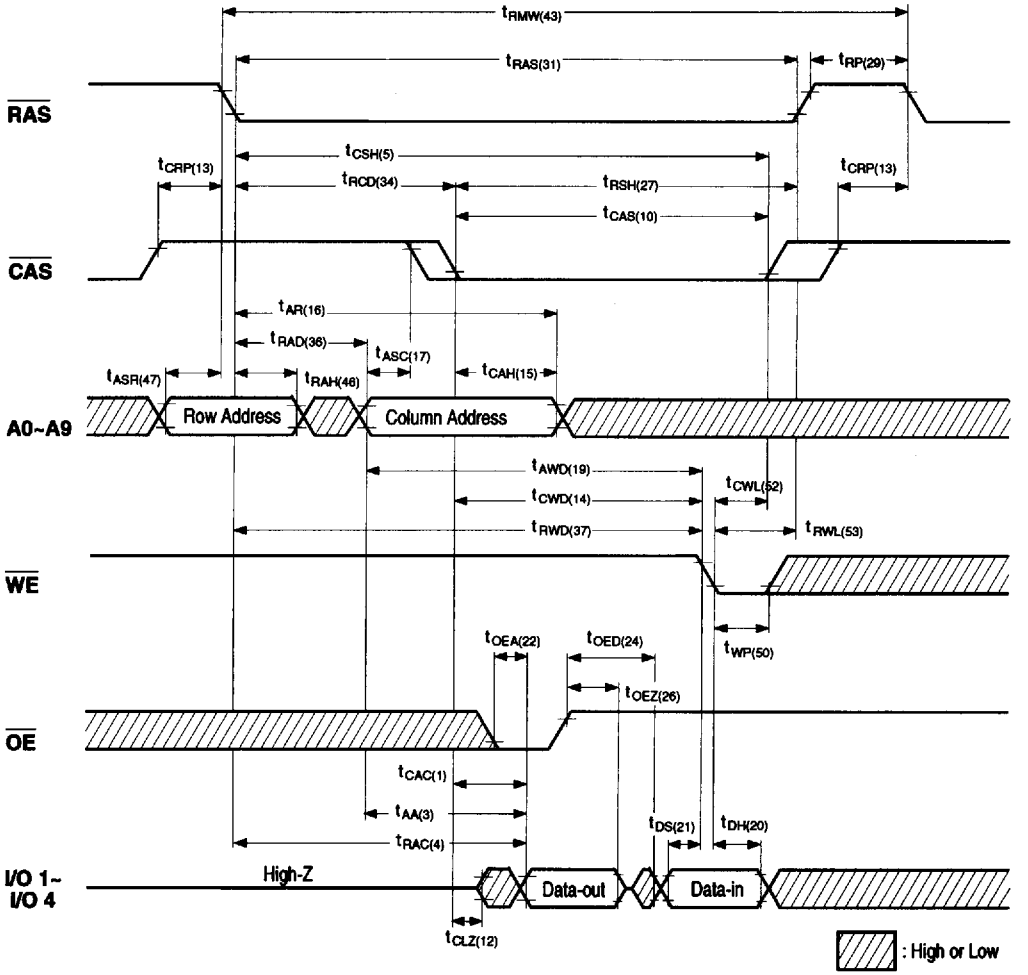
WRITE CYCLE (EARLY WRITE)



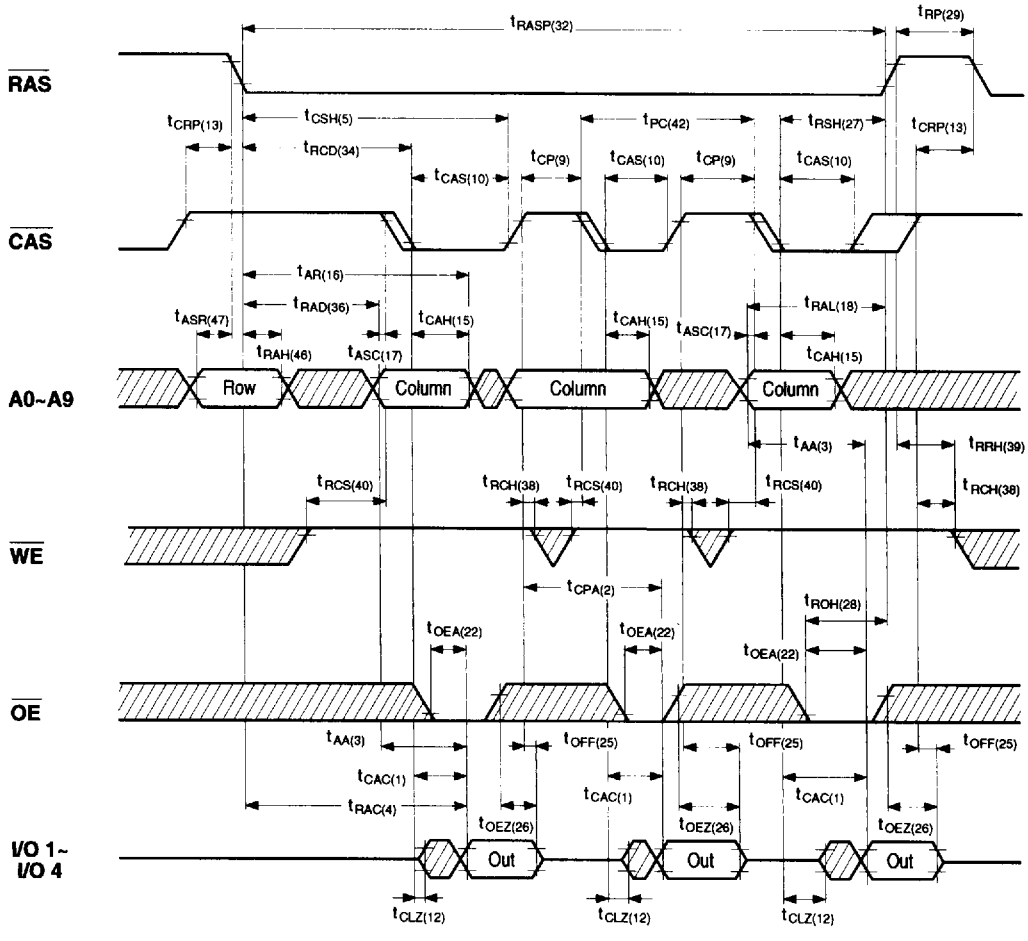
WRITE CYCLE ($\overline{OE}$-CONTROLLED WRITE)



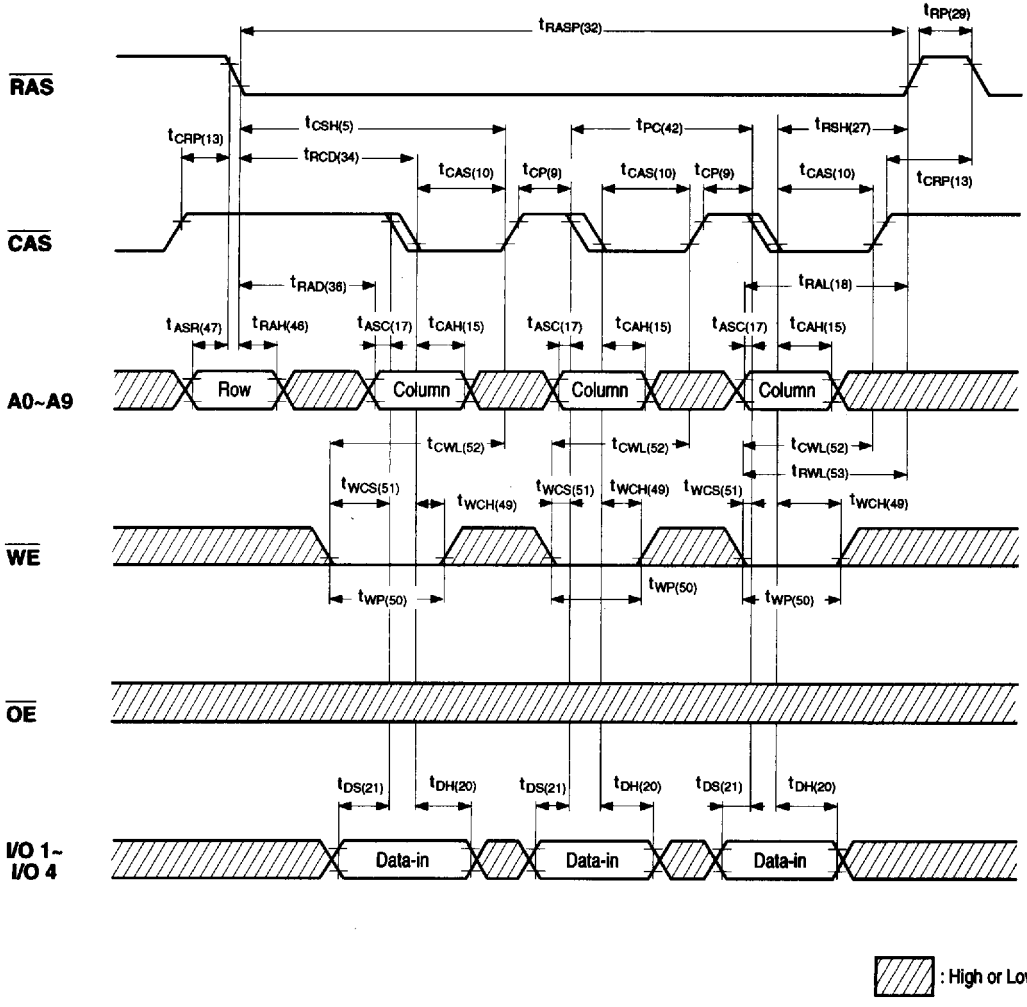
READ-MODIFY-WRITE CYCLE



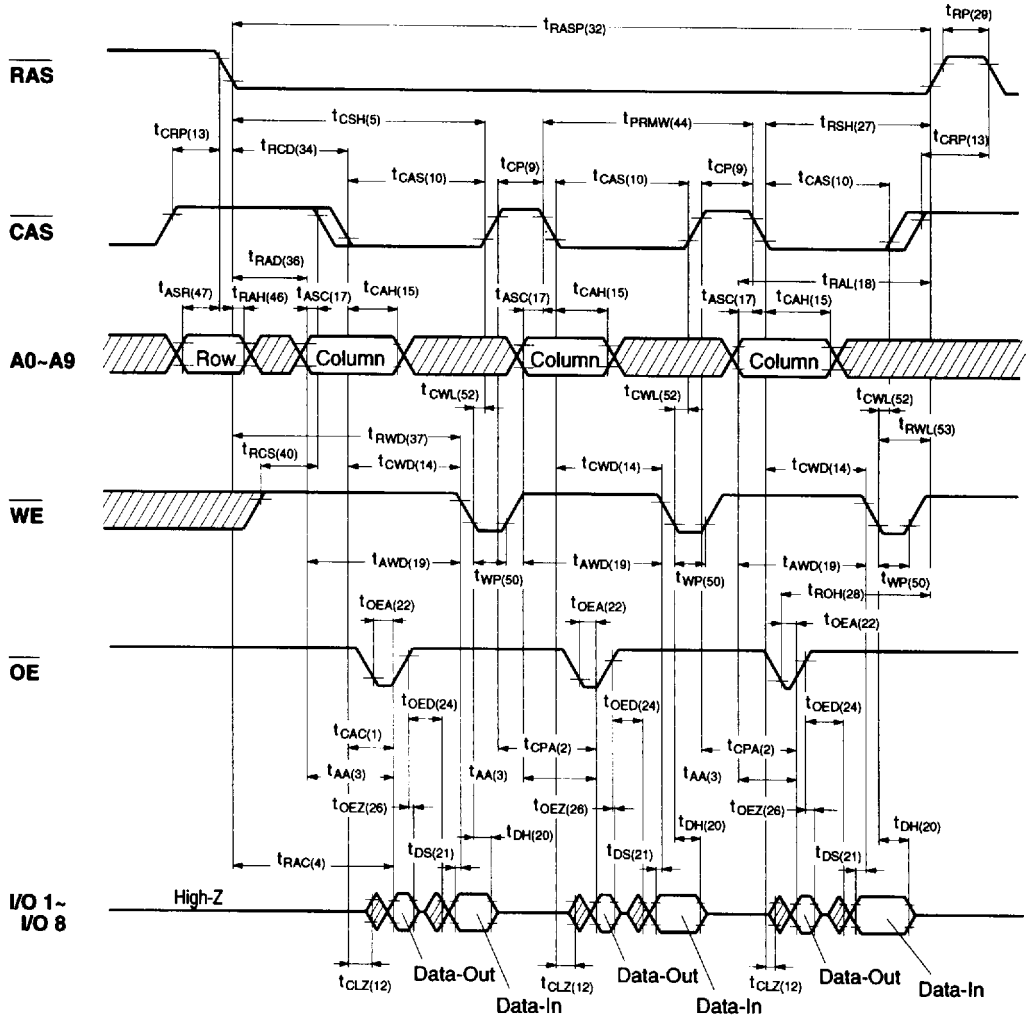
FAST PAGE MODE READ CYCLE



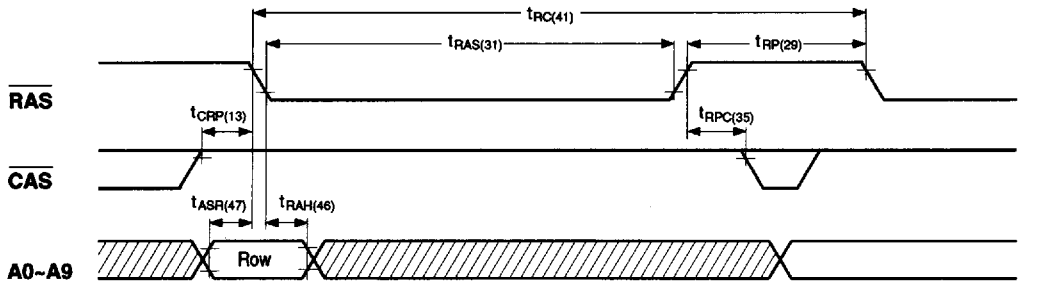
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



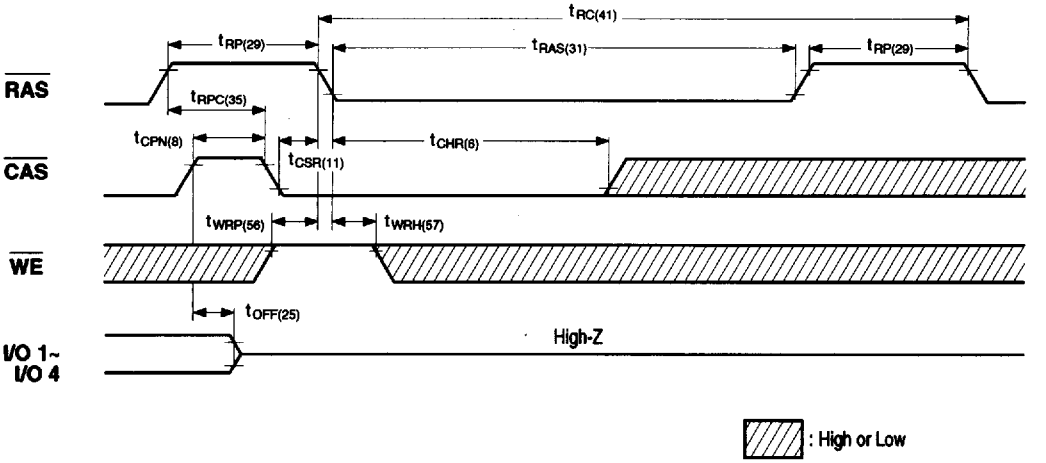
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

: High or Low

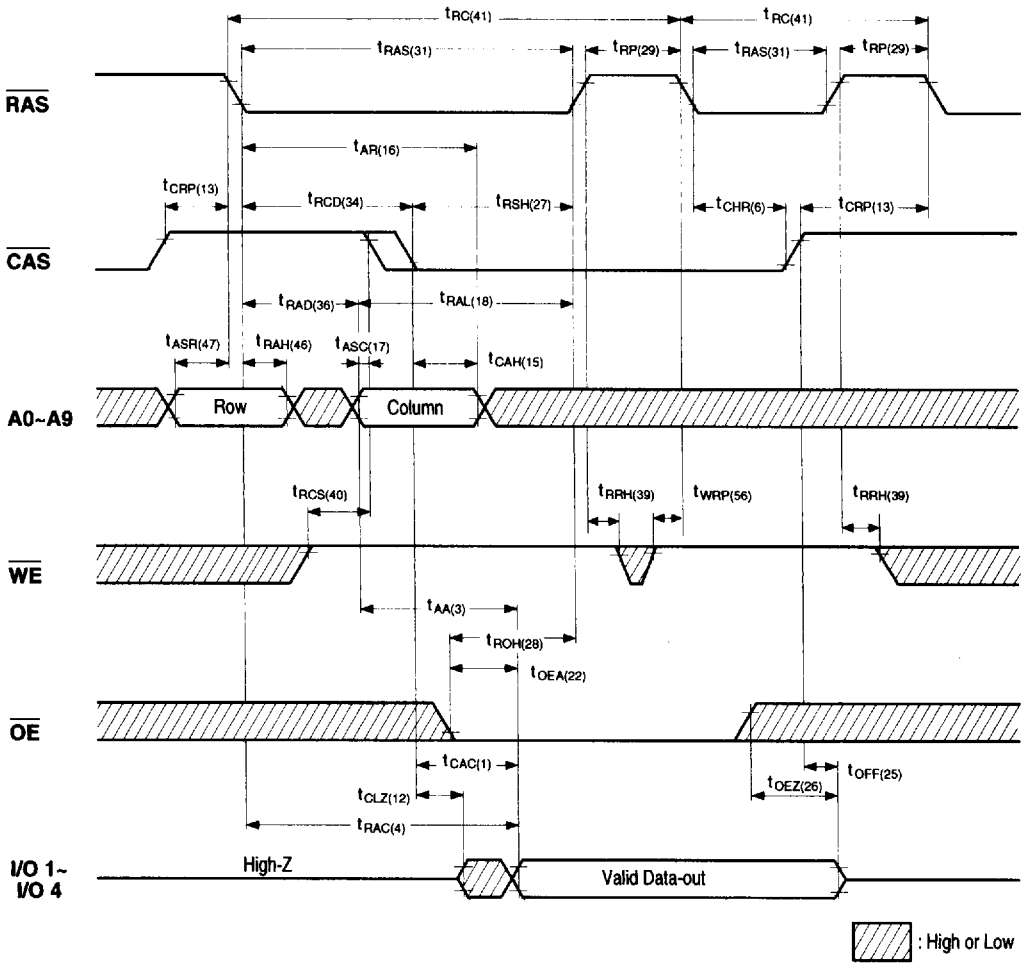
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



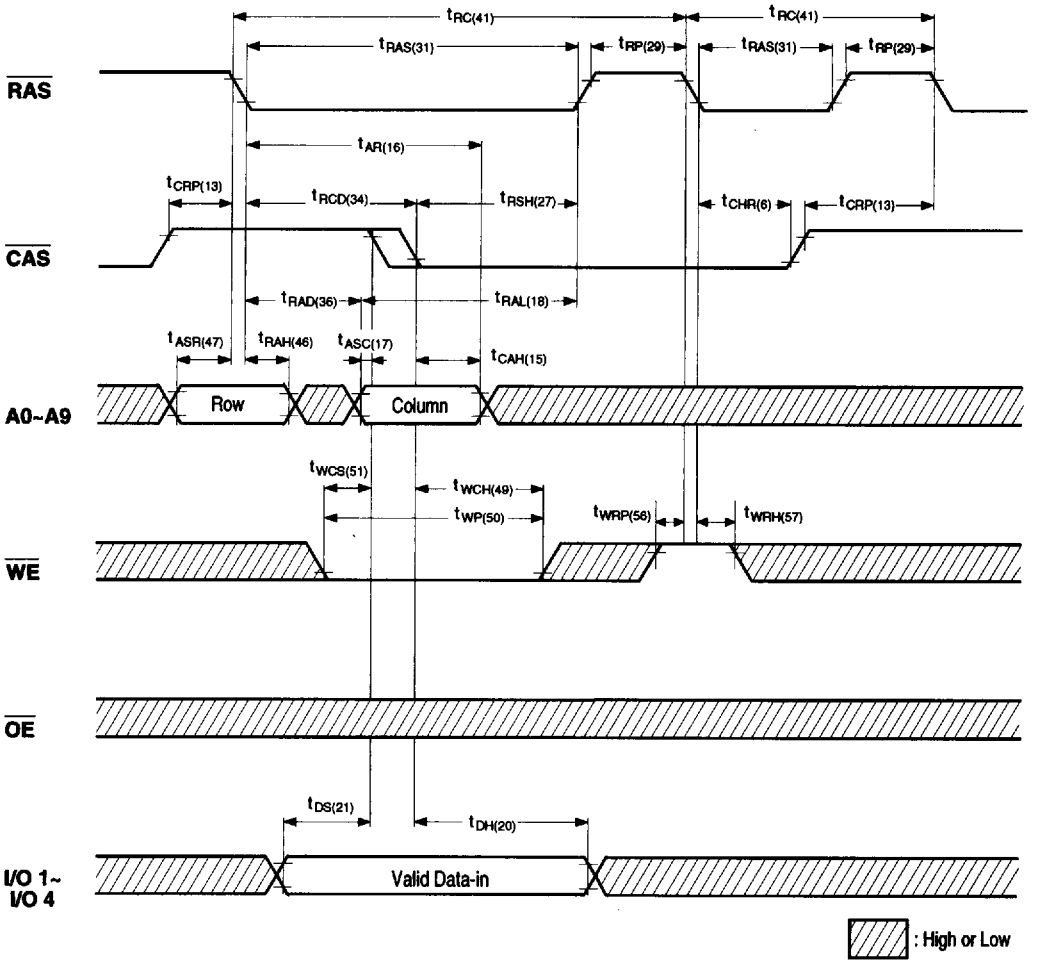
: High or Low

Note: $\overline{OE}$, A0~A9 = Don't care.
$\overline{WE}$ must be high at the falling edge of $\overline{RAS}$ in order to prevent from entering test mode.

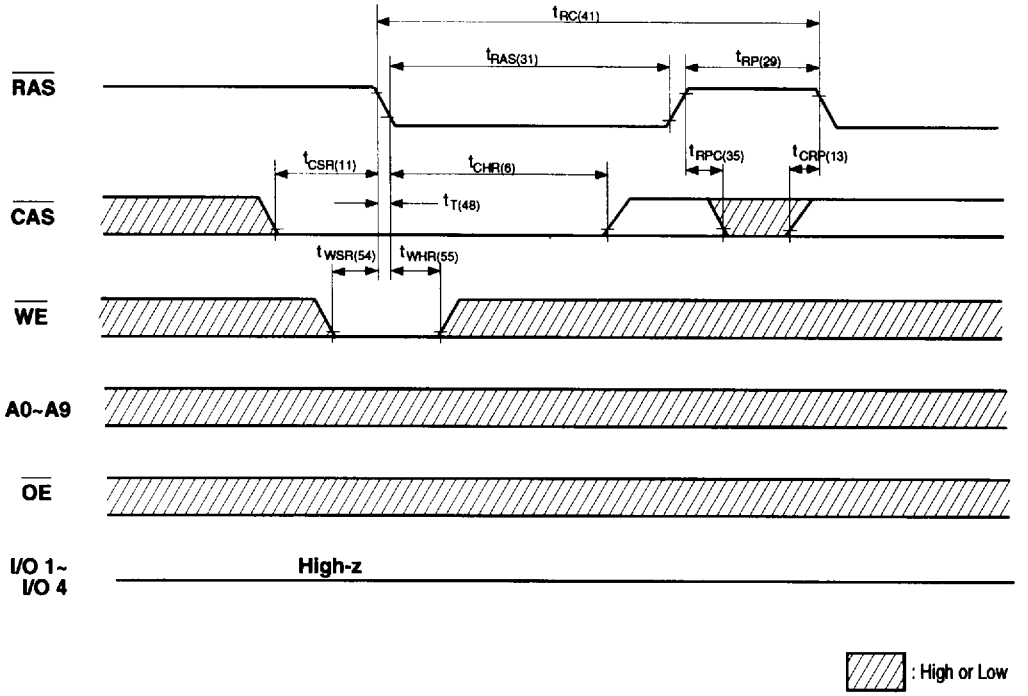
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



TEST MODE SET CYCLE (WE, CAS BEFORE RAS REFRESH CYCLE)



■ The NN514400A/B has an 8 bit parallel Test Mode Function for reducing test time. In the Test Mode, memory configuration is 512K x 8 bits and the Column address A0 address is ignored.

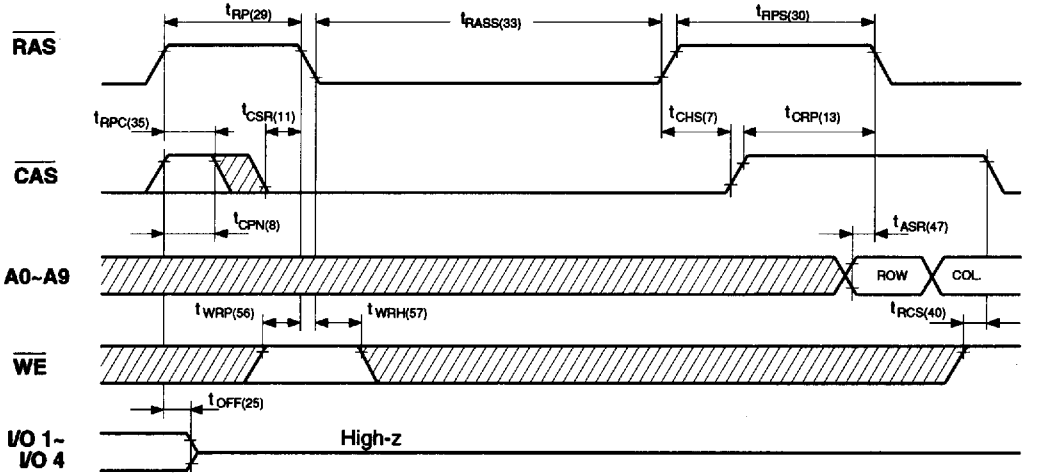
a. Entering the test mode:
The NN514400A/B test mode is entered by using the test mode set cycle (WE,CAS before RAS cycle).

b. Read/Write operation in test mode:
For Write cycle, data input from each I/O (I/O1~I/O4) is written to 2 bit memory cells (total 8bits) at the same time.
During the read cycle, if the 2 bits of data are equal. then a "1" is output from each I/O.
If there is a difference in the read data for a given 2 bit pair, a "0" will be output from that I/O.

c. Exiting the test mode:
The NN514400A/B will exit the test mode by either a RAS only refresh cycle or a CAS before RAS refresh cycle width WE "high".

d. Refresh during test mode:
During test mode refresh must be executed by a normal Read cycle or a WE, CAS before RAS refresh cycle.

SELF REFRESH MODE



■ The NN514400AL/BL version has a Self Refresh Mode.

a. Entering the Self Refresh Mode:
The NN514400AL/BL Self Refresh Mode is entered by using $\overline{CAS}$ before $\overline{RAS}$ cycle with $\overline{WE}$ " high " and holding $\overline{RAS}$ and $\overline{CAS}$ signal " low " longer than 300μs.

b. Continuing the Self Refresh Mode:
The Self Refresh Mode is continued by holding $\overline{RAS}$ " low " after entering the Self Refresh Mode.
It does not depend on $\overline{CAS}$ being " high " or " low " after entering the Self Refresh Mode for to continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:
The NN514400AL/BL exits the Self Refresh Mode when the $\overline{RAS}$ signal is brought " high ".

ORDERING INFORMATION

NN514400XXX(X) - XX

SPEED	45	:	45ns
	50	:	50ns
	60	:	60ns
	70	:	70ns
PACKAGE	J	:	Plastic SOJ
	TT	:	Plastic TSOP TYPE II (Normal Bend)
	RR	:	Plastic TSOP TYPE II (Reverse Bend)
VERSION	BLANK	:	Standard Version
	L	:	Long Refresh Version 128ms Refresh
DESIGN CODE	A	:	NN514400A
	B	:	NN514400B
MODE	4400	:	Fast Page 1M x 4