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# 1/3-INCH SOC MEGAPIXEL CMOS DIGITAL IMAGE SENSOR

**MT9M111I29STC**
*(Micron Part Number)*

## Features

- DigitalClarity CMOS Imaging Technology
- System-on-a-Chip (SOC)—Completely integrated camera system
- Ultra-low power, low cost, progressive scan CMOS image sensor
- Superior low-light performance
- On-chip image flow processor (IFP) performs sophisticated processing:
  Color recovery and correction
  Sharpening, gamma, lens-shading correction
  On-the-fly defect correction
- Filtered image downscaling to arbitrary size with smooth, continuous zoom and pan
- Automatic Features:
  Auto exposure, auto white balance (AWB), auto black reference (ABR), auto flicker avoidance, auto color saturation, auto defect identification and correction
- Fully automatic Xenon and LED-type flash support
  Fast exposure adaptation
- Multiple parameter contexts
  Easy/fast mode switching
- Camera control sequencer automates:
  Snapshots
  Snapshots with flash
  Video clips
- Simple two-wire serial programming interface
- ITU-R BT.656 (YCbCr), 565RGB, 555RGB, or 444RGB formats (progressive scan)
- Raw and processed Bayer formats
- Output FIFO and integer clock divider:
  "Uniform" pixel clocking

## Applications

- Cellular phones
- PDAs
- Toys
- Other battery-powered products

## Table 1: Key Performance Parameters

| PARAMETER | | TYPICAL VALUE |
|---|---|---|
| Optical Format | | 1/3-inch (5:4) |
| Active Imager Size | | 4.6mm(H) x 3.7mm (V), 5.9mm diagonal |
| Active Pixels | | 1,280H x 1,024V |
| Pixel Size | | 3.6µm x 3.6µm |
| Color Filter Array | | RGB Bayer Pattern |
| Shutter Type | | Electronic Rolling Shutter (ERS) |
| Maximum Data Rate/ Maximum Master Clock | | 27 MPS/54 MHz |
| Frame Rate | SXGA (1,280 x 1,024) | 15 fps at 54 MHz |
| | QSXGA (640 x 512) | 30 fps at 54 MHz |
| ADC Resolution | | 10 bit, dual on-chip |
| Responsivity | | 1.0 V/lux-sec (550nm) |
| Dynamic Range | | 71dB |
| $SNR_{MAX}$ | | 44dB |
| Supply Voltage | I/O Digital | 1.7V–3.6V |
| | Core Digital | 2.5V–3.1V |
| | Analog | 2.5V–3.1V |
| Power Consumption | | 170mW SXGA at 15 fps (54 MHz CLKIN) |
| | | 90mW QSXGA at 30 fps (54 MHz low-power mode) |
| Operating Temperature | | -30°C to +70°C |
| Packaging | | 44-Ball iCSP wafer or die |



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## General Description

The Micron® Imaging MT9M111 is an SXGA-format single-chip camera with a 1/3-inch CMOS active-pixel digital image sensor. This device combines the MT9M011 image sensor core with fourth-generation digital image flow processor technology from Micron Imaging. It captures high-quality color images at SXGA resolution.

The MT9M111 features DigitalClarity, Micron's breakthrough, low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost and integration advantages of CMOS.

The sensor is a complete camera-on-a-chip solution designed specifically to meet the low-power, low-cost demands of battery-powered products such as cellular phones, PDAs, and toys. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface.

The MT9M111 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure, automatic 50Hz/60Hz flicker avoidance, lens-shading correction, auto white balance (AWB), and on-the-fly defect identification and correction. Additional features include day/night mode configurations; special camera effects such as sepia tone and solarization; and interpolation to arbitrary image size with continuous filtered zoom and pan. The device supports both Xenon and LED-type flash light sources in several snapshot modes.

The MT9M111 can be programmed to output progressive-scan images up to 30 frames per second (fps) in preview power-saving mode, and 15 fps in full-resolution (SXGA) mode. In either mode, the image data can be output in any one of six 8-bit formats:

- ITU-R BT.656 (formerly CCIR656, progressive scan only) YCbCr
- 565RGB
- 555RGB
- 444RGB
- Raw Bayer
- "Processed" Bayer

The FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.



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## Functional Overview

The MT9M111 is a fully-automatic, single-chip camera, requiring only a power supply, lens and clock source for basic operation. Output video is streamed via a parallel 8-bit DOUT port, shown in Figure 1 on page 8. The output pixel clock is used to latch data, while FRAME_VALID and LINE_VALID signals indicate the active video. The MT9M111 internal registers are configured using a two-wire serial interface.

The device can be put in low-power sleep mode by asserting the standby pin and shutting down the clock. Output pins can be tri-stated by de-asserting the OE# pin. Both tri-stating output pins and entry in standby mode also can be achieved via two-wire serial interface register writes.

The MT9M111 accepts input clocks up to 54 MHz, delivering up to 15 fps for SXGA resolution images, and up to 30 fps for QSXGA (full field-of-view, sensor pixel skipping) images. The device also supports a low-power preview configuration that delivers SXGA images at 7.5 fps and QSXGA images at 30 fps. The device can be programmed to slow the frame rate in low-light conditions to achieve longer exposures and better image quality.

### Internal Architecture

Internally, the MT9M111 consists of a sensor core and an IFP. The IFP is divided in two sections: the colorpipe (CP), and the camera controller (CC). The sensor core captures raw Bayer-encoded images that are then input in the IFP. The CP section of the IFP processes the incoming stream to create interpolated, color-corrected output, and the CC section controls the sensor core to maintain the desired exposure and color balance, and to support snapshot modes. The sensor core, CP, and CC registers are grouped in three separate address spaces, shown in Figure 2. When accessing internal registers via the two-wire serial interface, select the desired address space by programming the R240 shared register.

The MT9M111 accelerates mode switching with hardware-assisted context switching, and supports taking snapshots, flash snapshots, and video clips using a configurable sequencer.

The MT9M111 supports a range of color formats derived from four primary color representations: YCbCr, RGB, raw Bayer (unprocessed, directly from the sensor), and processed Bayer (Bayer format data regenerated from processed RGB). The device also supports a variety of output signaling/timing options:

- Standard FRAME_VALID/LINE_VALID video interface with gated pixel clocks
- Standard video interface with uniform clocking
- ITU-R BT.656 marker-embedded video interface with either gated or uniform pixel clocking.

### Register Notation

The following register address notations are used in this document:

- R<decimal address>:<address page>
  Example: R9:0—Shutter width register in sensor page (page 0). Used to uniquely specify a register.
- R<decimal address>
  Example: R240—Page address register. Used when the register address is the same in all three pages or when by context the address page is understood.
- 0x<2 digit hex address>
  Example: 0xF0—Page address register. Used when the register address is the same in all three pages, or when by context the address page is understood.


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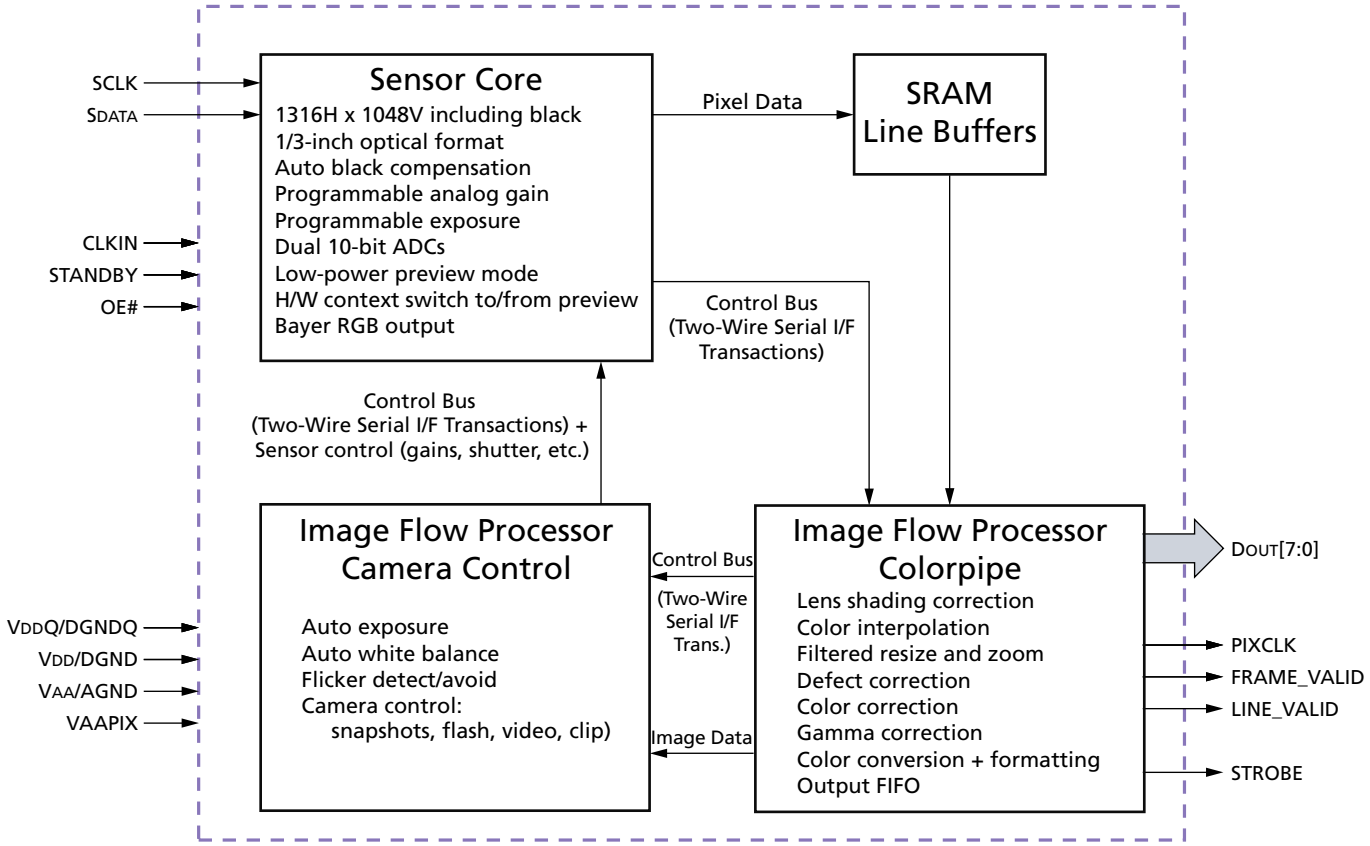
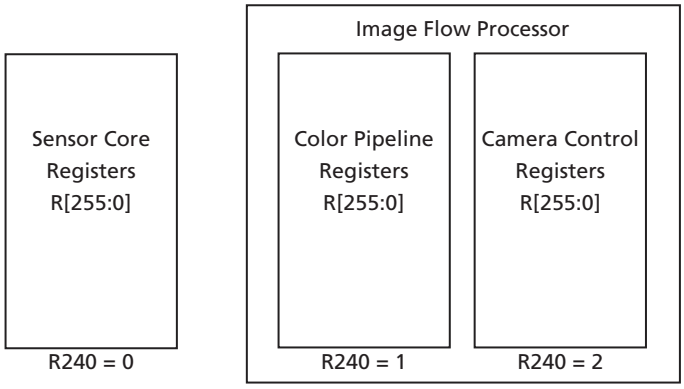
## Figure 1: Functional Block Diagram




## Figure 2: Internal Registers Grouping




NOTE:

Internal registers are grouped in three address spaces. Program R240 to select the desired address space.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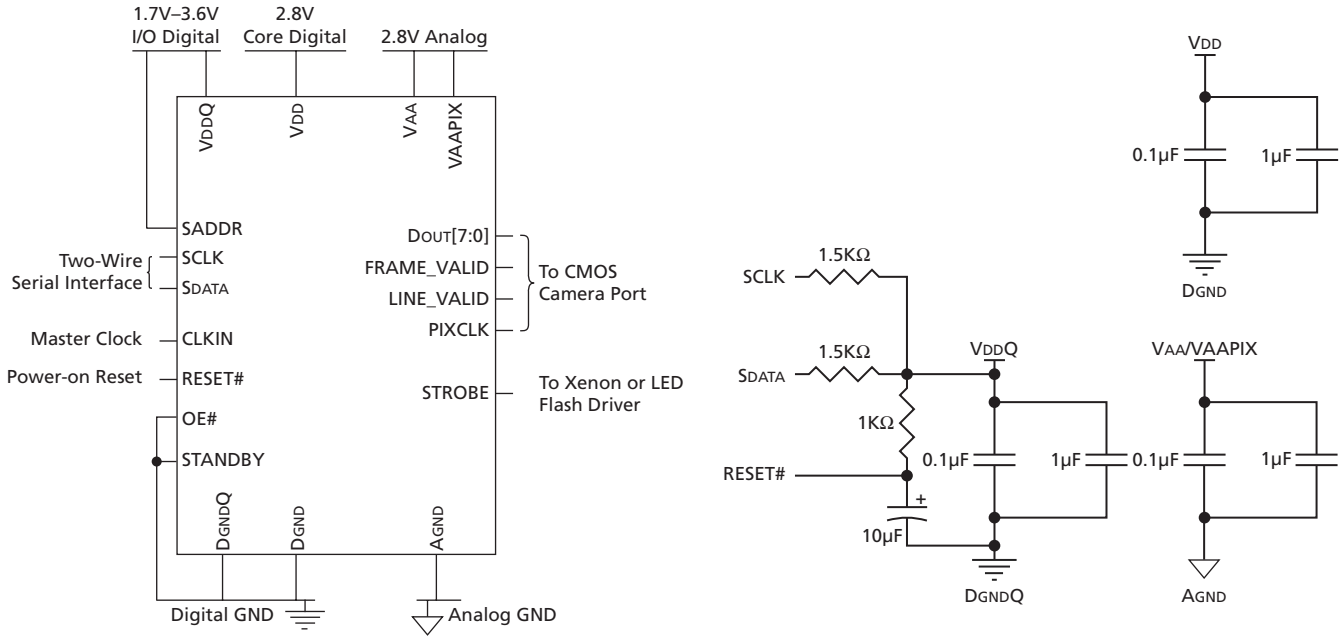
## Typical Connections

Figure 3 shows typical MT9M111 device connections. For low-noise operation, the MT9M111 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled to ground using ceramic capacitors. The use of inductance filters is not recommended.

The MT9M111 also supports different digital core (VDD/DGND) and I/O power (VDDQ/DGNDQ) power domains that can be at different voltages.

**Figure 3: Typical Configuration (Connection)**




NOTE:

1. 1.5KΩ resistor value recommended, but may be greater for slower two-wire speed.
2. VDD, VAA, VAAPIX must all be at the same potential, though if connected, care must be taken to avoid excessive noise injection in the VAA/VAAPIX power domains.



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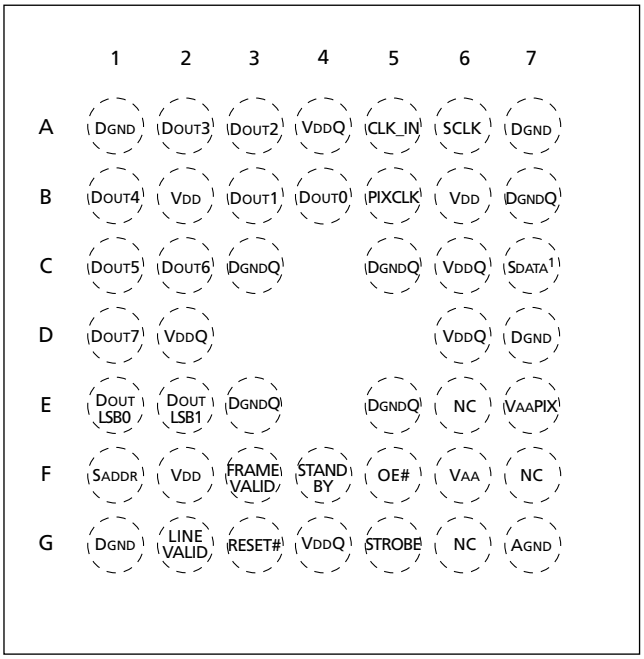
## Figure 4: 44-Ball iCSP Assignment




Top View
(Ball Down)

NOTE:
1. Bidirectional.

## Table 2: Pin Descriptions

| PIN NAME | PIN TYPE | DEFAULT OPERATION | DESCRIPTION |
|---|---|---|---|
| CLKIN | Bidirectional | Input | Master Clock in Sensor. |
| OE# | Bidirectional | Input | Active LOW: output enable for Data[7:0]. |
| RESET# | Bidirectional | Input | Active LOW: asynchronous reset. |
| SADDR | Bidirectional | Input | Two-Wire Serial Interface DeviceID selection 1:0xBA, 0:0x90. |
| SCLK | Bidirectional | Input | Two-Wire Serial Interface Clock. |
| STANDBY | Bidirectional | Input | Active HIGH: disables imager. |
| SDATA | Bidirectional | Input | Two-Wire Serial Interface Data I/O. |
| DOUT0 | Bidirectional | Output | Pixel Data Output 0 (LSB). |
| DOUT1 | Bidirectional | Output | Pixel Data Output 1. |
| DOUT2 | Bidirectional | Output | Pixel Data Output 2. |
| DOUT3 | Bidirectional | Output | Pixel Data Output 3. |
| DOUT4 | Bidirectional | Output | Pixel Data Output 4. |
| DOUT5 | Bidirectional | Output | Pixel Data Output 5. |
| DOUT6 | Bidirectional | Output | Pixel Data Output 6. |
| DOUT7 | Bidirectional | Output | Pixel Data Output 7 (MSB). |
| DOUT_LSB0 | Bidirectional | Output | Sensor bypass mode output 0—typically left unconnected for normal SOC operation. |



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## Table 2: Pin Descriptions (continued)

| PIN NAME | PIN TYPE | DEFAULT OPERATION | DESCRIPTION |
|---|---|---|---|
| DOUT_LSB1 | Bidirectional | Output | Sensor bypass mode output 1—typically left unconnected for normal SOC operation. |
| FRAME_VALID | Bidirectional | Output | Active HIGH: FRAME_VALID; indicates active frame. |
| LINE_VALID | Bidirectional | Output | Active HIGH: LINE_VALID, DATA_VALID; indicates active pixel. |
| PIXCLK | Bidirectional | Output | Pixel Clock Output. |
| STROBE | Bidirectional | Output | Active HIGH: strobe (Xenon) or turn on (LED) flash. |
| AGND | Supply | | Analog Ground. |
| DGND | Supply | | Core Digital Ground. |
| DGNDQ | Supply | | I/O Digital Ground. |
| VAA | Supply | | Analog Power (2.5V–3.1V). |
| VAAPIX | Supply | | Pixel Array Analog Power Supply (2.5V–3.1V). |
| VDD | Supply | | Core Digital Power (2.5V–3.1V). |
| VDDQ | Supply | | I/O Digital Power (1.7V–3.6V). |
| NC | — | | No connect. |

NOTE:

All inputs and outputs are implemented with bidirectional buffers. Care must be taken that all inputs are driven and all outputs are driven if tri-stated.



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## Architecture Overview

The MT9M111 consists of a sensor core, the color-processing pipeline, and a measurement and control-logic block (the camera controller). The following is a brief overview of the architecture.

### Sensor Core

The sensor core is taken from the MT9M011 stand-alone sensor and includes a number of features specifically targeting the mobile market. Of primary interest is support for low-power preview/viewfinding with hardware-accelerated switching to full-resolution for snapshots. This switch can be achieved without adversely affecting exposure or color balance. This enables taking single-frame and Xenon flash snapshots while minimizing snapshot lag. LED snapshots are discussed below; they also benefit significantly from this feature.

### Lens-Shading Correction and Black Level Conditioning

The stream of raw data from the sensor enters the pipeline and undergoes several transformations. Image stream processing starts with conditioning the black level and applying a digital gain.

The lens-shading block compensates for spatially varying signal loss caused by the lens. The block is programmable and implements separate correction functions for R,G, and B independently.

### Defect Correction

Following lens correction, the data stream is analyzed for the presence of defects. A two-dimensional digital filter calculates suitable replacement values. Edge sensitivity minimizes false detections, helping to preserve image sharpness.

### Interpolation, Aperture, and Color Correction

The Bayer pixel pattern data is interpolated to recover missing color components for each pixel following defect correction. Configurable aperture correction sharpens the image and to avoid amplifying noise, can be programmed to be less aggressive in low-light conditions.

The resulting interpolated RGB data passes through the current color correction matrix (CCM), gamma, and color saturation corrections.

The CCM can be manually loaded or dynamically configured by the AWB unit. The gamma correction unit is fully user-programmable, and color saturation adjustments can be made both by the user and the auto exposure unit (for dynamic saturation reduction in high or low-lighting situations).

### Resize

The IFP can resize to virtually any output resolution through digitally filtered sub-sampling. Output resolutions include, but are not limited to, VGA, QVGA, CIF, and QCIF. When the output resolution is smaller than the sensor-generated image, smooth, continuous zoom and pan become available. The user simply defines the zoom window, pan offset, and output resolution, and the resizer calculates all other parameters for the resize function.

### Camera Control

The camera controller continuously accumulates image brightness and color statistics. Two units use these measurements to adjust the sensor and color-pipe settings. The auto exposure unit adjusts gain and shutter width to maintain a user-defined luma target. The image measurement region can be modified to permit, for example, backlight compensation. The user can also control the speed and sensitivity of the algorithm from highly responsive (for LED flash and viewfinding) to somewhat dampened (for video). Finally, the unit can detect 50Hz or 60Hz rolling flicker bars (due to ambient illumination) and adjusts exposure appropriately to eliminate this adverse effect on image quality.

The AWB module adjusts gains and the CCM to compensate for the effects of changing scene illumination on the quality of the color rendition. The user has control over the region of the scene to be analyzed as well as the responsivity of the algorithm to illuminant changes.

### Camera Interface and Test Patterns

The MT9M111 outputs processed video as a standard ITU-R BT.656 stream, an RGB stream, or as processed or unprocessed Bayer data. The ITU-R BT.656 stream contains YCbCr 4:2:2 data with optional embedded synchronization codes. This output is typically suitable for subsequent display by standard (progressive scan) video equipment, or JPEG/MPEG compression. RGB functionality provides support for LCD devices.

The MT9M111 can be configured to output 16-bit RGB (RGB565), 15-bit RGB (RGB555), and two types of 12-bit RGB (RGB444). The user can configure internal


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registers to swap odd and even bytes, chrominance channels, and luminance and chrominance components to ease interfacing to application processors.

To assist in integration and system debug, a variety of test patterns are provided, from simple ramps to colorbars.

### Contexts, Snapshots, and Flash

For a number of parameters, registers are provided for storing two "contexts": Context A and Context B. These contexts enable the user to setup the camera for a number of different modes, then switch between modes with a single register write to the Global Context Control Register (GCCR). A typical example is to use Context A for viewfinder/preview settings and Context B for snapshots. Functions supporting context switching include:

- Sensor core image array readout (e.g., low-power QSXGA preview to/from full-power SXGA snapshot)
- The resizer (output resolutions for preview and snapshot)
- Camera interface (e.g., RGB565 for LCD preview and YCbCr for snapshots)

To facilitate taking snapshots and flash snapshots, the IFP includes a camera-control sequencer that automates the process of stepping through a number of preset configurable programs. In addition to basic snapshots, there are programs for both Xenon and LED assisted snapshots. A flash-triggering controller provides an appropriate timing strobe for synchronizing the onset of flash illumination with the rolling shutter.


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## *Output Data Ordering*

### Table 3: Data Ordering in YCbCr Mode

| MODE | BYTE | | | |
|---|---|---|---|---|
| Default | Cbi | Yi | Cri | Yi+1 |
| Swap CrCb | Cri | Yi | Cbi | Yi+1 |
| SwapYC | Yi | Cbi | Yi+1 | Cri |
| Swap CrCb, SwapYC | Yi | Cri | Yi+1 | Cbi |

### Table 4: Output Data Ordering in Processed Bayer Mode

| MODE | LINE | BYTE | | | |
|---|---|---|---|---|---|
| Default | First | Gi | Ri+1 | Gi+2 | Ri+3 |
| | Second | Bi | Gi+1 | Bi+2 | Gi+3 |
| Flip Bayer Col | First | Ri | Gi+1 | Ri+2 | Gi+3 |
| | Second | Gi | Bi+1 | Gi+2 | Bi+3 |
| Flip Bayer Row | First | Bi | Gi+1 | Bi+2 | Gi+3 |
| | Second | Gi | Ri+1 | Gi+2 | Ri+3 |
| Flip Bayer Col, Flip Bayer Row | First | Gi | Bi+1 | Gi+2 | Bi+3 |
| | Second | Ri | Gi+1 | Ri+2 | Gi+3 |

### Table 5: Output Data Ordering in RGB Mode

| MODE (SWAP DISABLED) | BYTE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| RGB565 | First | R7 | R6 | R5 | R4 | R3 | G7 | G6 | G5 |
| | Second | G4 | G3 | G2 | B7 | B6 | B5 | B4 | B3 |
| RGB555 | First | 0 | R7 | R6 | R5 | R4 | R3 | G7 | G6 |
| | Second | G5 | G4 | G3 | B7 | B6 | B5 | B4 | B3 |
| RGB444x | First | R7 | R6 | R5 | R4 | G7 | G6 | G5 | G4 |
| | Second | B7 | B6 | B5 | B4 | 0 | 0 | 0 | 0 |
| RGBx444 | First | 0 | 0 | 0 | 0 | R7 | R6 | R5 | R4 |
| | Second | G7 | G6 | G5 | G4 | B7 | B6 | B5 | B4 |

### Table 6: Output Data Ordering in (8 + 2) Bypass Mode

| MODE | BYTE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 8 + 2 bypass | First | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 |
| | Second | 0 | 0 | 0 | 0 | 0 | 0 | B1 | B0 |



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## IFP Register List

### Table 7: Colorpipe Registers (Address Page 1)

| REGISTER #DEC (HEX) | REGISTER NAME | DATA FORMAT | DEFAULT VALUE DEC (HEX) | MODULE |
|---|---|---|---|---|
| 5 (05) | Aperture Correction | 0000 0000 0000 dddd | 3 (0003) | Interp |
| 6 (06) | Operating Mode Control | dddd dddd 0ddd dddd | 28686 (700E) | Cfg |
| 8 (08) | Output Format Control | 0000 0ddd dddd dddd | 128 (0080) | Cfg |
| 16 (10) | Reserved | — | 61437 (EFFD) | — |
| 17 (11) | Reserved | — | 64831 (FD3F) | — |
| 18 (12) | Reserved | — | 16367 (3FEF) | — |
| 19 (13) | Reserved | — | N/A | — |
| 20 (14) | Reserved | — | N/A | — |
| 21 (15) | Reserved | — | N/A | — |
| 27 (1B) | Reserved | — | 0 (0000) | — |
| 28 (1C) | Reserved | — | 0 (0000) | — |
| 29 (1D) | Reserved | — | N/A | — |
| 30 (1E) | Reserved | — | 512 (0200) | — |
| 37 (25) | Color Saturation Control | 0000 0000 00dd dddd | 5 (0005) | rgb2yuv |
| 52 (34) | Luma Offset | dddd dddd dddd dddd | 16 (0010) | CamInt |
| 53 (35) | Luma Clip | dddd dddd dddd dddd | 61456 (F010) | CamInt |
| 58 (3A) | Output Format Control 2—Context A | 0ddd dddd dddd dddd | 512 (0200) | CamInt |
| 59 (3B) | Lens Correction Parameter 1 | — | 1066 (042A) | LensCorr |
| 60 (3C) | Lens Correction Parameter 2 | — | 1024 (0400) | LensCorr |
| 71 (47) | Reserved | — | 24 (0018) | — |
| 72 (48) | Test Pattern Generator Control | 0000 0000 d000 0ddd | 0 (0000) | FifoInt |
| 76 (4C) | Defect Correction Context A | 0000 0000 0000 0ddd | 0 (0000) | DfctCorr |
| 77 (4D) | Defect Correction Context B | 0000 0000 0000 0ddd | 0 (0000) | DfctCorr |
| 78 (4E) | Reserved | — | 10 (000A) | — |
| 80 (50) | Reserved | — | N/A | — |
| 82 (52) | Reserved | — | 0 (0000) | — |
| 83 (53) | Gamma Correction Parameter 1 | — | 7700 (1E14) | GmaCorr |
| 84 (54) | Gamma Correction Parameter 2 | — | 17966 (462E) | GmaCorr |
| 85 (55) | Gamma Correction Parameter 3 | — | 34666 (876A) | GmaCorr |
| 86 (56) | Gamma Correction Parameter 4 | — | 47008 (B7A0) | GmaCorr |
| 87 (57) | Gamma Correction Parameter 5 | — | 57548 (E0CC) | GmaCorr |
| 88 (58) | Gamma Correction Parameter 6 | — | 0 (0000) | GmaCorr |
| 104 (68) | Reserved | — | 17 (0011) | — |
| 128 (80) | Lens Correction Parameter 3 | — | 7 (0007) | LensCorr |
| 129 (81) | Lens Correction Parameter 4 | — | 56588 (DD0C) | LensCorr |
| 130 (82) | Lens Correction Parameter 5 | — | 62696 (F4E8) | LensCorr |
| 131 (83) | Lens Correction Parameter 6 | — | 1276 (04FC) | LensCorr |
| 132 (84) | Lens Correction Parameter 7 | — | 57868 (E20C) | LensCorr |
| 133 (85) | Lens Correction Parameter 8 | — | 63212 (F6EC) | LensCorr |
| 134 (86) | Lens Correction Parameter 9 | — | 764 (02FC) | LensCorr |
| 135 (87) | Lens Correction Parameter 10 | — | 56588 (DD0C) | LensCorr |
| 136 (88) | Lens Correction Parameter 11 | — | 62696 (F4E8) | LensCorr |
| 137 (89) | Lens Correction Parameter 12 | — | 250 (00FA) | LensCorr |



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## Table 7: Colorpipe Registers (Address Page 1) (continued)

| REGISTER #DEC (HEX) | REGISTER NAME | DATA FORMAT | DEFAULT VALUE DEC (HEX) | MODULE |
|---|---|---|---|---|
| 138 (8A) | Lens Correction Parameter 13 | — | 34866 (8832) | LensCorr |
| 139 (8B) | Lens Correction Parameter 14 | — | 56754 (DDB2) | LensCorr |
| 140 (8C) | Lens Correction Parameter 15 | — | 63466 (F7EA) | LensCorr |
| 141 (8D) | Lens Correction Parameter 16 | — | 2 (0002) | LensCorr |
| 142 (8E) | Lens Correction Parameter 17 | — | 47646 (BA1E) | LensCorr |
| 143 (8F) | Lens Correction Parameter 18 | — | 60627 (ECD3) | LensCorr |
| 144 (90) | Lens Correction Parameter 19 | — | 63473 (F7F1) | LensCorr |
| 145 (91) | Lens Correction Parameter 20 | — | 255 (00FF) | LensCorr |
| 146 (92) | Lens Correction Parameter 21 | — | 48926 (BF1E) | LensCorr |
| 147 (93) | Lens Correction Parameter 22 | — | 61142 (EED6) | LensCorr |
| 148 (94) | Lens Correction Parameter 23 | — | 63474 (F7F2) | LensCorr |
| 149 (95) | Lens Correction Parameter 24 | — | 3 (0003) | LensCorr |
| 153 (99) | Line Counter | ???? ???? ???? ???? | N/A | CamInt |
| 154 (9A) | Frame Counter | ???? ???? ???? ???? | N/A | CamInt |
| 155 (9B) | Output Format Control 2—Context B | 0ddd dddd dddd dddd | 512 (0200) | CamInt |
| 157 (9D) | Reserved | — | 9390 (24AE) | — |
| 158 (9E) | Reserved | — | N/A | — |
| 159 (9F) | Reducer Horizontal Pan—Context B | 0d00 0ddd dddd dddd | 0 (0000) | Interp |
| 160 (A0) | Reducer Horizontal Zoom—Context B | 0000 0ddd dddd dddd | 1280 (0500) | Interp |
| 161 (A1) | Reducer Horizontal Size—Context B | 0000 0ddd dddd dddd | 1280 (0500) | Interp |
| 162 (A2) | Reducer Vertical Pan—Context B | 0d00 0ddd dddd dddd | 0 (0000) | Interp |
| 163 (A3) | Reducer Vertical Zoom—Context B | 0000 0ddd dddd dddd | 1024 (0400) | Interp |
| 164 (A4) | Reducer Vertical Size—Context B | 0000 0ddd dddd dddd | 1024 (0400) | Interp |
| 165 (A5) | Reducer Horizontal Pan—Context A | 0d00 0ddd dddd dddd | 0 (0000) | Interp |
| 166 (A6) | Reducer Horizontal Zoom—Context A | 0000 0ddd dddd dddd | 1280 (0500) | Interp |
| 167 (A7) | Reducer Horizontal Size—Context A | 0000 0ddd dddd dddd | 640 (0280) | Interp |
| 168 (A8) | Reducer Vertical Pan—Context A | 0d00 0ddd dddd dddd | 0 (0000) | Interp |
| 169 (A9) | Reducer Vertical Zoom—Context A | 0000 0ddd dddd dddd | 1024 (0400) | Interp |
| 170 (AA) | Reducer Vertical Size—Context A | 0000 0ddd dddd dddd | 512 (0200) | Interp |
| 171 (AB) | Reducer Current Zoom Horizontal | ???? 0??? ???? ???? | N/A | Interp |
| 172 (AC) | Reducer Current Zoom Vertical | ???? 0??? ???? ???? | N/A | Interp |
| 174 (AE) | Reducer Zoom Step Size | dddd dddd dddd dddd | 1284 (0504) | Interp |
| 175 (AF) | Reducer Zoom Control | 0000 00dd 0ddd dddd | 16 (0010) | Interp |
| 179 (B3) | Global Clock Control | 0000 0000 0000 00dd | 2 (0002) | ClockRst |
| 180 (B4) | Reserved | — | 32 (0020) | — |
| 181 (B5) | Uniform Clocking Control Parameter | — | 257 (0101) | — |
| 182 (B6) | Lens Correction Parameter 25 | — | 4363 (110B) | LensCorr |
| 183 (B7) | Lens Correction Parameter 26 | — | 15399 (3C27) | LensCorr |
| 184 (B8) | Lens Correction Parameter 27 | — | 4362 (110A) | LensCorr |
| 185 (B9) | Lens Correction Parameter 28 | — | 12834 (3222) | LensCorr |
| 186 (BA) | Lens Correction Parameter 29 | — | 5643 (160B) | LensCorr |
| 187 (BB) | Lens Correction Parameter 30 | — | 12836 (3224) | LensCorr |
| 188 (BC) | Lens Correction Parameter 31 | — | 9228 (240C) | LensCorr |
| 189 (BD) | Lens Correction Parameter 32 | — | 24124 (5E3C) | LensCorr |
| 190 (BE) | Lens Correction Parameter 33 | — | 127 (007F) | LensCorr |



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## Table 7: Colorpipe Registers (Address Page 1) (continued)

| REGISTER #DEC (HEX) | REGISTER NAME | DATA FORMAT | DEFAULT VALUE DEC (HEX) | MODULE |
|---|---|---|---|---|
| 191 (BF) | Lens Correction Parameter 34 | — | 8200 (2008) | LensCorr |
| 192 (C0) | Lens Correction Parameter 35 | — | 20023 (4E37) | LensCorr |
| 193 (C1) | Lens Correction Parameter 36 | — | 100 (0064) | LensCorr |
| 194 (C2) | Lens Correction Parameter 37 | — | 8463 (210F) | LensCorr |
| 195 (C3) | Lens Correction Parameter 38 | — | 19250 (4B32) | LensCorr |
| 196 (C4) | Lens Correction Parameter 39 | — | 100 (0064) | LensCorr |
| 200 (C8) | Global Context Control | dddd dddd dddd dddd | 0 (0000) | CntxCtl |
| 201 (C9) | Reserved | — | N/A | — |
| 202 (CA) | Reserved | — | N/A | — |
| 203 (CB) | Reserved | — | N/A | — |
| 204 (CC) | Reserved | — | N/A | — |
| 205 (CD) | Reserved | — | N/A | — |
| 206 (CE) | Reserved | — | N/A | — |
| 207 (C) | Reserved | — | N/A | — |
| 208 (D0) | Reserved | — | N/A | — |
| 220 (DC) | Gamma Correction Parameter 7 | — | 7700 (1E14) | GmaCorr |
| 221 (DD) | Gamma Correction Parameter 8 | — | 17966 (462E) | GmaCorr |
| 222 (DE) | Gamma Correction Parameter 9 | — | 34666 (876A) | GmaCorr |
| 223 (DF) | Gamma Correction Parameter 10 | — | 47008 (B7A0) | GmaCorr |
| 224 (E0) | Gamma Correction Parameter 11 | — | 57548 (E0CC) | GmaCorr |
| 225 (E1) | Gamma Correction Parameter 12 | — | 0 (0000) | GmaCorr |
| 226 (E2) | Effects Mode | dddd dddd 0000 0ddd | 28672 (7000) | GmaCorr |
| 227 (E3) | Effects Sepia | dddd dddd dddd dddd | 45091 (B023) | GmaCorr |
| 240 (F0) | Page Map | 0000 0000 0000 0ddd | 0 (0000) | Cfg |
| 241 (F1) | Byte-wise Address | — | Reserved | — |

## Table 8: Camera Control Registers (Address Page 2)

| REGISTER #DEC (HEX) | REGISTER NAME | DATA FORMAT | DEFAULT VALUE DEC (HEX) | MODULE |
|---|---|---|---|---|
| 2 (02) | Color Correction Parameter 1 | — | 110 (006E) | ColorCorr |
| 3 (03) | Color Correction Parameter 2 | — | 10531 (2923) | ColorCorr |
| 4 (04) | Color Correction Parameter 3 | — | 1316 (0524) | ColorCorr |
| 9 (09) | Color Correction Parameter 4 | — | 146 (0092) | ColorCorr |
| 10 (0A) | Color Correction Parameter 5 | — | 22 (0016) | ColorCorr |
| 11 (0B) | Color Correction Parameter 6 | — | 8 (0008) | ColorCorr |
| 12 (0C) | Color Correction Parameter 7 | — | 171 (00AB) | ColorCorr |
| 13 (0D) | Color Correction Parameter 8 | — | 147 (0093) | ColorCorr |
| 14 (0E) | Color Correction Parameter 9 | — | 88 (0058) | ColorCorr |
| 15 (0F) | Color Correction Parameter 10 | — | 77 (004D) | ColorCorr |
| 16 (10) | Color Correction Parameter 11 | — | 169 (00A9) | ColorCorr |
| 17 (11) | Color Correction Parameter 12 | — | 160 (00A0) | ColorCorr |
| 18 (12) | Color Correction Parameter 13 | — | N/A | ColorCorr |
| 19 (13) | Color Correction Parameter 14 | — | N/A | ColorCorr |



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## Table 8: Camera Control Registers (Address Page 2) (continued)

| REGISTER #DEC (HEX) | REGISTER NAME | DATA FORMAT | DEFAULT VALUE DEC (HEX) | MODULE |
|---|---|---|---|---|
| 20 (14) | Color Correction Parameter 15 | — | N/A | ColorCorr |
| 21 (15) | Color Correction Parameter 16 | — | 373 (0175) | ColorCorr |
| 22 (16) | Color Correction Parameter 17 | — | 22 (0016) | ColorCorr |
| 23 (17) | Color Correction Parameter 18 | — | 67 (0043) | ColorCorr |
| 24 (18) | Color Correction Parameter 19 | — | 12 (000C) | ColorCorr |
| 25 (19) | Color Correction Parameter 20 | — | 0 (0000) | ColorCorr |
| 26 (1A) | Color Correction Parameter 21 | — | 21 (0015) | ColorCorr |
| 27 (1B) | Color Correction Parameter 22 | — | 31 (001F) | ColorCorr |
| 28 (1C) | Color Correction Parameter 23 | — | 22 (0016) | ColorCorr |
| 29 (1D) | Color Correction Parameter 24 | — | 152 (0098) | ColorCorr |
| 30 (1E) | Color Correction Parameter 25 | — | 76 (004C) | ColorCorr |
| 31 (1F) | AWB Parameter 1 | — | 160 (00A0) | AWB |
| 32 (20) | AWB Parameter 2 | — | 51220 (C814) | AWB |
| 33 (21) | AWB Parameter 3 | — | 32896 (8080) | AWB |
| 34 (22) | AWB Parameter 4 | — | 55648 (D960) | AWB |
| 35 (23) | AWB Parameter 5 | — | 55648 (D960) | AWB |
| 36 (24) | AWB Parameter 6 | — | 32512 (7F00) | AWB |
| 38 (26) | Auto Exposure Window Horizontal Boundaries | dddd dddd dddd dddd | 32768 (8000) | AutoExp |
| 39 (27) | Auto Exposure Window Vertical Boundaries | dddd dddd dddd dddd | 32776 (8008) | AutoExp |
| 40 (28) | AWB Parameter 7 | — | 61188 (EF04) | AWB |
| 41 (29) | AWB Parameter 8 | — | 36211 (8D73) | AWB |
| 42 (2A) | AWB Parameter 9 | — | 208 (00D0) | AWB |
| 43 (2B) | Auto Exposure Center Horizontal Window Boundaries | dddd dddd dddd dddd | 24608 (6020) | AutoExp |
| 44 (2C) | Auto Exposure Center Vertical Window Boundaries | dddd dddd dddd dddd | 24608 (6020) | AutoExp |
| 45 (2D) | AWB Window Boundaries | dddd dddd dddd dddd | 61600 (F0A0) | AWB |
| 46 (2E) | Auto Exposure Target and Precision Control | dddd dddd dddd dddd | 3146 (0C4A) | AutoExp |
| 47 (2F) | Auto Exposure Speed and Sensitivity Control—Context A | dddd dddd dddd dddd | 57120 (DF20) | AutoExp |
| 48 (30) | AWB Parameter 10 | — | N/A | AWB |
| 49 (31) | AWB Parameter 11 | — | N/A | AWB |
| 50 (32) | AWB Parameter 12 | — | N/A | AWB |
| 51 (33) | Auto Exposure Parameter 1 | — | 5230 (146E) | AutoExp |
| 54 (36) | Auto Exposure Parameter 2 | — | 30736 (7810) | AutoExp |
| 55 (37) | Auto Exposure Parameter 3 | — | 768 (0300) | AutoExp |
| 56 (38) | Auto Exposure Parameter 4 | — | 1088 (0440) | AutoExp |
| 57 (39) | Auto Exposure Parameter 5 | — | 1676 (068C) | AutoExp |
| 58 (3A) | Auto Exposure Parameter 6 | — | 1676 (068C) | AutoExp |
| 59 (3B) | Auto Exposure Parameter 7 | — | 1676 (068C) | AutoExp |
| 60 (3C) | Auto Exposure Parameter 8 | — | 1676 (068C) | AutoExp |
| 61 (3D) | Auto Exposure Parameter 9 | — | 6105 (17D9) | AutoExp |
| 62 (3E) | AWB Parameter 13 | — | 7423 (1CFF) | AWB |
| 63 (3F) | Auto Exposure Parameter 10 | — | N/A | AutoExp |
| 70 (46) | Auto Exposure Parameter 11 | — | 55552 (D900) | AutoExp |
| 75 (4B) | Reserved | — | 0 (0000) | — |
| 76 (4C) | Auto Exposure Parameter 12 | — | N/A | AutoExp |



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## Table 8: Camera Control Registers (Address Page 2) (continued)

| REGISTER #DEC (HEX) | REGISTER NAME | DATA FORMAT | DEFAULT VALUE DEC (HEX) | MODULE |
|---|---|---|---|---|
| 77 4D) | Auto Exposure Parameter 13 | — | N/A | AutoExp |
| 79 (4F) | Reserved | — | N/A | — |
| 87 (57) | Auto Exposure Parameter 14 | — | 537 (0219) | AutoExp |
| 88 (58) | Auto Exposure Parameter 15 | — | 644 (0284) | AutoExp |
| 89 (59) | Auto Exposure Parameter 16 | — | 537 (0219) | AutoExp |
| 90 (5A) | Auto Exposure Parameter 17 | — | 644 (0284) | AutoExp |
| 91 (5B) | Flicker Control 0 | ?000 0000 0000 0ddd | 2 (0002) | FD |
| 92 (5C) | Reserved | — | 4620 (120C) | — |
| 93 (5D) | Reserved | — | 5394 (1512) | — |
| 94 (5E) | Color Correction Parameter 26 | — | 26684 (683C) | ColorCorr |
| 95 (5F) | Color Correction Parameter 27 | — | 12296 (3008) | ColorCorr |
| 96 (60) | Color Correction Parameter 28 | — | 2 (0002) | ColorCorr |
| 97 (61) | Reserved | — | 32896 (8080) | — |
| 98 (62) | Auto Exposure Digital Gains Monitor | ???? ???? ???? ???? | N/A | AutoExp |
| 99 (63) | Reserved | — | N/A | — |
| 100 (64) | Reserved | — | 23036 (59FC) | — |
| 101 (65) | Auto Exposure Parameter 18 | — | 0 (0000) | AutoExp |
| 103 (67) | Auto Exposure Digital Gain Limits | dddd dddd dddd dddd | 16400 (4010) | AutoExp |
| 104 (68) | Reserved | — | 17 (0011) | — |
| 106 (6A) | Reserved | — | N/A | — |
| 107 (6B) | Reserved | — | N/A | — |
| 108 (6C) | Reserved | — | N/A | — |
| 109 (6D) | Reserved | — | N/A | — |
| 110 (6E) | Reserved | — | N/A | — |
| 111 (6F) | Reserved | — | N/A | — |
| 112 (70) | Reserved | — | N/A | — |
| 113 (71) | Reserved | — | N/A | — |
| 114 (72) | Reserved | — | N/A | — |
| 115 (73) | Reserved | — | N/A | — |
| 116 (74) | Reserved | — | N/A | — |
| 117 (75) | Reserved | — | N/A | — |
| 118 (76) | Reserved | — | N/A | — |
| 119 (77) | Reserved | — | N/A | — |
| 120 (78) | Reserved | — | N/A | — |
| 121 (79) | Reserved | — | N/A | — |
| 122 (7A) | Reserved | — | N/A | — |
| 123 (7B) | Reserved | — | N/A | — |
| 124 (7C) | Reserved | — | N/A | — |
| 125 (7D) | Reserved | — | N/A | — |
| 130 (82) | Auto Exposure Parameter 19 | — | 1020 (03FC) | AutoExp |
| 131 (83) | Auto Exposure Parameter 20 | — | 769 (0301) | AutoExp |
| 132 (84) | Auto Exposure Parameter 21 | — | 193 (00C1) | AutoExp |
| 133 (85) | Auto Exposure Parameter 22 | — | 929 (03A1) | AutoExp |
| 134 (86) | Auto Exposure Parameter 23 | — | 980 (03D4) | AutoExp |
| 135 (87) | Auto Exposure Parameter 24 | — | 983 (03D7) | AutoExp |



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## Table 8: Camera Control Registers (Address Page 2) (continued)

| REGISTER #DEC (HEX) | REGISTER NAME | DATA FORMAT | DEFAULT VALUE DEC (HEX) | MODULE |
|---|---|---|---|---|
| 136 (88) | Auto Exposure Parameter 25 | — | 921 (0399) | AutoExp |
| 137 (89) | Auto Exposure Parameter 26 | — | 1016 (03F8) | AutoExp |
| 138 (8A) | Auto Exposure Parameter 27 | — | 28 (001C) | AutoExp |
| 139 (8B) | Auto Exposure Parameter 28 | — | 957 (03BD) | AutoExp |
| 140 (8C) | Auto Exposure Parameter 29 | — | 987 (03DB) | AutoExp |
| 141 (8D) | Auto Exposure Parameter 30 | — | 957 (03BD) | AutoExp |
| 142 (8E) | Auto Exposure Parameter 31 | — | 1020 (03FC) | AutoExp |
| 143 (8F) | Auto Exposure Parameter 32 | — | 990 (03DE) | AutoExp |
| 144 (90) | Auto Exposure Parameter 33 | — | 990 (03DE) | AutoExp |
| 145 (91) | Auto Exposure Parameter 34 | — | 990 (03DE) | AutoExp |
| 146 (92) | Auto Exposure Parameter 35 | — | 990 (03DE) | AutoExp |
| 147 (93) | Auto Exposure Parameter 36 | — | 31 (001F) | AutoExp |
| 148 (94) | Auto Exposure Parameter 37 | — | 65 (0041) | AutoExp |
| 149 (95) | Auto Exposure Parameter 38 | — | 867 (0363) | AutoExp |
| 150 (96) | Reserved | — | 0 (0000) | — |
| 151 (97) | Reserved | — | N/A | — |
| 152 (98) | Reserved | — | 255 (00FF) | — |
| 153 (99) | Reserved | — | 1 (0001) | — |
| 156 (9C) | Auto Exposure Speed and Sensitivity Control—Context B | dddd dddd dddd dddd | 57120 (DF20) | AutoExp |
| 180 (B4) | Reserved | — | 32 (0020) | — |
| 181 (B5) | Reserved | — | N/A | — |
| 198 (C6) | Reserved | — | 0 (0000) | — |
| 199 (C7) | Reserved | — | N/A | — |
| 200 (C8) | Global Context Control | dddd dddd dddd dddd | 0 (0000) | CntxCtl |
| 201 (C9) | Camera Control Sequencer Parameter 1 | — | N/A | CamCtl |
| 202 (CA) | Camera Control Sequencer Parameter 2 | — | N/A | CamCtl |
| 203 (CB) | Camera Control Sequencer Parameter 3 | — | 0 (0000) | CamCtl |
| 204 (CC) | Camera Control Sequencer Parameter 4 | — | 0 (0000) | CamCtl |
| 205 (CD) | Camera Control Sequencer Parameter 5 | — | 8608 (21A0) | CamCtl |
| 206 (CE) | Camera Control Sequencer Parameter 6 | — | 7835 (1E9B) | CamCtl |
| 207 (CF) | Camera Control Sequencer Parameter 7 | — | 19018 (4A4A) | CamCtl |
| 208 (D0) | Camera Control Sequencer Parameter 8 | — | 5773 (168D) | CamCtl |
| 209 (D1) | Camera Control Sequencer Parameter 9 | — | 77 (004D) | CamCtl |
| 210 (D2) | Camera Control Sequencer Parameter 10 | — | 0 (0000) | CamCtl |
| 211 (D3) | Context Control Parameter 1 | — | 0 (0000) | CntxCtl |
| 212 (D4) | Camera Control Sequencer Parameter 11 | — | 520 (0208) | CamCtl |
| 213 (D5) | Camera Control Sequencer Parameter 12 | — | 0 (0000) | CamCtl |
| 239 (EF) | AWB Parameter 14 | — | 8 (0008) | AWB |
| 240 (F0) | Page Map | 0000 0000 0000 0ddd | 0 (0000) | Cfg |
| 241 (F1) | Byte-wise Address | — | Reserved | — |
| 242 (F2) | AWB Parameter 15 | — | 0 (0000) | AWB |
| 243 (F3) | Reserved | — | 0 (0000) | — |
| 244 (F4) | Color Correction Parameter 29 | — | 110 (006E) | ColorCorr |
| 245 (F5) | Color Correction Parameter 30 | — | 135 (0087) | ColorCorr |



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## Table 8: Camera Control Registers (Address Page 2) (continued)

| REGISTER #DEC (HEX) | REGISTER NAME | DATA FORMAT | DEFAULT VALUE DEC (HEX) | MODULE |
|---|---|---|---|---|
| 246 (F6) | Color Correction Parameter 31 | — | 54 (0036) | ColorCorr |
| 247 (F7) | Color Correction Parameter 32 | — | 13 (000D) | ColorCorr |
| 248 (F8) | Color Correction Parameter 33 | — | 171 (00AB) | ColorCorr |
| 249 (F9) | Color Correction Parameter 34 | — | 136 (0088) | ColorCorr |
| 250 (FA) | Color Correction Parameter 35 | — | 72 (0048) | ColorCorr |
| 251 (FB) | Color Correction Parameter 36 | — | 87 (0057) | ColorCorr |
| 252 (FC) | Color Correction Parameter 37 | — | 94 (005E) | ColorCorr |
| 253 (FD) | Color Correction Parameter 38 | — | 122 (007A) | ColorCorr |
| 254 (FE) | Color Correction Parameter 39 | — | 20543 (503F) | ColorCorr |
| 255 (FF) | Color Correction Parameter 40 | — | 43136 (A880) | ColorCorr |

NOTE:

Data Format Key:
0 = “Don't Care” bit. The exceptions: R0:0 and R255:0, which are hardwired R/O binary values.
d = R/W bit
? = R/O bit.



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## IFP Register Description

### *Configuration*

The vast majority of IFP registers associate naturally to one of the IFP modules. These modules are identified in Table 8 on page 17. Detailed register descriptions follow in Table 9. A few registers create effects across a number of module functions. These include R240 page map register (R/W); R6:1 0x106 operating mode control register (R/W); R8:1 0x108 output format control register (R/W); the R62:2 0x23E gain types and CCM threshold register—the gain threshold for CCM adjustment (R/W).

### Table 9: Colorpipe Register Description

| REGISTER# (HEX) | DESCRIPTION |
|---|---|
| **R5:1—0X105 - APERTURE CORRECTION** | |
| Default | 0x0003 |
| Description | Aperture correction scale factor, used for sharpening. |
| Bit 3 | Enables automatic sharpness reduction control (see R51:2 0x233). |
| Bits 2:0 | Sharpening factor:<br>“000”—No sharpening.<br>“001”—25% sharpening.<br>“010”—50% sharpening.<br>“011”—75% sharpening.<br>“100”—100% sharpening.<br>“101”—125% sharpening.<br>“110”—150% sharpening.<br>“111”—200% sharpening. |
| **R6:1—0X106 - OPERATING MODE CONTROL (R/W)** | |
| Default | 0x700E |
| Description | This register specifies the operating mode of the IFP. |
| Bit 15 | Enables manual white balance. User can set the base matrix and color channel gains. This bit must be asserted and de-asserted with a frame in between to force new color correction settings to take effect. |
| Bit 14 | Enables auto exposure. |
| Bit 13 | Enables on-the-fly defect correction. |
| Bit 12 | Clips aperture corrections. Small aperture corrections (< 8) are attenuated to reduce noise amplification. |
| Bit 11 | Load color correction matrix<br>1: In manual white balance mode, triggers the loading of a new base matrix in color correction and the loading of new base sensor gain ratios.<br>0: Enables the matrix to be changed “offline.” |
| Bit 10 | Enables lens-shading correction.<br>1: Enables lens-shading correction. |
| Bit 9 | Reserved. |
| Bit 8 | Reserved. |
| Bit 7 | Enables flicker detection.<br>1: Enables automatic flicker detection. |
| Bit 6 | Reserved for future expansion. |
| Bit 5 | Reserved. |
| Bit 4 | Bypasses color correction matrix.<br>1: Outputs “raw” color bypassing color correction.<br>0: Normal color processing. |



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## Table 9: Colorpipe Register Description (continued)

| | |
|---|---|
| Bits 3:2 | Auto exposure back light compensation control.<br>"00"—Auto exposure sampling window is specified by R38:2 and R39:2 ("large window").<br>"01"—Auto exposure sampling window is specified by R43:2 and R44:2 ("small window").<br>"1X"—Auto exposure sampling window is specified by the weighted sum of the large window and the small window, with the small window weighted four times more heavily. |
| Bit 1 | Enables AWB.<br>1: Enables auto white balance.<br>0: Freezes white balance at current values. |
| Bit 0 | Reserved for future expansion. |
| **R8:1—0X108 - OUTPUT FORMAT CONTROL (R/W)** | |
| Default | 0x0080 |
| Description | This register specifies the output timing and format in conjunction with R58:1 or R155:1 (depending on the context). |
| Bits 15:10 | Reserved for future expansion. |
| Bit 9 | Flip Bayer columns in processed Bayer output mode.<br>0: Column order is green, red and blue, green.<br>1: Column order is red, green and green, blue. |
| Bit 8 | Flip Bayer row in processed Bayer output mode.<br>0: First row contains green and red; the second row contains blue and green.<br>1: First row contains blue and green; the second row contains green and red. |
| Bit 7 | Controls the values used for the protection bits in Rec. ITU-R BT.656 codes.<br>0: Use zeros for the protection bits.<br>1: Use the correct values. |
| Bit 5 | Multiplexes Y (in YCbCr mode) or green (in RGB mode) channel on all channels (monochrome).<br>1: Forces Y/G onto all channels. |
| Bit 4 | Disables Cab color output channel (Cb = 128) in YCbCr mode and disables the blue color output channel (B = 0) in RGB mode.<br>1: Forces Cab to 128 or B to 0. |
| Bit 3 | Disables Y color output channel (Y = 128) in YCbCr and disables the green color output channel (G = 0) in RGB mode.<br>1: Forces Y to 128 or G to 0. |
| Bit 2 | Disables Cr color output channel (Cr = 128) in YCbCr mode and disables the red color output channel (R = 0) in RGB mode.<br>1: Forces Cr to 128 or R to 0. |
| Bit 1 | Toggles the assumptions about Bayer vertical CFA shift.<br>0: Row containing red comes first.<br>1: Row containing blue comes first. |
| Bit 0 | Toggles the assumptions about Bayer horizontal CFA shift.<br>0: Green comes first.<br>1: Red or blue comes first. |



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## Table 9: Colorpipe Register Description (continued)

| R37:1—0X125 - COLOR SATURATION CONTROL (R/W) | |
|---|---|
| Default | 0x0005 |
| Description | This register specifies the color saturation control settings. |
| Bit 5:3 | Specify overall attenuation of the color saturation.<br>“000”—Full color saturation<br>“001”—75% of full saturation<br>“010”—50% of full saturation<br>“011”—37.5% of full saturation<br>“100”—25% of full saturation<br>“101”—150% of full saturation<br>“110”—black and white |
| Bit 2:0 | Specify color saturation attenuation at high luminance (linearly increasing attenuation from no attenuation to monochrome at luminance of 224).<br>“000”—No attenuation.<br>“001”—Attenuation starts at luminance of 216.<br>“010”—Attenuation starts at luminance of 208.<br>“011”—Attenuation starts at luminance of 192.<br>“100”—Attenuation starts at luminance of 160.<br>“101”—Attenuation starts at luminance of 96. |
| **R52:1—0X134 - LUMA OFFSET (R/W)** | |
| Default | 0x0010 |
| Description | Offset added to the luminance prior to output. |
| Bits 15:8 | Y Offset in YCbCr mode. |
| Bits 7:0 | Offset in RGB mode. |
| **R53:1—0X135 - LUMA CLIP (R/W)** | |
| Default | 0xF010 |
| Description | Clipping limits for output luminance. |
| Bits 15:8 | Highest value of output luminance. |
| Bits 7:0 | Lowest value of output luminance. |
| **R58:1—0X13A - OUTPUT FORMAT CONTROL 2—CONTEXT A (R/W)** | |
| Default | 0x0200 |
| Description | Output format control 2A. |
| Bit 14 | Output processed Bayer data. |
| Bit 13 | Reserved |
| Bit 12 | Reserved |
| Bit 11 | Enables embedding Rec. ITU-R BT.656 synchronization codes in the output data. See R155:1 |
| Bit 10 | Entire image processing is bypassed and raw bayer is output directly.<br>In YCbCr or RGB mode:<br>0: Normal operation, sensor core data flows through IFP.<br>1: Bypass IFP and output Imager data directly (full 10 bits). The image data still passes through the camera interface FIFO and the 10 bits are formatted to two output bytes through the camera interface; i.e., 8 + 2. Data rate is effectively the same as default 16-bit /per pixel modes. Auto exposure/AWB, etc. still function and control the sensor, though they are assuming some gain/correction through the colorpipe. See R155:1 |
| Bit 9 | Inverts output pixel clock. By default, this bit it asserted and data is launched off the falling edge of PIXCLK for capture by the receiver on the rising edge. See R155:1 |
| Bit 8 | Enables RGB output.<br>0: Output YCbCr data.<br>1: Output RGB format data as defined by R58:1[7:6]. |



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## Table 9: Colorpipe Register Description (continued)

| | |
|---|---|
| Bits 7:6 | RGB output format:<br>“00”—16-bit RGB565.<br>“01”—15-bit RGB555.<br>“10”—12-bit RGB444x.<br>“11”—12-bit RGBx444. |
| Bits 5:4 | Test Ramp output:<br>“00”—Off.<br>“01”—By column.<br>“10”—By row.<br>“11”—By frame. |
| Bit 3 | Outputs RGB or YCbCr values are shifted 3 bits up. Use with R58:1[5:4] to test LCDs with low color depth. |
| Bit 2 | Averages two nearby chrominance bytes. See R155:1 |
| Bit 1 | In YCbCr mode swap C and Y bytes. In RGB mode, swap odd and even bytes. See R155:1 |
| Bit 0 | In YCbCr mode, swaps Cb and Cr channels. In RGB mode, swaps R and B channels. See R155:1 |
| **R72:1—0X148 - TEST PATTERN GENERATOR CONTROL (R/W)** | |
| Default | 0x0000 |
| Description | This register enables test pattern generation at the input of the image processor. Values greater than “0” turn on the test pattern generator. The brightness of the flat color areas depends on the value programmed (from 6–1) in this register. The value 7 produces the color bar pattern. Value 0 selects the sensor image. |
| Bit 7 | 1: Forces WB digital gains to 1.0.<br>0: Normal operation. |
| Bits 2:0 | Test pattern selection. |
| **R76:1—0X14C - DEFECT CORRECTION—CONTEXT A (R/W)** | |
| Default | 0x0000 |
| Description | Context A register with defect correction, mode enables, and calibration bits. |
| Bit 2 | Reserved |
| Bit 1 | Reserved |
| Bit 0 | Enables 2D defect correction. |
| **R77:1—0X14D - DEFECT CORRECTION—CONTEXT B (R/W)** | |
| Default | 0x0000 |
| Description | Context B register with defect correction, mode enables, and calibration bits. |
| Bit 2 | Reserved |
| Bit 1 | Reserved |
| Bit 0 | Enables 2D defect correction. |
| **R153:1—0X199 - LINE COUNTER (R/O)** | |
| Default | N/A |
| Description | Use line counter to determine the number of the line currently being output. |
| Bits 12:0 | Line count. |
| **R154:1—0X19A - FRAME COUNTER (R/O)** | |
| Default | N/A |
| Description | Use frame counter to determine the index of the frame currently being output. |
| Bits 15:0 | Frame count. |
| **R155:1—0X19B - OUTPUT FORMAT CONTROL 2—CONTEXT B (R/W)** | |
| Default | 0x0200 |
| Description | Output format control 2B. |
| Bit 14 | Output processed Bayer data. |



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## Table 9: Colorpipe Register Description (continued)

| | |
|---|---|
| Bit 13 | Reserved. |
| Bit 12 | Reserved |
| Bit 11 | Enables embedding Rec. ITU-R BT.656 synchronization codes to the output data. See R58:1 |
| Bit 10 | Entire image processing is bypassed and raw bayer is output directly.<br>In YCbCr or RGB mode:<br>0: Normal operation, sensor core data flows through IFP.<br>1: Bypass IFP and output Imager data directly (full 10 bits). The image data still passes through the camera interface FIFO and the 10 bits are formatted to two output bytes through the camera interface; i.e., 8 + 2. Data rate is effectively the same as default 16-bit /per pixel modes. Auto exposure/AWB, etc. still function and control the sensor, though they are assuming some gain/correction through the colorpipe. See R58:1 |
| Bit 9 | Inverts output pixel clock. By default, this bit it asserted and data is launched off the falling edge of PIXCLK for capture by the receiver on the rising edge. See R58:1 |
| Bit 8 | Enables RGB output.<br>0: Output YCbCr data.<br>1: Output RGB format data as defined by R155:1[7:6]. See R58:1 |
| Bits 7:6 | RGB output format:<br>“00”—16-bit RGB565.<br>“01”—15-bit RGB555.<br>“10”—12-bit RGB444x.<br>“11”—12-bit RGBx444. |
| Bits 5:4 | Test Ramp output:<br>“00”—Off.<br>“01”—By column.<br>“10”—By row.<br>“11”—By frame. |
| Bit 3 | Output RGB or YCbCr values are shifted 3 bits up. Use with R58:1[5:4] to test LCDs with low color depth. |
| Bit 2 | Averages two nearby chrominance bytes. See R58:1 |
| Bit 1 | In YCbCr mode swap C and Y bytes. In RGB mode, swap odd and even bytes. See R58:1 |
| Bit 0 | In YCbCr mode, swaps Cb and Cr channels. In RGB mode, swaps R and B channels. See R58:1 |
| **R159:1—0X19F - REDUCER HORIZONTAL PAN—CONTEXT B (R/W)** | |
| Default | 0x0000 |
| Description | Controls reducer horizontal pan in Context B |
| Bit 14 | 0: MT9V111-compatible origin at X = 0.<br>1: Centered origin at 640 for more convenient zoom and resize. |
| Bits 10:0 | X Pan: Unsigned offset from x = 0 (Bit 14 = 0), or two’s complement from X = 640 (Bit 14 = 1). |
| **R160:1—0X1A0 - REDUCER HORIZONTAL ZOOM—CONTEXT B (R/W)** | |
| Default | 0x0500 |
| Description | Controls reducer horizontal width of zoom window for field of view in Context B. |
| Bits 10:0 | X Zoom B. Must be ≥ X Size B |
| **R161:1—0X1A1 - REDUCER HORIZONTAL OUTPUT SIZE—CONTEXT B (R/W)** | |
| Default | 0x0500 |
| Description | Controls reducer horizontal output size in Context B. |
| Bits 10:0 | X Size B. Must be ≤ X Zoom B. |
| **R162:1—0X1A2 - REDUCER VERTICAL PAN—CONTEXT B (R/W)** | |
| Default | 0x0000 |
| Description | Controls reducer vertical pan in Context B. |
| Bit 14 | 0: MT9V111-compatible origin at Y = 0.<br>1: Centered origin at Y = 512 for more convenient zoom and resize. |



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## Table 9: Colorpipe Register Description (continued)

| | |
|---|---|
| Bits 10:0 | Y Pan: unsigned offset from Y = 0 (Bit 14 = 0), or two's complement from Y = 512 (Bit 14 = 1). |
| **R163:1—0X1A3 - REDUCER VERTICAL ZOOM—CONTEXT B (R/W)** | |
| Default | 0x0400 |
| Description | Controls reducer vertical height of zoom window for field of view in Context B. |
| Bits 10:0 | Y Zoom B. Must be ≥ Y Size B. |
| **R164:1—0X1A4 - REDUCER VERTICAL OUTPUT SIZE—CONTEXT B (R/W)** | |
| Default | 0x0400 |
| Description | Controls reducer vertical output size in Context B. |
| Bits 10:0 | Y Size B. Must be ≤ Y Zoom B. |
| **R165:1—0X1A5 - REDUCER HORIZONTAL PAN—CONTEXT A (R/W)** | |
| Default | 0x0000 |
| Description | Controls reducer horizontal pan in Context A. |
| Bit 14 | 0: MT9V111-compatible offset from X = 0.<br>1: Centered origin at 640 for more convenient zoom and resize. |
| Bits 10:0 | X Pan: Unsigned offset from X = 0 (Bit 14 = 0), or two's complement from X = 640 (Bit 14 = 1). |
| **R166:1—0X1A6 - REDUCER HORIZONTAL ZOOM—CONTEXT A (R/W)** | |
| Default | 0x0500 |
| Description | Controls reducer horizontal width of zoom window for field of view in Context A. |
| Bits 10:0 | X Zoom A. Must be ≥ X Size A. |
| **R167:1—0X1A7 - REDUCER HORIZONTAL OUTPUT SIZE—CONTEXT A (R/W)** | |
| Default | 0x0280 |
| Description | Controls reducer horizontal output size in Context A. |
| Bits 10:0 | X Size A. Must be ≤ X Zoom A.. |
| **R168:1—0X1A8 - REDUCER VERTICAL PAN—CONTEXT A (R/W)** | |
| Default | 0x0000 |
| Description | Controls reducer vertical pan in Context A. |
| Bit 14 | 0: MT9V111-compatible origin at Y = 0.<br>1: Centered origin at Y = 512 for more convenient zoom and resize. |
| Bits 10:0 | Y Pan: unsigned offset from y = 0 (Bit 14 = 0), or two's complement from Y = 512 (Bit 14 = 1). |
| **R169:1—0X1A9 - REDUCER VERTICAL ZOOM—CONTEXT A (R/W)** | |
| Default | 0x0400 |
| Description | Controls reducer vertical height of zoom window for field of view in Context A. |
| Bits 10:0 | Y Zoom A. Must be ≥ Y Size A. |
| **R170:1—0X1AA - REDUCER VERTICAL OUTPUT SIZE—CONTEXT A (R/W)** | |
| Default | 0x0200 |
| Description | Controls reducer vertical output size in Context A. |
| Bits 10:0 | Y SizeA. Must be ≤ Y Zoom A. |
| **R171:1—0X1AB - REDUCER CURRENT HORIZONTAL ZOOM (R/O)** | |
| Default | N/A |
| Description | Current horizontal zoom. |
| Bits 10:0 | Current Zoom Window Width. After automatic zoom (R175:1), copy R171:1 to the snapshot X Zoom register R166:1 (Context A) or R160:1 (Context B) so the snapshot has the same field of view as preview. Also copy to snapshot X Size register R167:1 (Context A) or R161 (Context B) for largest snapshot. |
| Bits 15:12 | Reserved. Mask off these bits before performing the above copy operation. |



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## Table 9: Colorpipe Register Description (continued)

| | |
|---|---|
| **R172:1—0X1AC - REDUCER CURRENT VERTICAL ZOOM (R/O)** | |
| Default | N/A |
| Description | Current vertical zoom. |
| Bits 10:0 | Current Zoom Window Height. After automatic zoom (R175:1), copy R172:1 to the snapshot Y Zoom register R169:1 (Context A) or R163:1 (Context B) so the snapshot will have the same field of view as preview. Also copy to snapshot X Size register R170:1 (Context A) or R164 (Context B) for largest snapshot. |
| Bits 15:12 | Reserved. Mask off these bits before performing the above copy operation. |
| **R174:1—0X1AE - REDUCER ZOOM STEP SIZE (R/W)** | |
| Default | 0x0504 |
| Description | Zoom step sizes. Should be a multiple of the aspect ratio 5:4 for SXGA or 4:3 VGA or 11:9 for CIF. |
| Bits 15:8 | Zoom step size in X. |
| Bits 7:0 | Zoom step size in Y. |
| **R175:1—0X1AF - REDUCER ZOOM CONTROL (R/W)** | |
| Default | 0x0010 |
| Description | Resize interpolation and zoom control. |
| Bit 9 | Starts automatic “zoom out” in step sizes defined in R174:1. |
| Bit 8 | Starts automatic “zoom in” in step sizes defined in R174:1. |
| Bit 6 | Reserved. |
| Bit 5 | Reserved. |
| Bit 4 | Reserved. |
| Bit 3 | Auto switch to classic interpolation at full resolution. |
| Bit 1 | Reserved. |
| Bit 0 | Reserved. |
| **R179:1—0X1B3 - GLOBAL CLOCK CONTROL (R/W)** | |
| Default | 0x0002 |
| Description | Configures assorted aspects of the clock controller. |
| Bits 15:2 | Not used. |
| Bit 1 | Tri-states pins in standby mode. |
| Bit 0 | SOC soft standby. |
| **R200:1—0X1C8 - GLOBAL CONTEXT CONTROL (R/W)** | |
| Default | 0x0000 |
| Description | Defines sensor and colorpipe context for current frame. Registers R200:0, R200:1, and R200:2 are shadows of each other. See description in R200:2. It is recommended that all updates to R200:n are handled by means of a write to R200:2. |
| Bit 15:0 | See R200:2[15:0]. |
| **R226:1—0X1E2 - EFFECTS MODE (R/W)** | |
| Default | 0x7000 |
| Description | This register specifies which of several special effects to apply to each pixel passing through the pixel pipe. |
| Bits 15:8 | Solarization threshold. |
| Bits 2:0 | Specification of the effects mode.<br>“000”—No effect (pixels pass through unchanged).<br>“001”—Monochrome (chromas set to 0).<br>“010”—Sepia (chromas set to the value in the Effects Sepia register).<br>“011”—Negative (all color channels inverted).<br>“100”—Solarize (luma conditionally inverted).<br>“101”—Solarize2 (luma conditionally inverted, chromas inverted when luma inverted). |



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## Table 9: Colorpipe Register Description (continued)

| | |
|---|---|
| **R227:1—0X1E3 - EFFECTS SEPIA (R/W)** | |
| Default | 0xB023 |
| Description | This register specifies the chroma values for the sepia effect. In sepia mode, the chroma values of each pixel are set to this value. By default, this register contains a brownish color, but it can be set to an arbitrary color. |
| Bit 15 | Sign of Cb. |
| Bits 14:8 | Magnitude of Cb in 0.7 fixed point. |
| Bit 7 | Sign of Cr. |
| Bits 6:0 | Magnitude of Cr in 0.7 fixed point. |
| **R240:1—0X1F0 - PAGE MAP (R/W)** | |
| Default | 0x0000 |
| Description | This register specifies the register address page for the two-wire interface protocol. |
| Bits 2:0 | Page Address:<br>“000”—Sensor address page<br>“001”—Colorpipe address page<br>“010”—Camera control address page |
| **R241:1—0X1F1 - BYTE-WISE ADDRESS (R/W)** | |
| Default | N/A |
| Description | Special address to perform 8-bit reads and writes to the sensor. For additional information, see “Two-Wire Serial Interface Sample” on page 57 and “APPENDIX A” on page 56. |



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## Table 10: Camera Control Register Description

| | |
|---|---|
| **R38:2—0X226 - AUTO EXPOSURE WINDOW HORIZONTAL BOUNDARIES (R/W)** | |
| Default | 0x8000 |
| Description | This register specifies the left and right boundaries of the window used by the auto exposure measurement engine. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the right-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the left-most edge of the frame. |
| Bits 15:8 | Right window boundary. |
| Bits 7:0 | Left window boundary. |
| **R39:2—0X227 - AUTO EXPOSURE WINDOW VERTICAL BOUNDARIES (R/W)** | |
| Default | 0x8008 |
| Description | This register specifies the top and bottom boundaries of the window used by the auto exposure measurement engine. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the bottom edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the top edge of the frame. |
| Bits 15:8 | Bottom window boundary. |
| Bits 7:0 | Top window boundary. |
| **R43:2—0X22B - AUTO EXPOSURE CENTER WINDOW HORIZONTAL BOUNDARIES (R/W)** | |
| Default | 0x6020 |
| Description | This register specifies the left and right boundaries of the window used by the auto exposure measurement engine in backlight compensation mode. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the right-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the left-most edge of the frame. |
| Bits 15:8 | Right window boundary. |
| Bits 7:0 | Left window boundary. |
| **R44:2—0X22C - AUTO EXPOSURE CENTER WINDOW VERTICAL BOUNDARIES (R/W)** | |
| Default | 0x6020 |
| Description | This register specifies the top and bottom boundaries of the window used by the auto exposure measurement engine in backlight compensation mode. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the bottom edge of the frame, 64 (decimal) is the middle of the frame, and “0” is the top edge of the frame. |
| Bits 15:8 | Bottom window boundary. |
| Bits 7:0 | Top window boundary. |
| **R45:2—0X22D - AWB WINDOW BOUNDARIES (R/W)** | |
| Default | 0xF0A0 |
| Description | This register specifies the boundaries of the window used by the AWB measurement engine. Essentially, it describes the AWB measurement window in terms relative to the size of the image—horizontally, in units of 1/10ths of the width of the image; vertically, in units of 1/16 of the height of the image. So although the positioning is highly quantized, the window remains roughly in place as the resolution changes. |
| Bits 15:12 | Bottom window boundary (in units of blocks). |
| Bits 11:8 | Top window boundary (in units of blocks). |
| Bits 7:4 | Right window boundary (in units of 2 blocks). |
| Bits 3:0 | Left window boundary (in units of 2 blocks). |
| **R46:2—0X22E - AUTO EXPOSURE TARGET AND PRECISION CONTROL (R/W)** | |
| Default | 0x0C4A |
| Description | This register specifies the luma target of the auto exposure algorithm and the size of the window/range around the target in which no auto exposure adjustment is made. This window is centered on target, but the value programmed in the register is 1/2 of the window size. |
| Bits 15:8 | Half-size of the auto exposure stability window/range. |
| Bits 7:0 | Luma value of the auto exposure target. |



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## Table 10: Camera Control Register Description (continued)

| | |
|---|---|
| **R47:2—0X22F - AUTO EXPOSURE SPEED AND SENSITIVITY CONTROL—CONTEXT A (R/W)** | |
| Default | 0xDF20 |
| Description | This register specifies the speed and sensitivity to changes of auto exposure in Context A. |
| Bit 15 | Reserved. |
| Bit 14 | Reserved. |
| Bits 13:12 | Reserved. |
| Bit 11 | Reserved. |
| Bit 10 | Reserved. |
| Bit 9 | Reserved. |
| Bits 8:6 | Factor of reduction of the difference between current luma and target luma. In one adjustment auto exposure advances from current luma to target as follows:<br>“000”—1/4 way going down, 1/8 going up.<br>“001”—1/4 way in both directions.<br>“010”—1/2 way in both directions.<br>“011”—1/2 way going down, 1/4 going up.<br>“100”—All the way in both directions (fast adaptation!).<br>“101”—3/4 way in both directions.<br>“110”—7/8 way in both directions.<br>“111”—Reserved. Currently the same as “100” |
| Bit 5 | Reserved |
| Bits 4:3 | Auto exposure luma is updated every N frames, where N is given by this field. |
| Bits 2:0 | Hysteresis control via time-averaged smoothing of luma data. Luma measurements for auto exposure are time-averaged as follows:<br>“000”—Auto exposure luma = current luma.<br>“001”—Auto exposure luma = 1/2 current luma + 1/2 buffered value.<br>“010”—Auto exposure luma = 1/4 current luma + 3/4 buffered value.<br>“011”—Auto exposure luma = 1/8 current luma + 7/8 buffered value.<br>“100”—Auto exposure luma = 1/16 current luma + 15/16 buffered value.<br>“101”—Auto exposure luma = 1/32 current luma + 31/32 buffered value.<br>“110”—Auto exposure luma = 1/64 current luma + 63/64 buffered value.<br>“111”—Auto exposure luma = 1/128 current luma + 127/128 buffered value. |
| **R91:2—0X25B - FLICKER CONTROL (R/W)** | |
| Default | 0x0002 |
| Description | Primary flicker control register. |
| Bit 15 | (Read only) 50Hz/60Hz detected.<br>0: 50Hz detected.<br>1: 60Hz detected. |
| Bit 2 | Reserved |
| Bit 1 | When in “manual” flicker mode (R91:2[0] = 1), defines which flicker frequency to avoid.<br>0: Forces 50Hz detection.<br>1: Forces 60Hz detection. |
| Bit 0 | 0: Auto flicker detection.<br>1: Manual mode. |
| **R98:2—0X262 - AUTO EXPOSURE DIGITAL GAINS MONITOR (R/W*)** | |
| Default | N/A |
| Description | These digital gains are applied within the IFP; they are independent of the Imager gains. |
| Bits 15:8 | Post-lens-correction digital gain (*writable if auto exposure is disabled). |
| Bits 7:0 | Pre-lens-correction digital gain (*writable if auto exposure is disabled). |



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## Table 10: Camera Control Register Description (continued)

| | |
|---|---|
| **R103:2—0X267 - AUTO EXPOSURE DIGITAL GAIN LIMITS (R/W)** | |
| Default | 0x4010 |
| Description | This register specifies the upper limits of the digital gains used by the auto exposure algorithm. The values programmed to this register are 16 times the absolute gain values. The value of 16 represents the gain 1.0. |
| Bits 15:8 | Maximum limit on post-lens-correction digital gain. |
| Bits 7:0 | Maximum limit on pre-lens-correction digital gain. |
| **R156:2—0X29C - AUTO EXPOSURE SPEED AND SENSITIVITY CONTROL—CONTEXT B (R/W)** | |
| Default | 0xDF20 |
| Description | This register specifies the speed and sensitivity to auto exposure changes in Context B. |
| Bit 15 | Reserved. |
| Bit 14 | Reserved. |
| Bits 13:12 | Reserved. |
| Bit 11 | Reserved. |
| Bit 10 | Reserved. |
| Bit 9 | Reserved. |
| Bits 8:6 | Factor of reduction of the difference between current luma and target luma. In one adjustment, auto exposure advances from current luma to target as follows:<br>“000”—1/4 way going down, 1/8 going up.<br>“001”—1/4 way in both directions.<br>“010”—1/2 way in both directions.<br>“011”—1/2 way going down, 1/4 going up.<br>“100”—All the way in both directions (fast adaptation!).<br>“101”—3/4 way in both directions.<br>“110”—7/8 way in both directions.<br>“111”—Reserved. Currently the same as “100.” |
| Bit 5 | Reserved. |
| Bits 4:3 | Auto exposure luma is updated every N frames, where N is given by this field. |
| Bits 2:0 | Hysteresis control via time-averaged smoothing of luma data. Luma measurements for auto exposure are time-averaged as follows:<br>“000”—Auto exposure luma = current luma.<br>“001”—Auto exposure luma = 1/2 current luma + 1/2 buffered value.<br>“010”—Auto exposure luma = 1/4 current luma + 3/4 buffered value.<br>“011”—Auto exposure luma = 1/8 current luma + 7/8 buffered value.<br>“100”—Auto exposure luma = 1/16 current luma + 15/16 buffered value.<br>“101”—Auto exposure luma = 1/32 current luma + 31/32 buffered value.<br>“110”—Auto exposure luma = 1/64 current luma + 63/64 buffered value.<br>“111”—Auto exposure luma = 1/128 current luma + 127/128 buffered value. |
| **R180:2—RESERVED** | |
| **R200:2—0X2C8 - GLOBAL CONTEXT CONTROL (R/W)** | |
| Default | 0x0000 |
| Description | Defines sensor and colorpipe context for current frame. Context A is typically used to define preview or viewfinder mode, while Context B is typically used for snapshots. The bits of this register *directly* control the respective functions, so care must be taken when writing to this register if a bad frame is to be avoided during the context switch. |
| Bit 15 | Controls assertion of sensor restart on update of global context control register. This helps ensure that the very next frame is generated with the new context (a problem with regard to exposure due to the rolling shutter). This bit is automatically cleared once the restart has occurred.<br>0: Do not restart sensor.<br>1: Restart sensor. |



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## Table 10: Camera Control Register Description (continued)

| | |
|---|---|
| Bit 14 | Reserved. |
| Bit 13 | Reserved. |
| Bit 12 | Defect correction context. See R76:1 and R77:1.<br>0: Context A<br>1: Context B |
| Bit 11 | Reserved. |
| Bit 10 | Resize/zoom context. Switch resize/zoom contexts:<br>0: Context A<br>1: Context B |
| Bit 9 | Output format Control 2 context. See R58:1 and R155:1.<br>0: Context A<br>1: Context B |
| Bit 8 | Gamma table context.<br>0: Context A<br>1: Context B |
| Bit 7 | Arm Xenon Flash. |
| Bit 6 | Blanking control. This is primarily for use by the internal sequencer when taking automated (e.g., flash) snapshots. Setting this bit stops frames from being sent over the BT656 external pixel interface. This is useful for ensuring that the desired frame during a snapshot sequence is the only frame captured by the host.<br>0: Do not blank frames to host.<br>1: Blank frames to host |
| Bit 5 | Reserved. |
| Bit 4 | Reserved. |
| Bit 3 | Sensor read mode context (skip mode, power mode, see R33:0 and R32:0.<br>0: Context A<br>1: Context B |
| Bit 2 | LED flash ON:<br>0: Turn off LED Flash<br>1: Turn on LED Flash |
| Bit 1 | Vertical blanking context:<br>0: Context A<br>1: Context B |
| Bit 0 | Horizontal blanking context:<br>0: Context A<br>1: Context B |
| **R240:2—0X2F0 - PAGE MAP (R/W)** | |
| Default | 0x0000 |
| Description | This register specifies the register address page for the two wire interface protocol. |
| Bits 2:0 | Page address:<br>“000”—Sensor address page.<br>“001”—Colorpipe address page.<br>“010”—Camera control address page. |
| **R241:2—0X2F1 - BYTE-WISE ADDRESS (R/W)** | |
| Default | N/A |
| Description | Special address to perform 8-bit reads and writes to the sensor. For additional information, see “Two-Wire Serial Interface Sample” on page 57 and “APPENDIX A” on page 56. |

NOTE:

Registers marked “(R/W*)”are normally read-only (R/O) registers, except under special circumstances (detailed in the register description), when some or all bits of the register become read-writeable (R/W).



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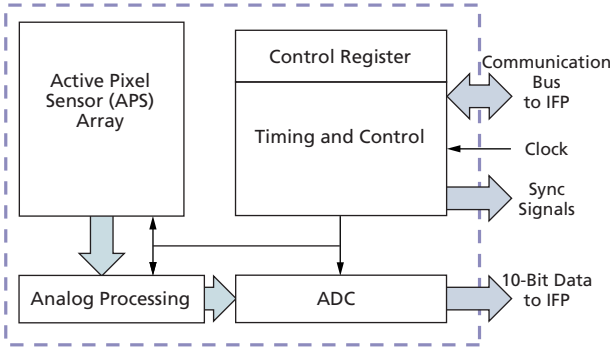
## Sensor Core Overview

The sensor consists of a pixel array of 1,316 x 1,048 total, an analog readout chain, 10-bit ADC with programmable gain and black offset, and timing and control.

### Figure 5: Sensor Core Block Diagram

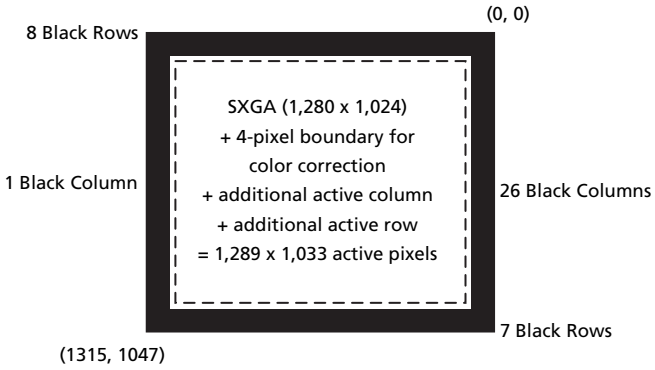



## Pixel Data Format

### *Pixel Array Structure*

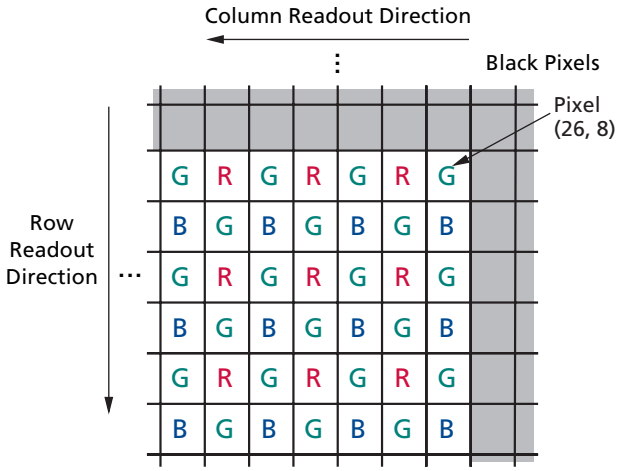
The MT9M111 sensor core pixel array is configured as 1,316 columns by 1,048 rows (shown in Figure 6). The first 24 columns and the first 8 rows of pixels are optically black, and can be used to monitor the black level. The last 3 columns and the last 7 rows of pixels also are optically black. The black row data is used internally for the automatic black level adjustment. However, the first 8 black rows can also be read out by setting the sensor to raw data output mode (Reg0x022). There are 1,289 columns by 1,033 rows of optically-active pixels that provide a 4-pixel boundary around the SXGA (1,280 x 1,024) image to avoid boundary effects during color interpolation and correction. The additional active column and additional active row are used to enable horizontally and vertically mirrored readout to start on the same color pixel.

### Figure 6: Pixel Array Description




The MT9M111 sensor core uses an RGB Bayer color pattern, shown in Figure 7. The even-numbered rows contain green and red color pixels, and odd numbered rows contain blue and green color pixels. Even numbered columns contain green and blue color pixels; odd-numbered columns contain red and green color pixels. Because there are odd numbers of rows and columns, the color order can be preserved during mirrored readout.

### Figure 7: Pixel Color Pattern Detail (Top Right Corner)





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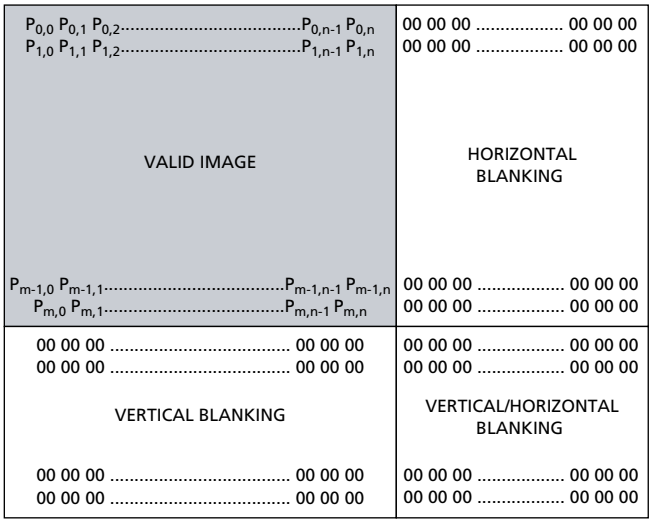
### Output Data Format

The MT9M011 sensor core image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, shown in Figure 8. LINE_VALID is HIGH during the shaded region of the figure. FRAME_VALID timing is described in "APPENDIX A" on page 56.

**Figure 8: Spatial Illustration of Image Readout**



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## Sensor Core Register List

### Table 11: Sensor Registers (Address Page 0)

| REGISTER# DEC (HEX) | REGISTER NAME | DATA FORMAT | DEFAULT VALUE DEC (HEX) |
|---|---|---|---|
| 0 (0x00) | Chip Version | 0001 0100 0011 1010 (LSB) | 5178 (0x143A) |
| 1 (0x01) | Row Start | 0000 0ddd dddd dddd | 12 (0x000C) |
| 2 (0x02) | Column Start | 0000 0ddd dddd dddd | 30 (0x001E) |
| 3 (0x03) | Window Height | 0000 0ddd dddd dddd | 1024 (0x0400) |
| 4 (0x04) | Window Width | 0000 0ddd dddd dddd | 1280 (0x0500) |
| 5 (0x05) | Horizontal Blanking—Context B | 00dd dddd dddd dddd | 388 (0x0184) |
| 6 (0x06) | Vertical Blanking—Context B | 0ddd dddd dddd dddd | 42 (0x002A) |
| 7 (0x07) | Horizontal Blanking—Context A | 00dd dddd dddd dddd | 190 (0x00BE) |
| 8 (0x08) | Vertical Blanking—Context A | 0ddd dddd dddd dddd | 17 (0x0011) |
| 9 (0x09) | Shutter Width | dddd dddd dddd dddd | 537 (0x0219) |
| 10 (0x0A) | Row Speed | ddd0 000d dddd dddd | 17 (0x0011) |
| 11 (0x0B) | Extra Delay | 00dd dddd dddd dddd | 0 (0x0000) |
| 12 (0x0C) | Shutter Delay | 00dd dddd dddd dddd | 0 (0x0000) |
| 13 (0x0D) | Reset | d000 00dd 00dd dddd | 8 (0x0008) |
| 32 (0x20) | Read Mode—Context B | dd00 0ddd dddd dddd | 768 (0x0300) |
| 33 (0x21) | Read Mode—Context A | 0000 0d00 0000 dd00 | 1036 (0x040C) |
| 34 (0x22) | Reserved | — | 297 (0x0129) |
| 35 (0x23) | Flash Control | ??dd dddd dddd dddd | 1544 (0x0608) |
| 36 (0x24) | Reserved | — | 32875 (0x806B) |
| 43 (0x2B) | Green1 Gain | 0000 0ddd dddd dddd | 32 (0x0020) |
| 44 (0x2C) | Blue Gain | 0000 0ddd dddd dddd | 32 (0x0020) |
| 45 (0x2D) | Red Gain | 0000 0ddd dddd dddd | 32 (0x0020) |
| 46 (0x2E) | Green2 Gain | 0000 0ddd dddd dddd | 32 (0x0020) |
| 47 (0x2F) | Global Gain | 0000 0ddd dddd dddd | 32 (0x0020) |
| 48 (0x30) | Reserved | — | 1066 (0x042A) |
| 49 (0x31) | Reserved | — | 7168 (0x1C00) |
| 50 (0x32) | Reserved | — | 0 (0x0000) |
| 51 (0x33) | Reserved | — | 841 (0x0349) |
| 52 (0x34) | Reserved | — | 49177 (0xC019) |
| 54 (0x36) | Reserved | — | 61680 (0xF0F0) |
| 55 (0x37) | Reserved | — | 0 (0x0000) |
| 59 (0x3B) | Reserved | — | 33 (0x0021) |
| 60 (0x3C) | Reserved | — | 6688 (0x1A20) |
| 61 (0x3D) | Reserved | — | 8222 (0x201E) |
| 62 (0x3E) | Reserved | — | 8224 (0x2020) |
| 63 (0x3F) | Reserved | — | 8224 (0x2020) |
| 64 (0x40) | Reserved | — | 8220 (0x201C) |
| 65 (0x41) | Reserved | — | 215 (0x00D7) |
| 66 (0x42) | Reserved | — | 1911 (0x0777) |
| 89 (0x59) | Reserved | — | 12 (0x000C) |
| 90 (0x5A) | Reserved | — | 49167 (0xC00F) |
| 91 (0x5B) | Reserved | — | N/A |



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## Table 11: Sensor Registers (Address Page 0) (continued)

| REGISTER# DEC (HEX) | REGISTER NAME | DATA FORMAT | DEFAULT VALUE DEC (HEX) |
|---|---|---|---|
| 92 (0x5C) | Reserved | — | N/A |
| 93 (0x5D) | Reserved | — | N/A |
| 94 (0x5E) | Reserved | — | N/A |
| 95 (0x5F) | Reserved | — | 8989 (0x231D) |
| 96 (0x60) | Reserved | — | 128 (0x0080) |
| 97 (0x61) | Reserved | — | 0 (0x0000) |
| 98 (0x62) | Reserved | — | 0 (0x0000) |
| 99 (0x63) | Reserved | — | 0 (0x0000) |
| 100 (0x64) | Reserved | — | 0 (0x0000) |
| 101 (0x65) | Reserved | — | 0 (0x0000) |
| 112 (0x70) | Reserved | — | 31498 (0x7B0A) |
| 113 (0x71) | Reserved | — | 31498 (0x7B0A) |
| 114 (0x72) | Reserved | — | 6414 (0x190E) |
| 115 (0x73) | Reserved | — | 6159 (0x180F) |
| 116 (0x74) | Reserved | — | 22322 (0x5732) |
| 117 (0x75) | Reserved | — | 22068 (0x5634) |
| 118 (0x76) | Reserved | — | 29493 (0x7335) |
| 119 (0x77) | Reserved | — | 12306 (0x3012) |
| 120 (0x78) | Reserved | — | 30978 (0x7902) |
| 121 (0x79) | Reserved | — | 29958 (0x7506) |
| 122 (0x7A) | Reserved | — | 30474 (0x770A) |
| 123 (0x7B) | Reserved | — | 30729 (0x7809) |
| 124 (0x7C) | Reserved | — | 32006 (0x7D06) |
| 125 (0x7D) | Reserved | — | 12560 (0x3110) |
| 126 (0x7E) | Reserved | — | 126 (0x007E) |
| 128 (0x80) | Reserved | — | 127 (0x007F) |
| 129 (0x81) | Reserved | — | 127 (0x007F) |
| 130 (0x82) | Reserved | — | 22282 (0x570A) |
| 131 (0x83) | Reserved | — | 22539 (0x580B) |
| 132 (0x84) | Reserved | — | 18188 (0x470C) |
| 133 (0x85) | Reserved | — | 18446 (0x480E) |
| 134 (0x86) | Reserved | — | 23298 (0x5B02) |
| 135 (0x87) | Reserved | — | 92 (0x005C) |
| 200 (0xC8) | Context Control | d000 0000 d000 dddd | 0 (0x0000) |
| 240 (0xF0) | Page Map | 0000 0000 0000 0ddd | 0 (0x0000) |
| 241 (0xF1) | Byte-Wise Address | Reserved | Reserved |
| 245 (0xF5) | Reserved | — | 2047 (0x07FF) |
| 246 (0xF6) | Reserved | — | 2047 (0x07FF) |
| 247 (0xF7) | Reserved | — | 0 (0x0000) |
| 248 (0xF8) | Reserved | — | 0 (0x0000) |
| 249 (0xF9) | Reserved | — | 124 (0x007C) |
| 250 (0xFA) | Reserved | — | 0 (0x0000) |
| 251 (0xFB) | Reserved | — | 0 (0x0000) |
| 252 (0xFC) | Reserved | — | 0 (0x0000) |
| 253 (0xFD) | Reserved | — | 0 (0x0000) |



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## Table 11: Sensor Registers (Address Page 0) (continued)

| REGISTER# DEC (HEX) | REGISTER NAME | DATA FORMAT | DEFAULT VALUE DEC (HEX) |
|---|---|---|---|
| 255 (0xFF) | Chip Version | 0001 0100 0011 1010 | 5178 (0x143A) |

NOTE:

Data Format Key:
0 = “Don't Care” bit
d = R/W bit
? = R/O bit. The exceptions: R0:0 and R255:0, which are hardwired R/O binary values.



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## *Sensor Core Register Descriptions*

### Table 12: Sensor Core Register Descriptions

| BIT FIELD | DESCRIPTION | DEFAULT (HEX) | SYNCED TO FRAME START | BAD FRAME | READ/ WRITE |
|---|---|---|---|---|---|
| **R0:0—0X000 - CHIP VERSION (R/O)** | | | | | |
| Bits 15:0 | Hardwired read-only. | 0x143A | | | R |
| **R1:0—0X001 - ROW START** | | | | | |
| Bits 10:0 Row Start | The first row to be read out (not counting dark rows that may be read). To window the image down, set this register to the starting Y value. Setting a value less than 8 is not recommended since the dark rows should be read using Reg0x022. | 0xC | Y | YM | W |
| **R2:0—0X002 - COLUMN START** | | | | | |
| Bits 10:0 Col Start | The first column to be read out (not counting dark columns that may be read). To window the image down, set this register to the starting X value. Setting a value below 0x18 is not recommended since readout of dark columns should be controlled by Reg0x022. | 0x1E | Y | YM | W |
| **R3:0—0X003 - WINDOW HEIGHT** | | | | | |
| Bits 10:0 Window Height | Number of rows in the image to be read out (not counting dark rows or border rows that may be read). | 0x400 | Y | YM | W |
| **R4:0—0X004 - WINDOW WIDTH** | | | | | |
| Bits 10:0 Window Width | Number of columns in image to be read out (not counting dark columns or border columns that may be read). | 0x500 | Y | YM | W |
| **R5:0—0X005 - HORIZONTAL BLANKING—CONTEXT B** | | | | | |
| Bits 10:0 Horizontal Blanking B | Number of blank columns in a row when Context B is chosen (bit 0, Reg0x0C8 = 1). If set smaller than the minimum value, the minimum value is used. With default settings, the minimum horizontal blanking is 202 columns in full-power readout mode and 114 columns in low-power readout mode. | 0x184 | Y | YM | W |
| **R6:0—0X006 - VERTICAL BLANKING—CONTEXT B** | | | | | |
| Bits 14:0 Vertical Blanking B | Number of blank rows in a frame when Context B is chosen (bit 1, Reg0x0C8 = 1). This number must be equal to or larger than the number of dark rows read out in a frame specified by Reg0x022. | 0x2A | Y | N | W |
| **R7:0—0X007 - HORIZONTAL BLANKING—CONTEXT A** | | | | | |
| Bits 10:0 Horizontal Blanking A | Number of blank columns in a row when Context A is chosen (bit 0, Reg0x0C8 = 0). The extra columns are added at the beginning of a row. If set smaller than the minimum value, the minimum value is used. With default settings, the minimum horizontal blanking is 202 columns in full-power readout mode and 114 columns in low-power readout mode. | 0xBE | Y | YM | W |
| **R8:0—0X008 - VERTICAL BLANKING—CONTEXT A** | | | | | |



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## Table 12: Sensor Core Register Descriptions (continued)

| BIT FIELD | DESCRIPTION | DEFAULT (HEX) | SYNCED TO FRAME START | BAD FRAME | READ/ WRITE |
|---|---|---|---|---|---|
| Bits 14:0 Vertical Blanking A | Number of blank rows in a frame when Context A is chosen (bit 1, Reg0x0C8 = 1). This number must be equal to or larger than the number of dark rows read out in a frame specified by Reg0x022. | 0x11 | Y | N | W |
| **R9:0—0X009 - SHUTTER WIDTH** | | | | | |
| Bits 15:0 Shutter Width | Integration time in number of rows. In addition to this register, the shutter delay register (Reg0x0C) and the overhead time influences the integration time for a given row time. | 0x219 | Y | N | W |
| **R10:0—0X00A - ROW SPEED** | | | | | |
| Bits 15:13 | Reserved. | — | — | — | — |
| Bit 8 Invert Pixel Clock | Invert pixel clock. When set, LINE_VALID, FRAME_VALID, and DATA_OUT are set to the falling edge of PIXCLK. When clear, they are set to the rising edge if there is no pixel clock delay. | 0x0 | N | 0 | W |
| Bits 7:4 Delay Pixel Clock | Delay PIXCLK in half-master-clock cycles. When set, the pixel clock can be delayed in increments of half-master- clock cycles compared to the synchronization of FRAME_VALID, LINE_VALID, and DATA_OUT. | 0x1 | N | 0 | W |
| Bits 3:0 Pixel Clock Speed | Pixel clock period in master clocks when full-power readout mode is used (Reg0x020/0x021, bit 10 = 0). In this case, the ADC clock has twice the clock period. If low-power readout mode is used, the pixel clock period is automatically doubled, so the ADC clock period remains the same for one programmed register value. The value “0” is not allowed, and “1” is used instead. | 0x1 | Y | YM | W |
| **R11:0—0X00B - EXTRA DELAY** | | | | | |
| Bits 13:0 Extra Delay | Extra blanking inserted between frames specified in pixel clocks. Can be used to get a more exact frame rate. For integration times less than a frame, however, it might affect the integration times for parts of the image. | 0x0 | Y | 0 | W |
| **R12:0—0X00C - SHUTTER DELAY** | | | | | |
| Bits 10:0 Shutter Delay | The amount of time from the end of the sampling sequence to the beginning of the pixel reset sequence. This variable is automatically halved in low-power readout mode, so the time in use remains the same. This register has an upper value defined by the fact that the reset needs to finish prior to readout of that row to prevent changes in the row time. | 0x0 | Y | N | W |
| **R13:0—0X00D - RESET** | | | | | |
| Bit 15 Synchronize Changes | 0: Normal operation, updates changes to registers that affect image brightness at the next frame boundary (integration time, integration delay, gain, horizontal blanking and vertical blanking, window size, row/column skip, or row mirror.<br>1: Do not update any changes to these settings until this bit is returned to “0.” All registers that are frame synchronized are affected by this bit setting. | 0x0 | N | 0 | W |
| Bit 9 Restart Bad Frames | When set, a forced restart occurs when a bad frame is detected. This can shorten the delay when waiting for a good frame because the delay when masking out a bad frame is the integration time rather than the full frame time. | 0x0 | N | 0 | W |



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## Table 12: Sensor Core Register Descriptions (continued)

| BIT FIELD | DESCRIPTION | DEFAULT (HEX) | SYNCED TO FRAME START | BAD FRAME | READ/ WRITE |
|---|---|---|---|---|---|
| Bit 8<br>Show Bad Frames | 0: Only output good frames (default)<br>A bad frame is defined as the first frame following a change to: window size or position, horizontal blanking, pixel clock speed, zoom, row or column skip, or mirroring.<br>1: Output all frames (including bad frames) | 0x0 | N | 0 | W |
| Bit 5<br>Reset SOC | This reset signal is fed directly to the SOC part of the chip, and has no functionality in a stand-alone sensor. | 0x0 | N | 0 | W |
| Bit 4<br>Output Disable | When set, the output pins are tri-stated. | 0x0 | N | 0 | W |
| Bit 3<br>Chip Enable | 0: Stop sensor readout.<br>1: Normal operation.<br>When this is returned to "1," sensor readout restarts and begins resetting the starting row in a new frame. To reduce the digital power, the master clock to the sensor can be disabled or the standby pin can be used. | 0x1 | N | YM | W |
| Bit 2<br>Analog Standby | 0: Normal operation (default)<br>1: Disable analog circuitry.<br>Whenever this bit is set to "1" the chip enable bit (bit 3) should be set to "0." | 0x0 | N | YM | W |
| Bit 1<br>Restart | Setting this bit causes the sensor to abandon the current frame and start resetting the first row. The delay before the first valid frame is read out equals the integration time. This bit always reads "0." | 0x0 | N | YM | W |
| Bit 0<br>Reset | Setting this bit puts the sensor in reset mode; this sets the sensor to its default power-up state. Clearing this bit resumes normal operation. | 0x0 | N | YM | W |
| **R32:0—0X020 - READ MODE—CONTEXT B** | | | | | |
| Bit 15<br>XOR Line Valid | 0: LINE_VALID determined by bit 9.<br>Ineffective if "Continuous" LINE_VALID is set.<br>1: LINE_VALID = Continuous LINE_VALID XOR FRAME_VALID. | 0x0 | N | 0 | W |
| Bit 14<br>Continuous Line Valid | 0: Normal LINE_VALID (default, no line valid during vertical blanking).<br>1: "Continuous" LINE_VALID (continue producing LINE_VALID during vertical blanking). | 0x0 | N | 0 | W |
| Bit 10<br>Power Readout Mode—Context B | When read mode Context B is selected (bit 3, Reg0x0C8 = 1):<br>0: Full-power readout mode, maximum readout speed.<br>1: Low-power readout mode. Maximum readout frequency is now half of the master clock, and the pixel clock is automatically adjusted as described for the pixel clock speed register. | 0x0 | Y | YM | W |
| Bit 9<br>Show Border | This bit indicates whether to show the border enabled by bit 8. When bit 8 is 0, this bit has no meaning. When bit 8 is 1, this bit decides whether the border pixels should be treated as extra active pixels (1) or extra blanking pixels (0). | 0x1 | N | 0 | W |
| Bit 8<br>Over Sized | When this bit is set, a 4-pixel border is output around the active image array independent of readout mode (skip, zoom, mirror, etc.). Setting this bit therefore adds eight to the numbers of rows and columns in the frame. | 0x1 | Y | YM | W |
| Bits 7:6 | Reserved. | 0x0 | Y | YM | W |



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## Table 12: Sensor Core Register Descriptions (continued)

| BIT FIELD | DESCRIPTION | DEFAULT (HEX) | SYNCED TO FRAME START | BAD FRAME | READ/ WRITE |
|---|---|---|---|---|---|
| Bit 5<br>Column Skip 4x | 0: Normal readout.<br>1: Readout two columns, and then skip six columns (as with rows). | 0x0 | Y | YM | W |
| Bit 4<br>Row Skip 4x | 0: Normal readout.<br>1:Readout two rows, and then skip six rows (i.e., row 8, row 9, row 16, row 17…). | 0x0 | Y | YM | W |
| Bit 3<br>Column Skip 2x —Context B | When read mode Context B is selected (bit 3, Reg0x0C8 = 1):<br>0: Normal readout.<br>1: Readout two columns, and then skip two columns (as with rows). | 0x0 | Y | YM | W |
| Bit 2<br>Row Skip 2x— Context B | When read mode Context B is selected (bit 3, Reg0x0C8 = 1):<br>0: Normal readout.<br>1: Readout two rows, then skip two rows (i.e., row 8, row 9, row 12, row 13…). | 0x0 | Y | YM | W |
| Bit 1<br>Mirror Columns | Readout columns from right to left (mirrored). When set, column readout starts from column (Col Start + Col Size) and continues down to (Col Start + 1). When clear, readout starts at Col Start and continues to (Col Start + Col Size - 1). This ensures that the starting color is maintained. | 0x0 | Y | YM | W |
| Bit 0<br>Mirror Rows | Readout rows from bottom to top (upside down). When set, row readout starts from row (Row Start + Row Size) and continues down to (Row Start + 1). When clear, readout starts at Row Start and continues to (Row Start + Row Size - 1). This ensures that the starting color is maintained. | 0x0 | Y | YM | W |
| **R33:0—0X021 - READ MODE—CONTEXT A** | | | | | |
| Bit 10<br>Power Readout Mode— Context A | When read mode Context A is selected (bit 3, Reg0x0C8 = 0):<br>0: Full-power readout mode, maximum readout speed.<br>1: Low-power readout mode. Maximum readout frequency is now half of the master clock, and the pixel clock is automatically adjusted as described for the pixel clock speed register. | 0x1 | Y | YM | W |
| Bit 3<br>Column Skip 2x —Context A | When read mode Context A is selected (bit 3, Reg0x0C8 = 0):<br>0: Normal readout.<br>1: Readout two columns, and then skip two columns (as with rows). | 0x1 | Y | YM | W |
| Bit 2<br>Row Skip 2x— Context A | When read mode Context A is selected (bit 3, Reg0x0C8 = 0):<br>0: Normal readout.<br>1: Readout two rows, and then skip two rows (i.e., row 8, row 9, row 12, row 13…). | 0x1 | Y | YM | W |
| **R35:0—0X023 - FLASH CONTROL** | | | | | |
| Bit 15<br>Flash Strobe | Read-only bit that indicates whether the FLASH_STROBE pin is enabled. | 0x0 | 0 | 0 | R |
| Bit 14 | Reserved. | — | — | — | — |
| Bit 13<br>Xenon Flash | Enable Xenon flash. When set, the FLASH_STROBE output pin is pulsed HIGH for the programmed period during vertical blanking. This is achieved by keeping the integration time equal to one frame and the pulse width less than the vertical blanking time. | 0x0 | Y | N | W |
| Bits 12:11<br>Frame Delay | Delay of the flash pulse measured in frames. | 0x0 | N | N | W |



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## Table 12: Sensor Core Register Descriptions (continued)

| BIT FIELD | DESCRIPTION | DEFAULT (HEX) | SYNCED TO FRAME START | BAD FRAME | READ/ WRITE |
|---|---|---|---|---|---|
| Bit 10<br>End of Reset | 0: In Xenon mode, the flash should be enabled after the readout of a frame.<br>1: In Xenon mode, the flash should be triggered after the resetting of a frame. | 0x1 | N | N | W |
| Bit 9<br>Every Frame | 0: Flash should be enabled for one frame only.<br>1: Flash should be enabled every frame. | 0x1 | N | N | W |
| Bit 8<br>LED Flash | Enables LED flash. When set, the FLASH_STROBE goes on prior to the start of a frame reset. When disabled, the FLASH_STROBE remains HIGH until readout of the current frame completes. | 0x0 | Y | Y | W |
| Bits 7:0<br>Xenon Count | Length of FLASH_STROBE pulse when Xenon flash is enabled. The value specifies the length in 1,024 master clock cycle increments. | 0x08 | N | N | W |
| **R43:0—0X02B - GREEN1 GAIN** | | | | | |
| Bits 6:0<br>Initial Gain | Initial gain = bits (6:0) x 0.03125. | 0x20 | Y | N | W |
| Bits 8:7<br>Analog Gain | Analog gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2x gain). | 0x0 | Y | N | W |
| Bits 10:9<br>Digital Gain | Total gain = (Bit 9 + 1) x (Bit 10 + 1) x analog gain (each bit gives 2x gain). | 0x0 | Y | N | W |
| **R44:0—0X02C - BLUE GAIN** | | | | | |
| Bits 10:9<br>Digital Gain | Total gain = (Bit 9 + 1) x (Bit 10 + 1) x analog gain (each bit gives 2x gain). | 0x0 | Y | N | W |
| Bits 8:7<br>Analog Gain | Analog gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2x gain). | 0x0 | Y | N | W |
| Bits 6:0<br>Initial Gain | Initial gain = bits (6:0) x 0.03125. | 0x20 | Y | N | W |
| **R45:0—0X02D - RED GAIN** | | | | | |
| Bits 10:9<br>Digital Gain | Total gain = (Bit 9 + 1) x (Bit 10 + 1) x analog gain (each bit gives 2x gain). | 0x0 | Y | N | W |
| Bits 8:7<br>Analog Gain | Analog gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2x gain). | 0x0 | Y | N | W |
| Bits 6:0<br>Initial Gain | Initial gain = bits (6:0) x 0.03125. | 0x20 | Y | N | W |
| **R46:0—0X02E - GREEN2 GAIN** | | | | | |
| Bits 10:9<br>Digital Gain | Total gain = (Bit 9 + 1) x (Bit 10 + 1) x analog gain threshold (each bit gives 2x gain). | 0x0 | Y | N | W |
| Bits 8:7<br>Analog Gain | Analog gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2x gain). | 0x0 | Y | N | W |
| Bits 6:0<br>Initial Gain | Initial gain = bits (6:0) x 0.03125. | 0x20 | Y | N | W |
| **R47:0—0X02F - GLOBAL GAIN** | | | | | |
| Bits 10:0<br>Global Gain | This register can be used to set all four gains at once. When read, it returns the value stored in Reg0x2B. | 0x20 | Y | N | W |
| **R200:0—0X0C8 - CONTEXT CONTROL** | | | | | |



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## Table 12: Sensor Core Register Descriptions (continued)

| BIT FIELD | DESCRIPTION | DEFAULT (HEX) | SYNCED TO FRAME START | BAD FRAME | READ/ WRITE |
|---|---|---|---|---|---|
| Bit 15<br>Restart | Setting this bit causes the sensor to abandon the current frame and start resetting the first row. Same physical register as Reg0x00D, bit 1. | 0x0 | N | YM | W |
| Bit 7<br>Xenon Flash Enable | Enable Xenon flash. Same physical register as Reg0x023, bit 13. | 0x0 | Y | N | W |
| Bit 3<br>Read Mode Select | 0: Use read mode, Context A, Reg0x021.<br>1: Use read mode, Context B, Reg0x020.<br>Note that bits found only in the read mode Context B register is always taken from that register. | 0x0 | Y | YM | W |
| Bit 2<br>LED Flash Enable | Enable LED flash. Same physical register as Reg0x023, bit 8. | 0x0 | Y | Y | W |
| Bit 1<br>Vertical Blanking Select | 0: Use vertical blanking, Context A, Reg0x008<br>1: Use vertical blanking, Context B, Reg0x006. | 0x0 | Y | YM | W |
| Bit 0<br>Horizontal Blanking Select | 0: Use horizontal blanking, Context A, Reg0x007.<br>1: Use horizontal blanking, Context B, Reg0x005. | 0x0 | Y | YM | W |
| **R240:0—0X0F0 - PAGE MAP** | | | | | |
| Bits 2:0<br>Page Map | Page mapping register. Must be kept at 0 to be able to write to/read from sensor. Used in the SOC to access other pages with registers. | 0x0 | N | 0 | W |
| **R241:0—0X0F1 - BYTE-WISE ADDRESS** | | | | | |
| Bit 0<br>Byte-Wise Address | Special address to perform 8-bit (instead of 16-bit) reads and writes to the sensor. For additional information, see "Two-Wire Serial Interface Sample" on page 57 and "APPENDIX A" on page 56. | N/A | 0 | 0 | 0 |
| **R255:0—0X0FF - CHIP VERSION (R/O)** | | | | | |
| Bits 15:0 | Hardwired value. | 0x143A | | | R |

NOTE:

**Notation used in the sensor core register description table:**

**Sync'd to frame start**

0 = Not applicable, e.g., read-only register.

N = No. The register value is updated and used immediately.

Y = Yes. The register value is updated at next frame start as long as the synchronize-changes bit is 0. Note also that frame start is defined as when the first dark row is read out. By default, this is 8 rows before FRAME_VALID goes HIGH.

**Bad frame**

A bad frame is a frame where all rows do not have the same integration time, or offsets to the pixel values changed during the frame.

0 = Not applicable, e.g., read-only register.

N = No. Changing the register value does not produce a bad frame.

Y = Yes. Changing the register value might produce a bad frame.

YM = Yes, but the bad frame is masked out unless the "show bad frames" feature is enabled.

**Read/Write**

R—Read-only register/bit.

W—Read/write register/bit.



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## Sensor Read Modes and Timing

This section provides an overview of typical usage modes for the MT9M111. It focuses on two primary configurations: the first is suitable for low-power viewfinding, the second for full-resolution snapshots. It also describes mechanisms for switching between these modes.

### *Contexts*

The MT9M111 supports hardware-accelerated context switching. A number of parameters have two copies of their setup registers; this allows two "contexts" to be loaded at any given time. These are referred to as Context A and Context B. Context selection for any single parameter is determined by the Global Context Control Register (GCCR, see R200:2). There are copies of this register in each address page. A write to any one of them has the identical effect. However, a READ from address page 0 only returns the subset bits of R200 that are specific to the sensor core.

The user can employ contexts for a variety of purposes; thus the generic naming convention. One typical usage model is to define Context A as "viewfinder" or "preview" mode and Context B as "snapshot" mode. The device defaults are configured with this in mind. This mechanism enables the user to have settings for viewfinder and snapshot modes loaded at the same time, and then switch between them with a single write to e.g. R200:2.

### *Viewfinder/Preview and Full-Resolution/Snapshot Modes*

In the MT9M111, the sensor core supports two primary readout modes: low-power preview mode and full-resolution snapshot mode.

#### Low-Power Preview Mode

QSXGA (640 x 512) images are generated at up to 30 fps. The reduced-size images are generated by skipping pixels in the sensor, i.e. decimation. The key sensor registers that define this mode are Read Mode Context A Register (R33:0) and Read Mode Context B Register (R32:0). Only certain bits in these registers are context switchable; any bits that do not have multiple contexts are always defined by their values in R32:0. Any active sets of these registers are defined by the state of R200:n[3]. On reset, R200:n[3] = 0 selecting R33:0; setups specific to preview are defined by this register.

#### Full-Resolution Snapshot Mode

SXGA (1,280 x 1,024) images are generated at up to 15 fps. This is typically selected by setting R200:n[3] = 1 selecting R32:0 (Context B) as the primary read mode register.

#### Switching Modes

Typically, switching to full-resolution or snapshot mode is achieved by writing R200:2 = 0x9F0B. This restarts the sensor and sets most contexts to Context B. Following this write, a READ from R200:1 or R200:2 results in 0x1F0B being read. Note that the most significant bit (MSB) is cleared automatically by the sensor. A READ from R200:0 results in 0x000B, as only the lower 4 bits and the restart MSB are implemented in the sensor core.

### *Clocks*

The sensor core is a master in the system. The sensor core frame rate defines the overall image flow pipeline frame rate. Horizontal and vertical blanking are influenced by the sensor configuration, and are also a function of certain IFP functions—particularly resize. The relationship of the primary clocks are depicted in Figure 9.


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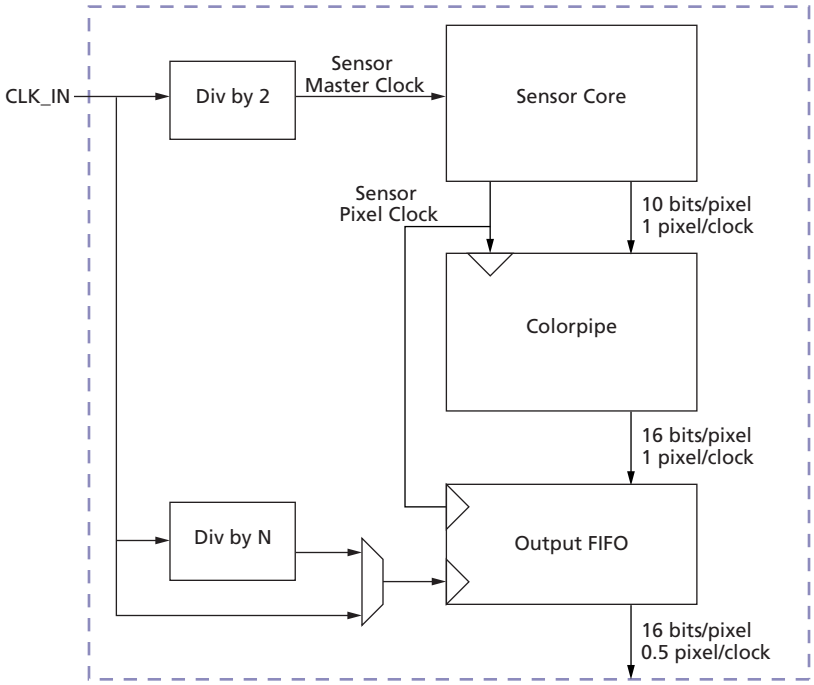
**Figure 9: Primary Sensor Core Clock Relationships**




The IFP typically generates up to 16 bits per pixel, for example YCbCr or RGB565, but has only an 8-bit port through which to communicate this pixel data. There is no phase locked loop (PLL), so the primary input clock (CLKIN) must be twice the fundamental pixel rate (defined by the sensor pixel clock).

To generate SXGA images at 15 fps, the sensor core requires a clock in the 24 MHZ to 27 MHz range; this is also the fundamental pixel clock rate (sensor pixel clock) for full-power operation. To achieve this pixel rate, CLKIN must be in the 48 MHz to 54 MHz range. The device defaults assume a 54 MHz clock. Minimum clock frequency is 2 MHz.

## *Primary Operating Modes*

The MT9M111 supports two primary modes of operation with respect to the sensor core that affect pixel rate, frame rate and blanking:

### Full-Power Readout Mode

The sensor is in full-resolution mode, generating 1.3 megapixels (SXGA = 1,280 x 1,024 + border) for interpolation. The SXGA image fed from the sensor to the colorpipe can be resized in the colorpipe, but the frame rate is still defined by sensor core operation. In full-power readout mode, with full field of view, the frame rate is invariant with the final image size:

| | |
|---|---|
| Context | Typically Context B |
| Sensor read mode settings | No skipping<br>Full-power readout, i.e., full data rate |
| Sensor pixel clock | 27 MHz for 54 MHz master clock: Maximum pixel rate of 27 megapixels/s |
| MAX frame rate | For 54 MHz master clock, 15 fps |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### Low-Power Readout Mode

Running under low-power readout, the sensor is in skip mode, and generates QSXGA frames (640 x 512 + border = 336,960 pixels). This full field of view QSXGA image can be resized, but only to resolutions smaller than QSXGA. The frame rate is defined by the operating mode of the sensor:

| | |
|---|---|
| Context | Typically Context A |
| Sensor read mode settings | Row skip 2x<br>Column skip 2x<br>Low-power readout maximum data rate is half that of full-power readout |
| Sensor pixel clock | 13.5 MHz for 54 MHz master clock: Maximum pixel rate of 13.5 megapixels/s |
| Maximum frame rate | For 54 MHz master clock, 30 fps |

### Tuning Frame Rates

Actual frame rates can be tuned by adjusting various sensor parameters. The sensor registers are in page 0, thus the ":0" after each register address:

## Table 13: Register Address Functions

| REGISTER | FUNCTION |
|---|---|
| R0x04:0 | Window Width, typically 1,280 in the MT9M111 |
| R0x03:0 | Window Height, typically 1,024 in the MT9M111 |
| **LOW-POWER READOUT MODE—CONTEXT A** | |
| R0x07:0 | Horizontal blanking, default is 190 (units of sensor pixel clocks) |
| R0x08:0 | Vertical blanking, default is 17 (rows including black rows) |
| **FULL-POWER READOUT MODE—CONTEXT B** | |
| R0x05:0 | Horizontal blanking, default is 388 (units of sensor pixel clocks) |
| R0x06:0 | Vertical blanking, default is 42 (rows including black rows) |

In the MT9M111, the sensor core adds four border pixels all the way around the image, taking the active image size to 1,288 x 1,032 in full-power Snapshot resolution, and 648 x 520 when skipping rows in low-power preview resolution. This is achieved through the default settings:

- Read mode Context B: R0x20:0
- Oversize and show border bits are set by default.
- Oversize and show border bits are not context switchable, thus their location only in read mode Context B.

### Default Blanking Calculations

The MT9M111 default blanking calculations are a function of context, as follows:

**[REG<a> | REG<b>]:**

- Reg<a>
  Low-power readout = Context A, typically used for viewfinder
- Reg<b>
  Full power readout = Context B, typically used for snapshots


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## Table 14: Blanking Parameter Calculations

| PARAMETER | CALCULATION |
|---|---|
| PC_PERIOD<br>Sensor Pixel Clock Period | Full-power readout: (2/54)µs = 0.0370µs<br>Low-power readout: (4/54)µs = 0.0185µs |
| A: Active Data Time (per line):<br>R0x04:0 + 8 (border) * PC_PERIOD | Full-power readout: A = 1288 * (2/54)µs = 47.704µs<br>Low-power readout: A = 648 * (4 / 54)µs = 48.000 µs |
| Q: Horizontal Blanking:<br>[R0x05:0 \| R0x07:0] * PC_PERIOD | Full-power readout: Q = 388 * (2/54)µs = 14.370µs<br>Low-power readout: Q = 190 * (4/54)µs = 14.074µs |
| Row Time = Q + A: | Full-power readout: 62.074µs<br>Low-power readout: 62.074µs |
| P: Frame Start / End Blanking:<br>6 * PC_PERIOD | Full-power readout: P = 6 * (2/54)µs = 0.222µs<br>Low-power readout: P = 6 * (4 / 54)µs = 0.444µs |
| V: Vertical Blanking:<br>[R0x06:0 \| R0x08:0] * (Q + A) + (Q - 2 * P) | Full-power readout: V = (42 * 62.074) + (14.370 - 0.444) = 2621.034 µs<br>Low-power readout: V = (17 * 62.074) + (14.074 - 0.888) = 1068.444 µs |
| F: Total Frame Time:<br>(R0x03:0 + [R0x06:0 \| R00x08:0]) * (A + Q) | Full-power readout: V = (1032 + 42) * 62.074µs = 66667.476µs ≥ 15 fps<br>Low-power readout: V = (520 + 17) * 62.074µs = 33333.738µs ≥ 30 fps |

NOTE:

The line rate (row rate) is the same for both low-power and full-power readout modes. This ensures that when switching modes, exposure time does not change; the pre-existing shutter width remains valid.

### User Blanking Calculations

When calculating blanking for different clock rates, minimum values for horizontal blanking and vertical blanking must be taken into account. Table 15 shows minimum values for each register

## Table 15: User Blanking Minimum Values

| PARAMETER | REGISTER | MINIMUM |
|---|---|---|
| Horizontal Blanking | Full-power readout (Context B): R0x05:0<br>Low-power readout (Context A): R0x07:0 | 202 (sensor pixel clocks)<br>114 (sensor pixel clocks) |
| Vertical Blanking | Full-power readout (Context B): R0x06:0<br>Low-power readout (Context A): R0x08:0 | 5 (rows)<br>5 (rows) |


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## Exposure and Sensor Context Switching

The MT9M111 incorporates device setup features that prevent changes in sensor context from causing a change in exposure when switching between preview/viewfinder and full-resolution/snapshot modes. This is achieved by keeping the line rate consistent between modes.

### Exposure

Defined by the shutter width. This is the number of lines to be reset before starting a frame read. If line rate does not change when a mode changes, exposure does not change.

### Switching From Context A to B

Under typical/default settings, the sensor pixel rate doubles when switching from preview (Context A) to full-resolution (Context B). Additionally, the number of pixels to be read per line nearly doubles. This naturally keeps the line rates roughly equal. The difference occurs due to border pixels: for SOC operation, there are always 8 border pixels regardless of context, thus the number of pixels in each line is not quite doubled.

### Horizontal Blanking

Defined in terms of "sensor pixel clocks." The sensor pixel clock rate doubles when switching from low-power readout mode (preview Context A) to full-power readout mode (full-resolution Context B). To maintain the same horizontal blanking time, the value for horizontal blanking must double. This is handled by the dual, context-switchable horizontal blanking registers.

### Switching Modes

Initiate mode switches from preview (Context A) to snapshot (Context B) during vertical blanking; switching should be accompanied by a sensor restart. Be sure R200:0[15] is written as "1" when changing contexts.

### Switching Frequency

The user can switch between sensor contexts as frequently as necessary (without affecting exposure) with the default values for horizontal blanking and vertical blanking (R5:0–R8:0).Usefully, constant switches can occur as often as once per frame.

### Simple Snapshots

To take a snapshot, simply switch from Context A to Context B (with restart) for a few frames, then switch back again, capturing one of the Context B frames as the snapshot. Alternative methods are supported by an internal sequencer. These additional methods are particularly useful for taking flash snapshots.


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## Output Timing

**Figure 10: Vertical Timing**

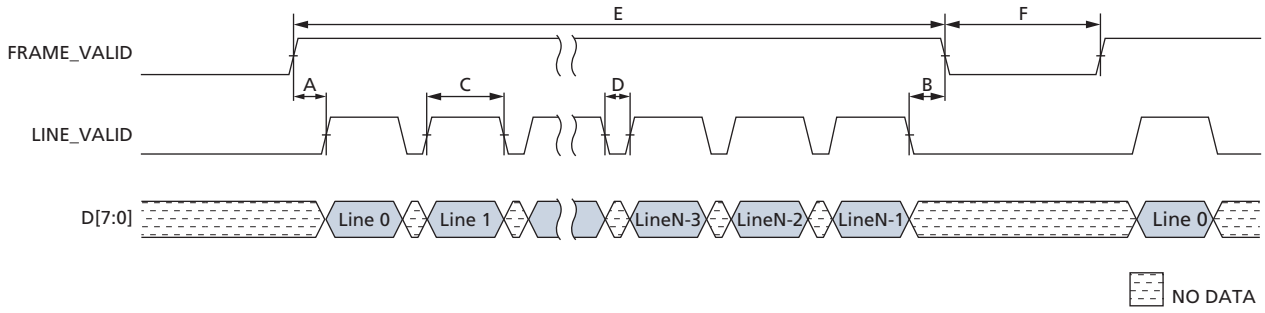
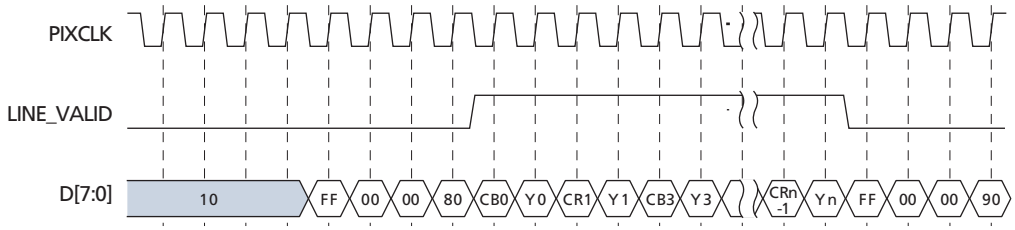



**Figure 11: Horizontal Timing**





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## Typical Resolutions, Modes and Timing

The parameters in Table 16 are illustrated in waveform diagram Figure 10 on page 50. Table 20 provides values for these parameters in some common resolutions and operating modes.

### Table 16: Blanking Definitions

| DESIGNATION | DEFINITION |
|---|---|
| (A) | FRAME_VALID (rising edge) to LINE_VALID (rising edge) delay |
| (B) | LINE_VALID (falling edge) to FRAME_VALID (falling edge) delay |
| (C) | LINE_VALID (HIGH/valid) time |
| (D) | LINE_VALID (LOW/horizontal blanking) time |
| (E) | FRAME_VALID (HIGH/valid) time |
| (F) | FRAME_VALID (LOW/vertical blanking) time |

## Reset, Clocks, and Standby

### Functional Operation

Power-up reset is asserted/de-asserted on the RESET# pin. It is active LOW. In this reset state, all control registers have the default values. All internal clocks are turned off except for the divided-by-2 clock to the sensor core.

Soft reset is asserted/de-asserted by the two-wire serial interface program. There are sensor hardmac soft resets and SOC soft resets. In soft reset mode, the two-wire serial interface and register ring bus are still running. All control registers are reset using default values. See R13:0.

Hard standby is asserted/de-asserted on the STANDBY pin. It is active HIGH. In this hard standby state, all internal clocks are turned off and analog block is in standby mode to save power consumption. (Note: following the assertion of hard standby, at least 24 master clock cycles must be delivered to complete the transition to the hard standby state.)

Soft standby is asserted/de-asserted differently in the sensor page or colorpipe page. The sensor soft standby bit is in R13:0[2]. Colorpipe soft standby disables some of the SOC clocks, including the pixel clock. This bit is R179:1[0]. The colorpipe should be brought out of standby first via R179:1[0].

The colorpipe soft standby is provided to enable the user to turn off the colorpipe and the sensor independently.

By default, all outputs except SDATA are disabled during hard standby. This feature can be disabled by setting R179:1[1] = 0. Independent control of the outputs is available either via the OE# pin or R13:0[4]. All outputs are implemented using bidirectional buffers, thus should not be left tri-stated. In dual camera applications, ensure that one camera is driving the bus, or that the bus is pulled to VGNDQ or VDDQ, even during standby.


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## Electrical Specifications

### Table 17: Electrical Characteristics and Operating Conditions

($T_A$ = Ambient = 25°C)

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| I/O digital voltage (VDDQ) | | 1.7V | | 3.6V | V |
| Core digital voltage (VDD) | | 2.5V | 2.8V | 3.1V | V |
| Analog voltage (VAA) | | 2.5V | 2.8V | 3.1V | V |
| Pixel supply voltage (VAAPIX) | | 2.5V | 2.8V | 3.1V | V |
| Leakage current | STANDBY, No clocks | | | 10 | µA |
| Operating Temperature | Measured at junction | -30 | | +70 | °C |

NOTE:

VDD, VAA, and VAAPIX must all be at the same potential to avoid excessive current draw. Care must be taken to avoid excessive noise injection in the analog supplies if all three supplies are tied together.

### Table 18: I/O Parameters

| PIN | PARAMETER | DEFINITIONS | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| All Outputs | | Load capacitance | | | | 30 | pF |
| | | Output pin slew | 2.8V, 30pF load | | 0.72 | | V/ns |
| | | | 2.8V, 5pF load | | 1.25 | | V/ns |
| | | | 1.8V, 30pF load | | 0.34 | | V/ns |
| | | | 1.8V, 5pF load | | 0.51 | | V/ns |
| | VOH | Output high voltage | | | | | V |
| | VOL | Output low voltage | | | | | V |
| | IOH | Output high current | VDDQ = 2.8V, VOH = 2.4V | 16 | | 26.5 | mA |
| | | | VDDQ = 1.8V, VOH = 1.4V | 8 | | 15 | mA |
| | IOL | Output low current | VDDQ = 2.8V, VOL = 0.4V | 15.9 | | 21.3 | mA |
| | | | VDDQ = 1.8V, VOL = 0.4V | 10.1 | | 16.2 | mA |
| | IOZ | Tri-state output leakage current | | | | | |
| All Inputs | VIH | Input high voltage | VDDQ = 2.8V | 1.48 | | | V |
| | | | VDDQ = 1.8V | 0.94 | | | V |
| | VIL | Input low voltage | VDDQ = 2.8V | | | 1.43 | V |
| | | | VDDQ = 1.8V | | | 0.84 | V |
| | IIN | Input leakage current | | -2µ | | | 2µA |
| | PIN CAP | Pin input capacitance | | | 3.5 | | pF |
| CLKIN | Freq | Master clock frequency | Absolute minimum | 2 | | | MHz |
| | | | SXGA @ 15 fps | 48 | | 54 | MHz |



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## *Power Consumption*

### Table 19: Power Consumption at 2.8V

| MODE | SENSOR/mW | IMAGE FLOW PROC/mW | I/OS (10pF)/mW | TOTAL M/mW |
|---|---|---|---|---|
| SXGA at 15 fps | 90 | 71 | 9 | 170 |
| QSXGA at 30 fps | 50 | 36 | 4 | 90 |
| QSXGA at 15 fps | 50 | 18 | 2 | 70 |
| QVGA at 30 fps | 50 | 32 | 1 | 83 |



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### I/O Timing

By default, the MT9M111 launches pixel data, FRAME_VALID, and LINE_VALID synchronously with the falling edge of PIXCLK. The expectation is that the user captures data, FRAME_VALID, and LINE_VALID using the rising edge of PIXCLK. The timings in Figure 12 assume that the sense of PIXCLK is inverted from the default. This is achieved by setting R58:1[9] and R155:[9] = 1.

**Figure 12: I/O Timing Diagram**

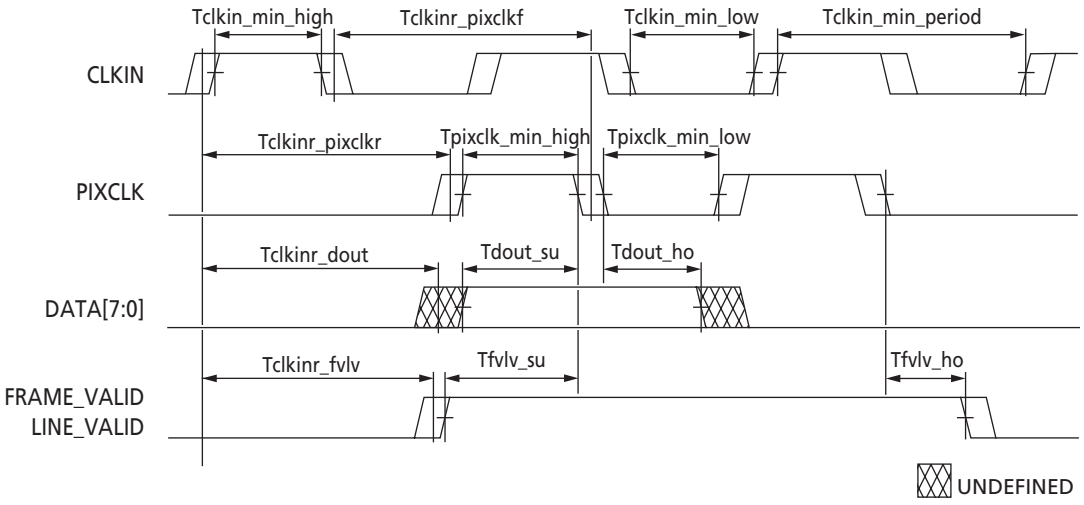


**Table 20: I/O Timing Table**

| SIGNAL | PARAMETER | CONDITIONS | SLOW | | FAST | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| CLKIN | Tclkin_min_high | | 7.4 | | 7.4 | | ns |
| | Tclkin_min_low | | 7.4 | | 7.4 | | ns |
| | Tclkin_min_period | | 18.5 | | 18.5 | | ns |
| PIXCLK | Tclkinr_pixclkr | | 16.5 | 16.9 | 7.7 | 7.9 | ns |
| | Tclkinf_pixclkfl | | 17.5 | 17.6 | 7.9 | 8.0 | ns |
| | Tpixclk_min_low | 50:50, 54 MHz CLKIN | 8.2 | | 9.0 | | ns |
| | Tpixclk_min_high | 50:50, 54 MHz CLKIN | 9.9 | | 9.3 | | ns |
| DATA[7:0] | Tclkinr_dout | | 15.7 | 18.6 | 7.6 | 8.6 | ns |
| | Tdout_su | 50:50, 54 MHz CLKIN | 8.2 | | 8.6 | | ns |
| | Tdout_ho | 50:50, 54 MHz CLKIN | 7.4 | | 8.9 | | ns |
| FRAME_VALID/LINE_VALID | Tclkinr_fvlv | | 18.0 | 21.0 | 8.8 | 9.9 | ns |
| | Tfvlv_su | 50:50, 54 MHz CLKIN | 5.8 | | 7.3 | | ns |
| | Tfvlv_ho | 50:50, 54 MHz CLKIN | 9.7 | | 10.1 | | ns |



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**Figure 13: Spectral Response Chart (Preliminary)**

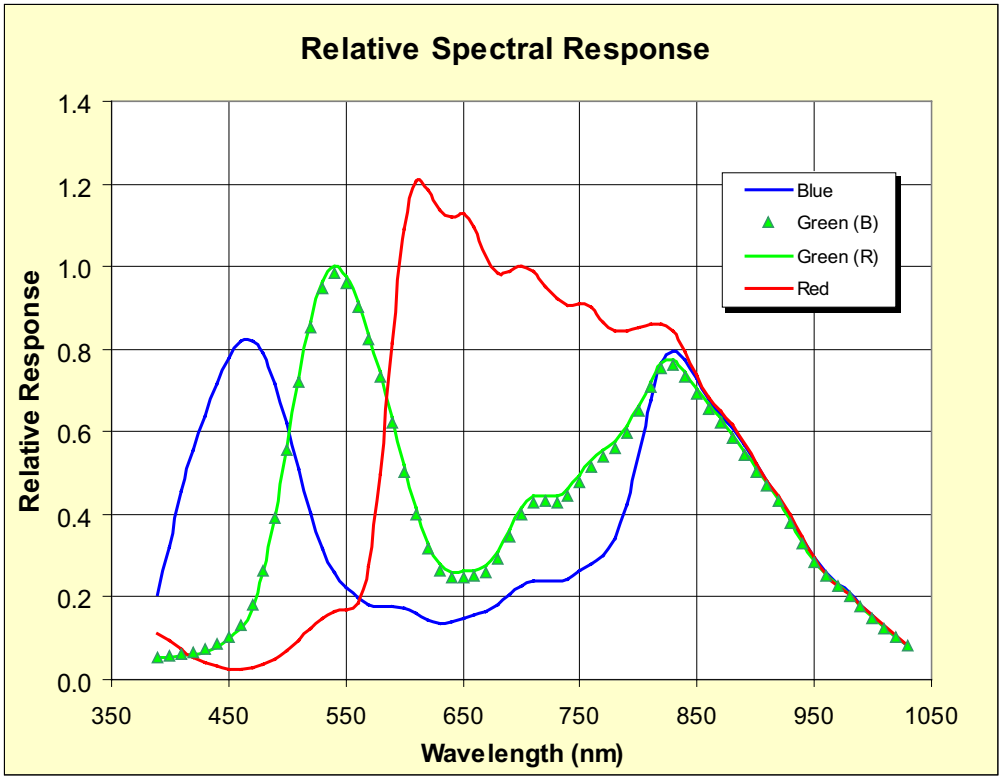
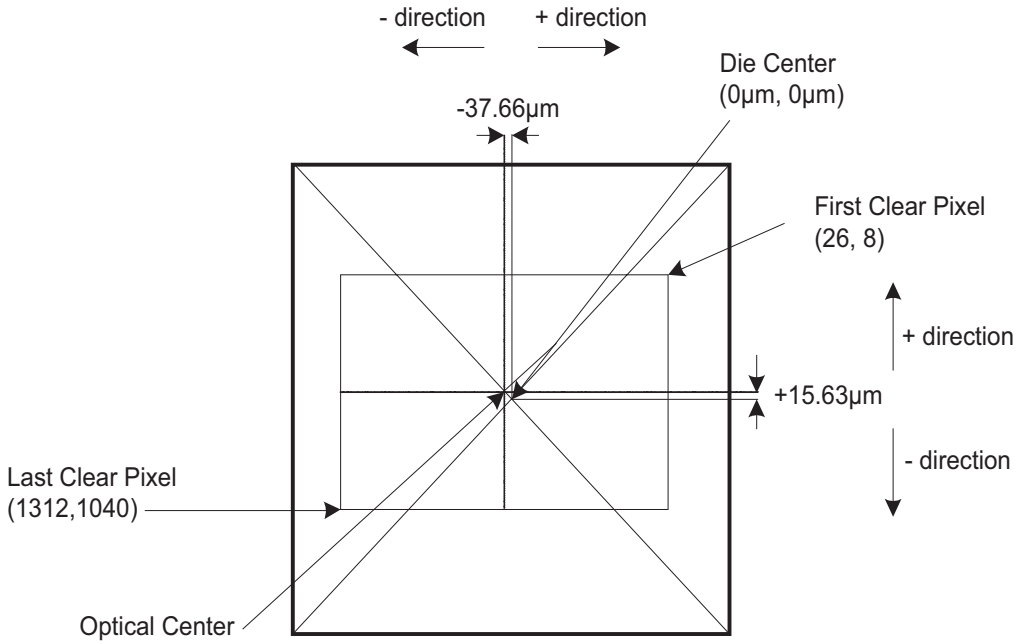



**Figure 14: Optical Center Diagram**




NOTE:
Figure not to scale.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# APPENDIX A

## Serial Bus Description

Registers are written to and read from the MT9M111 through the two-wire serial interface bus. The sensor is a serial interface slave and is controlled by the serial clock (SCLK). SLCK is driven by the serial interface master. Data is transferred into and out of the MT9M111 through the serial data (SDATA) line. The SDATA line is pulled up to 2.8V off-chip by a 1.5KΩ resistor. Either the slave or the master device can pull the SDATA line down—the two-wire serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

### *Protocol*

The two-wire serial interface defines several different transmission codes, as follows:

- a start bit
- the slave device 8-bit address. The SADDR pin is used to select between two different addresses in case of conflict with another device. If SADDR is LOW, the slave address is 0x90; if SADDR is HIGH, the slave address is 0xBA.
- an acknowledge or a no-acknowledge bit
- an 8-bit message
- a stop bit.

### *Sequence*

A typical read or write sequence begins with the master sending a start bit. After the start bit, the master sends the 8-bit slave device address. The last bit of the address determines if the request is a read or a write, where a "0" indicates a write and a "1" indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data, 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits.

The MT9M111 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. The master sends the write-mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master clocks out the register data, 8 bits at a time, and sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

### *Bus Idle State*

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

### *Start Bit*

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

### *Stop Bit*

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

### *Slave Address*

The 8-bit address of a two-wire serial interface device consists of seven bits of address and 1 bit of direction. A "0" in the least significant bit (LSB) of the address indicates write mode, and a "1" indicates read mode. The write address of the sensor is 0xBA; the read address is 0xBB. This applies only when the SADDR is set HIGH.

### *Data Bit Transfer*

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

### *Acknowledge Bit*

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver signals an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

### *No-Acknowledge Bit*

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.


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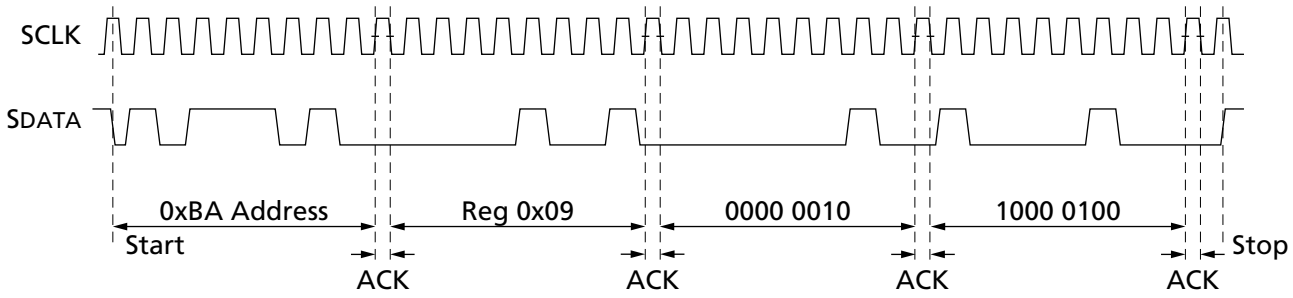
## Two-Wire Serial Interface Sample Write and Read Sequences (SADDR = 1)

### 16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 15. A start bit sent by the master starts the sequence, followed by the write address. The image sensor sends an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each 8-bit transfer, the image sensor sends an acknowledge bit. All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

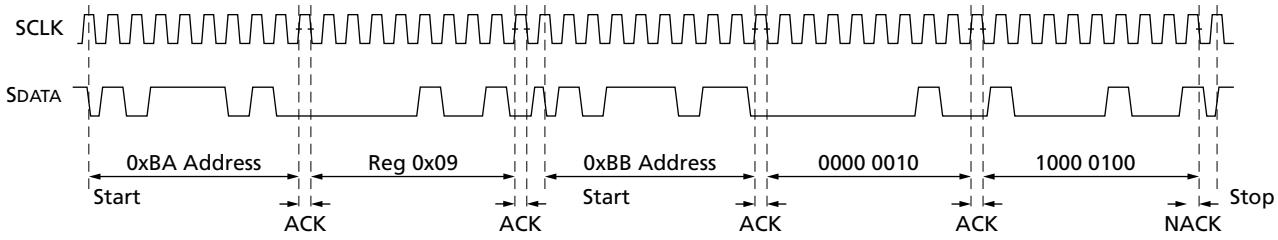
**Figure 15: Write Timing to R0x09:0—Value 0x0284**




### 16-Bit Read Sequence

A typical read sequence is shown in Figure 16. The master writes the register address, as in a write sequence. Then a start bit and the read address specify that a read is about to occur from the register. The master then clocks out the register data, 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

**Figure 16: Read Timing from R0x09:0; Returned Value 0x0284**





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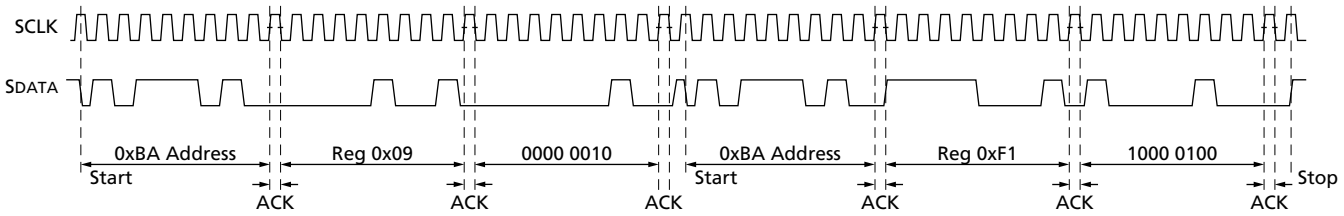
### 8-Bit Write Sequence

To be able to write one byte at a time to the register, a special register address is added. The 8-bit write is started by writing the upper 8 bits to the desired register, then writing the lower 8 bits to the special register address (R0xF1:0). The register is not updated until all 16 bits have been written. It is not possible to update just half of a register. Figure 17 shows a typical sequence for an 8-bit write. The second byte is written to the special register (R0xF1:0).

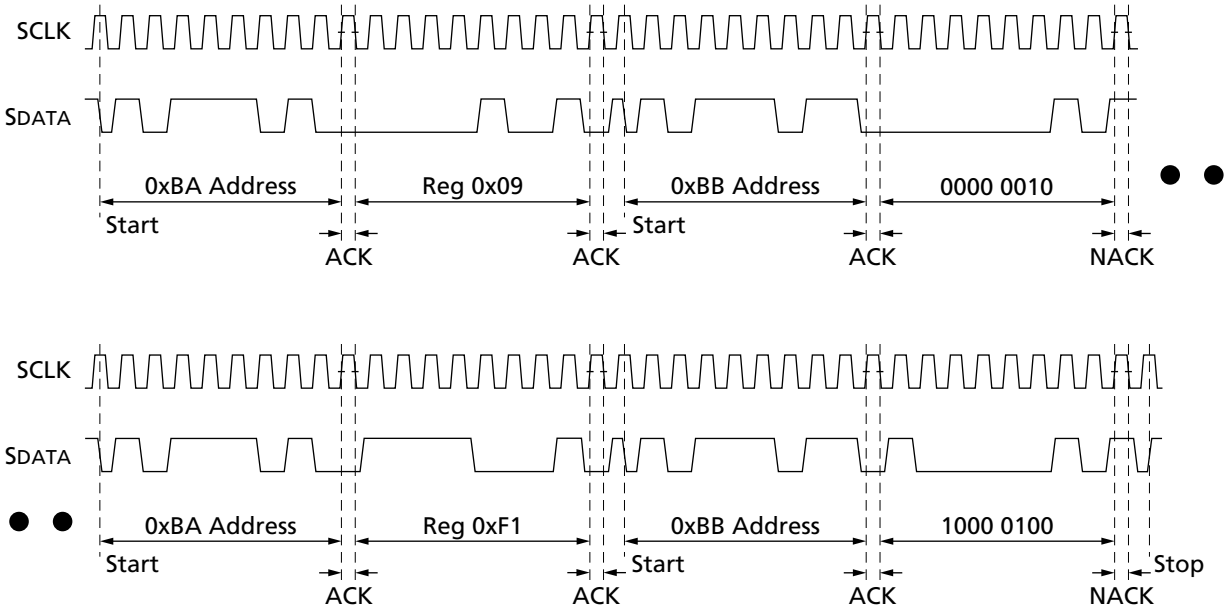
**Figure 17: Write Timing to R0x09:0—Value 0x0284**




### 8-Bit Read Sequence

To read one byte at a time, the same special register address is used for the lower byte. The upper 8 bits are read from the desired register. By following this with a read from the special register (R0xF1:0), the lower 8 bits are accessed (Figure 18). The master sets the no-acknowledge bits shown.

**Figure 18: Read Timing from R0x09:0; Returned Value 0x0284**




### Two-Wire Serial Bus Timing

The two-wire serial bus operation requires certain minimum master clock cycles between transitions. These are specified in the following diagrams in master clock cycles.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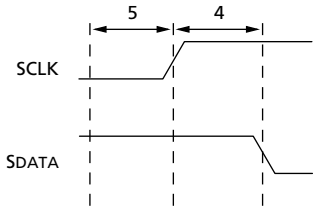
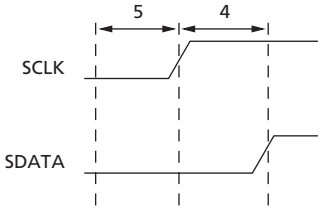
## Figure 19: Serial Host Interface: Start Condition Timing

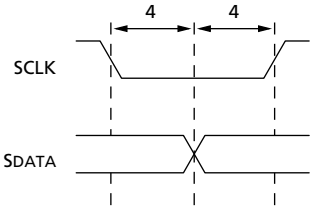



## Figure 20: Serial Host Interface: Stop Condition Timing



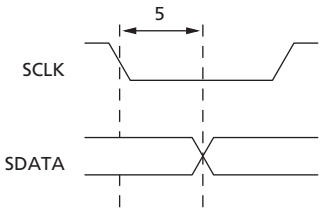

NOTE:
All timing in master clock cycle units.

## Figure 21: Serial Host Interface Write



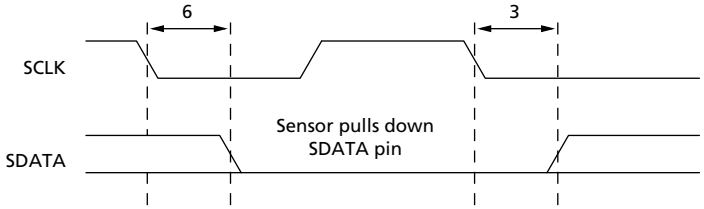

NOTE:
SDATA is driven by an off-chip transmitter.

## Figure 22: Serial Host Interface Read

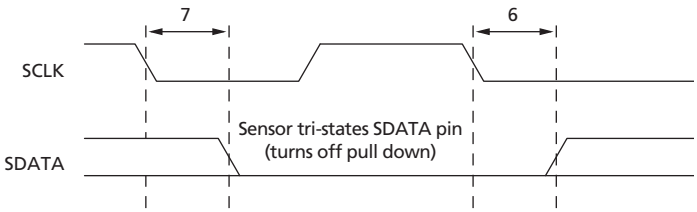



NOTE:
SDATA is pulled LOW by the sensor, or allowed to be pulled HIGH by an off-chip pull-up resistor.

## Figure 23: Acknowledge Signal Timing After an 8-Bit Write to Sensor




## Figure 24: Acknowledge Signal Timing After an 8-Bit Read from Sensor




NOTE:
After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. When the read sequence is complete, the master generates a no-acknowledge bit by leaving SDATA to float HIGH. On the following cycle, either a start or stop bit can be used.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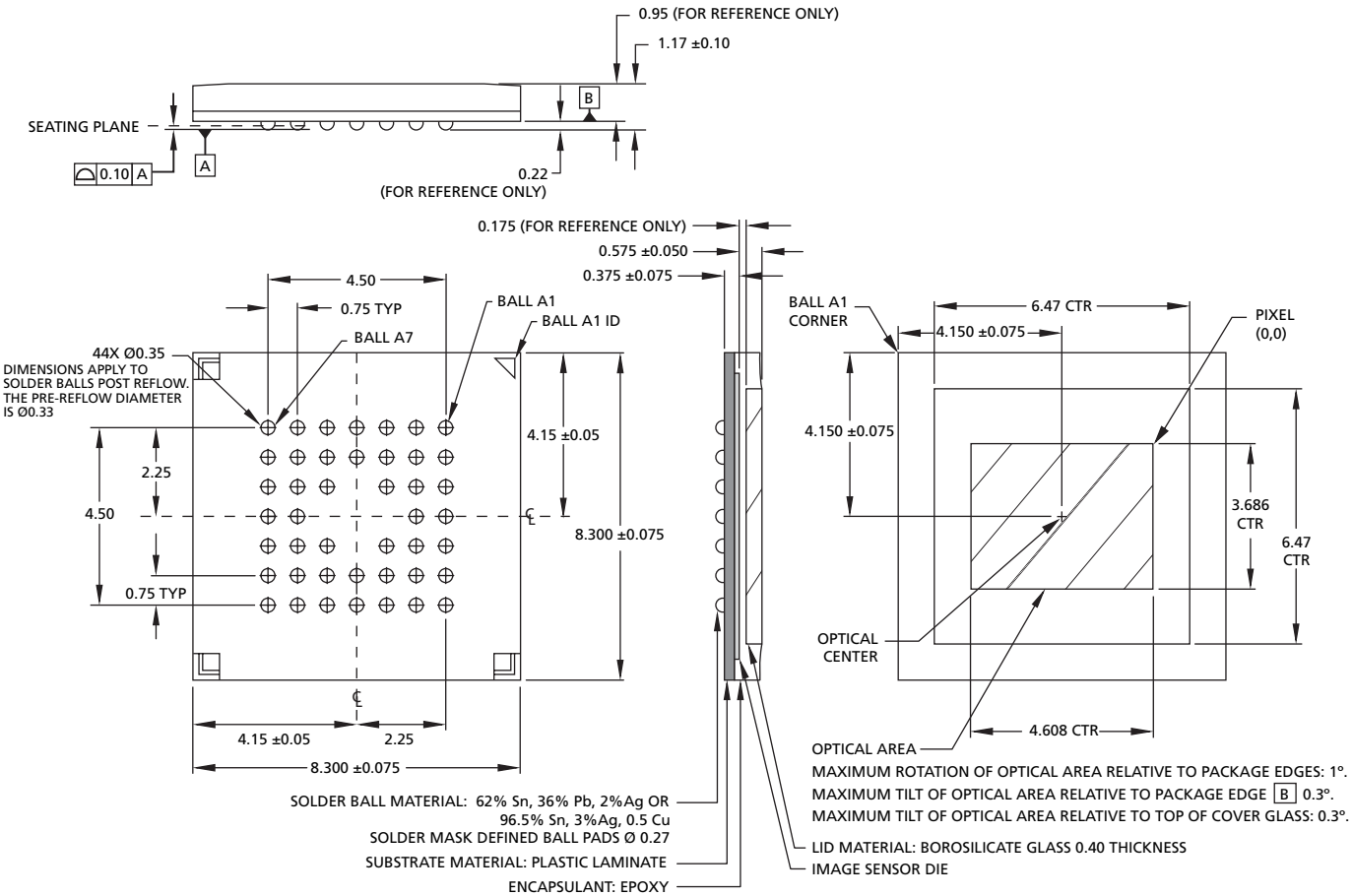
## Figure 25: 44-Ball iCSP Package




NOTE:

Dimensions are in millimeters MIN/MAX or typical where noted.

## Data Sheet Designation: Preliminary

This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

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## Revision History

Rev. C, Preliminary . . . . . 10/04

- Added STANDBY to Figure 3, Typical Configuration (Connection), on page 9.

Rev. B, Preliminary . . . . . 7/04

- Updated package diagram.
- Clarified low-power readout mode.

Rev. A, Preliminary . . . . . 5/04

- Initial release.



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