

N-Channel MOSFET

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Features

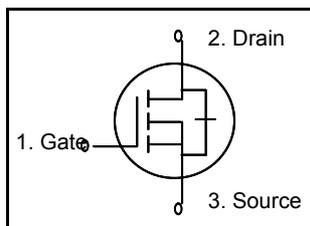
High ruggedness

$R_{DS(on)}$ (Max 5.5)@ $V_{GS}=10V$

Gate Charge (Typical 15nC)

Improved dv/dt Capability

100% Avalanche Tested



$BV_{DSS} = 600V$

$R_{DS(ON)} = 5.5 \text{ ohm}$

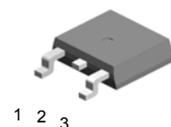
$I_D = 2.1A$

General Description

This N-channel enhancement mode field-effect power transistor using DI semiconductor's advanced planar stripe, DMOS technology intended for off-line switch mode power supply.

Also, especially designed to minimize $r_{ds(on)}$ and high rugged avalanche characteristics. The D-PAK pkg is well suited for charger SMPS and small power inverter application.

D-PAK



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DSS}	Drain to Source Voltage	600	V
I_D	Continuous Drain Current(@ $T_C = 25^\circ C$)	2.1	A
	Continuous Drain Current(@ $T_C = 100^\circ C$)	1.3	A
I_{DM}	Drain Current Pulsed (Note 1)	8.0	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	148	mJ
E_{AR}	Repetitive Avalanche Energy (Note 1)	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Total Power Dissipation(@ $T_C = 25^\circ C$)	45	W
	Derating Factor above $25^\circ C$	0.36	W/ $^\circ C$
T_{STG}, T_J	Operating Junction Temperature & Storage Temperature	- 55 ~ 150	$^\circ C$
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.	300	$^\circ C$

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min.	Typ.	Max.	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	-	-	2.78	$^\circ C/W$
$R_{\theta CS}$	Thermal Resistance, Case to Sink	-	-	50	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	-	-	110	$^\circ C/W$

DFD2N60

Electrical Characteristics ($T_C = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	600	-	-	V
BV_{DSS}/T_J	Breakdown Voltage Temperature coefficient	$I_D = 250\mu A$, referenced to $25\text{ }^\circ\text{C}$	-	0.4	-	$V/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 600V, V_{GS} = 0V$	-	-	10	μA
		$V_{DS} = 480V, T_C = 125\text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	Gate-Source Leakage, Forward	$V_{GS} = 30V, V_{DS} = 0V$	-	-	100	nA
	Gate-source Leakage, Reverse	$V_{GS} = -30V, V_{DS} = 0V$	-	-	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain-Source On-state Resistance	$V_{GS} = 10V, I_D = 1.0A$	-	4.5	5.5	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 25V, f = 1\text{MHz}$	-	570	720	pF
C_{oss}	Output Capacitance		-	150	215	
C_{rss}	Reverse Transfer Capacitance		-	310	450	
Dynamic Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 300V, I_D = 2.0A, R_G = 25$ see fig. 13. (Note 4, 5)	-	15	35	ns
t_r	Rise Time		-	75	140	
$t_{d(off)}$	Turn-off Delay Time		-	30	60	
t_f	Fall Time		-	35	60	
Q_g	Total Gate Charge	$V_{DS} = 480V, V_{GS} = 10V, I_D = 2.0A$ see fig. 12. (Note 4, 5)	-	15	20	nC
Q_{gs}	Gate-Source Charge		-	1.6	-	
Q_{gd}	Gate-Drain Charge(Miller Charge)		-	6	-	

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
I_S	Continuous Source Current	Integral Reverse p-n Junction Diode in the MOSFET	-	-	2.0	A
I_{SM}	Pulsed Source Current		-	-	8.0	
V_{SD}	Diode Forward Voltage	$I_S = 2.0A, V_{GS} = 0V$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$I_S = 2.0A, V_{GS} = 0V, di/dt = 100A/\mu s$	-	600	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.1	-	μC

NOTES

1. Repeativity rating : pulse width limited by junction temperature
2. $L = 68\text{mH}, I_{AS} = 2.0A, V_{DD} = 50V, R_G = 50$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} = 2.0, di/dt = 300A/\mu s, V_{DD} = BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse Width 300 μs , Duty Cycle 2%
5. Essentially independent of operating temperature.

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Fig 1. On-State Characteristics

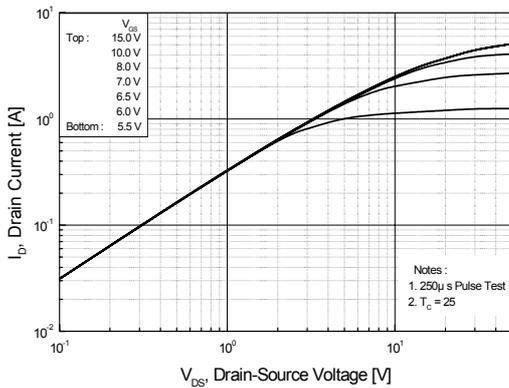


Fig 2. Transfer Characteristics

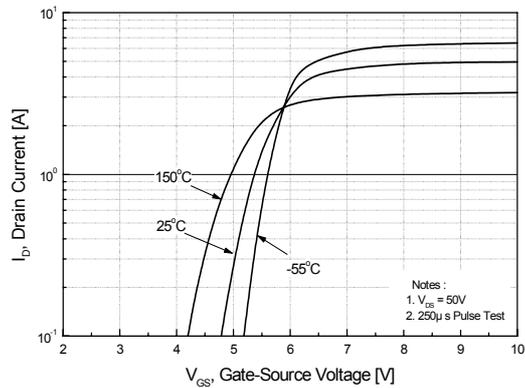


Fig 3. On Resistance Variation vs. Drain Current and Gate Voltage

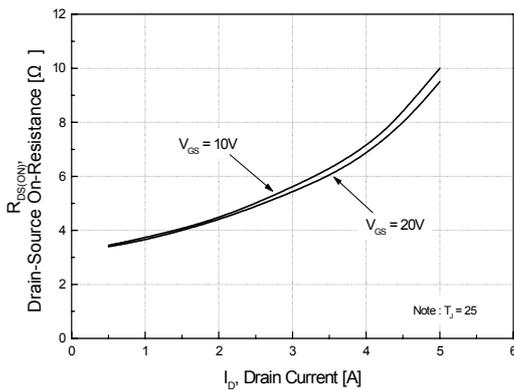


Fig 4. On State Current vs. Allowable Case Temperature

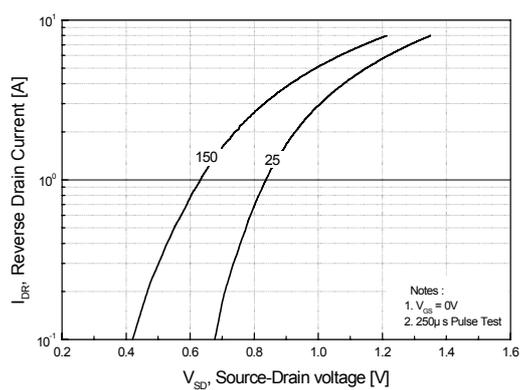


Fig 5. Capacitance Characteristics (Non-Repetitive)

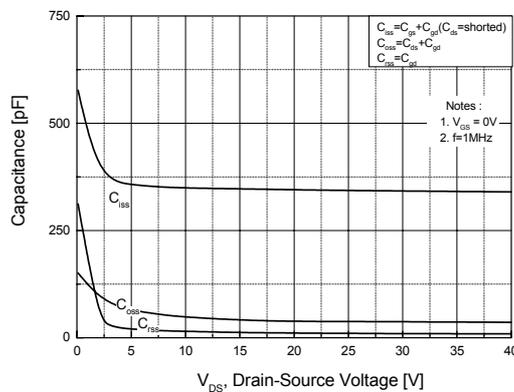
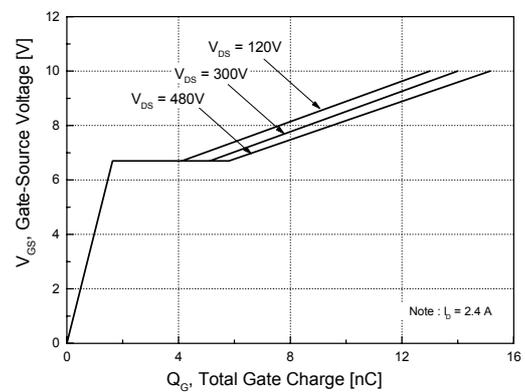


Fig 6. Gate Charge Characteristics



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Fig 7. Breakdown Voltage Variation vs. Junction Temperature

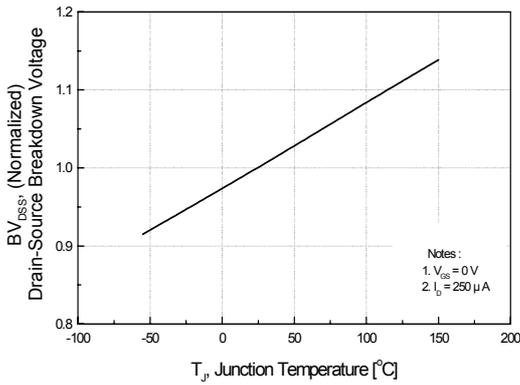


Fig 8. On-Resistance Variation vs. Junction Temperature

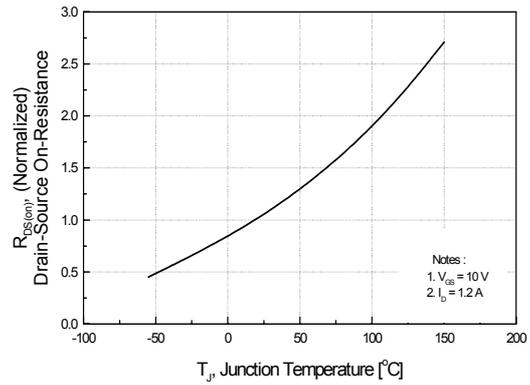


Fig 9. Maximum Safe Operating Area

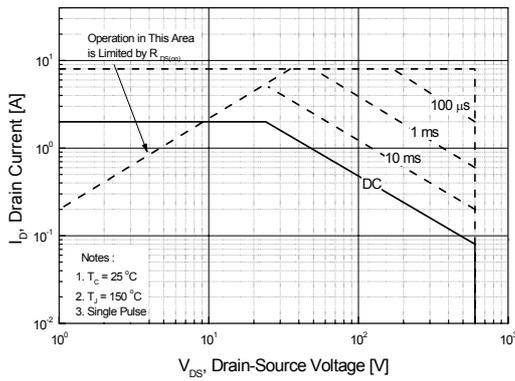


Fig 10. Maximum Drain Current

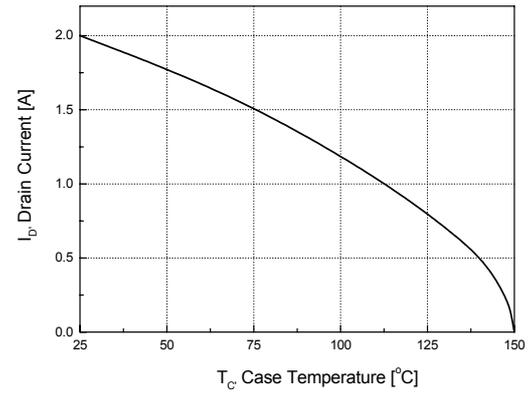
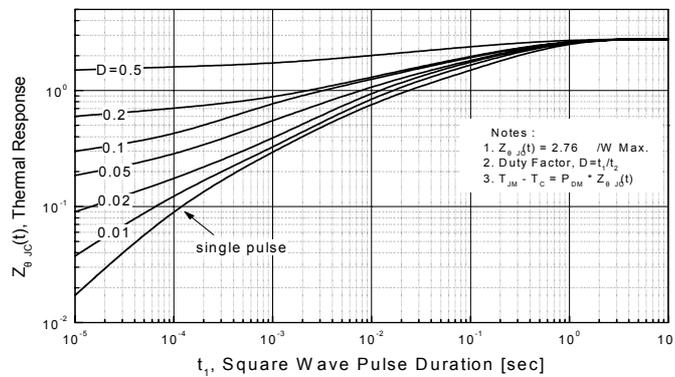


Fig 11. Transient Thermal Response Curve



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Fig. 12. Gate Charge Test Circuit & Waveforms

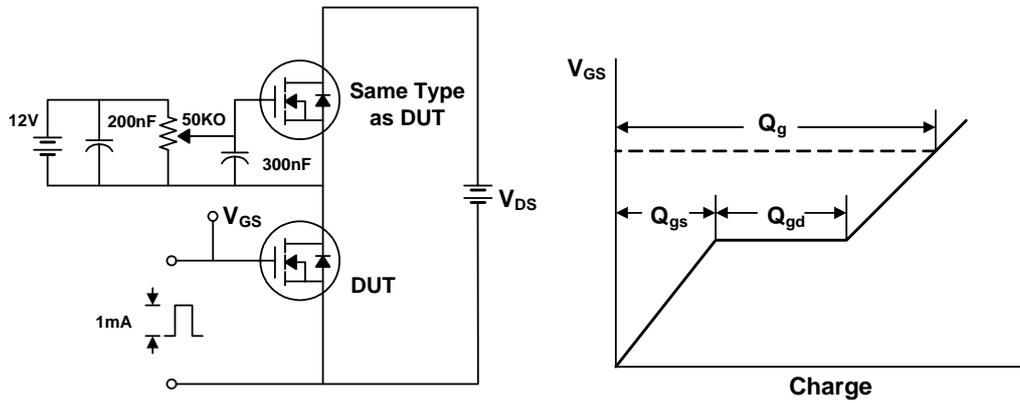


Fig 13. Switching Time Test Circuit & Waveforms

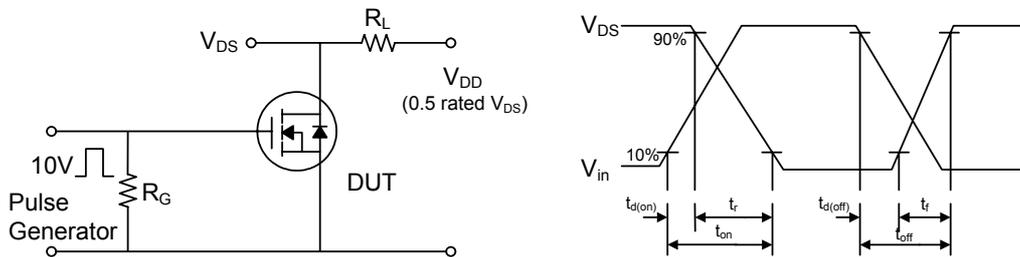
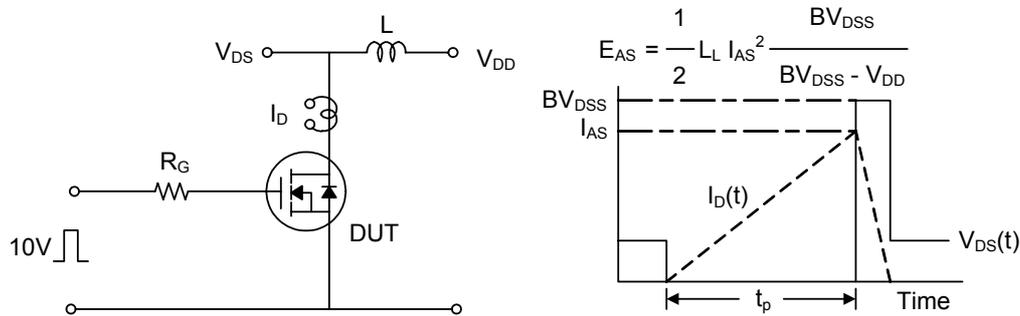
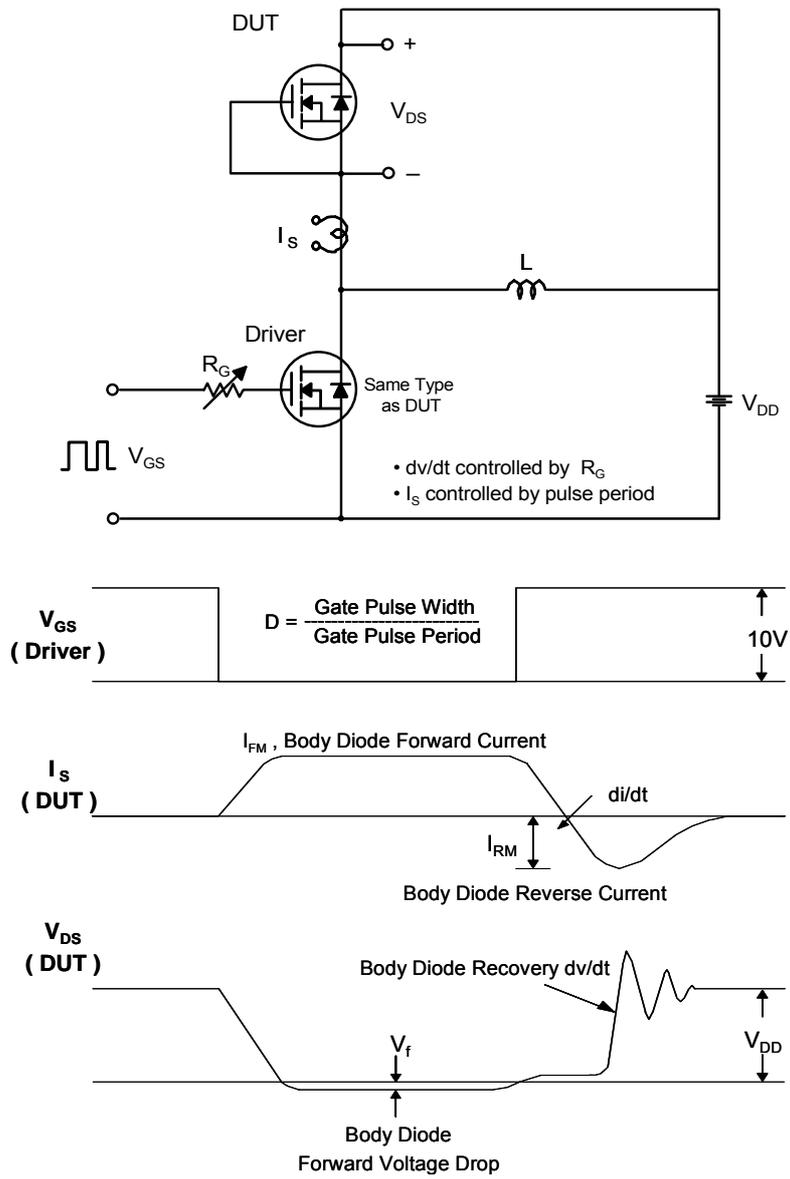


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms



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Fig. 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



DFD2N60

TO-252(D-PAK) Package Dimension

Dim.	mm			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	6.48	6.604	6.73	0.255	0.26	0.265
B	5.0	5.08	5.21	0.197	0.2	0.205
C	7.42	7.8	8.18	0.292	0.307	0.322
D	2.184	2.286	2.388	0.086	0.09	0.094
E	0.762	0.813	0.864	0.03	0.032	0.034
F	1.016	1.067	1.118	0.04	0.042	0.044
G		2.286			0.09	
H		2.286			0.09	
I	0.534	0.61	0.686	0.021	0.024	0.027
J	1.016	1.067	1.118	0.04	0.042	0.044
K		0.508			0.02	
L		0.762			0.03	
		1.57			0.06	

