

A6841

DABiC-5 8-Bit Serial Input Latched Sink Drivers

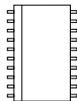
Package A
18-pin DIP



Package LW
18-pin Wide Body SOIC



Package LW-20
20-pin Wide Body SOIC



ABSOLUTE MAXIMUM RATINGS

Output Voltage	
V_{CE}	50 V
$V_{CE(SUS)}$ (for inductive load applications)	35 V
Logic Supply Voltage, V_{DD}	7 V
Emitter Supply Voltage, V_{EE}	-20 V
Input Voltage Range, V_{IN}	-0.3 V to $V_{DD}+0.3$ V
Continuous Output Current (each output), I_{OUT} ...	500 mA
Package Power Dissipation, P_D , see chart, page 6	
Operating Temperature Range	
Ambient Temperature, T_A	-20°C to +85°C
Storage Temperature, T_S	-55°C to +150°C

Caution: CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static-electrical charges.

The merging of low-power CMOS logic and bipolar output power drivers permit the A6841 integrated circuits to be used in a wide variety of peripheral power driver applications. Each device has an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sinking Darlington output drivers. The 500 mA NPN Darlington outputs, with integral transient-suppression diodes, are suitable for use with relays, solenoids, and other inductive loads.

All package variations of the A6841 offer premium performance with a minimum output-breakdown voltage rating of 50 V (35 V sustaining). All drivers can be operated with a split supply where the negative supply is up to -20 V.

The CMOS inputs are compatible with standard CMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, drivers can be cascaded for interface applications requiring additional drive lines.

The A6841SA devices are furnished in a standard 18-pin plastic DIP. The A6841SLW device is available in an 18-lead SOIC package. A 20-pin SOIC version, A6841SLW-20 has improved thermal characteristics. The SOIC drivers are also available for operation to a temperature of -40°C (part number suffix *ELW*). These devices are lead (Pb) free, with 100% matte tin plated leadframes.

FEATURES

- 3.3 V to 5 V logic supply range
- Power on reset (POR)
- To 10 MHz data input rate
- CMOS, TTL compatible inputs
- -40°C operation available
- Low-power CMOS logic and latches
- Schmitt trigger inputs for improved noise immunity
- High-voltage current-sink outputs
- Internal pull-up/pull down resistors
- Output transient-protection diodes
- Single or split supply operation

APPLICATIONS

- Relays
- Solenoids
- Inductive loads

Use the following complete part numbers when ordering:

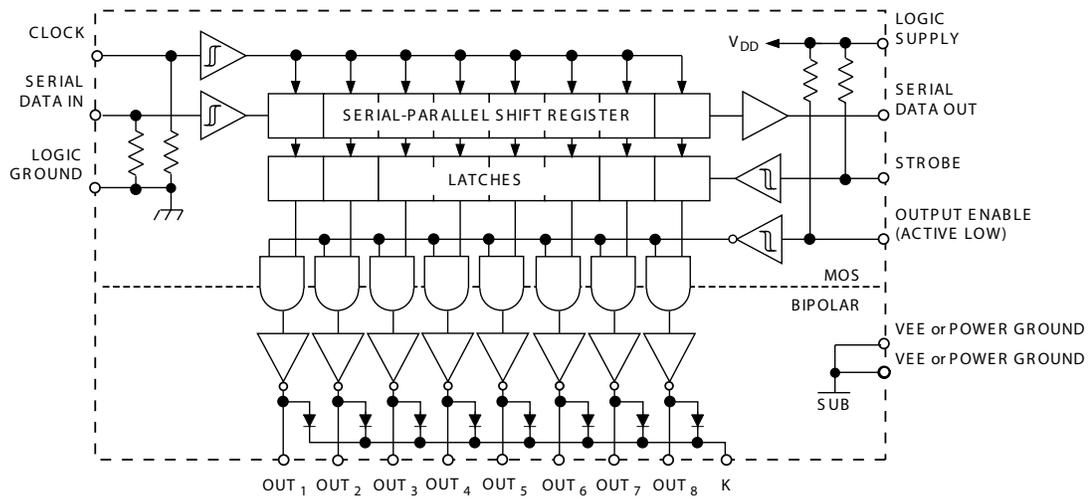


Part Number	Package	Ambient
A6841SA-T	18-pin DIP	-20°C to +85°C
A6841SLW-T	18-pin wide body SOIC	-20°C to +85°C
A6841SLW-20-T	20-pin wide body SOIC (enhanced thermals)	-20°C to +85°C
A6841ELW-T	18-pin wide body SOIC	-40°C to +85°C
A6841ELW-20-T	20-pin wide body SOIC (enhanced thermals)	-40°C to +85°C

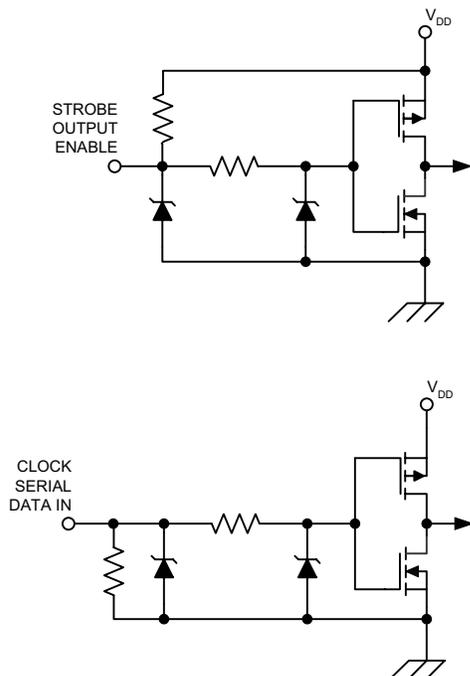
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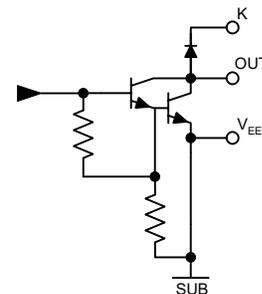
Functional Block Diagram



Typical Input Circuits



Typical Output Driver



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ELECTRICAL CHARACTERISTICS¹ Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{ee} = 0\text{ V}$, logic supply operating voltage $V_{dd} = 3.0\text{ V to }5.5\text{ V}$

Characteristic	Symbol	Test Conditions	$V_{dd} = 3.3\text{ V}$			$V_{dd} = 5\text{ V}$			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{OUT} = 50\text{ V}$	–	–	10	–	–	10	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	$I_{OUT} = 350\text{ mA}$, $L = 3\text{ mH}$	35	–	–	35	–	–	V
Collector–Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\text{ mA}$	–	–	1.1	–	–	1.1	V
		$I_{OUT} = 200\text{ mA}$	–	–	1.3	–	–	1.3	V
		$I_{OUT} = 350\text{ mA}$	–	–	1.6	–	–	1.6	V
Input Voltage	$V_{IN(1)}$		2.2	–	–	3.3	–	–	V
	$V_{IN(0)}$		–	–	1.1	–	–	1.7	V
Input Resistance	R_{IN}		50	–	–	50	–	–	k Ω
Serial Data Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -200\ \mu\text{A}$	2.8	3.05	–	4.5	4.75	–	V
	$V_{OUT(0)}$	$I_{OUT} = 200\ \mu\text{A}$	–	0.15	0.3	–	0.15	0.3	V
Maximum Clock Frequency ²	f_c		10	–	–	10	–	–	MHz
Logic Supply Current	$I_{DD(1)}$	One output on, OE = L, ST = H	–	–	2.0	–	–	2.0	mA
	$I_{DD(0)}$	All outputs off, OE = H, ST = H, P1 through P8 = L	–	–	100	–	–	100	μA
Clamp Diode Leakage Current	I_r	$V_r = 50\text{ V}$	–	–	50	–	–	50	μA
Clamp Diode Forward Voltage	V_f	$I_f = 350\text{ mA}$	–	–	2	–	–	2	V
Output Enable-to-Output Delay	$t_{dis(BQ)}$	$V_{CC} = 50\text{ V}$, $R_1 = 500\ \Omega$, $C_1 \leq 30\text{ pF}$	–	–	1.0	–	–	1.0	μs
	$t_{en(BQ)}$	$V_{CC} = 50\text{ V}$, $R_1 = 500\ \Omega$, $C_1 \leq 30\text{ pF}$	–	–	1.0	–	–	1.0	μs
Strobe-to-Output Delay	$t_{p(STH-QL)}$	$V_{CC} = 50\text{ V}$, $R_1 = 500\ \Omega$, $C_1 \leq 30\text{ pF}$	–	–	1.0	–	–	1.0	μs
	$t_{p(STH-QH)}$	$V_{CC} = 50\text{ V}$, $R_1 = 500\ \Omega$, $C_1 \leq 30\text{ pF}$	–	–	1.0	–	–	1.0	μs
Output Fall Time	t_f	$V_{CC} = 50\text{ V}$, $R_1 = 500\ \Omega$, $C_1 \leq 30\text{ pF}$	–	–	1.0	–	–	1.0	μs
Output Rise Time	t_r	$V_{CC} = 50\text{ V}$, $R_1 = 500\ \Omega$, $C_1 \leq 30\text{ pF}$	–	–	1.0	–	–	1.0	μs
Clock-to-Serial Data Out Delay	$t_{p(CH-SQX)}$	$I_{OUT} = \pm 200\ \mu\text{A}$	–	50	–	–	50	–	ns

¹Positive (negative) current is defined as conventional current going into (coming out of) the specified device pin.

²Operation at a clock frequency greater than the specified minimum value is possible but not warranted.

Truth Table

Serial Data Input	Clock Input	Shift Register Contents				Serial Data Output	Strobe Input	Latch Contents				Output Enable Input	Output Contents					
		I_1	I_2	I_3	... I_8			I_1	I_2	I_3	... I_8		I_1	I_2	I_3	... I_8		
H		H	R_1	R_2	... R_7	R_7												
L		L	R_1	R_2	... R_7	R_7												
X		R_1	R_2	R_3	... R_8	R_8												
		X	X	X	... X	X	L	R_1	R_2	R_3	... R_8							
		P_1	P_2	P_3	... P_8	P_8	H	P_1	P_2	P_3	... P_8	L	P_1	P_2	P_3	... P_8		
								X	X	X	... X	H	H	H	... H			

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State

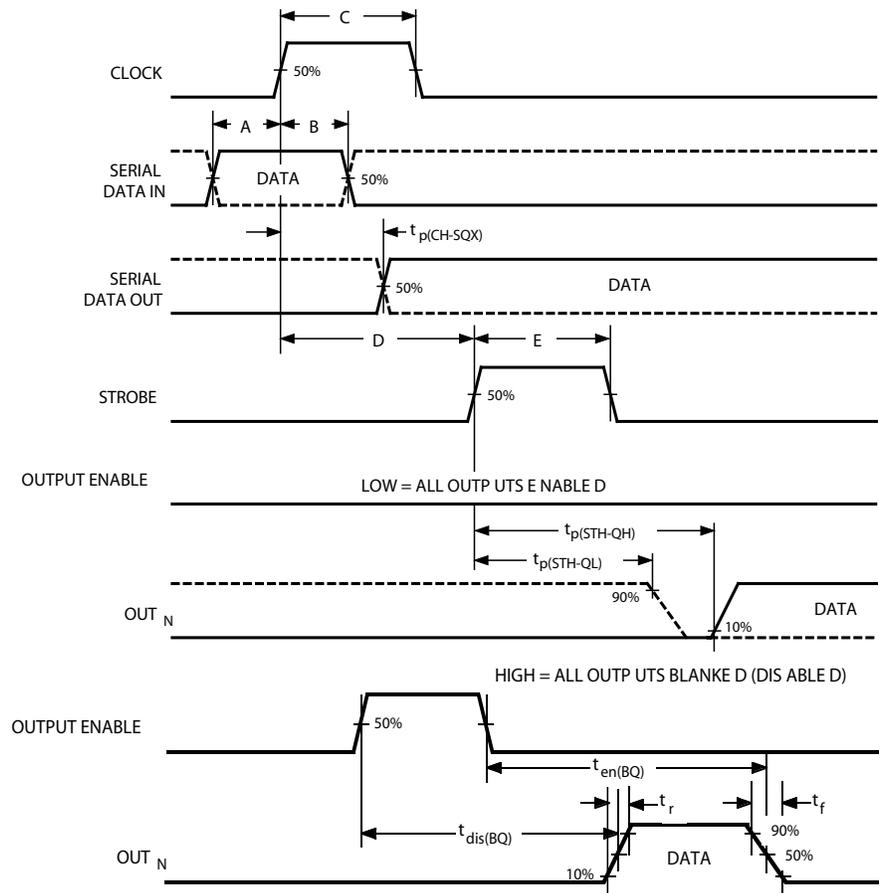
R = Previous State
OE = Output Enable
ST = Strobe

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Timing Requirements and Specifications

(Logic Levels are V_{DD} and Ground)



Key	Description	Symbol	Time (ns)
A	Data Active Time Before Clock Pulse (Data Set-Up Time)	$t_{su(D)}$	25
B	Data Active Time After Clock Pulse (Data Hold Time)	$t_{h(D)}$	25
C	Clock Pulse Width	$t_{w(CH)}$	50
D	Time Between Clock Activation and Strobe	$t_{su(C)}$	100
E	Strobe Pulse Width	$t_{w(STH)}$	50

NOTE: Timing is representative of a 10 MHz clock. Higher speeds may be attainable; operation at high temperatures will reduce the specified maximum clock frequency.

Powering-on with the inputs in the low state ensures that the registers and latches power-on in the low state (POR).

Serial Data present at the input is transferred to the shift register on the logical 0 to logical 1 transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

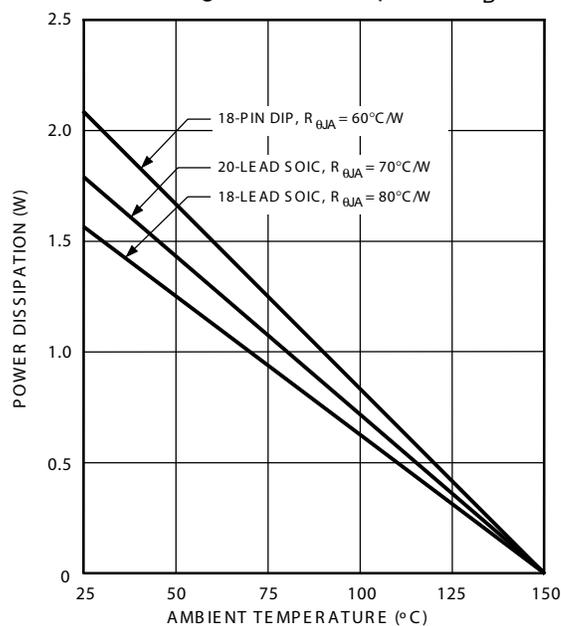
When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF). The information stored in the latches or shift register is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

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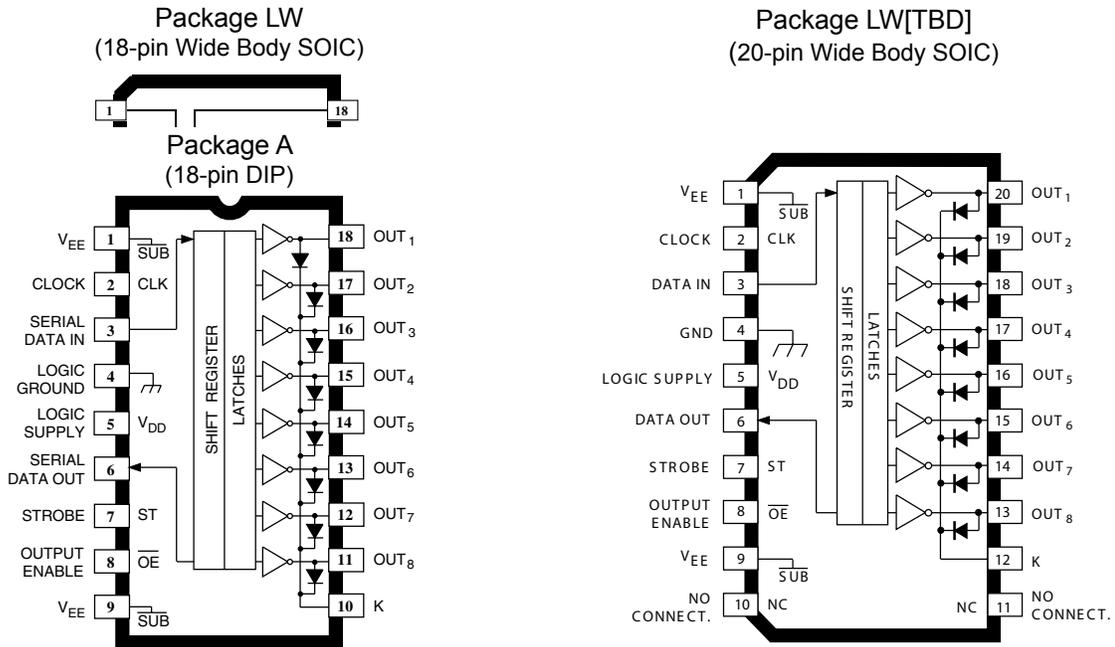
Terminal List Table

Name	Description	Pin	
		18-pin	20-pin
VEE	Power Ground to substrate	1, 9	1, 9
CLK	Clock	2	2
DATA IN	Serial Data In	3	3
GND	Logic Ground	4	4
V _{DD}	Logic Supply	5	5
DATA OUT	Serial Data Out, for cascading devices	6	6
ST	Strobe	7	7
\overline{OE}	Output Enable (active low)	8	8
K	Common to +V _L , for inductive loads	10	12
NC	Not connected	–	10, 11
OUT ₈	Sink Output 8	11	13
OUT ₇	Sink Output 7	12	14
OUT ₆	Sink Output 6	13	15
OUT ₅	Sink Output 5	14	16
OUT ₄	Sink Output 4	15	17
OUT ₃	Sink Output 3	16	18
OUT ₂	Sink Output 2	17	19
OUT ₁	Sink Output 1	18	20

Allowable Package Power Dissipation, P_D

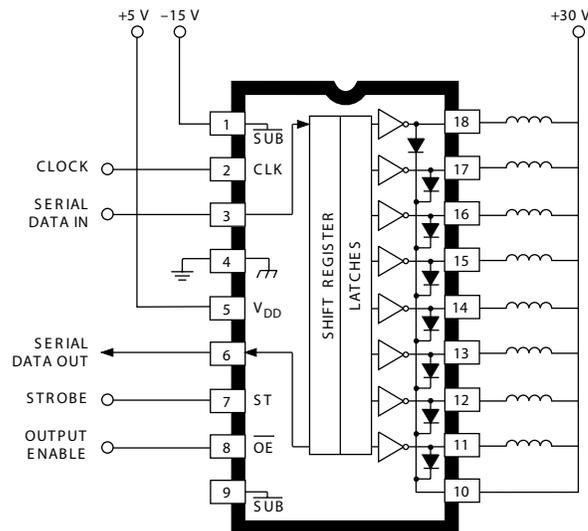
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Note the 18-pin DIP package and the SOIC packages are electrically identical and share common terminal number assignments.

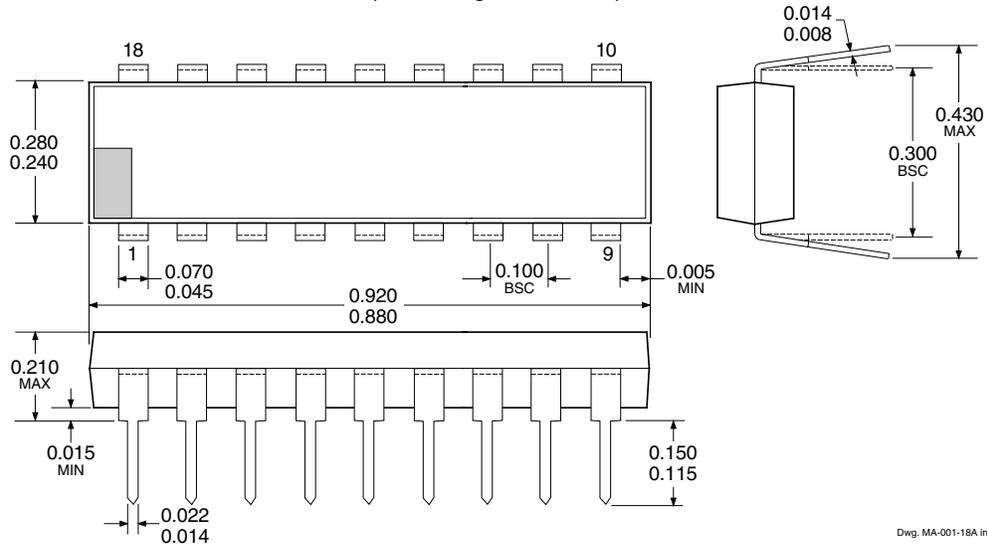
Typical Application Relay/solenoid driver using split supply



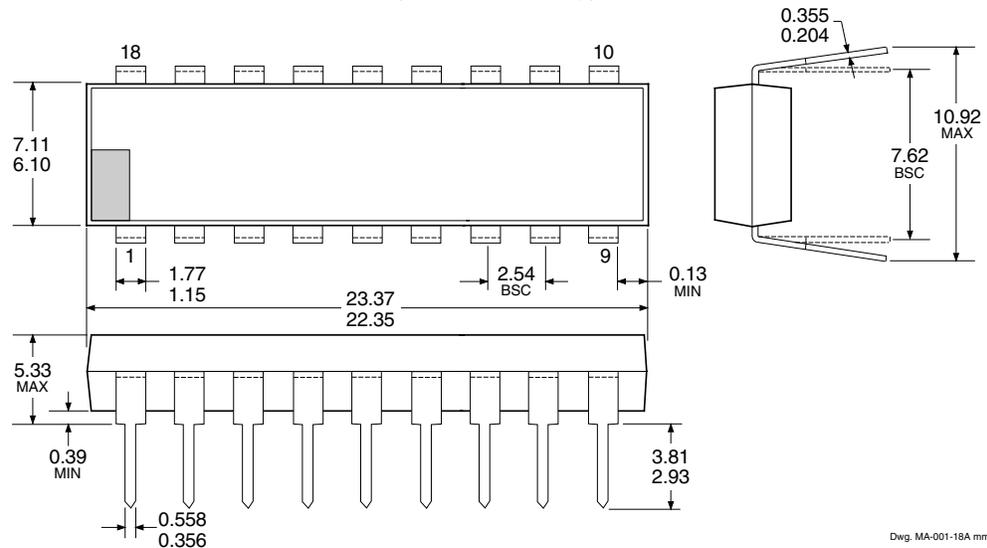
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Package A 18-pin DIP

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only)



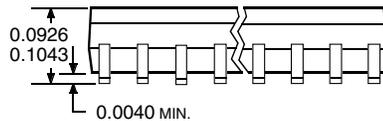
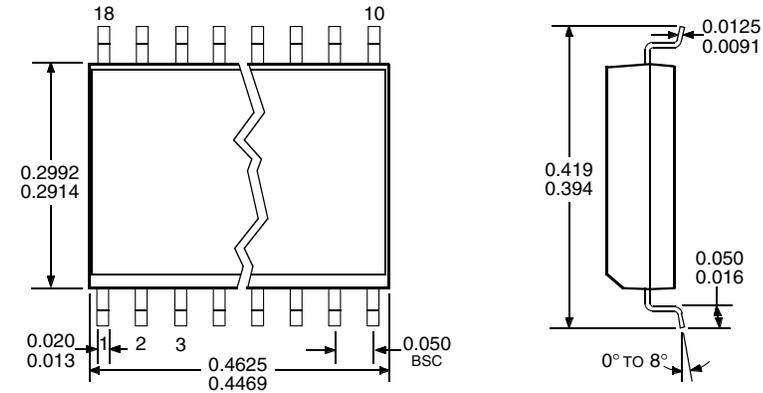
- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
 2. Lead spacing tolerance is non-cumulative.
 3. Lead thickness is measured at seating plane or below.

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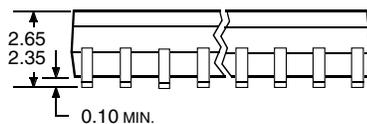
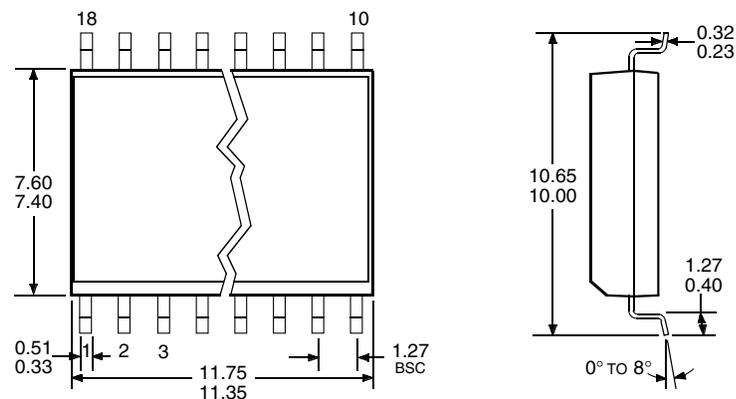
Package LW 18-pin Wide Body SOIC

Dimensions in Inches
(for reference only)



Dwg. MA-008-18A in

Dimensions in Millimeters
(controlling dimensions)



Dwg. MA-008-18A mm

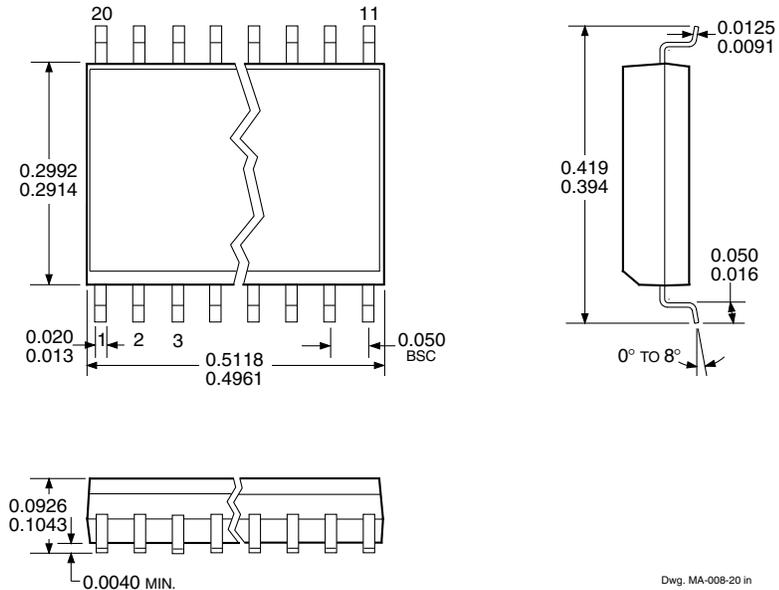
- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

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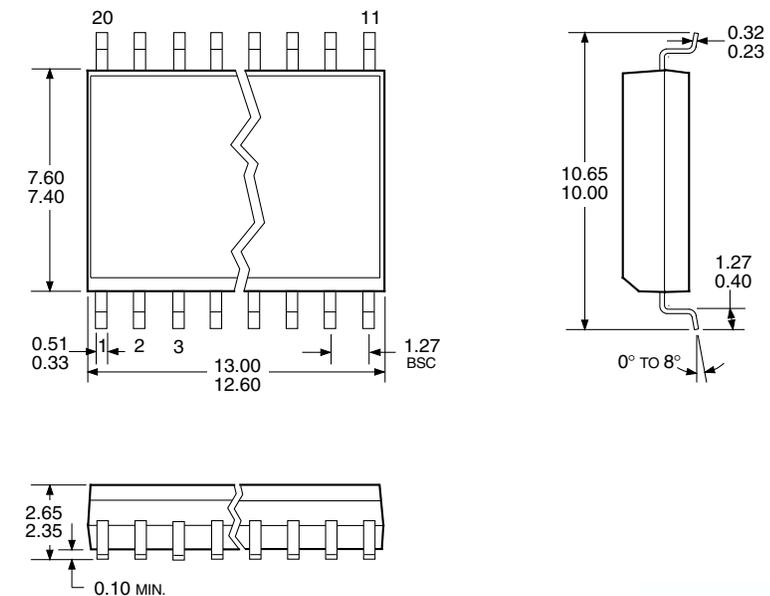
DABiC-5 8-Bit Serial Input Latched Sink Drivers

Package LW-20 20-pin Wide Body SOIC

Dimensions in Inches
(for reference only)



Dimensions in Millimeters
(controlling dimensions)



- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

A6841 *DABiC-5 8-Bit Serial Input Latched Sink Drivers*

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