I²C BUS - Controlled 11-Input 3-Output Audio Switch
Monolithic IC MM1631

Outline

This is an I²C BUS controlled audio switch developed for use in TVs, PDP and projection TVs.

It can switch among 11 audio signal (R, L) lines and 3 output lines.

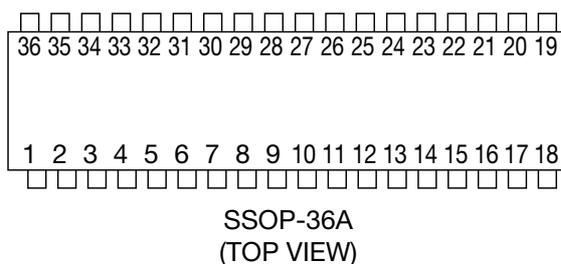Input switching block design is simple when this IC and MM1630 (video switch) are used as a pair.

Features

1. The desired input can be selected for each of the 3 independent output lines.
2. Wide dynamic range (3vrms).
3. Serial control possible through I²C BUS.
4. Forced mute enabled by external pin.
5. Built-in Power Save function.
6. I²C BUS line maintains high impedance when power is off.
7. No output waveform folding with 7.1Vrms input

Package

SSOP-36A

Pin Assignment

```
   36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19

    1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18
```

SSOP-36A
(TOP VIEW)

1	L3	10	R7	19	BIAS	28	L$_{OUT}$2
2	R3	11	L8	20	MUTE	29	R$_{OUT}$1
3	L4	12	R8	21	ADR	30	L$_{OUT}$1
4	R4	13	L9	22	SDA	31	V$_{CC}$
5	L5	14	R9	23	SCL	32	V$_{CC}$
6	R5	15	L10	24	GND	33	L1
7	L6	16	R10	25	R$_{OUT}$3	34	R1
8	R6	17	L11	26	L$_{OUT}$3	35	L2
9	L7	18	R11	27	R$_{OUT}$2	36	R2

Block Diagram
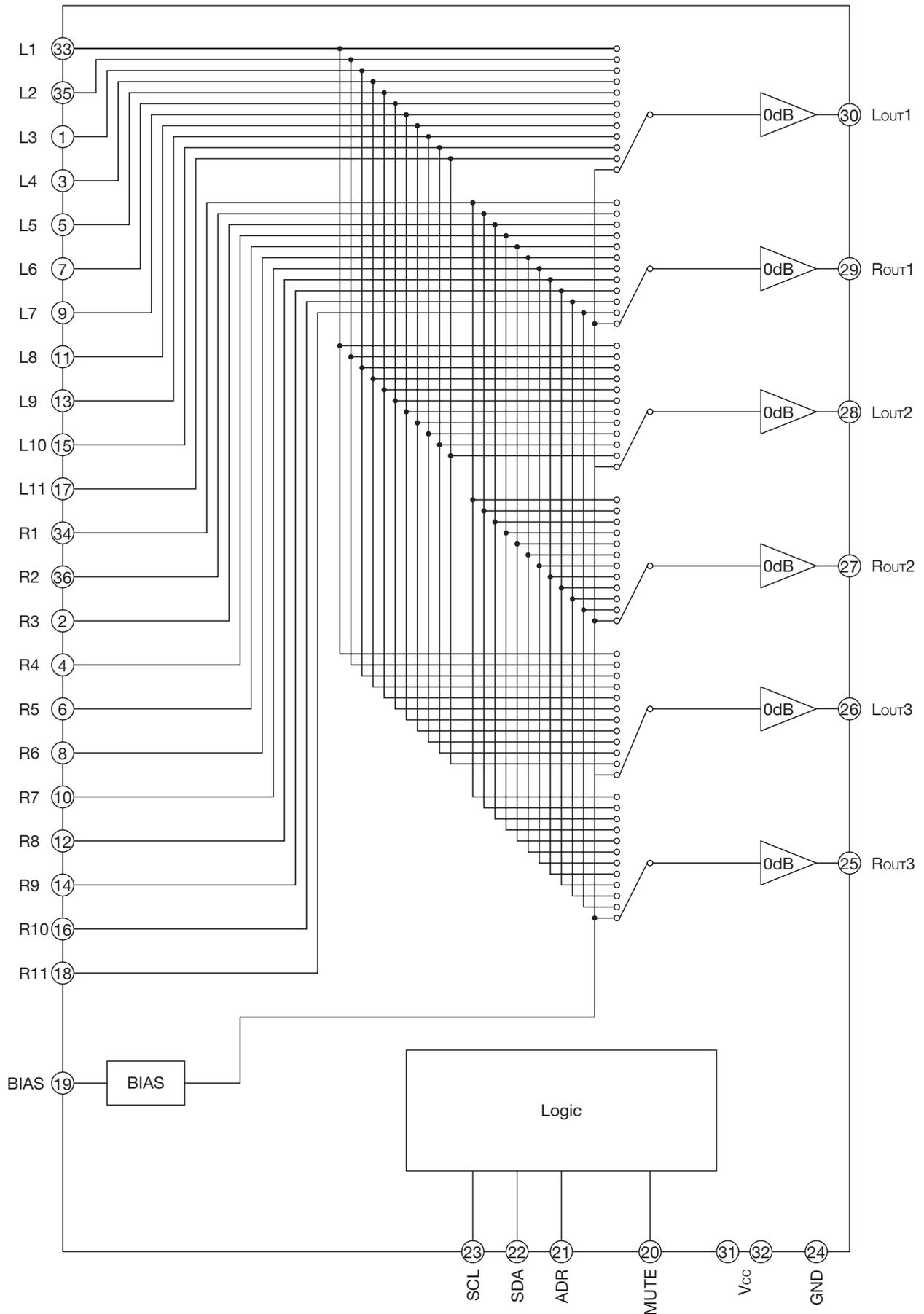
Pin Description

Pin no.	Pin name	Functions	Internal equivalent circuit diagram
1~18 33~36	L1~L11 R1~R11	Line input of Audio	
25~30	Lout1~3 Rout1~3	Line output of Audio	
21	ADR	Slave address select pin	
22	SDA	Data input of I²C BUS	
23	SCL	CLK input of I²C BUS	

Pin no.	Pin name	Function	Internal equivalent circuit diagram
20	MUTE	Mute select pin	V_{CC} MUTE
19	BIAS	Connect 22μF between this pin and CND for stabilize internal reference voltage	V_{CC} 25k BIAS 25k
31 32	V_{CC}	V_{CC}	
24	GND	GND	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	−65~+150	°C
Operating temperature	T_{OPR}	−40~+85	°C
Supply voltage	V_{CC} max.	−0.2~+13	V
I/0 terminal voltage	V_{IN} max. V_{OUT} max.	−0.2~V_{CC}+0.2	V
Output current	I_{OUT} max.	25	mA
Junction temperature	Tj max.	150	°C
Allowable loss *1	Pd	1.0	W

Note: *1   Board mounting power dissipation. Board size 100×100×1.6mm
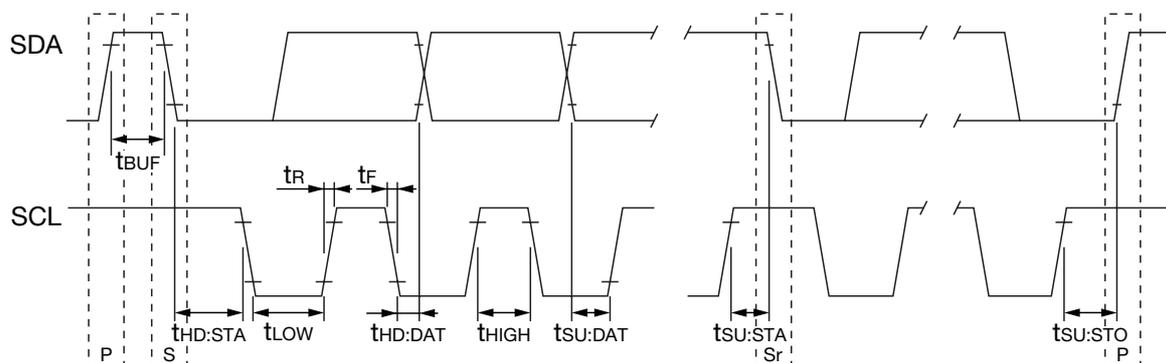
Recommended Operating Conditions

| Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}	−40~+85	°C
Operating voltage	V_{CCOP}	+8.0~+10.0	V
Operating I/0 voltage	V_{INOP} V_{OUTOP}	0~V_{CC}	V

Electrical Characteristics (Except where noted otherwise, Ta=25°C, Vcc=9V, SW1 ON, SW2 OFF, SW3 ON)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Current consumption	I_{CC0}	No signal , No Load		35	46	mA
Current of power-save 1	I_{CC1}	OUT1 (or OUT2): Power-Save OUT2 (or OUT1)&3: Active		28	37	mA
Current of power-save 2	I_{CC2}	OUT1 & 2: Power-Save OUT3: Active		21	28	mA
Voltage gain	G_V	SG: 1Vrms, 1kHz	−0.5	0	0.5	dB
Frequency characteristic	FBW	SG: 1Vrms, 50kHz	−3			dB
Total harmonic distortion	THD	SG: 1Vrms, 1kHz		0.03	0.05	%
Input dynamic range	DR	f=1kHz, THD=0.5%	2.8	3.0		Vrms
Crosstalk	CT	SG: 1Vrms, f=1kHz, Without power-save mode		−90	−80	dB
Rippler rejection	PSRR	Vr: 100mVrms, 100kHz SW1 OFF, SW2 ON, SW3 OFF		−50	−40	dB
Output offset voltage	V_{OFF}	V_{OUT} (Active)−V_{OUT} (Mute)	−15	0	15	mV
S/N ratio	S/N	SG: 1Vrms, 1kHz, A curve		−100	−90	dB
Input impedance of input terminal	Z_{IN}		47	60	73	kΩ
Input terminal voltage	V_{IN}	No signal , No Load	4.25	4.50	4.75	V
Output terminal voltage	V_{OUT}	No signal , No Load	4.25	4.50	4.75	V
Audio signal input voltage	V_{SG}	No output signal turnup			7.1	Vrms
I²C condition						
Input voltage L	V_{IL}		0.0		0.8	V
Input voltage H	V_{IH}		2.2		5.0	V
SDA low level output voltage	V_{OL}	SDA sink 3mA	0.0		0.4	V
High level input current	I_{IH}	SDA, SCL=4.5V	−10		10	μA
Low level input current	I_{IL}	SDA, SCL=0.4V	−10		10	μA
Clock frequency	f_{SCL}				100	kHz
Data transfer wait time	t_{BUF}		4.7			μs
SCL start hold time	$t_{HD;STA}$		4.0			μs
SCL low level hold time	t_{LOW}		4.7			μs
SCL high level hold time	t_{HIGH}		4.0			μs
Start condition setup time	$t_{SU;STA}$		4.7			μs
SDA data hold time	$t_{HD;DAT}$		200			ns
SDA data setup time	$t_{SU;DAT}$		250			ns
SDA, SCL rise time	t_R				1000	ns
SDA, SCL fall time	t_F				300	ns
Stop condition setup time	$t_{SU;STO}$		4.0			μs

Note   I²C condition

Measuring Circuit
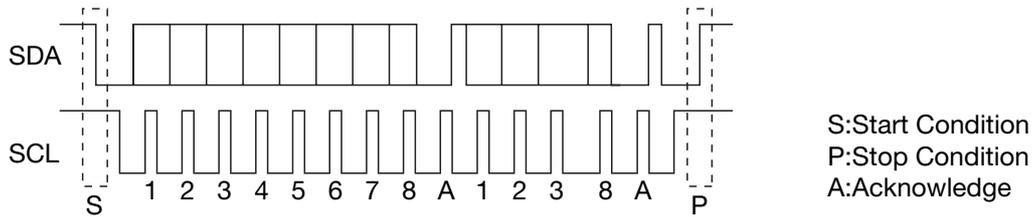

SG: Input signal
TP: Test pin

I²C BUS

S:Start Condition
P:Stop Condition
A:Acknowledge
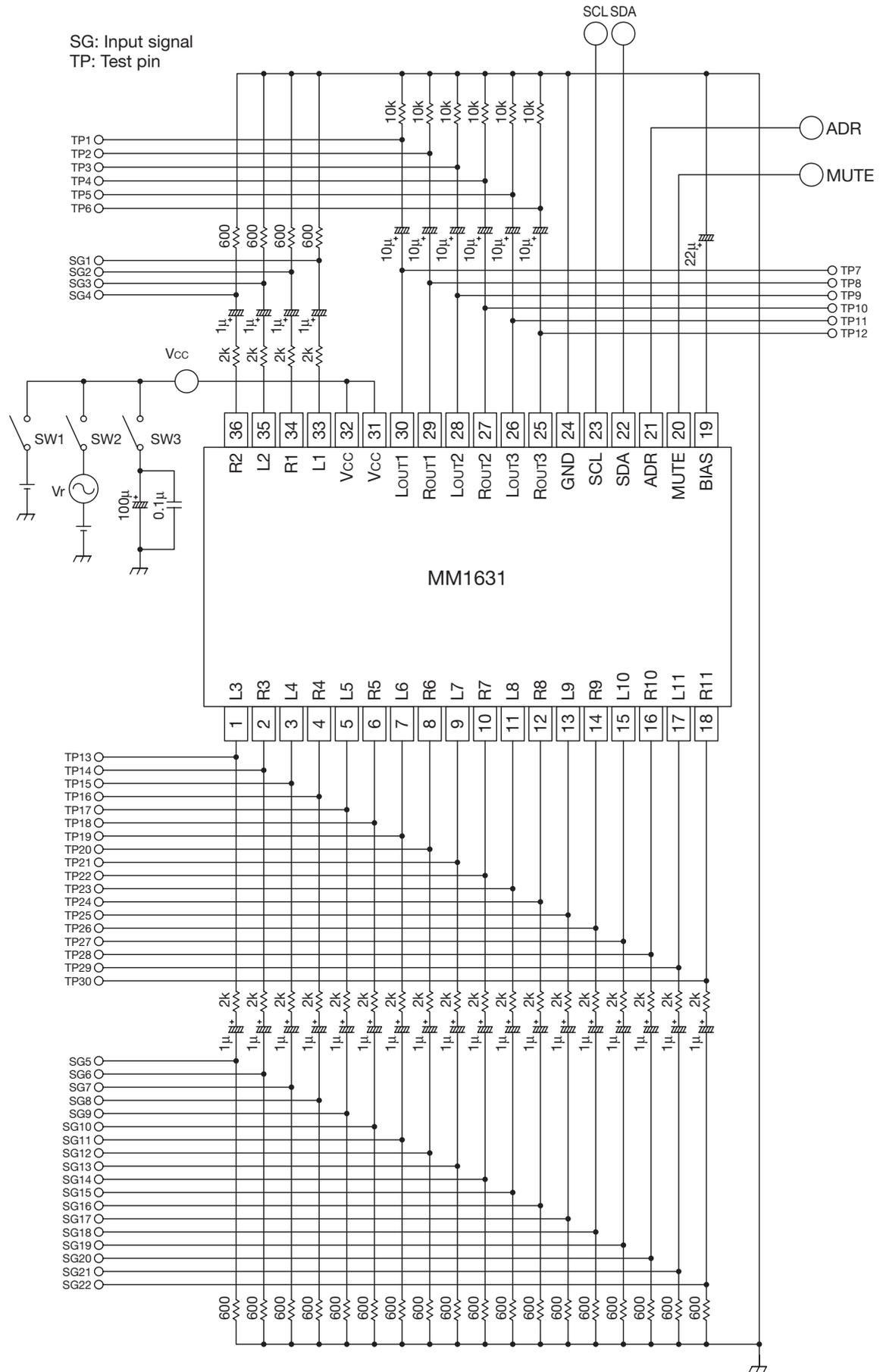
I²C BUS is inter bus system controlled by 2 lines (SDA, SCL).

Data are transmitted and received in the units of byte and acknowledge.

It is transmitted by MSB first from the start conditions.

[Control registers]

Control registers are data sent from the master for determining the switch conditions.

The data format is set as shown in the following figure.
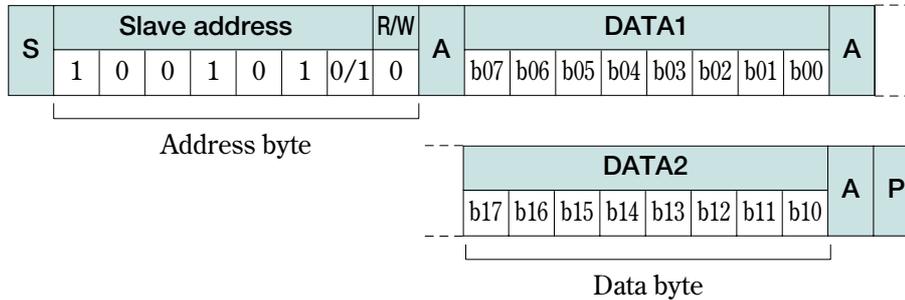
Out of the Address byte, first 7bit are assigned to the slave address,while the residual

1bit is assigned to the R/W bit.

Set the R/W bit to 0 when data are used control registers.

As MM1631 slave address, either 94H or 96H can be selected according to the ADR

terminal conditions. When ADR terminal is L94H is selected.

The relationship between each bit of the control register and the switch controls are as shown in the figure.

Each bit of control registers is reset to 0, when power-on.)

No.	DATA condition							
DATA1 (00H)	b07	b06	b05	b04	b03	b02	b01	b00
	L1, R2 line select				L1, R2 line select			
DATA2 (00H)	b17	b16	b15	b14	b13	b12	b11	b10
			Power Save (OUT2)	Power Save (OUT2)	L3, R3 line select			

MM1631 consists of one address byte and two control data bytes (3 bytes in total).

All data over the limited length (4th and subsequent bytes) are fully neglected.

For details of the control contents of switches, refer to the another table.

Switch Control Table

■ L1, R1 OUT select

b03	b02	b01	b00	L1, R1 OUT
0	0	0	0	Mute
0	0	0	1	L1, R1
0	0	1	0	L2, R2
0	0	1	1	L3, R3
0	1	0	0	L4, R4
0	1	0	1	L5, R5
0	1	1	0	L6, R6
0	1	1	1	L7, R7
0	0	0	0	L8, R8
1	0	0	1	L9, R9
1	0	1	0	L10, R10
1	0	1	1	L11, R11
1	1	0	0	Mute
1	1	0	1	Mute
1	1	1	0	Mute
1	1	1	1	Mute

■ L2, R2 OUT select

b07	b06	b05	b04	L2, R2 OUT
0	0	0	0	Mute
0	0	0	1	L1, R1
0	0	1	0	L2, R2
0	0	1	1	L3, R3
0	1	0	0	L4, R4
0	1	0	1	L5, R5
0	1	1	0	L6, R6
0	1	1	1	L7, R7
0	0	0	0	L8, R8
1	0	0	1	L9, R9
1	0	1	0	L10, R10
1	0	1	1	L11, R11
1	1	0	0	Mute
1	1	0	1	Mute
1	1	1	0	Mute
1	1	1	1	Mute

■ L3, R3 OUT select

b13	b12	b11	b10	L3, R3 OUT
0	0	0	0	Mute
0	0	0	1	L1, R1
0	0	1	0	L2, R2
0	0	1	1	L3, R3
0	1	0	0	L4, R4
0	1	0	1	L5, R5
0	1	1	0	L6, R6
0	1	1	1	L7, R7
0	0	0	0	L8, R8
1	0	0	1	L9, R9
1	0	1	0	L10, R10
1	0	1	1	L11, R11
1	1	0	0	Mute
1	1	0	1	Mute
1	1	1	0	Mute
1	1	1	1	Mute

■ Power Save select

b15	b14	L2, R2 OUT	L1, R1 OUT
0	0	Active	Active
0	1	Active	Power Save
1	0	Power Save	Active
1	1	Power Save	Power Save

[Status registers]
There is no preparation of th status register in MM1631. A status register returns all the 1
when 1 is set in the R/W bit. At this time, the control of each SW is not done at all.

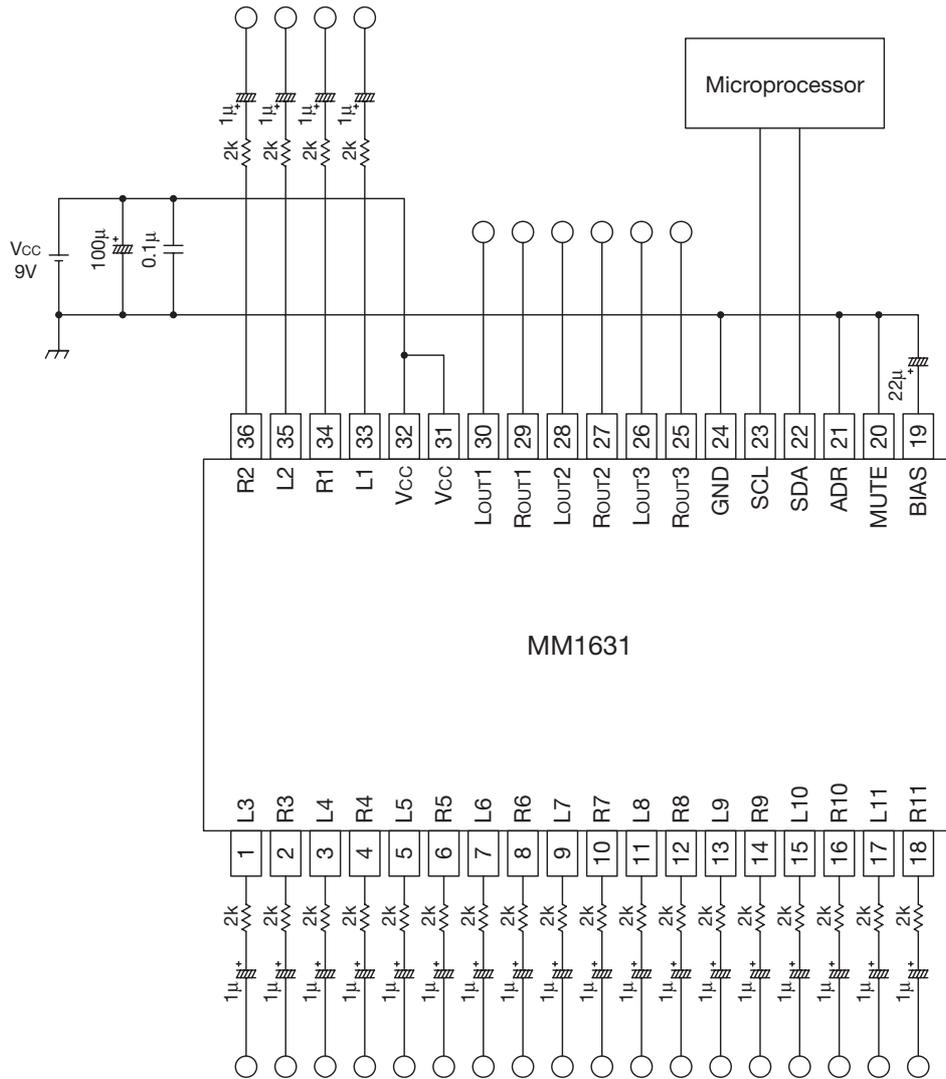| S	Slave address						R/W	A	DATA								A	P
	1	0	0	1	0	1	0/1 1		1	1	1	1	1	1	1	1		

Address byte   Status byte
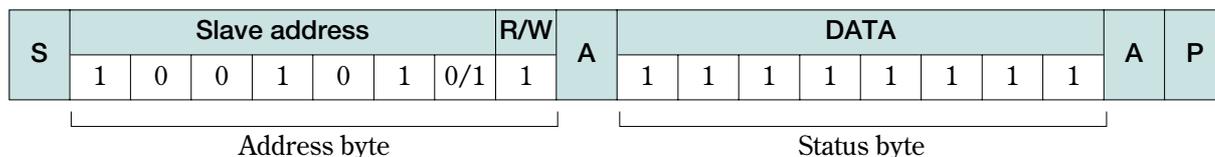
·Mute terminal operation
 All of audio output is connected with internal bias-voltage when Mute terminal is "H". And when
 Mute level return from "H" to "L" , audio output selections return to previous conditions.
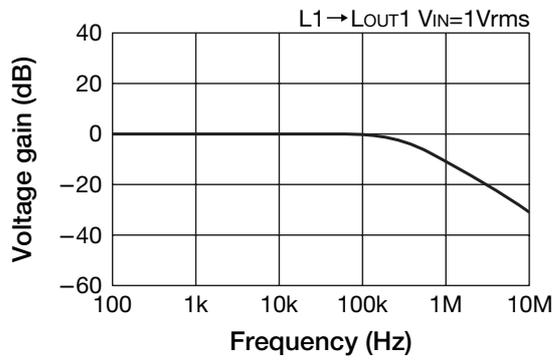
■ Mute select

Mute	Output
H	Mute
L	Active

Application Circuit

Characteristics

■ **Frequency characteristic**

L1→LOUT1 VIN=1Vrms

Voltage gain (dB) vs Frequency (Hz)

■ **THD VS Input voltage**

L1→LOUT1 f=1kHz

THD (%) vs Input voltage (Vrms)