FLI8125 LF-BC

PRELIMINARY Datasheet

ADVANCE INFORMATION – SUBJECT TO CHANGE

GENESIS MICROCHIP CONFIDENTIAL

C8125-DAT-05A

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1 Overview

The FLI8125 is a cost-effective, highly-integrated, mixed signal solution for TV and Digital Video applications. Capable of meeting global market requirements, the FLI8125 incorporates a multi-standard video decoder, high-speed triple 8-bit Analog-to-Digital Converter (ADC), and front end switching. An integrated VBI Slicer adds Closed Captioning (CC) and Teletext service support, and the built-in microprocessor enables full system control without external devices.

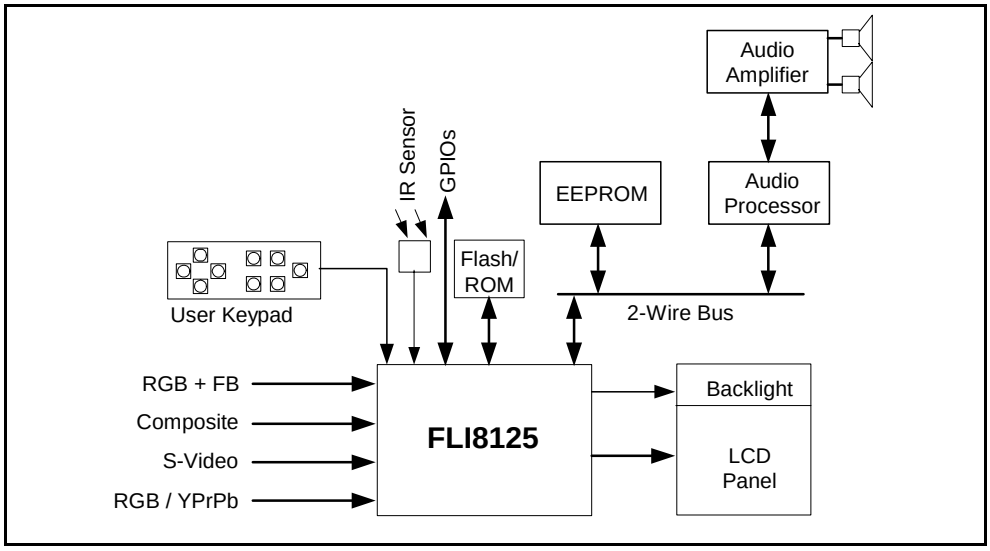
The FLI8125 can capture and process both video and RGB graphics streams. The multi-standard decoder is capable of accepting NTSC, PAL or SECAM and all sub-formats. The integrated ADC accepts both analog RGB and YPrPb inputs.

Interlaced video signals are converted into progressive scan using a memory-less deinterlacing technique incorporating Faroudja Edge Processing eliminating objectionable stair casing on diagonal lines. After deinterlacing, the video image is enhanced using Faroudja TrueLife™ horizontal processing resulting in an image that looks crisper and more realistic.

Adaptive Contrast and Color (ACC) enables dynamic contrast enhancement and color saturation correction. Active Color Management-II (ACM-II) enables color correction/manipulation for subtle changes in color that can dramatically improve image (e.g., Flesh Tone, Green Stretch, etc.). A fully programmable 3x3 matrix provides color space conversion and global color manipulation technology. Programmable Color Look Up Tables (CLUT) provides gamma correction of the output signal. Combined, these features facilitate accurate color reproduction that enables use of the full dynamic range on any display device.

1.1 System Design Example

Figure 1: System Design Example



1.2 Features

INTEGRATED TRIPLE ADC

- RGB / YPbPr support up to 135MHz
- SCART – RGB + Fast Blank support
- Interlaced and progressive scan
- External OSD support

DIGITAL INPUT PORT

- 24-bit re-configurable input port

INTEGRATED 2D VIDEO DECODER

- Worldwide NTSC/PAL/SECAM support
- Macrovision / VCR trick mode support

EMBEDDED MICROPROCESSOR

- Turbo 186 core
- Internal RAM / ROM
- Serial Flash / Parallel ROM support
- 2-wire slave controller, UART / JTAG support
- Internal RESET Controller
- GPIOs , Low Bandwidth ADC – 6 input
- Infra-red Interface

SCALING ENGINE

- Independent H & V scaling factors
- 4:2:2 YPbPr or 4:4:4 RGB scaling
- Anamorphic scaling (non-linear)

FAROUDJA DCDI – EDGE™

- Edge Correction
  - Eliminates objectionable stair casing
  - Enhances clarity and realism
- Horizontal Enhancement
- Adaptive Contrast and Color (ACC)
- Active Color Management - II (ACM-II)

DIGITAL OUTPUT

- 18/24-bit 85Mhz TTL output
- Dual LVDS up to SXGA
- Energy Spectrum Management for reducing EMI
- Programmable CLUT for gamma correction

OSD CONTROLLER

- Up to 4 windows: 1, 2 or 4-bits per pixel color
- Programmable Font scalar to meet Teletext requirements.

VBI SLICER

- V-Chip, Closed Captioning, XDS, CGMS, WSS decode
- Teletext 1.5 support

JTAG SUPPORT

- Boundary Scan support

2 Pin Diagram

The FLI8125 device is packaged in a 208-pin Plastic Quad Flat Pack (PQFP).

Figure 2: FLI8125 Pinout

3 Pin List

I/O Legend: A = Analog, **I** = Input, **O** = Output, **P** = Power, **G**= Ground

Note: Many pins have multiple functions. Such pins may appear under more than one of the pin function tables below. These functions may be configured through hardware control or register control.

Table 1: Analog Input Port

Pin Name	No.	I/O	Description
VDD18_AB	158	AP	Analog Power (1.8V) for A & B Channels. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
NC	159		No Connection. Leave this pin open for normal operation.
GND18_C	160	AG	Analog Ground (1.8V Return) for C channel. Must be directly connected to the analog system ground plane on board.
VDD18_C	161	AP	Analog Power (1.8V) for C Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
ADC_TEST	162	O	Analog Front End Test O/P. Leave this Pin open. Used for factory testing purpose only.
AVDD_ADC	163	AP	Analog Power (3.3V) for ADC. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
AGND	164	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
AGND	165	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV1P	166	AI	Positive analog sync input for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	167	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A1P	168	AI	Positive analog input ‘A’ for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	169	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B1P	170	AI	Positive analog input ‘B’ for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	171	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C1P	172	AI	Positive analog input ‘C’ for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_A	173	AP	Analog Power (3.3V) for ADC of Channel-A. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
AN	174	AI	Negative analog input ‘A’ for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-A Inputs. This has to be AC coupled using a series 57.6 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	175	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV2P	176	AI	Positive analog sync input for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	177	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A2P	178	AI	Positive analog input ‘A’ for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	179	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B2P	180	AI	Positive analog input ‘B’ for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	181	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C2P	182	AI	Positive analog input ‘C’ for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_B	183	AP	Analog Power (3.3V) for ADC of Channel-B. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
BN	184	AI	Negative analog input ‘B’ for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-B Inputs. This has to be AC coupled using a series 57.6 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	185	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.

Pin Name	No.	I/O	Description
SV3P	186	AI	Positive analog sync input for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	187	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A3P	188	AI	Positive analog input 'A' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	189	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B3P	190	AI	Positive analog input 'B' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	191	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C3P	192	AI	Positive analog input 'C' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_C	193	AP	Analog Power (3.3V) for ADC of Channel-C. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
CN	194	AI	Negative analog input 'C' for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-C Inputs. This has to be AC coupled using a series 57.6 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	195	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV4P	196	AI	Positive analog sync input for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	197	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A4P	198	AI	Positive analog input 'A' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	199	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B4P	200	AI	Positive analog input 'B' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	201	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C4P	202	AI	Positive analog input 'C' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_SC	203	AP	Analog Power (3.3V) for ADC of SYNC Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
SVN	204	AI	Negative analog sync input for channels 1 through 4. This acts as the return Path for the Sources connected to SV Channel Inputs. This has to be AC coupled using a series 57.6 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
VO_GND	205	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
VOUT2	206	AO	Analog VOUT signal This is the Analog Video Output from the Decoder in the Composite Video format. This can be amplified and be fed to any video display device.
VDD18_SC	207	AP	Analog Power (1.8V) for SYNC Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
GND18_SC	208	AG	Analog Ground (1.8V Return) for SYNC channel. Must be directly connected to the analog system ground plane on board.

Table 2: Low Bandwidth ADC Input Port

Pin Name	No	I/O	Description
VDDA33_LBADC	1	AP	Analog Power (3.3V) for Low Bandwidth ADC Block. Must be bypassed with 0.1uF capacitor.
LBADC_IN1	2	AI	Low Bandwidth Analog Input-1. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN2	3	AI	Low Bandwidth Analog Input-2. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN3	4	AI	Low Bandwidth Analog Input-3. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN4	5	AI	Low Bandwidth Analog Input-4. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN5	6	AI	Low Bandwidth Analog Input-5. The Input signal connected to this Pin, must be bypassed with

Pin Name	No	I/O	Description
			a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN6	7	AI	Low Bandwidth Analog Input-6. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_RTN	8	AG	This Pin provides the Return Path for LBADC inputs. Must be directly connected to the analog system ground plane on board.
VSSA33_LBADC	9	AG	Analog Ground for Low Bandwidth ADC Block. Must be directly connected to the analog system ground plane on board.

Table 3: RCLK PLL Pins

Pin Name	No	I/O	Description
GND_RPLL	11	DG	Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane.
VDD_RPLL_18	12	DP	Digital power (1.8V) for ADC digital logic. Must be bypassed with capacitor to Ground Plane.
VBUFC_RPLL	13	O	Test Output. Leave this Pin Open. This is reserved for Factory Testing Purpose.
AGND_RPLL	14	AG	Analog ground for the Reference DDS PLL. Must be directly connected to the analog system ground plane.
XTAL	15	AO	Crystal oscillator output. Connect to external crystal.
TCLK	16	AI	Reference clock (TCLK) from the 19.6608 MHz crystal oscillator. Connect to external crystal/ oscillator.
AVDD_RPLL_33	17	AP	Analog Power (3.3V) for RCLK PLL. Must be bypassed with 0.1uF capacitor.

Table 4: Digital Video Input Port

Pin Name	No	I/O	Description
VID_CLK_1	153	I	Video port data clock input meant for Video Input – 1. Up to 135Mhz [Input, 5V-tolerant]
VIDIN_HS	122	I	When Video Input – 1 is in BT656 Mode, this Pin acts as Horizontal Sync Input for Video Input – 2. OR when Video Input – 1 is in 16 Bit Mode this Pin acts as Horizontal Sync Input for Video Input – 1. OR this Pin acts as Horizontal Sync Input for 24 Bit Video Input
VIDIN_VS	121	I	When Video Input – 1 is in BT656 Mode, this Pin acts as Vertical Sync Input for Video Input – 2. OR when Video Input – 1 is in 16 Bit Mode this Pin acts as Vertical Sync Input for Video Input – 1. OR this Pin acts as Vertical Sync Input for 24 Bit Video Input
VID_DATA_IN_0 VID_DATA_IN_1 VID_DATA_IN_2 VID_DATA_IN_3 VID_DATA_IN_4 VID_DATA_IN_5 VID_DATA_IN_6 VID_DATA_IN_7	135 136 137 138 139 140 141 142	IO	Input YUV data in 8-bit BT656 of Video Input – 1 [Bi-Directional, 5V-tolerant] OR Input Y Data in case of 16 Bit Video Input (CCIR601) of Video Input – 1 OR Input Green Data in case of 24 Bit Video Input
VID_DATA_IN_8 VID_DATA_IN_9 VID_DATA_IN_10 VID_DATA_IN_11 VID_DATA_IN_12 VID_DATA_IN_13 VID_DATA_IN_14 VID_DATA_IN_15	145 146 147 148 149 150 151 152	IO	Input Pr / Pb Data in case of 16 Bit Video Input (CCIR601) of Video Input – 1 OR Input Blue/ Pb Data in case of 24 Bit Video Input
VID_DATA_IN_16 VID_DATA_IN_17 VID_DATA_IN_18 VID_DATA_IN_19 VID_DATA_IN_20 VID_DATA_IN_21 VID_DATA_IN_22	123 124 125 128 129 130 131	IO	Input Red / Pr Data in case of 24 Bit Video Input OR Video Input – 2 in 8-bit with Embedded Sync / Separate Sync

Pin Name	No	I/O	Description
VID_DATA_IN_23	132		
VID_CLK2	118	I	Video port data clock input meant for Video Input – 2. Up to 135Mhz [Input, 5V-tolerant]
VID_DE/FLD	115	I	Video Active Signal Input or the Field Signal Input from external Digital Video Source.

Note: In case of Multiple Digital Video Input Sources, only one digital source can be in separate sync mode format. Other digital inputs should be in embedded sync (656) format.

Table 5: System Interface

Pin Name	No	I/O	Description
RESETn	10	I	Hardware Reset (active low) [Schmitt trigger, 5v-tolerant] Connect to ground with 0.01uF capacitor.
TEST	20	I	For normal mode of operation connect this Pin to Ground. Has an internal pulldown resistor of 50 K ohm.
GPIO15	21	IO	This pin is available as a general-purpose input/output port. Also it is optionally programmable to give out the external chip select signal meant for external SRAM. Connect pullup resistor to supply if external SRAM used. It is also address line A19 when 1MB parallel flash is used.
JTAG_BS_ENn	22	I	JTAG Boundary Scan enabling pin. Has an internal pulldown resistor of 50 K ohm. If this pin is left open or pulled down, Boundary Scan Mode is enabled. If this pin is pulled high, Boundary Scan functionality is not available, and pins 34~37 are available as GPIO 0~3
SCART16	23	I	This pin can be programmed to sense the Fast Blank Input signal from a SCART I/P source
HOST_SCLK	24	IO	Host input clock or 186 UART Data In or JTAG clock signal. [Input, Schmitt trigger, 5V-tolerant]
HOST_SDATA	25	IO	Host input data or 186 UART Data Out or JTAG mode signal. [Bi-directional, Schmitt trigger, slew rate limited, 5V-tolerant]
DDC_SCLK	26	IO	DDC2Bi clock for VGA Port
DDC_SDATA	27	IO	DDC2Bi data for VGA Port
MSTR_SCLK	30	O	Clock signal from Master Serial 2 Wire Interface Controller
MSTR_SDATA	31	IO	Data signal meant for Master Serial 2 Wire interface Controller
GPIO0/TCK	34	IO	This Pin accepts the Input Clock signal in case of Boundary Scan Mode. Else, this pin is available as General Purpose Input/output Port.
GPIO1/TDI	35	IO	This Pin accepts the Input Data signal in case of Boundary Scan Mode. Else, this pin is available as General Purpose Input/output Port.
GPIO2/TMS	36	IO	This Pin accepts the Input Test Mode Select signal in case of Boundary Scan Mode. Else, this pin is available as General Purpose Input/output Port.
GPIO3/TRST	37	IO	This Pin accepts the Boundary Scan Reset signal in case of Boundary Scan Mode. Else, this pin is available as General Purpose Input/output Port.
GPIO6/IRin	38	IO	Input from Infra Red Decoder can be connected to this Pin. Else, this pin is available as General Purpose Input/output Port.
GPIO7/IRQin	41	IO	Input Interrupt Request signal can be connected to this Pin. Else, this pin is available as General Purpose Input/output Port.
GPIO8/IRQout	42	IO	This Pin will give out the Interrupt Signal to interrupt external Micro. Else, this pin is available as General Purpose Input/output Port.
GPIO9/SIPC_SCLK	43	IO	This Pin accepts the Clock signal from External Serial 2 Wire interface Bus if FLI8125 is programmed to be in Slave mode. Else, this pin is available as General Purpose Input/output Port.
GPIO10/SIPC_SDATA/ A18	44	IO	This Pin acts as the Data I/O signal when used with External Serial 2 Wire interface Bus if FLI8125 is programmed to be in Slave mode. Or this Pin is programmable to give out Address line 18 from the Internal Micro when used with 512K External Memory. Else, this pin is available as General Purpose Input/output Port.
GPIO11/PWM0	47	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. Else, this pin is available as General Purpose Input/output Port.
GPIO12/PWM1	48	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. Else, this pin is available as General Purpose Input/output Port.

Pin Name	No	I/O	Description
GPIO13/PWM2	51	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. Else, this pin is available as General Purpose Input/output Port.
GPIO14/PWM3/ SCART16	52	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. Or it can be programmed to sense the Fast Blank Input signal from a SCART I/P source. Else, this pin is available as General Purpose Input/output Port.
TDO	55	O	This Pin provides the Output Data in case of Boundary Scan Mode.
HSYNC1	156	I	Horizontal Sync signal Input-1. Used when Analog RGB component signal carries separate HSYNC signal. Has programmable Schmitt trigger.
VSYNC1	157	I	Vertical Sync signal Input-1. Used when Analog RGB component signal carries separate VSYNC signal. Has programmable Schmitt trigger.
XOSD_CLK	101	O	Clock Output meant for External OSD Controller
XOSD_HS	102	O	Horizontal Sync Output meant for External OSD Controller
XOSD_VS	103	O	Vertical Sync Output meant for External OSD Controller
XOSD_FLD	104	O	Field Signal Output meant for External OSD Controller
PD20/B4/GPIO0 PD21/B5/GPIO1 PD22/B6/GPIO2 PD23/B7/GPIO3	86 87 88 89	IO	These Pins provide the Panel Data as shown in the TTL Display Interface Table below. These are available as General Purpose Input / Output Pins when not used as Panel Data.

Table 6: LVDS Display Interface

Pin Name	No	I/O	Description
PBIAS	53	O	Panel Bias Control (backlight enable) [Tri-state output, 5V- tolerant]
PPWR	54	O	Panel Power Control [Tri-state output, 5V- tolerant]
AVDD_LV_33	56	DP	Digital Power for LVDS Block. Connect to digital 3.3V supply.
VCO_LV	57	O	Reserved. Output for Testing Purpose only at Factory.
AVSS_LV	58	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	59	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.
CH3P_LV_E	60	O	These form the Differential Data Output for Channel – 3 (Even).
CH3N_LV_E	61	O	
CLKP_LV_E	62	O	These form the Differential Clock Output Even Channel.
CLKN_LV_E	63	O	
CH2P_LV_E	64	O	These form the Differential Data Output for Channel – 2 (Even).
CH2N_LV_E	65	O	
CH1P_LV_E	66	O	These form the Differential Data Output for Channel – 1 (Even).
CH1N_LV_E	67	O	
CH0P_LV_E	68	O	These form the Differential Data Output for Channel – 0 (Even).
CH0N_LV_E	69	O	
AVSS_OUT_LV	70	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	71	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.
CH3P_LV_O	72	O	These form the Differential Data Output for Channel – 3 (Odd).
CH3N_LV_O	73	O	
CLKP_LV_O	74	O	These form the Differential Clock Output Odd Channel.
CLKN_LV_O	75	O	
CH2P_LV_O	76	O	These form the Differential Data Output for Channel – 2 (Odd).
CH2N_LV_O	77	O	
CH1P_LV_O	78	O	These form the Differential Data Output for Channel – 1 (Odd).
CH1N_LV_O	79	O	
CH0P_LV_O	80	O	These form the Differential Data Output for Channel – 0 (Odd).
CH0N_LV_O	81	O	

Pin Name	No	I/O	Description
AVSS_OUT_LV	82	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	83	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.

Table 7: TTL Display Interface

Pin Name	No	I/O	Description For 8-bit panels	For 6-bit panels
PBIAS	53	O	Panel Bias Control (backlight enable) [Tri-state output, 5V- tolerant]	
PPWR	54	O	Panel Power Control [Tri-state output, 5V- tolerant]	
AVDD_LV_33	56	DP	Digital Power for TTL Block. Connect to digital 3.3V supply.	
VCO_LV	57	O	Reserved. Output for Testing Purpose only at Factory.	
AVSS_LV	58	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	59	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
R0	60	O	Red channel bit 0 (Even)	Not used.
R1	61	O	Red channel bit 1 (Even)	Not used.
R2	62	O	Red channel bit 2 (Even)	Red channel bit 0 (Even)
R3	63	O	Red channel bit 3 (Even)	Red channel bit 1 (Even)
R4	64	O	Red channel bit 4 (Even)	Red channel bit 2 (Even)
R5	65	O	Red channel bit 5 (Even)	Red channel bit 3 (Even)
R6	66	O	Red channel bit 6 (Even)	Red channel bit 4 (Even)
R7	67	O	Red channel bit 7 (Even)	Red channel bit 5 (Even)
G0	68	O	Green channel bit 0 (Even)	Not used.
G1	69	O	Green channel bit 1 (Even)	Not used.
AVSS_OUT_LV	70	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	71	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
G2	72	O	Green channel bit 2 (Even)	Green channel bit 0 (Even)
G3	73	O	Green channel bit 3 (Even)	Green channel bit 1 (Even)
G4	74	O	Green channel bit 4 (Even)	Green channel bit 2 (Even)
G5	75	O	Green channel bit 5 (Even)	Green channel bit 3 (Even)
G6	76	O	Green channel bit 6 (Even)	Green channel bit 4 (Even)
G7	77	O	Green channel bit 7 (Even)	Green channel bit 5 (Even)
B0	78	O	Blue channel bit 0 (Even)	Not used.
B1	79	O	Blue channel bit 1 (Even)	Not used.
B2	80	O	Blue channel bit 2 (Even)	Blue channel bit 0 (Even)
B3	81	O	Blue channel bit 3 (Even)	Blue channel bit 1 (Even)
AVSS_OUT_LV	82	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	83	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
PD20/B4	86	O	Blue channel bit 4 (Even)	Blue channel bit 2 (Even)
PD21/B5	87	O	Blue channel bit 5 (Even)	Blue channel bit 3 (Even)
PD22/B6	88	O	Blue channel bit 6 (Even)	Blue channel bit 4 (Even)
PD23/B7	89	O	Blue channel bit 7 (Even)	Blue channel bit 5 (Even)
DEN	90	O	Display Data Enable	
DHS	91	O	Display Horizontal Sync.	
DVS	92	O	Display Vertical Sync.	
DCLK	93	O	Display Pixel Clock	
PD24	115	O	Red channel bit 0 (Odd)	Not used.
PD25	114	O	Red channel bit 1 (Odd)	Not used.
PD26	113	O	Red channel bit 2 (Odd)	Red channel bit 0 (Odd)
PD27	112	O	Red channel bit 3 (Odd)	Red channel bit 1 (Odd)

Pin Name	No	I/O	Description For 8-bit panels	For 6-bit panels
PD28	111	O	Red channel bit 4 (Odd)	Red channel bit 2 (Odd)
PD29	110	O	Red channel bit 5 (Odd)	Red channel bit 3 (Odd)
PD30	109	O	Red channel bit 6 (Odd)	Red channel bit 4 (Odd)
PD31	108	O	Red channel bit 7 (Odd)	Red channel bit 5 (Odd)
PD32	107	O	Green channel bit 0 (Odd)	Not used.
PD33	106	O	Green channel bit 1 (Odd)	Not used.
PD34	105	O	Green channel bit 2 (Odd)	Green channel bit 0 (Odd)
PD35	104	O	Green channel bit 3 (Odd)	Green channel bit 1 (Odd)
PD36	103	O	Green channel bit 4 (Odd)	Green channel bit 2 (Odd)
PD37	102	O	Green channel bit 5 (Odd)	Green channel bit 3 (Odd)
PD38	101	O	Green channel bit 6 (Odd)	Green channel bit 4 (Odd)
PD39	123	O	Green channel bit 7 (Odd)	Green channel bit 5 (Odd)
PD40	124	O	Blue channel bit 0 (Odd)	Not used.
PD41	125	O	Blue channel bit 1 (Odd)	Not used.
PD42	128	O	Blue channel bit 2 (Odd)	Blue channel bit 0 (Odd)
PD43	129	O	Blue channel bit 3 (Odd)	Blue channel bit 1 (Odd)
PD44	130	O	Blue channel bit 4 (Odd)	Blue channel bit 2 (Odd)
PD45	131	O	Blue channel bit 5 (Odd)	Blue channel bit 3 (Odd)
PD46	132	O	Blue channel bit 6 (Odd)	Blue channel bit 4 (Odd)
PD47	118	O	Blue channel bit 7 (Odd)	Blue channel bit 5 (Odd)

Note: In case of 24 Bit TTL Panels the RGB Odd Channel Outputs will not be used. In that case they can be made available for other purposes as Address & Data from On-Chip Micro or Digital Video Input Data.

Table 8: Parallel/Serial ROM/ SRAM Interface

Pin Name	No	I/O	Description
A19	21	O	Address Signal A19 for 1M X 8 PROM. This pin also acts as Chip select for external SRAM when PROM of 512KB or less is used. Else this pin acts as GPIO15.
A18	44	O	Address Signal A18 for 512K X 8 PROM / SRAM. Else this pin acts as GPIO10.
A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	95 96 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115	O	256K x8 PROM /SRAM Address. Some of these pins also have bootstrap functionality. For serial SPI ROM interface: - ROM_ADDR17 will be Serial Clock (ROM_SCLK) - ROM_ADDR16 will be Serial Data Output (ROM_SDO)
D7 D6 D5 D4 D3 D2 D1 D0	132 131 130 129 128 125 124 123	IO	External PROM / SRAM data input.

ROM_OEN	118	O	External PROM / SRAM data Output Enable.
ROM_SDI/ ROM_WEN	97	O	External PROM / SRAM data Write Enable (for In-System-Programming of FLASH) or Serial Data Input (SDI) for SPI ROM interface.
ROM_SCSN/ ROM_CSN	94	O	External PROM / SRAM data Chip Select or Serial PROM Chip Select (ROM_SCSN) for SPI ROM interface.

Note: External SRAM is supported only with parallel ROM. Serial ROM and external SRAM cannot be used together.

Table 9: Digital Power and Ground

Pin Name	No	I/O	Description
RVDD_3.3	32 49 98 116 154	P	Ring VDD. Connect to digital 3.3V.
CVDD_1.8	18 28 39 45 84 119 126 133 143	P	Core VDD. Connect to digital 1.8V.
CRVSS	19 29 33 40 46 50 85 99 117 120 127 134 144 155	G	Chip ground for core and ring.

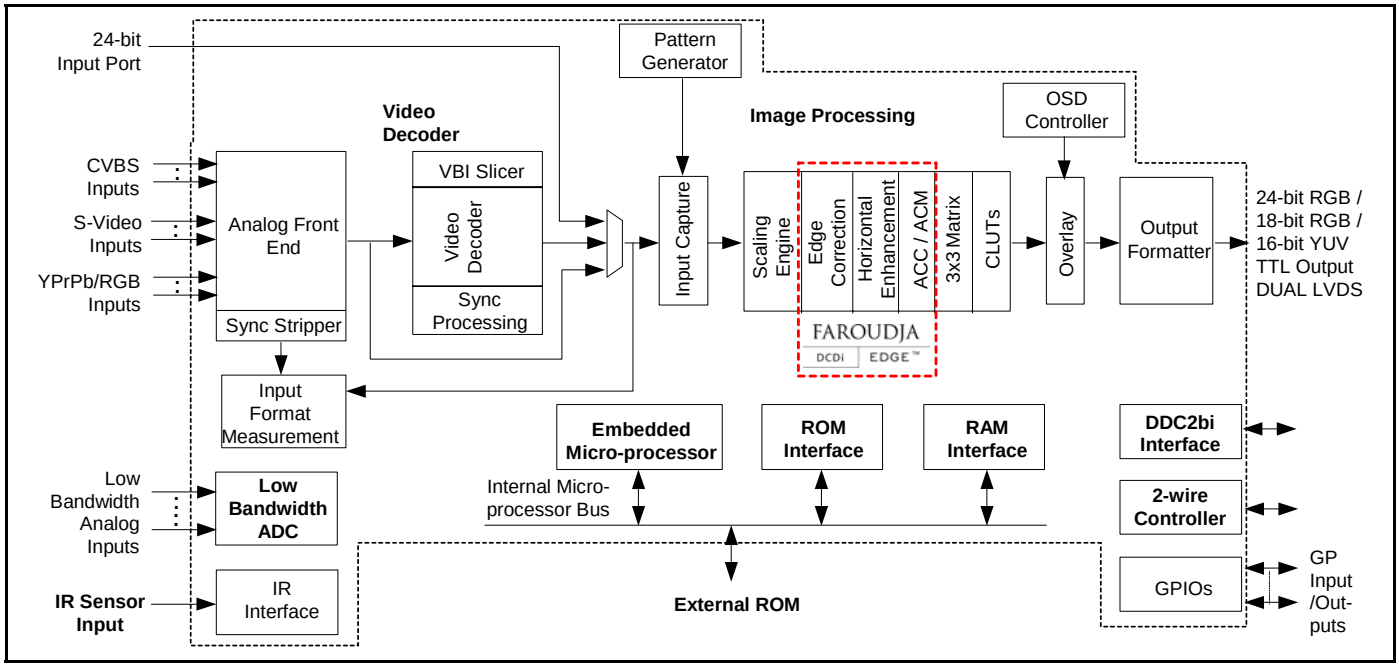
Table 10: JTAG Boundary Scan

Pin Name	No	I/O	Description
TCK	34	I	JTAG Boundary Scan TCK signal
TDO	55	O	JTAG Boundary Scan TDO signal
TDI	35	I	JTAG Boundary Scan TDI signal. Pad has internal 50K pull-up resistor.
TMS	36	I	JTAG Boundary Scan TMS signal. Pad has internal 50K pull-up resistor.
TRST	37	I	JTAG Boundary Scan RST signal. Pad has internal 50K pull-up resistor.

Note: JTAG boundary scan functionality is available when JTAG_BS_ENn pin, pin 22 is open or pulled low.

4 Functional Description

Figure 3: Functional Block Diagram



4.1 Clock Generation

The FLI8125 accepts the following input sources:

1. Crystal Input Clock (TCLK and XTAL). This is the input pair to an internal crystal oscillator and corresponding logic. Alternatively, a single ended TTL/CMOS clock input can be driven into the XTAL pin (leave TCLK as n/c in this case).
2. External Clocks on various GPIOs for test purposes
3. Host Interface Transfer Clock (SCL), I2C slave SCL for DDC2Bi and another SCL for Serial Inter-Processor Communication (SIPC)
4. Video Port VCLK
5. Second Video port clock. This is shared with ROM Address line 11. This is available only when parallel ROM interface is not used.

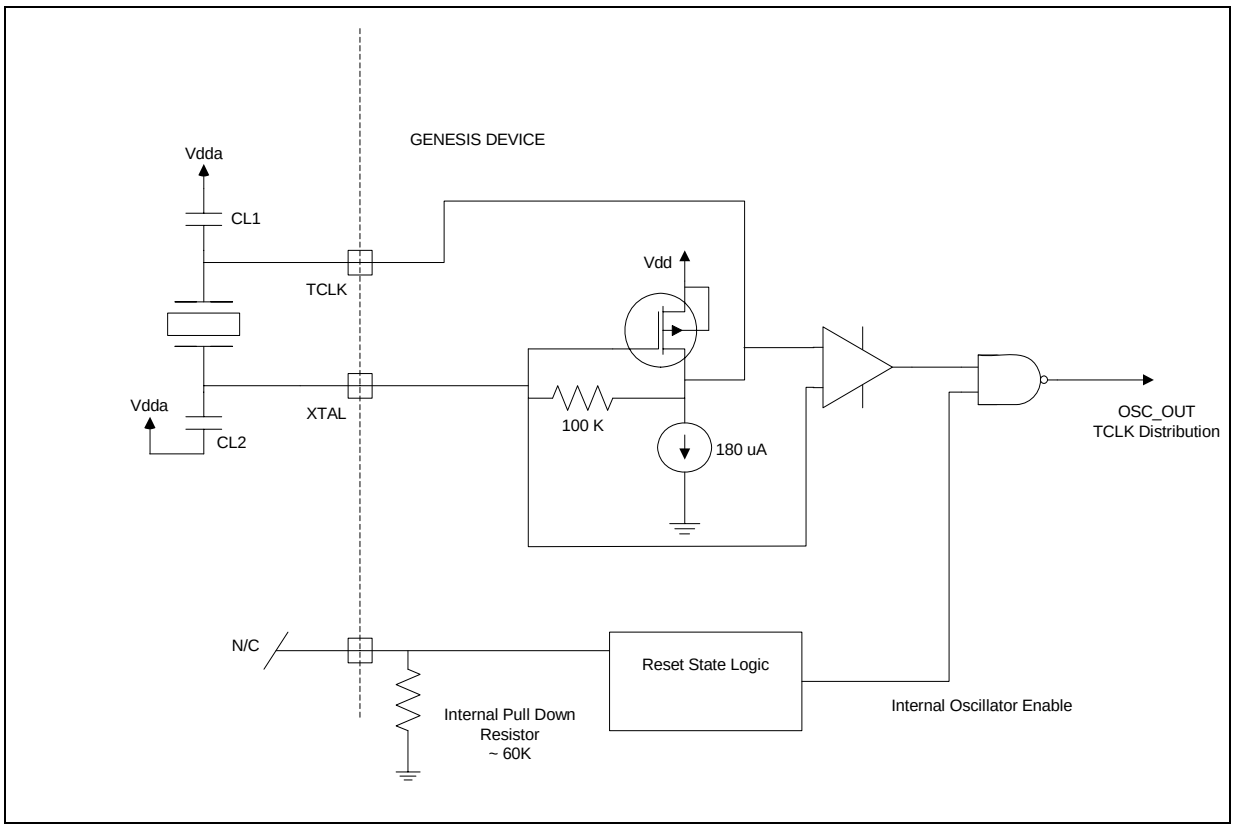
4.1.1 Using the Internal Oscillator with External Crystal

The first option for providing a clock reference is to use the internal oscillator with an external crystal. The oscillator circuit is designed to provide a very low jitter and very low harmonic clock to the internal circuitry of the chip. An Automatic Gain Control (AGC) is used to insure startup and operation over a wide range of conditions. The oscillator circuit also minimizes the overdrive of the crystal, which reduces the aging of the crystal.

When the internal oscillator is enabled a crystal resonator is connected between TCLK and the XTAL with the appropriately sized loading capacitors C_{L1} and C_{L2}. The size of

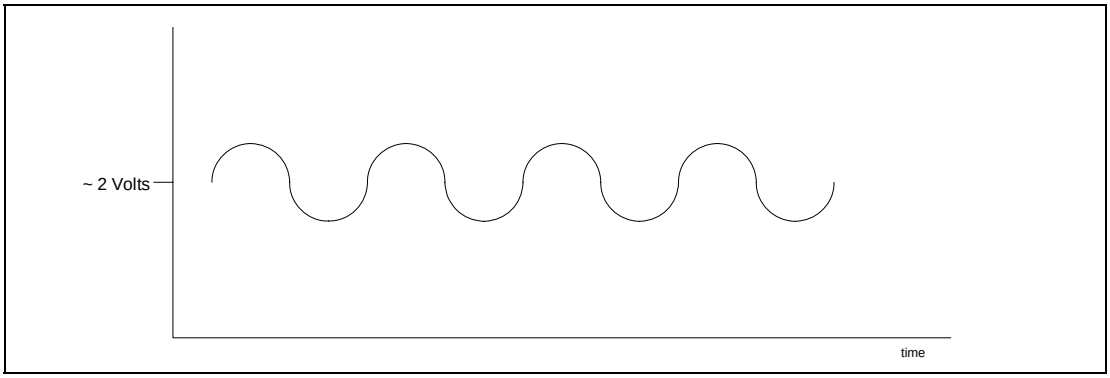
C_{L1} and C_{L2} are determined from the crystal manufacturer's specification and by compensating for the parasitic capacitance of the Genesis device and the printed circuit board traces. The loading capacitors are terminated to the analog VDD power supply. This connection increases the power supply rejection ratio when compared to terminating the loading capacitors to ground.

Figure 4: Using the Internal Oscillator with External Crystal



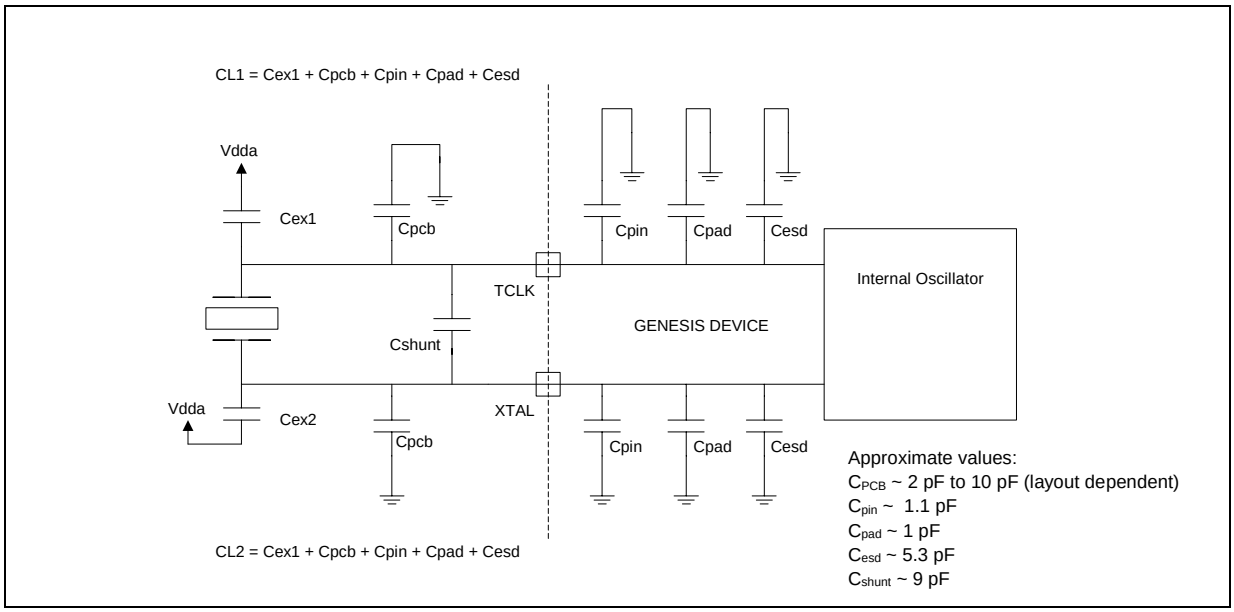
The TCLK oscillator uses a Pierce Oscillator circuit. The output of the oscillator circuit, measured at the TCLK pin, is an approximate sine wave with a bias of about 2 volts above ground. The peak-to-peak voltage of the output can range from 250 mV to 1000 mV depending on the specific characteristics of the crystal and variation in the oscillator characteristics. The output of the oscillator is connected to a comparator that converts the sine wave to a square wave. The comparator requires a minimum signal level of about 50-mV peak to peak to function correctly. The output of the comparator is buffered and then distributed to the internal circuits.

Figure 5: Internal Oscillator Output



One of the design parameters that must be given some consideration is the value of the loading capacitors used with the crystal. The loading capacitance (C_{load}) on the crystal is the combination of C_{L1} and C_{L2} and is calculated by $C_{load} = ((C_{L1} * C_{L2}) / (C_{L1} + C_{L2})) + C_{shunt}$. The shunt capacitance C_{shunt} is the effective capacitance between the XTAL and TCLK pins. For the FLI8125 this is approximately 9 pF. C_{L1} and C_{L2} are a parallel combination of the external loading capacitors (C_{ex}), the PCB board capacitance (C_{pcb}), the pin capacitance (C_{pin}), the pad capacitance (C_{pad}), and the ESD protection capacitance (C_{esd}). The capacitances are symmetrical so that $C_{L1} = C_{L2} = C_{ex} + C_{PCB} + C_{pin} + C_{pad} + C_{ESD}$. The correct value of C_{ex} must be calculated based on the values of the load capacitances.

Figure 6: Sources of Parasitic Capacitance

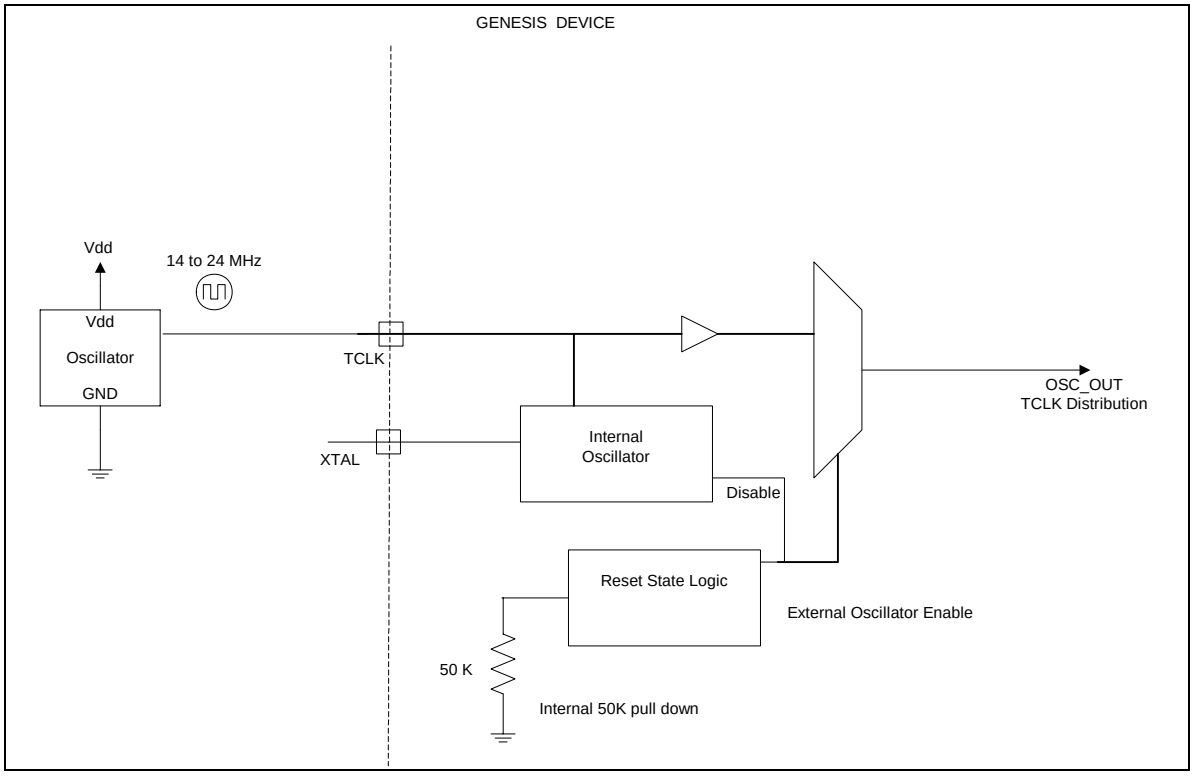


Some attention must be given to the details of the oscillator circuit when used with a crystal resonator. The PCB traces should be as short as possible. The value of C_{load} that is specified by the manufacturer should not be exceeded because of potential start up problems with the oscillator. Additionally, the crystal should be a parallel resonate-cut and the value of the equivalent series resistance must be less then 90 Ω.

4.1.2 Using an External Clock Oscillator

Another option for providing the reference clock is to use a single-ended external clock oscillator. When the internal oscillator is disabled the external oscillator mode is enabled.

Figure 7: Using an External Single-Ended Clock Oscillator



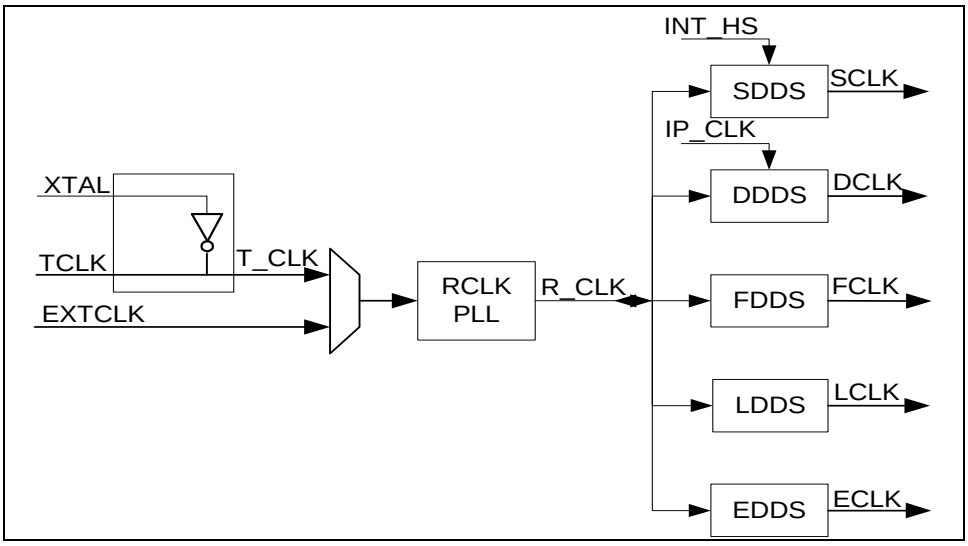
4.1.3 Clock Synthesis

Additional synthesized clocks using PLLs:

1. Main Timing Clock (T_CLK) is the output of the chip internal crystal oscillator. T_CLK is derived from the TCLK/XTAL pad input.
2. Reference Clock (R_CLK) synthesized by RCLK PLL using T_CLK or EXTCLK as the reference.
3. Input Source Clock (SCLK) synthesized by SDDS PLL using input HS as the reference. In case of analog composite video input this runs in open loop. The SDDS also uses the R_CLK to drive internal digital logic.
4. Display Clock (DCLK) synthesized by DDDS PLL using IP_CLK as the reference. The DDDS also uses the R_CLK to drive internal digital logic.
5. Fixed Frequency Clock (FCLK) synthesized by FDDS. Used as OCM_CLK domain driver.
6. Extended Clock (ECLK) synthesized by EDDS. Used by the decoder.

7. A fixed frequency clock created by LDDS (LCLK). Used by the expander in case of panoramic scaling.

Figure 8: Internally Synthesized Clocks



4.1.4 Clock Domains

Internally, there are several clock domains.

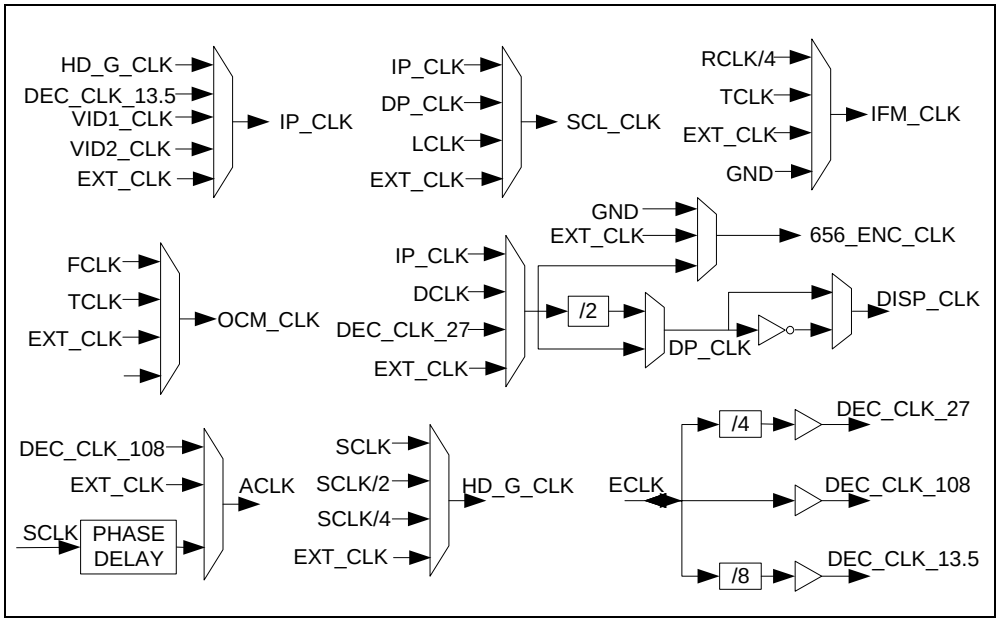
1. Input Clock Domain (IP_CLK). Max = 135MHz
2. Input Clock Domain (T_CLK). Max = 24MHz.
3. Host Interface and On-chip Micro-controller Clock (OCM_CLK). Max = 100MHz
4. Display Pixel Clock (DP_CLK). Max = 135MHz
5. Source Timing Measurement Domain (IFM_CLK). Max = 50MHz
6. Reference Clock Domain (R_CLK output by RCLK PLL). Max = 240 MHz
7. ADC Clock Domain (A_CLK). Max = 165MHz.
8. Decoder clock Domain DEC_CLK_108. This is derived from ECLK. Max = 108MHz
9. Decoder clock domain (DEC_CLK_54). This is derived from DEC_CLK_108. 54MHz
10. Decoder clock domain (DEC_CLK_27). This is derived from DEC_CLK_108. 27 MHz
11. Decoder clock domain (DEC_CLK_13.5).This is derived from DEC_CLK_108.13.5 MHz
12. HD and Graphics clock Domain (HD_G_CLK) Max = 135MHz
13. Expander Clock (EXP_CLK). Max = 135Mhz

The clock selection for each domain as shown in the figure in next page is controlled using the CLOCK_CONFIG register.

Additional Notes on clock domains:

1. The T_CLK is the output from a crystal oscillator embedded within the analog clock block. The external connection to the oscillator is via the TCLK and XTAL pads. All logic in the IC using T_CLK as an input reference source shall assume T_CLK will operate at a frequency between 14MHz to 24MHz. In lieu of using a crystal oscillator, the XTAL input pad can be driven with a single ended TTL/CMOS input clock (eg. for testing of the IC); XTAL would be N/C in this case.

Figure 9: On-Chip Clock Domains



4.2 Chip Initialization

4.2.1 Power Sequencing

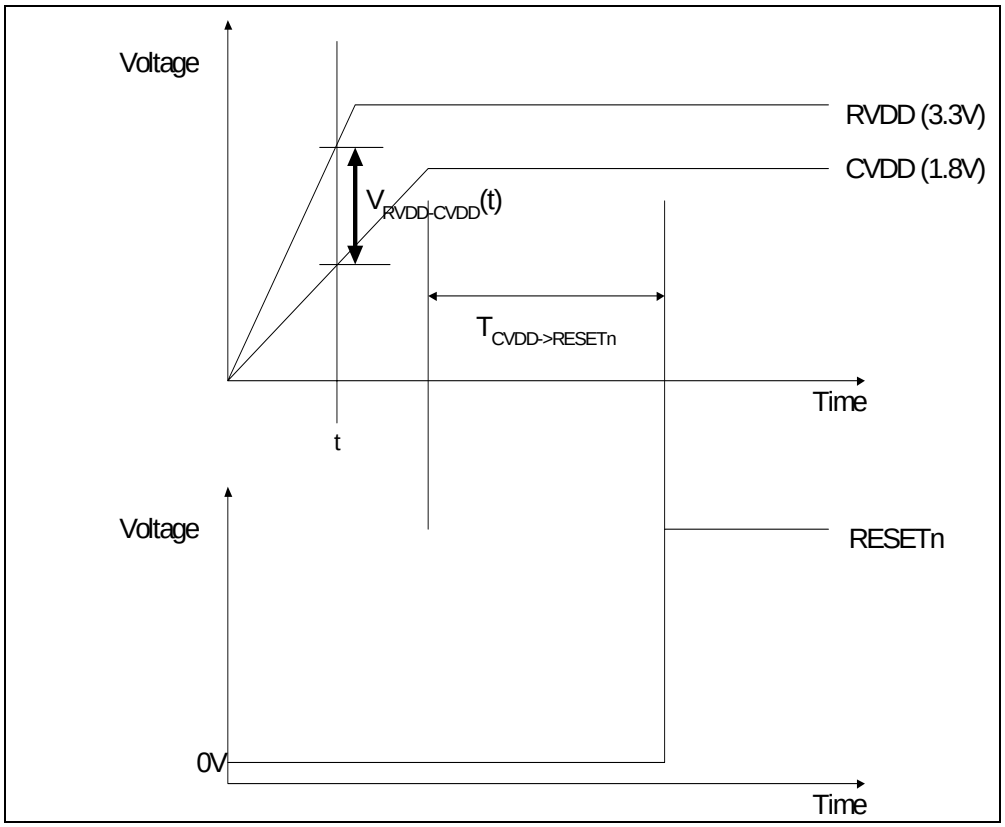
At any time during the power-up sequence the actual voltage of the 3.3V RVDD power supply should always be equal to or higher than the actual voltage of the 1.8V CVDD power supply. In mathematical terms, $V_{RVDD} >= V_{CVDD}$ at all times.

In addition, the system designer must ensure that the 1.8V core VDD supply must be active for at least 1ms before the rising edge of the chip RESETn signal during the chip power-up sequence. The rising edge of RESETn signal is used to latch the bootstrap configurations, so its correct timing relationship to the core VDD is critical for correct chip operation.

Table 11: Power Sequencing Requirements

Parameter	Min	Typ	Max
VRVDD-CVDD(for all t>0)	0V		
TCVDD->RESETn	150ms		

Figure 10: Correct Power Sequencing



4.2.2 Hardware Reset

Hardware Reset is performed automatically on chip power up by the internal Reset Generator or by holding the RESETn pin low for a minimum of 1 us. When the reset period is complete (150ms) and RESETn is de-asserted, the IC power up sequence is:

1. Reset all registers to their default state (00h unless otherwise specified in the register requirements).
2. Force each clock domain to reset. Reset will remain asserted for 64 local clock domain cycles following the de-assertion of RESETn.
3. OCM starts operating with OCM_CLK domain at the T_CLK frequency.
4. Preset the RCLK PLL to output ~240 MHz clock (assumes 19.6608 MHz TCLK crystal frequency).
5. OCM waits for RCLK PLL to lock and programs FDDS (fixed frequency clock) to produce 100 MHz clock.
6. OCM changes OCM_CLK domain to FDDS frequency.

The following figure shows the relationship between RESETn and 3.3V AVDD power rail (AVDD_3.3): Tr is the reset active period, and Tp is the hold time of push button that grounds RESETn pin.

Figure 11: Reset Pulse vs. +3.3V_AVDD Power Line

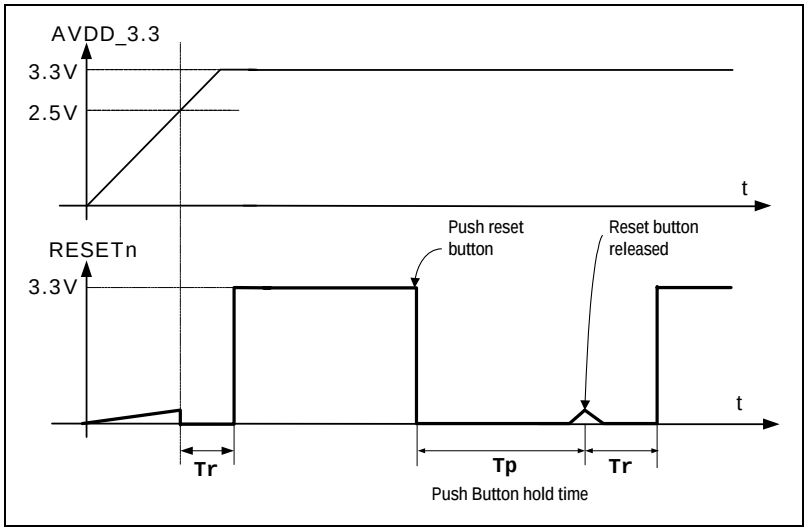


Table 12: RESETn Active Period (Tr) Specification

Parameter	Min	Max
Tr	100	160

The reset threshold for the 3.3V AVDD power rail is 2.5V, and a glitch filter in the reset circuitry will ignore the AVDD_3.3 glitch if the glitch duration is less than 100 ns. However, if AVDD_3.3 voltage drops below 2.5V and the glitch duration is more than 100ns, the RESETn will be asserted to reset the chip. Figure 10 below illustrates the AVDD_3.3V glitch that will cause RESETn to be asserted.

Figure 12: Glitch in 3.3V AVDD

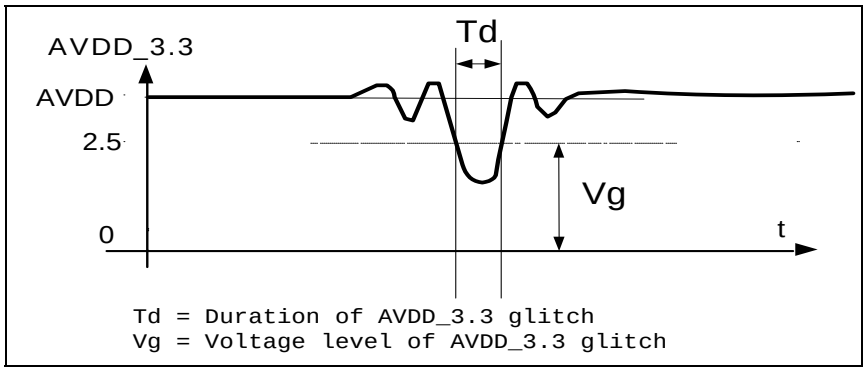


Table 13: RESETn Requirements Due to Glitch in AVDD_3.3V

Parameter	Min	Max
Td	100ns	
Vg		2.5V

NOTE: The RESETn pin should be connected to ground with a 0.01uF capacitor to avoid spontaneous reset conditions.

4.2.3 Software Reset

Main blocks may be independently hardware reset by setting software reset bits in the SOFT_RESETS register.

Software Reset is performed by programming the HOST_CONTROL register bit SOFT_RESET=0. The SOFT_RESET bit will self clear to 0 upon completion of reset. A software reset:

1. Resets all active registers and status registers. Pending and read/write registers are not affected by Software Reset.
2. Force each clock domain to remain in reset for 64 local clock domain cycles and then begin operation.

NOTE: Software Reset will not reset the analog parts of the Clocks or ADC.

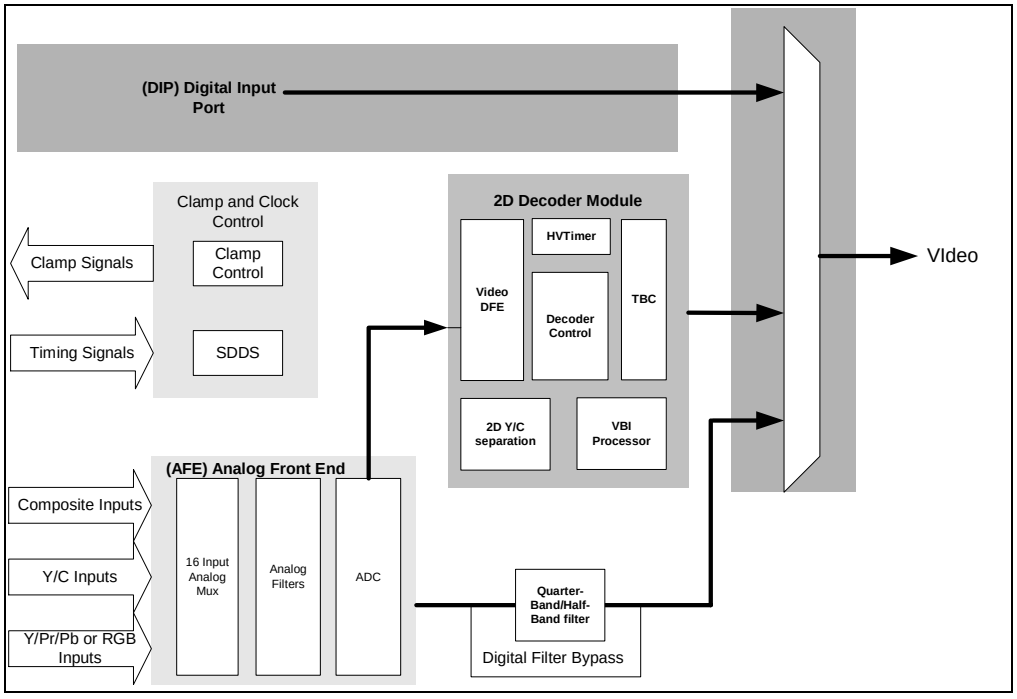
4.3 Analog Front End

The Analog Front End is responsible for selecting and capturing the desired analog input video stream. Overall application cost is reduced by providing analog switching capabilities for 16 separate analog signals. These signals are re-configurable as different combinations of composite, S-Video, YPrPb and RGB video streams depending upon the end application.

The Analog Front End (AFE) directs inputs through an analog multiplexer to anti-alias filters before the Analog to Digital Converters (ADCs). These integrated features eliminate the need for any devices between the input connector and the AFE pin connection.

The following figure depicts the data-path for the AFE and Decoder blocks with connections to the input multiplexer.

Figure 13: Analog Front End



Composite / S-Video

The Analog Front End provides the ability to extract a stable sync signal even under poor signal to noise ratios.

Component YPrPb / RGB

YPrPb / RGB inputs are assumed to have stable sync patterns. As such, the Analog Front End is solely responsible for extracting any embedded sync information. The Analog Front End is capable of accepting separate Horizontal and Vertical sync signals for RGB inputs.

RGB Processing

RGB input originating from a computer (max SXGA @ 75Hz) is processed as 4:4:4 RGB data to offer maximum resolution and clarity to images. Some image processing blocks are not used with 4:4:4 RGB Data. See the Input Color Space Conversion section for more information.

RGB inputs originating from motion video sources (e.g., RGB input on SCART connector) containing data from DVD players or VCRs is converted to and processed as 4:2:2 YUV data. This enables all the various enhancement blocks to act on the data stream.

4.3.1 16 Channel Analog Input Multiplexer

The Analog Front End provides the capability to capture 16 analog video inputs which can be a combination of Composite (CVBS), S-Video (SY, SC), YPrPb (Y, Pr, Pb) or RGB (R, G, B).

The Analog Source Selectors are responsible for switching the desired analog inputs to the ADCs for digitization. There are two types of switching required: Channel Selection, Fast Blank Switching.

Channel Selection

Typically input selection is made on video input channel basis (i.e., selection between different video sources such as a DVD or VCR input). This type of switching is considered “static.”

NOTE: Switching speed of the Analog Source Selectors can be greater than one input frame.

Fast Blank Switching

Fast Blank Switching is supported for SCART connectors or external OSD controllers that require the merging of a line locked analog RGB stream with the viewed composite or S-Video input.

4.3.2 Direct SCART Input Support

Direct connection to SCART devices such as DVD players and Set-top boxes in Europe is supported by enabling Fast Blank Switching and Composite Video Output in the Analog Front End.

Fast Blank Switching

Some applications (e.g., SCART connectors, external VBI, OSD controllers) require the merging of a line locked analog RGB stream with the viewed composite or S-Video input (i.e., RGB Fast Blank Switching). An extra signal named Fast Blank is supplied along with the RGB input to control when the RGB data is inserted into the viewed video data stream. In most applications, the transition of the fast blank signal is not synchronized to the video data stream pixel clock. To avoid artifacts at the fast blank switching points, both the fast blank and RGB signals are sampled. All signals are then filtered down to the video data stream pixel clock and the fast blank signal is used as a blend control signal.

The maximum signal bandwidth for RGB Fast Blank inputs is 13.5 MHz; these signals can be sampled with a line locked 27MHz clock. As with the composite and S-Video inputs, DC Restoration must also be performed on the RGB inputs.

NOTE: The fast blank signal is DC coupled.

Composite Video Output

To enable the connection of external VBI processors, external OSD controllers and support for SCART connectors, the Analog Front End supports a composite video output signal

4.3.3 DC Restoration

The various analog inputs to the Analog Front End (i.e., S-Video, YPrPb, RGB, etc.) may have DC offsets. The Analog Front End provides a means to remove DC offsets so that the full dynamic range of the ADC can be used. Typically, this is achieved by clamping the input signal during the horizontal back porch region. Full control over any such clamping pulse is provided so that the position and size can be controlled via programmable registers.

It is also possible to output the clamping pulse to external devices using one of the GPIO pins.

NOTE: Disable the internal clamping when outputting the clamping pulse to external device.

To allow maximum flexibility, the enabling/disabling of internal clamping and the control of outputting the clamping pulse uses separate register bits. This enables external analog switches to be connected, extending the amount of input switching possible.

The external analog switch requires a clamp signal to DC restore the signal and pass the signal undistorted through its switching matrix. The output of the external analog switch may still have a DC offset based on the linear voltage region of the switch. This requires another (internal) DC restore to ensure correct sampling of the signal.

4.3.4 Sync Extraction

The composite sync pattern may be input on either the HSync input pin or be embedded into G or Y. An internal sync stripper is responsible for extracting composite sync signals embedded in G or Y. Input measurement circuitry is used to

determine the polarity and whether the sync signals are separate Hsync / VSync, composite sync or sync on G / Y.

Figure 14: Composite Sync Support

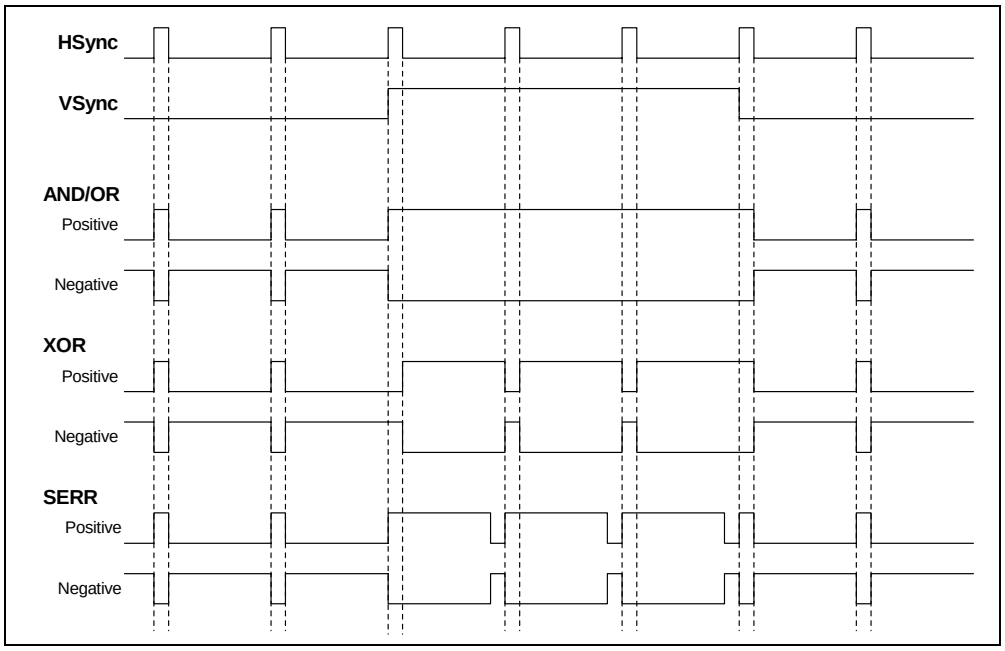
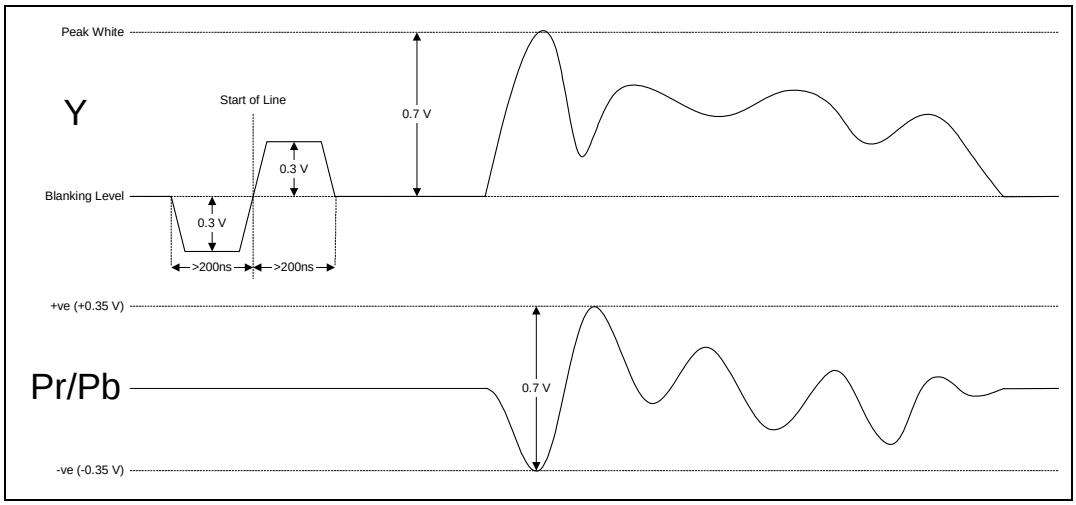


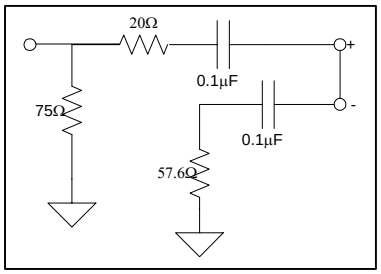
Figure 15: Tri-Level Sync & YPrPb Input



4.3.5 AFE Pin Connection

Much of the necessary external hardware is integrated into the Analog Front End to support direct connection to the physical analog signal connector on the PCB. Only an AC coupling capacitor and a termination resistor are needed between the physical connector and the Genesis device.

Figure 16: Sample Connection for Analog Input Signal



NOTE: It is very important to follow the recommended layout guidelines for this circuit. For more information see the FLI8125 System Layout Guidelines document, C8125 – SLG -01.

4.3.6 Input Filtering

The front end provides filtering capability depending on the type of input video signal in use. The use of these filters eliminates the need to have any external filter components. The filters included are both in the analog as well as digital domain. The digital filter eases design requirements of the analog anti-aliasing filter.

The analog filter is implemented with the following 3dB cutoff definition.

- 10 MHz – for SDTV
- 20 MHz – for 480p/576p
- 40 MHz – for 720p/1080i
- 180 MHz – for Graphics

The digital filters are implemented as Quarter Band (QB), for SDTV and 480p/576p and as Half Band (HB), for 720p/1080i modes.

4.3.7 ADC Characteristics

Table 14: ADC Characteristics

Characteristic	MIN	TYP	MAX	Note
Track & Hold Amp Bandwidth		250 MHz		
Full Scale Adjust Range at RGB Inputs	0.55 V		1.3 V	
Full Scale Adjust Sensitivity		**TBD**		Measured at ADC Output. Independent of full scale RGB input.
Zero Scale Adjust Sensitivity		**TBD**		Measured at ADC Output.
Sampling Frequency (Fs)	10 MHz		162.5 MHz	
Differential Non-Linearity (DNL)		+/-0.5 LSB		Fs = 135 MHz
Integral Non-Linearity (INL)		+/- 1.0 LSB		Fs =135 MHz

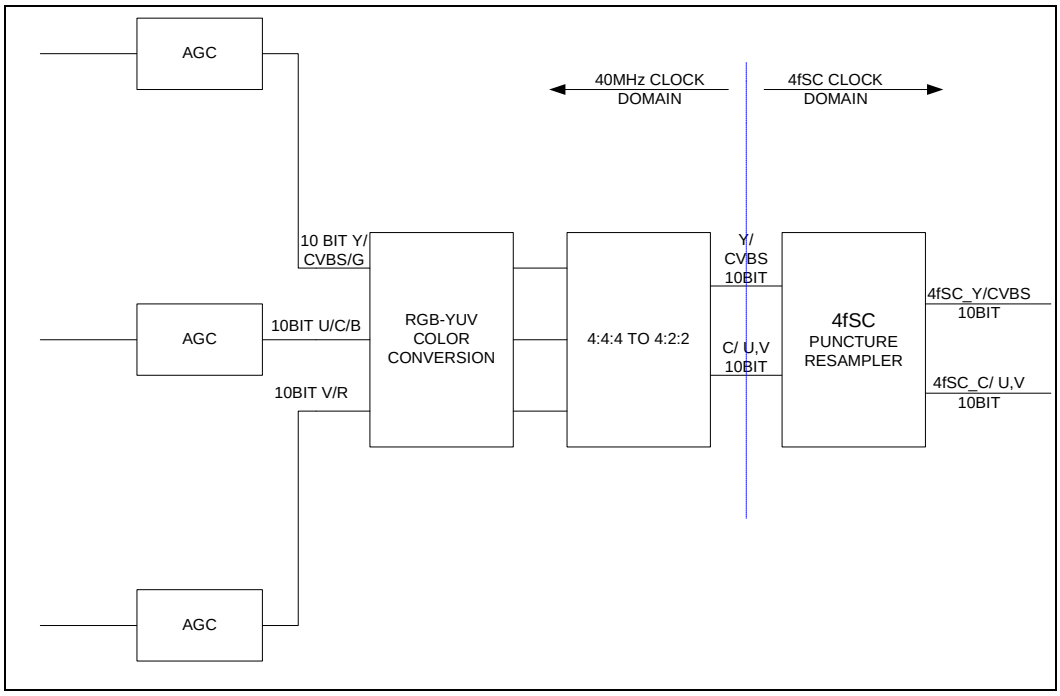
Input formats with resolutions or refresh rates higher than that supported by the LCD panel are supported as recovery modes only. This is called RealRecovery™. For example, it may be necessary to shrink the image. This may introduce image artifacts. However, the image is clear enough to allow the user to change the display properties.

The ADC has a built in clamp circuit for AC-coupled inputs. By inserting series capacitors, the DC offset of an external video source can be removed. The clamp pulse position and width are programmable.

4.4 Digital Front End (Digital Processing after AFE)

The DFE consists of 3 channels that can support the following Fixed-position formats: Channels 1, 2 and 3 can be either R,G,B, or Y,U,V or 2 channels of Y and C or one channel of CVBS. The DFE performs Digital Clamp Loop Control for each channel, AGC Control, Color Conversion, Chroma Downscaling and 4fSC re-sampling. The Input to the DFE is 10 bit 40MHz Data. The Output is 4fsc Sampled CVBS, Y, C or YUV or just 10 bit CVBS.

Figure 17: DFE Datapath



4.5 Multi-Standard Video Decoder

An integrated optimized video decoder capable of decoding composite and S-Video signals from the Analog Front End offers multi-standard operation, decoding NTSC, PAL, SECAM and all sub formats to enable worldwide use.

The Decoder uses a Time Base Correction (TBC) module to stabilize input timing information of the input signal. This will correct unstable or jittery input signals, ensuring they are processed with proper timing, such as VCR signals or non-standard terrestrial signals.

Supported standards include:

- NTSC-M, NTSC 4.43
- PAL B, G, D, H, I, N, M, PAL60
- SECAM

The Video Decoder incorporates a mechanism for automatic detection of the current input video standard. For increased precision, the Video Decoder processes 10-bit data when only an 8-bit output is required (output stream is 16-bit 4:2:2 YUV).

4.5.1 Luminance/Chrominance Separation

The integrated Video Decoder uses an adaptive 2D comb filter to separate luminance and chrominance information. The 2D comb filter changes its operation based upon the horizontal and vertical color transitions to ensure a sharper color response in the vertical direction and stop color bleeding.

4.5.2 Unstable Sync Support

To ensure that a representative image is displayed, the Video Decoder provides additional sync processing in addition to the sync processing by the Analog Front End. The Video Decoder is able to handle the sync variation introduced by VCRs.

4.5.3 Macrovision Input Support

The Video Decoder is capable of accepting video inputs protected by the Macrovision scheme. Macrovision pulses are intended to affect the sync discrimination and AGC circuitry of the receiver. These pulses are ignored so that normal operation of the video decoder is not effected. Macrovision pulses are removed from the output data stream of the video decoder so that other circuitry is not inadvertently affected.

4.6 Multi-Standard VBI Data Processing

The Vertical Blanking Interval (VBI) decoding process runs continuously in the background for inputs that contain VBI data. Decoded data bytes from the VBI Slicer are stored in a memory buffer for subsequent processing by the Embedded Microprocessor. Software running on the Embedded Microprocessor enables access to all the features offered by VBI Data, such as Closed Captions, V-Chip, Teletext, etc.

For maximum compatibility and functionality, the VBI Slicer is able to extract data from a CVBS input when RGB fast blanking is active and the viewed input is RGB. An example of this may be a set top box that outputs programming on the CVBS and RGB signal lines of a SCART connector.

Note: For optimal image quality view the RGB signal, but VBI data may still need to be sliced from the CVBS input.

VBI Slicer

The VBI Slicer is used to extract data contained in the VBI (**V**ertical **B**lanking **I**nterval). Uses of this block include processing for:

- CC (**C**losed **C**aptioning) as per EIA/CEA-608-B
- V-Chip as per EIA/CEA-608-B
- XDS (e**X**tended **D**ata **S**ervices) as per EIA/CEA-608-B
- WSS (**W**ide **S**creen **S**ignaling) as per ITU-R BT.1119-1
- CGMS (**C**opy **G**eneration **M**anagement **S**ystem)
- Teletext up to Level 1.5 as per ETS 300 706

4.7 Digital Input Port

The Digital Input Port is 24-bit input bus that can be connected to external DVI receivers, video decoders, etc. and is able to accept either 8-bit CCIR656 data, 16-bit 4:2:2 YUV data or 24-bit RGB data.

For RGB input data, a selectable color space converter is used to transform RGB video input data from a DVI Rx to internal 16-bit 4:2:2 YUV. This allows the input data to be processed by the Horizontal Enhancement Module (HEM), ACC, and ACM in the image processing block. Other RGB input data streams, such as computer inputs, remain in the RGB space and are processed as such.

The 24-bit Digital Input Port provides control signals to simplify signal detection. CCIR656 data streams embed all timing markers, for the 24-bit and 16-bit inputs the following signals are provided:

- CLK – Input pixel clock for 24-bit, 16-bit or CCIR656 inputs
- HS/CSYNC – Horizontal sync or composite sync signal
- VS – Vertical sync input or SOG input
- DE/FIELD – Data valid input indicator OR Field identification input signal

NOTE: Unused pins of the Digital Input Port can be reprogrammed as GPIOs to increase the total number of GPIOs available.

Inputs to the digital input port are TTL compatible with a maximum clock speed of 135MHz. Sync and clock polarity is programmable.

4.7.1 Supported Digital Input Formats

The following digital video formats are supported by digital video graphic port:

- ITU-BT-656
- 8-bit 4:2:2 YCbCr or YPbPr
- 16-bit 4:2:2 YCbCr or YPbPr
- 24-bit 4:4:4 YCbCr or YPbPr
- 24-bit RGB

The timing of these video formats is shown in the following figures.

Figure 18: ITU-R BT656 Input

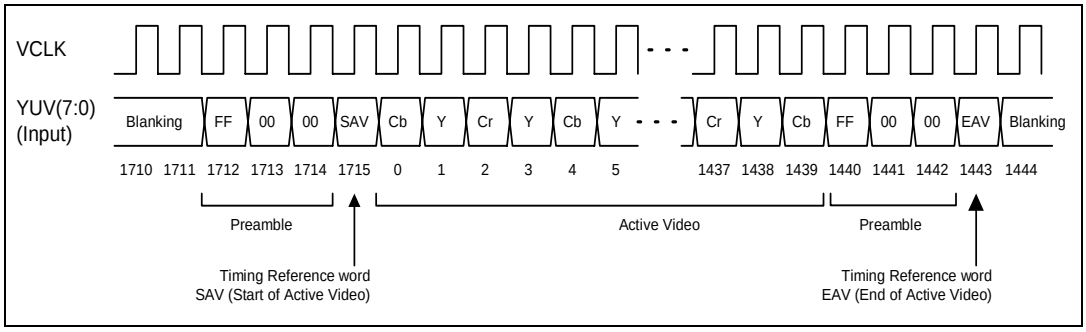
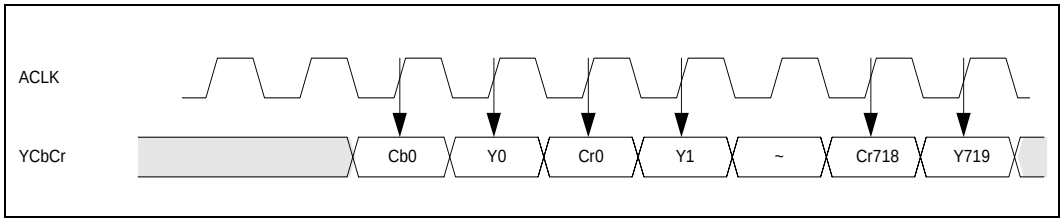


Figure 19: 8-bit 4:2:2 YCbCr/YPbPr



YCbCr input is always automatically clamped to restrict the input data to ITU-R BT601 levels:

- Y Bottom clamping: Y data < 16 is clamped to 16.
- Y Top clamping: Y data > 235 is clamped to 235.
- CbCr Bottom clamping: CbCr data < 16 is clamped to 16.
- CbCr Top clamping: CbCr data > 240 is clamped to 240.

Figure 20: 16-bit 4:2:2 YCbCr/YPbPr

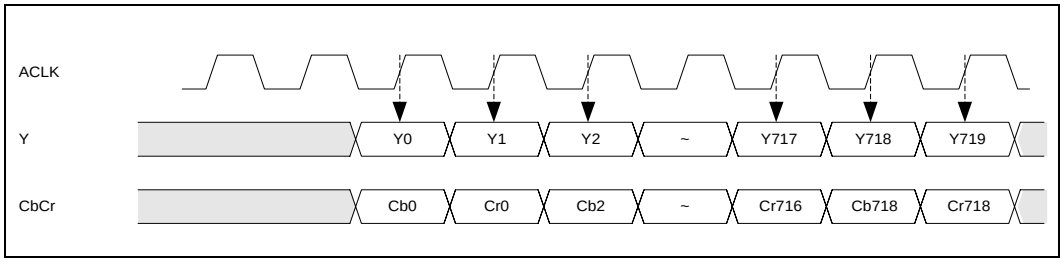


Figure 21: 24-bit 4:4:4 YCbCr/YPbPr

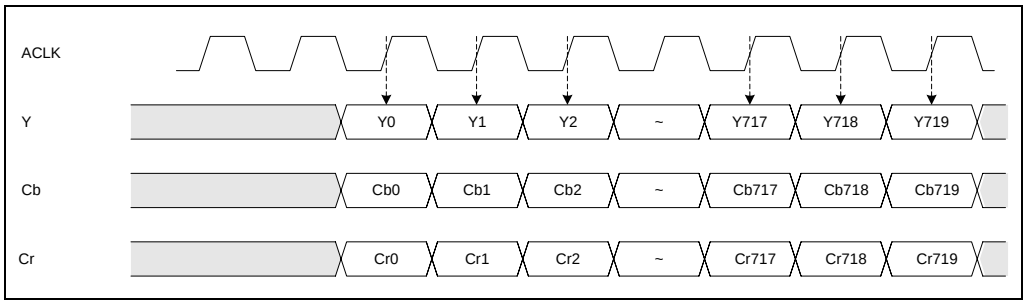
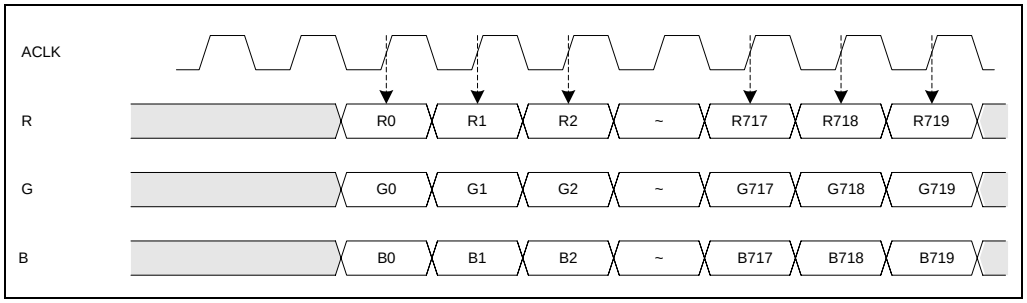


Figure 22: 24-bit RGB

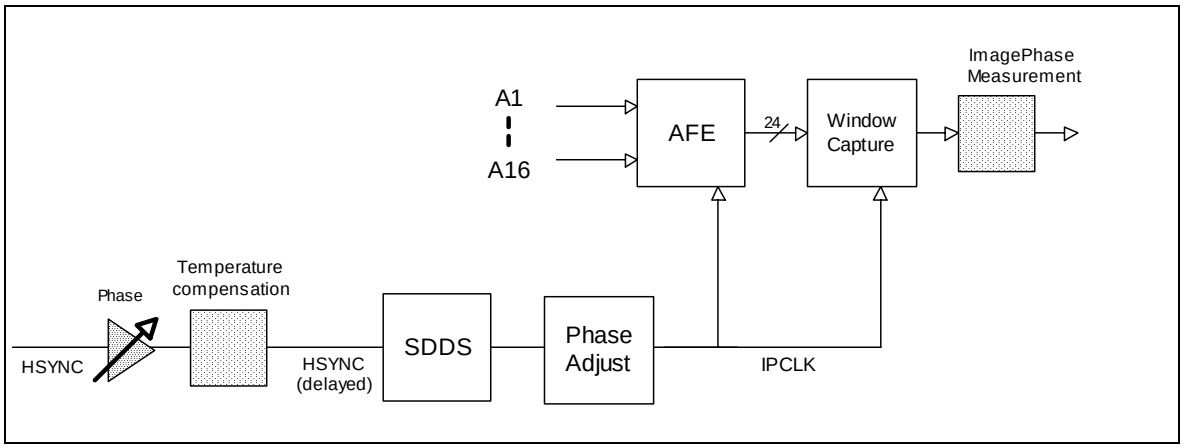


4.7.2 Clock Recovery Circuit

The SDDS (Source Direct Digital Synthesis) clock recovery circuit generates the clock used to sample analog RGB data (IP_CLK or source clock). SDDS is also used for capturing video (up to 150MHz closed loop for HD, 160MHz openloop for SD). This circuit is locked to the HSYNC of the incoming video signal.

Patented digital clock synthesis technology makes the clock circuits resistant to temperature/voltage drift. Using DDS (Direct Digital Synthesis) technology, the clock recovery circuit can generate any IP_CLK clock frequency within the range of 10MHz to 135MHz.

Figure 23: Clock Recovery



4.7.3 Sampling Phase Adjustment

The programmable ADC sampling phase is adjusted by delaying the SDDS clock with respect to the HSYNC input. The accuracy of the sampling phase is checked and the result is read from a register. This feature enables accurate auto-adjustment of the ADC sampling phase.

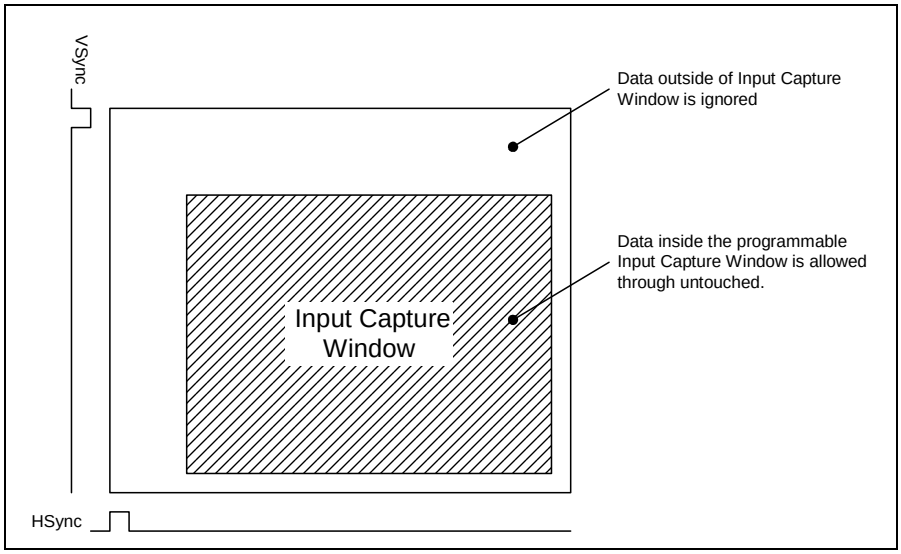
4.8 Input Capture

The Input Capture block is responsible for extracting valid data from the input data stream and creating the required synchronization signals required by the data pipeline. This block also provides stable timing when no stable input timing exists.

4.8.1 Input Capture Window

The selected input data stream is cropped using a programmable input capture window. Only data within the programmable window is allowed through the data pipeline for subsequent processing. Data that lies outside of the window is ignored.

Figure 24: Input Capture Window



Input cropping is required in a video system since video signals are normally over scanned. For a flat panel TV, in order to over scan the image, a smaller portion of the input image needs to be selected and then expanded to fill the entire screen.

Input data streams originating from CCIR656 sources are cropped with reference to the start and end of active video flags encoded into the data stream. For all other inputs, the Input Capture Window is referenced with respect to Horizontal and Vertical Sync.

4.8.2 Source Standalone Mode

In Source Standalone Mode the Input Capture block produces all input timing. This allows OSD and test patterns to be displayed even when there is no stable input timing present.

Source Standalone Mode can be entered either automatically when input timing goes unstable beyond programmable thresholds or forced by programming a register bit. In this mode, unless a test pattern is being displayed, the active data specified by the Input Capture Window is forced to a programmable color.

4.9 Input Color Space Conversion

Some elements within the processing paths are only able to process 16-bit 4:2:2 YUV data. Since the input may be either 24-bit RGB, 24-bit 4:4:4 YUV or 16-bit 4:2:2 YUV, a color space conversion block is used. The color space conversion block performs the following:

- 24-bit full scale (0-255) RGB to 24-bit 4:4:4 YUV
- 24-bit reduced range (16-235) RGB to 24-bit 4:4:4 YUV

NOTE: reduced range (16-235) RGB inputs are only expected to come from external HDMI receivers that are processing an EIA861 or EIA861B stream.

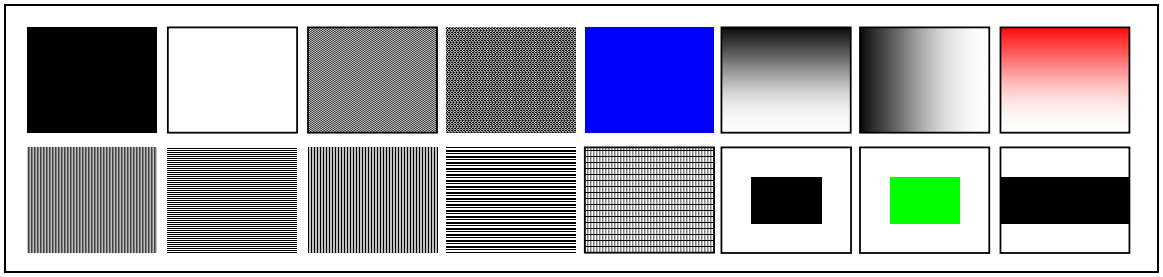
The RGB to YUV conversion can be bypassed. After conversion to the 24-bit 4:4:4 YUV domain, an optional half-band decimation filter is used to convert the data stream to 16-bit 4:2:2 YUV. This process can also by bypassed.

The resultant YUV color space is as specified in CCIR601. High Definition inputs such as 1920x1080i and 1280x720p are encoded in the CCIR709 YUV color space. This is slightly different to CCIR601. The color space conversions blocks do not compensate for the difference between these two color spaces. To compensate for this, blocks which process color, such as ACM, must be loaded with different coefficients when processing CCIR709 encoded data streams. Final conversion to the output color space is handled by a separate programmable 3x3 color matrix . Altering the coefficients of these matrixes ensures that CCIR601 and CCIR709 color spaces are handled correctly.

4.10 Test Pattern Generator (TPG)

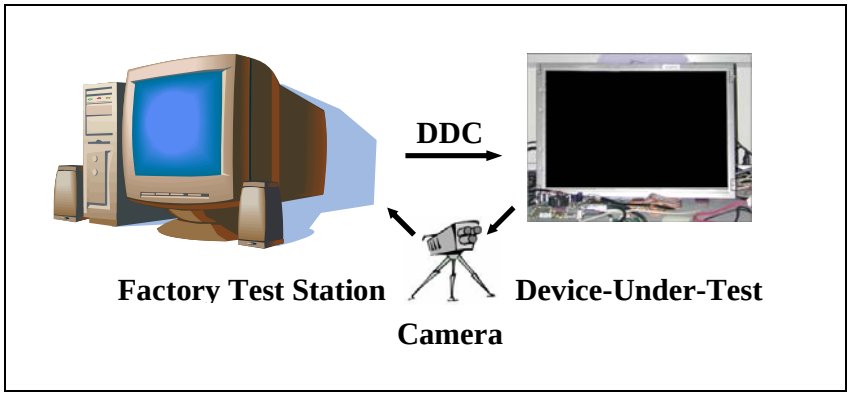
Once programmed, the integrated test pattern generator can replace a video source (e.g. a PC) during factory calibration and test. This simplifies the test procedure and eliminates the possibility of image noise being injected into the system from the source. Foreground and background colors are programmable, and the OSD controller can be used to produce other patterns.

Figure 25: Built-in Test Pattern Examples



The DDC2Bi port can be used for factory testing. In this example, the factory test station is connected through the Direct Data Channel (DDC) of the DSUB15 connectors. The device is then able to display test patterns. A camera can be used to automate the calibration of the LCD panel.

Figure 26: Factory Calibration and Test Environment



4.11 Input Format Measurement

The Input Format Measurement block (IFM) provides the capability of measuring the horizontal and vertical timing parameters of the input video source. Horizontal measurements are measured in terms of the selected IFM_CLK (either TCLK or

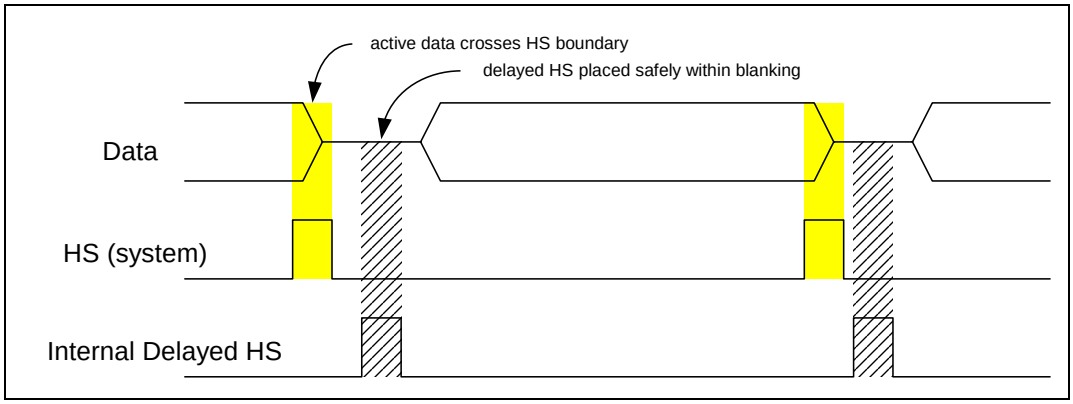
RCLK/4), while vertical measurements are measured in terms of HSYNC pulses. This information is used to determine the video format and to detect a change in the input format. It is also capable of detecting the field type of interlaced formats.

The IFM features a programmable reset, separate from the regular soft reset. This reset disables the IFM, reducing power consumption. The IFM is capable of operating during power down mode.

HSYNC / VSYNC Delay

The active input region captured is specified with respect to internal HSYNC and VSYNC. By default, internal syncs are equivalent to the HSYNC and VSYNC at the input pins and thus force the captured region to be bounded by external HSYNC and VSYNC timing. However, an internal HSYNC and VSYNC delay feature removes this limitation. The HSYNC and VSYNC delay is used for image positioning of ADC input data. HSYNC is delayed by a programmed number of selected input clocks.

Figure 27: Active Data Crosses HSYNC Boundary



Horizontal and Vertical Measurement

The IFM is able to measure the horizontal period and active high pulse width of the HSYNC signal, in terms of the TCLK period. Horizontal measurements are performed on only a single line per frame (or field). The line used is programmable. It is able to measure the vertical period and VSYNC pulse width in terms of rising edges of HSYNC. Once enabled, measurement begins on the rising VSYNC and is completed on the following rising VSYNC. Measurements are made on every field / frame until disabled.

Format Change Detection

The IFM is able to detect changes in the input format relative to the last measurement and then alert both the system and the on-chip microcontroller. The microcontroller sets a measurement difference threshold separately for horizontal and vertical timing. If the current field / frame timing is different from the previously captured measurement by an amount exceeding this threshold, a status bit is set. An interrupt can also be programmed to occur.

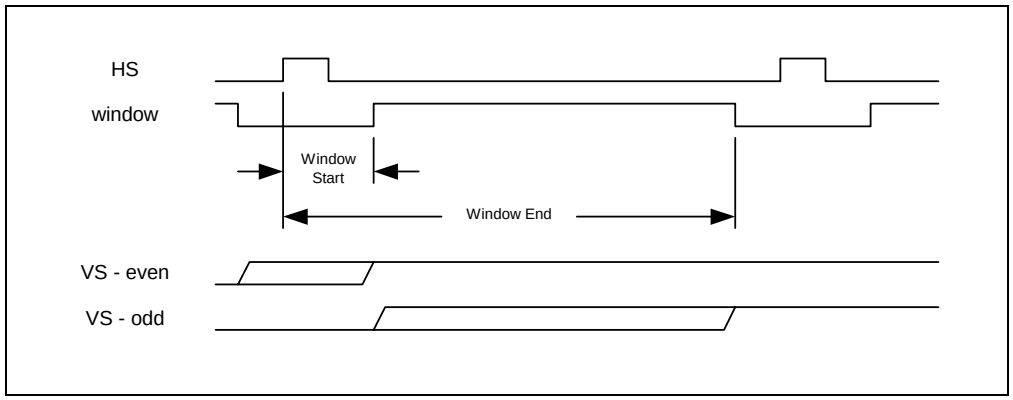
IFM Watchdog

The watchdog monitors input VSYNC / HSYNC. When any HSYNC period exceeds the programmed timing threshold (in terms of the selected IFM_CLK), a register bit is set. When any VSYNC period exceeds the programmed timing threshold (in terms of HSYNC pulses), a second register bit is set. An interrupt can also be programmed to occur.

Internal Odd/Even Field Detection (For Interlaced Inputs to ADC Only)

The IFM has the ability to perform field decoding of interlaced inputs to the ADC. The user specifies start and end values to outline a "window" relative to HSYNC. If the VSYNC leading edge occurs within this window, the IFM signals the start of an ODD field. If the VSYNC leading edge occurs outside this window, an EVEN field is indicated (the interpretation of odd and even can be reversed). The window start and end points are selected from a predefined set of values.

Figure 28: ODD/EVEN Field Detection



Input Pixel Measurement

Pixel measurement functions are provided to assist in configuring system parameters such as pixel clock, SDDS sample clocks per line and phase setting, centering the image, or adjusting the contrast and brightness.

Image Phase Measurement

This function measures the sampling phase quality over a selected active window region. This feature may be used when programming the source DDS to select the proper phase setting.

Image Boundary Detection

Image boundary detection is used when programming the Active Window and centering the image. Functions perform measurements to determine the image boundary.

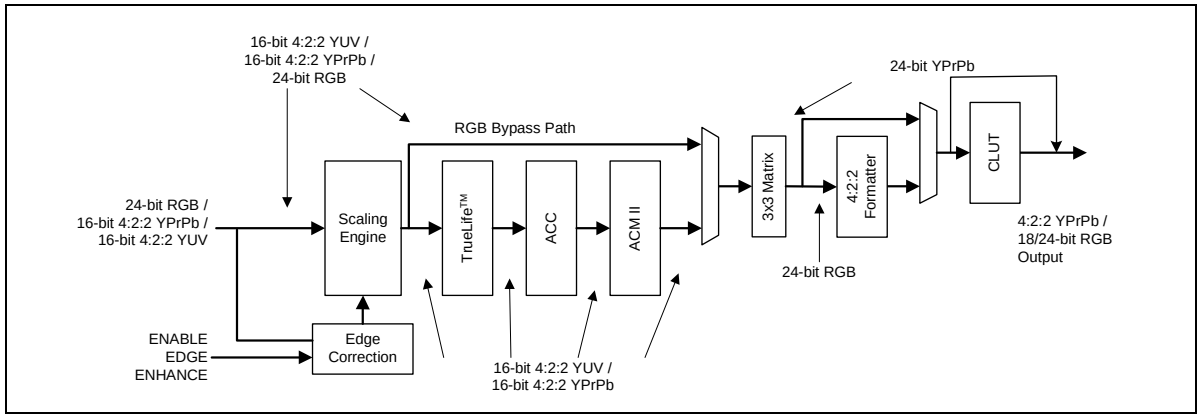
Image Auto Balance

Image auto balance functions perform MIN and MAX pixel value measurements on the input data that is used to adjust brightness and contrast.

4.12 Image Processing

The following figure shows the various image processing blocks that operate on the captured video data stream. Each block is individually selectable and can be removed from the processing chain via a selectable bypass path. When a processing block is bypassed, it automatically enters a low power mode to help reduce overall power consumption.

Figure 29: Image Processing Block Diagram



4.12.1 Faroudja DCDi Edge Processing

Faroudja DCDi Edge processing is used to reduced/eliminate objectionable stair stepping that occurs on interlaced diagonal lines. DCDi Edge processing is optimized for a memory architecture that is unified with the memory used for scaling. This block can process 24-bit RGB, 16-bit 4:2:2 YUV or 16-bit 4:2:2 YPrPb data streams.

4.12.2 Scaling Engine

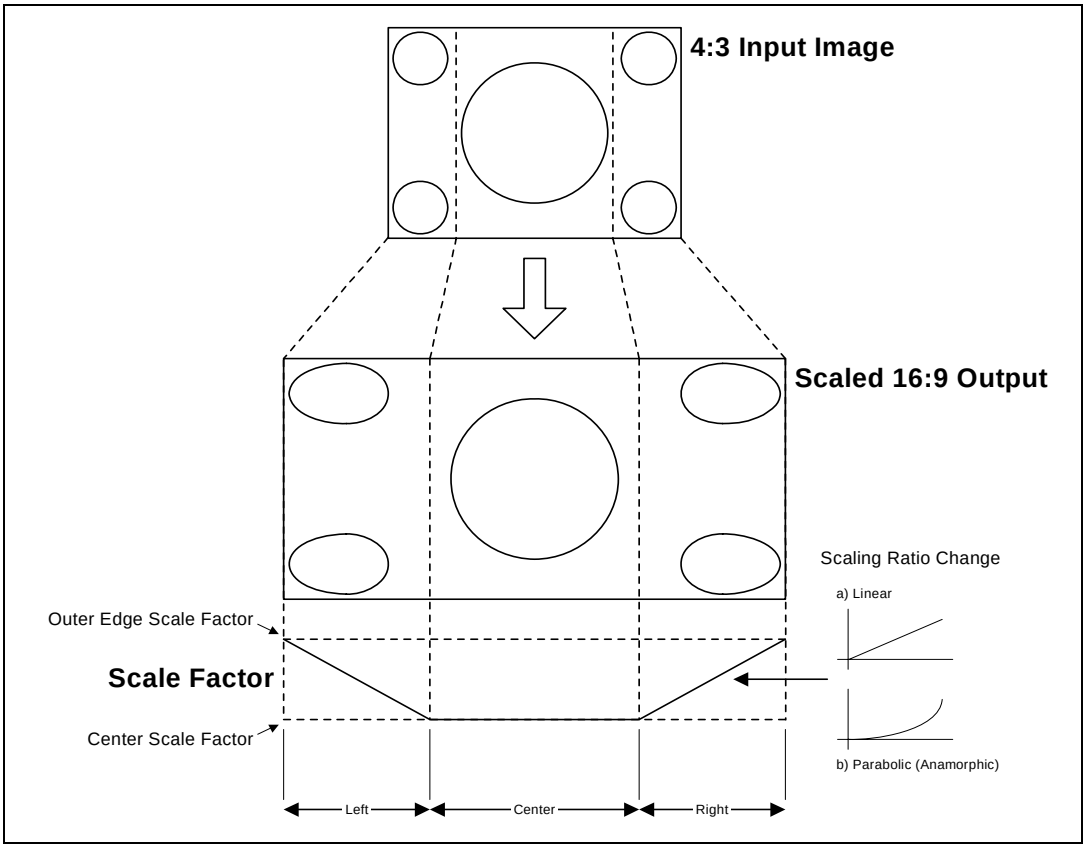
The Scaling Engine accepts both 16-bit 4:2:2 YUV and 24-bit RGB inputs. It is capable of scaling the input by a factor of 0.05 to 5.0. A flexible tap structure is used so that the number of taps can be increased based on the number of pixels per line and whether the input is 4:2:2 YUV or 4:4:4 RGB.

To reduce the amount of memory required for the vertical scaling process, horizontal shrink is performed prior to vertical scaling and horizontal expansion happens after vertical scaling. The maximum number of pixels per line supported by the vertical scalar is 1366.

Non-linear Scaling

The Scaling Engine supports non-linear scaling in the horizontal direction to enable aspect ratio conversion of images such as 4:3 to full screen 16:9

Figure 30: Non-linear Scaling



The input image is separated into three zones horizontally; left, center, and right. The center zone is scaled at a programmable fixed ratio. The left and right zones have a linearly changing scale factor that changes from left to right across the zone. The scale ratio for all zones can vary from 1x to greater than 1x, 1x to less than 1x, but not less than 1x to greater than 1x, i.e. the scale ratio can not cross the unity boundary. The function of scale ratio change can either be linear or parabolic. The parabolic function is required for true Anamorphic conversion.

4.12.3 Faroudja TrueLife™

The Faroudja TrueLife™ Enhancer provides a non-linear enhancement of both Chroma and Luma to give video images a more realistic and life-like appearance. The enhancement algorithms consist of both large edge and detail enhancements.

Pixels to pixel transitions above a programmable "Noise Threshold" and below a programmable "Large Edge" threshold are considered to be small transitions, or image detail. When the pixel-to-pixel transitions are above the programmable "Large Edge" transition threshold, they are considered to "Large Edge" transitions.

Figure 31: Luma Enhancement

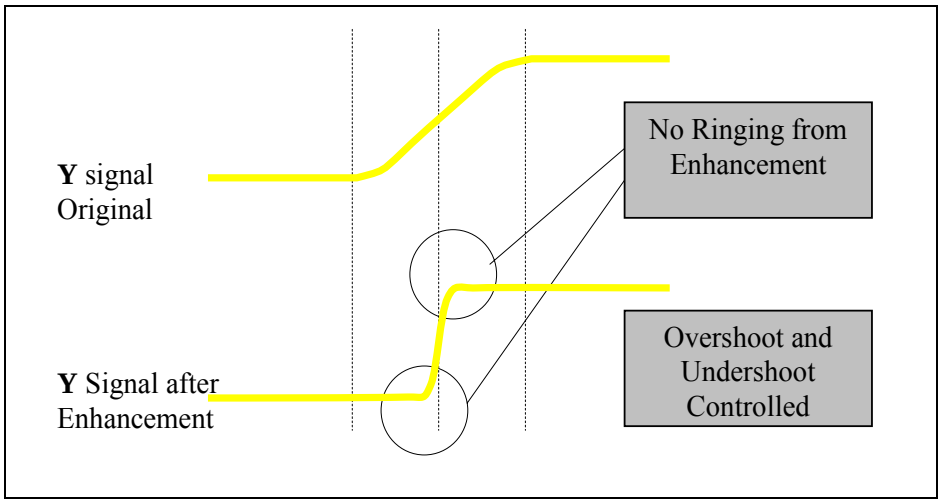
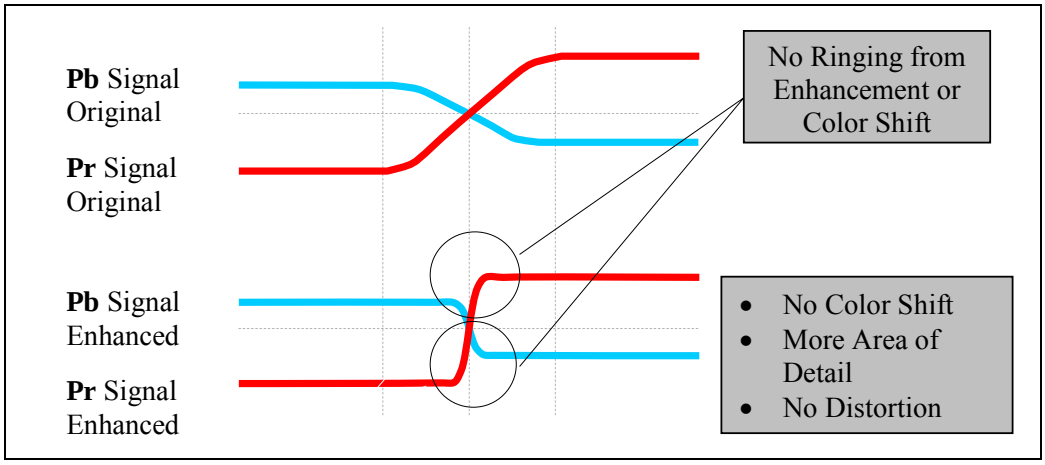


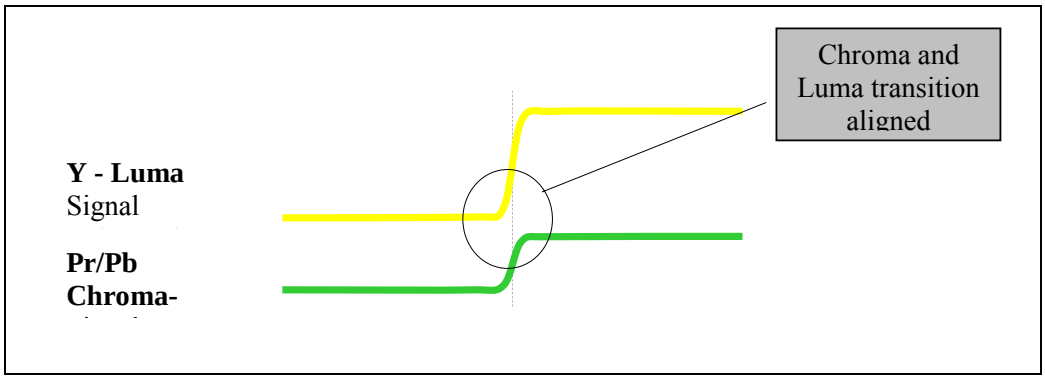
Figure 32: Chroma Enhancement



The TrueLife Enhancer is able to properly align the chroma and luma transition after enhancement. If simple enhancement is used, a shift between the luma and chroma transition will appear due to the difference in bandwidth of the two signals resulting in misalignment of the transition and creation of an incorrect color transition at the edge being enhanced.

- NTSC: Luma B/W = 4.5MHz Chroma B/W = 1MHz
- HDTV: Luma B/W = 37MHz Chroma B/W = 18.5MHz

Figure 33: Luma/Chroma Alignment



4.12.4 Adaptive Contrast and Color (ACC)

To enhance image quality, the contrast and color of the image data is adaptively adjusted based on image content. This process allows dark image images to be visible even in conditions that have high ambient lighting by utilizing the entire dynamic range of the digital display, regardless of the scene brightness.

The **A**daptive **C**ontrast and **C**olor (ACC) block processes 16-bit 4:2:2 YUV or 16-bit 4:2:2 YPrPb data streams. A user programmable window defines the region which ACC operates on and enhances.

4.12.5 Active Color Management II (ACM-II)

The Active Color Management (ACM) block enables advanced manipulation of the colors; refer to Genesis Microchip document "Active Color Management II". Using ACM is it possible to warp colors so that they shift to different colors as well as perform tasks such as flesh tone compensation and green enhancement. The ACM block supports gray guarding to ensure that the gray scale response of the display is not affected.

The ACM block can operate on either the main channel data, or a portion of it, under the control of the Enhancement Window.

4.12.6 Programmable 3x3 Color Matrix

An integrated programmable 3x3 color matrix enables the following functions:

- YPrPb/YUV to RGB Conversion
- RGB to YPrPb Conversion
- CCIR709 to CCIR 601 Color Space Conversion
- sRGB Color Mapping
- Black Level (Luminance DC Offset)
- Contrast (Luminance Gain)
- Saturation (Chrominance Gain)
- Hue (Chrominance Phase – color tone)

The 3x3 matrix has two sets of coefficients. Data outside the Enhancement Window uses one set while data inside is processed using a different set of coefficients.

4.12.7 Enhancement Window

An Enhancement Window can be used in applications where the input originates from a computer and the graphical image contains a video window (e.g., a DVD ROM drive playing a video in a window on the desktop). In this type of application (video in a window) it is desirable to be able to enhance the video window so that it stands out from the graphical background.

The Enhanced Window controls the following blocks:

- ACC
- ACM
- 3x3 Matrix

Each block can be independently programmed to be always on, always off or controlled by the Enhancement Window

NOTE: When processing RGB data, the data outside of the Enhancement Window should not be sub-sampled to 4:2:2 and must remain in either the RGB or 4:4:4 YUV color space. Converting this data to 4:2:2 would cause loss of detail that would be unacceptable.

To showcase the Faroudja DCDi Edge and Faroudja HEM (Truelife™) features a demo mode support feature is incorporated. This concept can also be used to show left and right images with enhancements turned on and off enabling display manufacturers to create on the shelf demonstrations of features to the end consumer. To enable this type of comparison, a programmable Enhancement Window (Demo Mode) specifies an area that is enhanced by the image processing blocks while data outside is not.

4.12.8 Color Look Up Table (CLUT)

The output of the 3X3 Color Matrix feeds three 256x10-bit programmable **C**olor **L**ook **U**p **T**ables (CLUT). These tables allow the user to apply complex gamma curves to the data stream. Programmable register bits control dithering from 10-bit to either 8 or 6-bits per channel. Dithering can be disabled and only the top 6 or 8-MSbits used to create the 18 or 24-bit output bus.

NOTE: Updates to the CLUT are invisible so that no visible artifacts occur during an update period.

4.12.9 Color Standardization and sRGB Support

Internet shoppers may be very picky about what color they experience on the display. RealColor™ digital color controls can be used to make the color response of an LCD monitor compliant with standard color definitions, such as sRGB. sRGB is a standard for color exchange proposed by Microsoft and HP (see www.srgb.com). RealColor controls can be used to make LCD monitors sRGB compliant, even if the native response of the LCD panel itself is not. For more information on sRGB compliance using Genesis devices refer to the *sRGB Application Brief* (C5115-APB-02).

4.13 Display Output Interface

The Display Output Port provides data and control signals that permit the connection to a variety of flat panel devices using a 24-bit TTL or LVDS interface. The output interface is configurable for single or dual wide LVDS in 18 or 24-bit RGB pixels format. All display data and timing signals are synchronous with the DCLK display clock. The integrated LVDS transmitter is programmable to allow the data and control signals to be mapped into any sequence depending on the specified receiver format. DC balanced operation is supported as described in the Open LDI standard.

Output timing is fully programmable via the host interface register set enabling this device to be used as a display controller of a PIP processor for other Genesis Microchip devices.

4.13.1 Output Mode

Output formats of 24 bit /16 bit /8 bit pseudo 656 from the back end block enables this device to be used as a capture and processing engine for delivery to other Genesis Microchip devices.

4.13.2 Display Synchronization

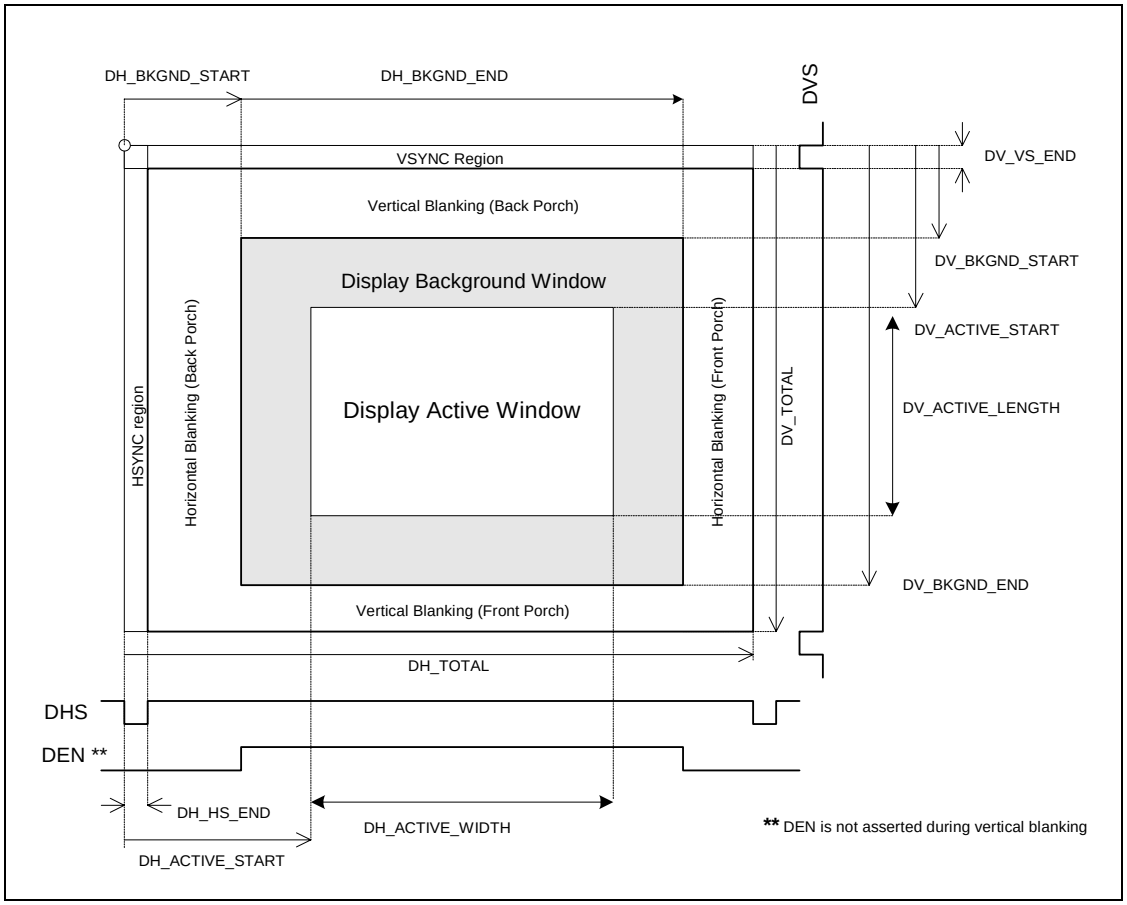
The following display synchronization modes are supported:

- **Frame Sync Mode:** The display frame rate is synchronized to the input frame or field rate. This mode is used for standard operation.
- **Free Run Mode:** No synchronization. This mode is used when there is no valid input timing (i.e. to display OSD messages or a splash screen) or for testing purposes. In free-run mode, the display timing is determined only by the values programmed into the display window and timing registers.

4.13.3 Display Timing Programming

Horizontal values are programmed in single-pixel increments relative to the leading edge of the horizontal sync signal. Vertical values are programmed in line increments relative to the leading edge of the vertical sync signal.

Figure 34: Display Windows and Timing



Display Active Window

Data captured by the Input Capture Window and processed by the various image manipulation blocks is output in the Display Active Window. This window is always in the foreground and lies on top of all other output windows, except OSD overlay windows.

Typically the Display Active Window is set to the same size as the output of the Scaling Engine. If the Display Active Window is set too small, then the bottom and right hand edges of the image data are cropped. If the Display Active Window is set too large, then the extra space to the left and bottom of the Display Active Window is forced to the Background Window color.

NOTE: A separate register bit is used to control whether the display active window is visible or not.

Display Background Window

The Background Window is a programmable window that specifies the total displayable area on the target flat panel, i.e. when region in which data is active. This window is typically programmed to the resolution of the flat panel device. The Display Active Window lies on top of this window, but is cropped by the Background Window. The Background Window has a programmable color. If the Display Active

Window is specified to be smaller than the Background Window then the programmable color is seen as a background color lying underneath the Display Active Window.

Frame Timing Window

The Frame Timing Window defines the horizontal and vertical totals (i.e. active + blanking) and is typically programmed to the desired panel timing. A register bit is used to define whether output timing is active or not. Disabling output timing completely disables all output timing, i.e. the output data bus and all output timing signals go high impedance.

OSD/Overlay Window

The OSD/Overlay Window can be programmed so that it lies anywhere within the Background Window.

4.13.4 Output Dithering

The CLUT outputs a 10-bit value for each color channel. This value is dithered down to either 8-bits for 24-bit per pixel panels, or 6-bits for 18-bit per pixel panels. In this way it is possible to display 16.7 million colors on a LCD panel with 6-bit column drivers.

The benefit of dithering is that the eye tends to average neighboring pixels and a smooth image free of contours is perceived. Dithering works by spreading the quantization error over neighboring pixels both spatially and temporally. Two dithering algorithms are available: random or ordered dithering. Ordered dithering is recommended when driving a 6-bit panel.

All gray scales are available on the panel output whether using 8-bit panel (dithering from 10 to 8 bits per pixel) or using 6-bit panel (dithering from 10 down to 6 bits per pixel).

4.13.5 Dual Channel LVDS Transmitter

An integrated LVDS transmitter with programmable input to output configuration is provided to enable drive of all known panels. The LVDS transmitter can support the following:

- Single pixel mode
- 24-bit panel mapping to the LVDS channels
- 18-bit panel mapping to the LVDS channels
- Programmable channel swapping (the clocks are fixed)
- Programmable channel polarity swapping
- Supports up to SXGA 75Hz output

Table 15: Supported LVDS 24-bit Panel Data Mappings

Channel 0	R0, R1, R2, R3, R4, R5, G0
Channel 1	G1, G2, G3, G4, G5, B0, B1
Channel 2	B2, B3, B4, B5, PHS, PVS, PDE
Channel 3	R6, R7, G6, G7, B6, B7, RES

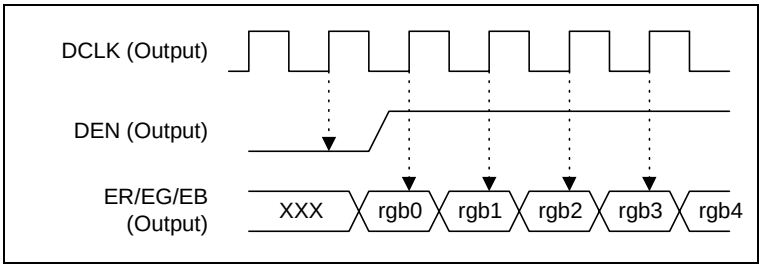
Channel 0	R2, R3, R4, R5, R6, R7, G2
Channel 1	G3, G4, G5, G6, G7, B2, B3
Channel 2	B4, B5, B6, B7, PHS, PVS, PDE
Channel 3	R0, R1, G0, G1, B0, B1, RES

Table 16: Supported LVDS 18-bit Panel Data Mapping

Channel 0	R0, R1, R2, R3, R4, R5, G0
Channel 1	G1, G2, G3, G4, G5, B0, B1
Channel 2	B2, B3, B4, B5, PHS, PVS, PDE
Channel 3	Disabled for this mode

4.13.6 Single Pixel TTL Output

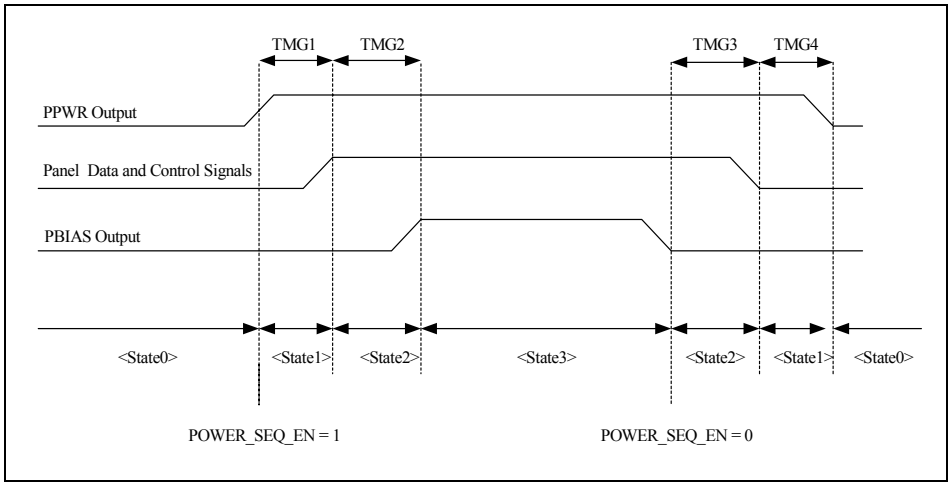
Figure 35: Single Pixel Width Display Data



4.13.7 Panel Power Sequencing (PPWR, PBIAS)

Two dedicated outputs (PPWR, PBIAS) control LCD power sequencing once data and control signals are stable. The timing of these signals is fully programmable.

Figure 36: Panel Power Sequencing



4.14 Energy Spectrum Management™ (ESM)

High spikes in the EMI power spectrum may cause LCD monitor products to violate emissions standards. Drive strength control and output clock modulation features have been included to reduce electromagnetic interference (EMI). These features spread EMI energy over a range of frequencies and reduce the concentration of EMI energy.

These features also help to eliminate the costs associated with EMI reducing components and shielding.

4.15 On-Screen Display (OSD)

An integrated fully programmable, high-quality OSD controller enables the creation and insertion of data that can be used for menus, system information, Closed Captioning, Teletext, etc. Graphics used are divided into "cells" of programmable size. The cells are stored in an on-chip static RAM and can be stored as 1-bit per pixel data, 2-bit per pixel data or 4-bit per pixel data.

General features of the OSD controller include:

- **Four OSD Rectangles –** The OSD can appear in four separately defined rectangular regions.
- **OSD Position –** The OSD menu can be positioned anywhere on the display region. The reference point is Horizontal and Vertical Display Background Start (DH_BKGND_START and DV_BKGND_START).
- **OSD Stretch –** The OSD image can be stretched horizontally and/or vertically by a factor of two. Pixel and line replication is used to stretch the image.
- **OSD Blending** – Sixteen levels of blending are supported for selected colors in the character-mapped.

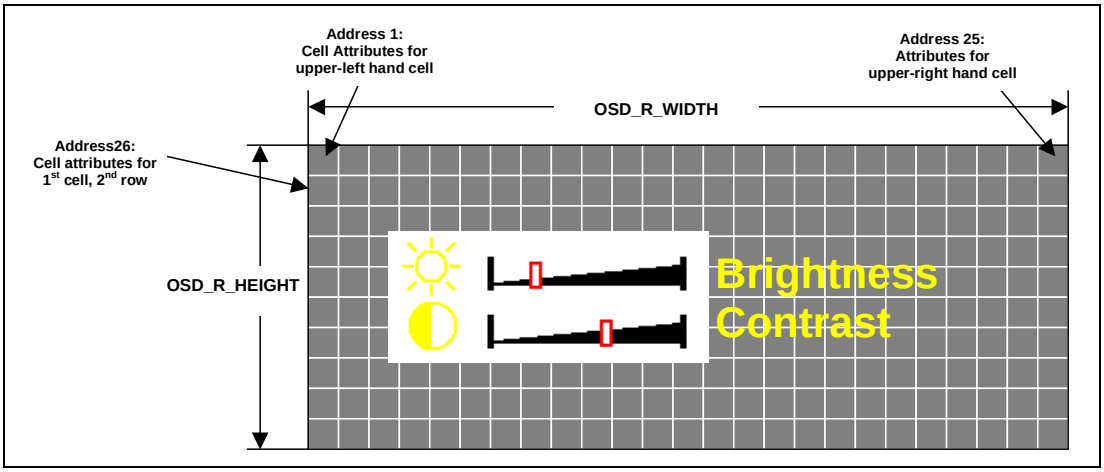
4.15.1 On-Chip OSD SRAM

The on-chip static RAM stores the cell map, cell definitions, and attribute map. The OSD SRAM is shared by the on-chip microcontroller as part of its normal addressable memory space.

In memory, the cell map is organized as an array of words, each defining the attributes of one visible character on the screen starting from upper left of the visible character array. These attributes specify which character to display, whether it is stored as 1, 2 or 4 bits per pixel, the foreground and background colors, blinking, etc.

Registers are used to define the visible area of the OSD image. See the OSD Cell Map figure.

Figure 37: OSD Cell Map



Cell definitions are stored as bit map data. On-chip registers point to the start of 1-bit per pixel definitions, 2-bit per pixel definitions and 4-bit per pixel definitions respectively.

Note that the cell map and the cell definitions share the same on-chip RAM. Thus, the size of the cell map can be traded off against the number of different cell definitions. In particular, the size of the OSD image and the number of cell definitions must fit in RAM.

4.15.2 OSD Color Look-up Table (CLUT)

The Color Look-up Table (CLUT) is stored in an on-chip RAM that is separate from the OSD RAM. The LUT consists of 64 color entries each 16-bit wide in a RGB 5:5:5 format (bit 0 selectively enables blending with background image data.

4.15.3 OSD Overlay

The data from the OSD controller is merged to the video data stream using a programmable blend ratio on the back end.

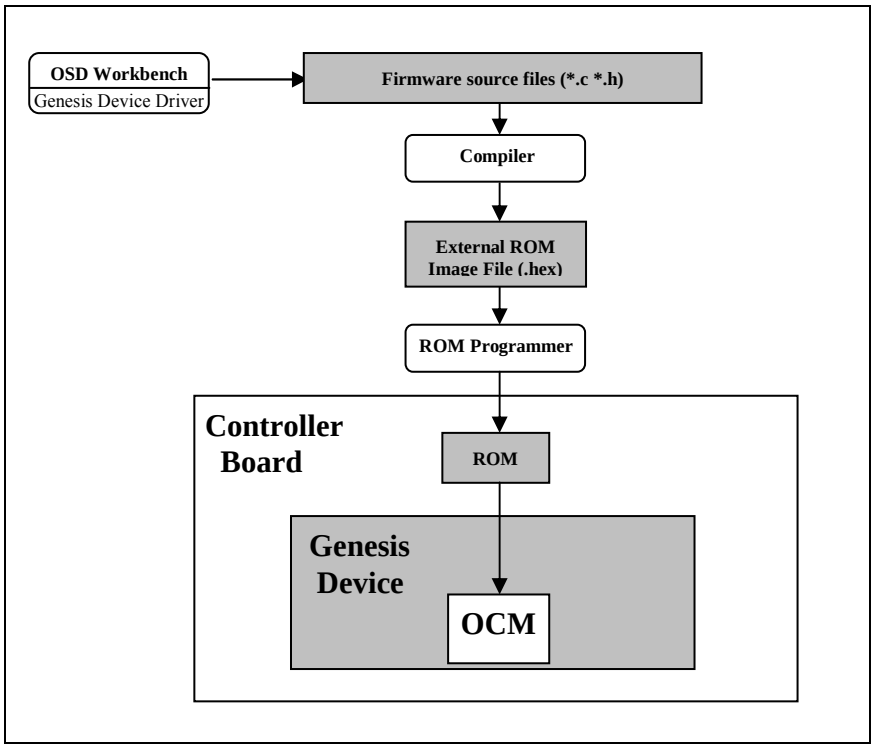
4.16 On-Chip Microcontroller (OCM)

The on-chip microcontroller (OCM) is a 16-bit x86 100MHz processor capable of acting as either the overall system controller or a slave controller, receiving commands from an external controller.

The OCM executes firmware running from external ROM, as well as driver-level (or Application Programming Interface – API) functions residing in internal ROM. A parallel port with separate address and data busses is available for this purpose. This port connects directly to standard, commercially available ROM or programmable FLASH ROM devices. A serial FLASH ROM may be used with the serial peripheral interface (SPI) and cache controller inside the Genesis device.

Both firmware and OSD content must be compiled into a HEX file and then loaded onto the external ROM. The OSD content is generated using Genesis Workbench. Genesis Workbench is a GUI based tool for defining OSD menus, navigation, and functionality.

Figure 38: OCM Programming



Genesis recommends using Paradigm compiler (http://www.devtools.com) to compile the firmware source code into a hex file. This hex file is then downloaded into the external ROM using In-System-Programming (Genesis debug software G-Probe communicates with the OCM which in turn programs a FLASH ROM in the system using the ROM_WEn signal) or using commercially available ROM programmers.

OCM Watchdog

A hardware watchdog is used to ensure the OCM resets after a programmable delay if the watchdog is not reset. This feature helps to ensure that the OCM does not hang indefinitely.

4.16.1 Embedded Bootstrap Function

An embedded ROM bootstrap function is provided from which to boot when external ROM is not present or does not contain data. It is always recommended to boot from embedded ROM. The OCM_ROM bootstrap selects the initial state of the internal OCM ROM.

The embedded ROM firmware first looks for a 'signature' in external ROM (either parallel ROM or serial ROM depending on the programming of the SPI_EN bootstrap). The 'signature' is the ASCII values for the character string "xROM" starting address. If this signature is found then it performs a CRC check. If CRC is valid then it jumps to the appropriate external ROM address.

If the signature is not present then the embedded firmware does not jump to external ROM. In this case it runs in its own loop that supports debugging commands (using G-Probe debugging software available from Genesis) over either the UART port or DDC2Bi port.

4.16.2 In-System Programming (ISP) of External FLASH ROM

Hardware support is provided for in-system programming of external FLASH ROM devices. The ROM_WEn pin can be connected to the write enable of the FLASH ROM. The embedded boot firmware performs the writes.

4.16.3 Serial Peripheral Interface (SPI) for SPI FLASH ROM

Hardware support is provided for SPI Serial FLASH ROM up to 4M-bits through SPI pins: ROM_SCSN, ROM_SCLK, ROM_SDO, ROM_SDI. The SPI interface is configured as follows:

- ROM_SCSN <-> CE# of SPIROM
- ROM_SCLK <-> SCK of SPI ROM
- ROM_SDO <-> SI of SPI ROM
- ROM_SDI <-> SO of SPI ROM

Pins WP# and HOLD# of SPI ROM are options for the control of SPI ROM. They can be pulled high all the time to disable their functions or can be controlled with GPIOs. Refer to SPI ROM specifications for details. In order to enable this SPI interface, ROM Address A15 needs to be pulled high during boot up.

4.16.4 UART Interface

The OCM has an integrated Universal Asynchronous Remote Terminal (UART) port that can be used as a factory debug port. The UART can be used to 1) read / write chip registers, 2) read / write to NVRAM, and 3) read / write to FLASH ROM (In-System Programming).

4.16.5 DDC2Bi Interface

Hardware support is provided for DDC2Bi communication over the DDC channel of the analog input port. The specification for the DDC2Bi standard can be obtained from VESA (www.vesa.org). The DDC2Bi port can be used as a factory debug port or for field programming. In particular, the DDC2Bi port can be used to 1) read / write chip registers, 2) read / write to NVRAM, and 3) read / write to FLASH ROM (In-System-Programming).

4.16.6 JTAG Interface

A JTAG interface is provided to allow in-circuit debugging of the internal OCM. The JTAG interface can operate in standard 5-wire JTAG mode or through a 2-wire serial interface. A 2-wire to JTAG bridge circuit is provided to allow JTAG commands to be issued using only two pins HOST_SCL and HOST_SDA.

4.16.7 Boundary Scan Interface IEEE 1149.1

Boundary Scan (1149.1) logic is implemented to allow system level PCB testing. All digital I/O pins are covered by the boundary scan logic. The TTL/LVDS display port is tested only at TTL levels.

4.16.8 Infra-Red receiver

An Infra-Red receiver is integrated to allow for the reception of Infra-Red signals from remote control units. Standard protocols are supported such as RECS 80 and RC5. The ability also exists to analyze raw signal streams for custom protocols. Optional Carrier filtering is available. Flow control is managed through host bit polling or an IRQ.

4.16.9 General Purpose Inputs and Outputs (GPIO)

There are 24 potential general-purpose input/output (GPIO) pins. Not all may be available depending on shared functionality of particular pins. These are used by the OCM to communicate with other devices in the system such as keypad buttons, NVRAM, LED's, audio controller, etc. Each GPIO has independent direction control and open drain enable for reading and writing.

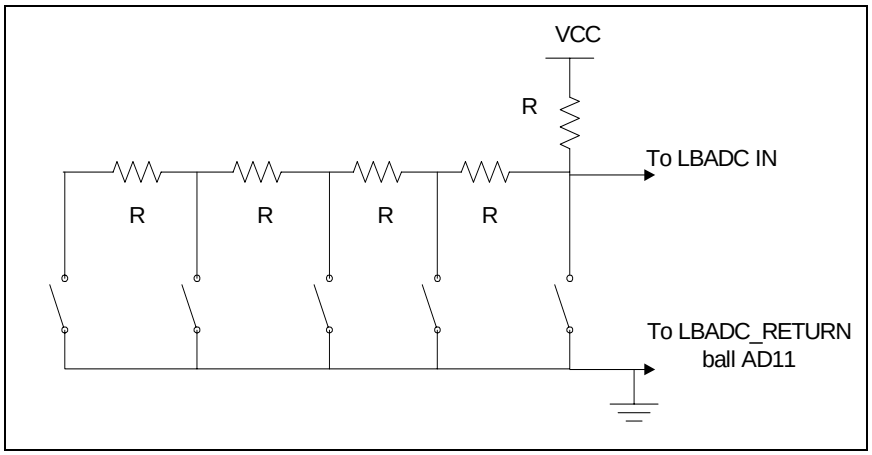
Table 17: GPIO and Alternate Functions

Pin Name	Pin Number	Alternate Function
GPIO0/PD20/B4 GPIO1/PD21/B5 GPIO2/PD22/B6 GPIO3/PD23/B7	86 87 88 89	Can be used as Panel Data 20 or Blue Channel Bit-4. Can be used as Panel Data 21 or Blue Channel Bit-5. Can be used as Panel Data 22 or Blue Channel Bit-6. Can be used as Panel Data 23 or Blue Channel Bit-7.
GPIO4/VIDIN_HS GPIO5/VIDIN_VS	122 121	Can be used as HSYNC Input while using Digital Video Input Port. Can be used as VSYNC Input while using Digital Video Input Port. **(see Digital Input Port).**
GPIO6/IRin	38	Can be used to connect Output from external Infra Red Detector Diode.
GPIO7/IRQin GPIO8/IRQout	41 42	Can be used to trigger an OCM interrupt. Can be used to interrupt an external Master Micro if needed. Level reflects an on-chip status change.
GPIO9/SIPC_SCLK GPIO10/SIPC_SDATA/A18	43 44	Can be used as the Clock (SIPC_SCL) & Data (SIPC_SDA) Signals while enabling the Serial Communication link between FLI8125 and an external Master Controller. GPIO10 could be used to provide Address 18 in case of 512K X8 Parallel ROM interface.
GPIO11/PWM0 GPIO12/PWM1 GPIO13/PWM2 GPIO14/PWM3/SCART16	47 48 51 52	These GPIOs can be used as General purpose PWM outputs (back light intensity control, etc.). And GPIO14 can be used to connect Pin16 (which is a Fast Blank Signal) of SCART connector to check signal status, in case of SCART enabled System.
GPIO15	21	If external SRAM is used in the System this Pin can be used to provide a Chip Select the address of which would range from 18000H to 1FFFFH (app. 412K X8 Space).
VID_DATA_IN_8/GPIO16 VID_DATA_IN_9/GPIO17 VID_DATA_IN_10/GPIO18 VID_DATA_IN_11/GPIO19 VID_DATA_IN_12/GPIO20 VID_DATA_IN_13/GPIO21 VID_DATA_IN_14/GPIO22 VID_DATA_IN_15/GPIO23	145 146 147 148 149 150 151 152	These GPIOs are shared with Digital Video Input Port as VID_D8 to VID_D15. **(see Digital Input Port).**

4.16.10 Low-Bandwidth ADC (LBADC)

A general-purpose ADC is integrated to allow for functions such as keypad scanning or for monitoring system temperature or voltage sensors. The ADC has 8 bits of resolution, and can perform a conversion in 13 TCLK periods (approximately 1 μsec). An analog multiplexer selects one of six analog input pins as the input to the ADC.

Figure 39: Typical Keypad Function



4.16.11 Low Power State

A low power state provides the ability to disable clocks to selected parts of the chip. The OCM_CLK can also be reduced so that the OCM itself consumes less power for TV standby mode. In this mode only IR and LB-ADC (keypad) functionality is available to wake up the system.

4.16.12 Pulse Width Modulation (PWM)

Many of today's LCD back light inverters require both a PWM input and variable DC voltage to minimize flickering due to the interference between panel timing and the inverter's AC timing, and adjust brightness. There are four pins available for PWM outputs: PWM0 (GPIO11), PWM1 (GPIO12), PWM2 (GPIO13) and PWM3 (GPIO14). The duty cycle of these signals is programmable. They may be connected to an external RC integrator to generate a variable DC voltage for a LCD back light inverter. Panel HSYNC is used as the clock for a counter generating this output signal.

4.16.13 Microprocessor External Interface

The Microprocessor Interface allows connection of external devices such as ROMs, FLASH card readers, etc. The interface consists of 8-bit data, 19-bit address bus and chip selects. External device selection is made via programmable chip selects lines. These chip select lines decode the internal Embedded Microprocessor address bus so that the external devices are memory mapped.

Note: The address pins of the External Microprocessor Interface specify the memory offset.

4.17 Bootstrap Configuration Pins

During hardware reset, external ROM address pins associated with bootstrap signals are configured as inputs. These pins have 50KΩ internal pull-down resistor. At the negating edge of RESETn, the value on these pins is latched and stored. This value is readable by the on-chip microcontroller. Install a 10K pull-up resistor to indicate a '1', otherwise a '0' is indicated due to the internal pull-down resistor.

Table 18: Bootstrap Signals

Bootstrap	Pin Name	Description
BT0 (pin # 107) BT1 (pin # 106) BT2 (pin # 105)	A8 A9 A10	These Bootstrap Pins are firmware configured
ROM_1MB (pin # 104)	XOSD_FLD/A11	Force 1 MB ROM support (Serial and parallel) 0 = ROM is 256 K/512K 1 = ROM is I MB
ROM_512K (pin # 103)	XOSD_VS/A12	Forces Address 18 to be enabled for 512K/ 1MB Parallel ROM. 0 = For 256K Flash (Pin meant for Address 18 is available as GPIO) 1 = For 512K/ 1MB Flash (Address 18 is available from FLI8125)
ATMEL_SPI_FLASH (pin # 108)	A7	Forces Atmel serial flash support 0 = For all non Atmel serial flash usage 1 = For Atmel serial flash usage
OP_MODE1 (pin # 102) OP_MODE0 (pin # 101)	XOSD_HS/A13 XOSD_CLK/A14	Operating Mode: Selects external register access method. 00 = UART (normal operation) 01 = 2-wire to JTAG Bridge 10 = 5-wire JTAG port 11 = Reserved
SPI_EN (pin # 100)	ADC_CLAMP/A15	SPI serial ROM interface enable 0 = Parallel ROM Interface 1 = SPI serial ROM and cache controller
OCM_ROM (pin # 96)	ROM_SDO/A16	Selects the initial state of internal OCM ROM 0 = Internal ROM on at top of 1M in X86 address space (normal operation) 1 = Internal ROM off (debug mode – illegal when SPI_EN bootstrap value on ADC_CLAMP/A15 = 1)
OSC_SEL (pin # 95)	ROM_SCLK/A17	Selection of TCLK source. 0 = Use Clock Signal at TCLK Pin of FLI8125 1 = Use external crystal connected to TCLK and XTAL Pins of FLI8125

5 Electrical Specification

The following targeted specifications have been derived by simulation.

5.1 Preliminary DC Characteristics

Table 19: Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages (1,2)	$V_{VDD\_3.3}$	-0.3		3.6	V
1.8V Supply Voltages (1,2)	$V_{VDD\_1.8}$	-0.3		1.98	V
Input Voltage (5V tolerant inputs) (1,2)	$V_{IN5Vtol}$	-0.3		5.5	V
Input Voltage (non 5V tolerant inputs) (1,2)	V_{IN}	-0.3		3.6	V
Electrostatic Discharge(4)	V_{ESD}			±2.0	kV
Latch-up	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		150	°C
Operating Junction Temperature	T_J	0		125	°C
Thermal Resistance (Junction to Air) Natural Convection FLI8125 on 4-layer PCB	θ_{JA_4L}			34.7	°C/W
Thermal Resistance (Junction to Case) Convection (3) FLI8125	θ_{JC}			15.6	°C/W
Soldering Temperature (30 sec.)	T_{SOL}			TBD	°C
Vapor Phase Soldering (30 sec.)	T_{VAP}			TBD	°C

NOTE (1): All voltages are measured with respect to GND.

NOTE (2): Absolute maximum voltage ranges are for transient voltage excursions.

NOTE (3): Based on the figures for the Operating Junction Temperature, θ_{JC} and Power Consumption, the maximum allowed case temperature is calculated as $T_{C(MAX)} = T_{J(MAX)} - P_{(MAX)} \times \theta_{JC}$.

For SXGA operation this is TBD.

NOTE (4): Electrostatic Discharge (ESD): Integrated ESD diodes are provided to protect the device during handling. External on-board ESD diodes are required on the analog RGB inputs, and DDC inputs for protection against electrical overstress (EOS).

Table 20: DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Power					
Power Consumption @ 135 MHz	P_{SXGA}		1.6		W
Power Consumption @ Low Power Mode (1)	P_{LP}		450		mW
3.3V Supply Voltages (AVDD and RVDD)	$V_{VDD\_3.3}$	3.15	3.3	3.45	V
1.8V Supply Voltages (VDD and CVDD)	$V_{VDD\_1.8}$		1.8		V
Supply Current @ CLK =135MHz • 1.8V digital supply (2) • 1.8V analog supply (3) • 3.3V digital supply (4) • 3.3V analog supply (5)	I $I_{VDD\_1.8}$ $I_{AVDD\_1.8}$ $I_{VDD\_3.3}$ $I_{AVDD\_3.3}$		750	 500 60 250 250	mA
Supply Current @ Low Power Mode*	I_{LP}		150		mA

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
High Voltage	V_{IH}	2.0		V_{DD}	V
Low Voltage	V_{IL}	GND		0.8	V
High Current (V_{IN} = 5.0 V)	I_{IH}	-25		25	µA
Low Current (V_{IN} = 0.8 V)	I_{IL}	-25		25	µA
Capacitance (V_{IN} = 2.4 V)	C_{IN}			8	pF
Outputs					
High Voltage (I_{OH} = 7 mA)	V_{OH}	2.4		V_{DD}	V
Low Voltage (I_{OL} = -7 mA)	V_{OL}	GND		0.4	V
Tri-State Leakage Current	I_{OZ}	-25		25	µA

NOTE (1): Low power figures result from setting the ADC and clock power down bits so that only the microcontroller is running.
NOTE (2): Includes all CVDD_1.8 pins.
NOTE (3): Includes VDD18_AB, VDD18_C, VDD18_SC, VDD_RPLL_18 pins.
NOTE (4): Includes all RVDD_3.3 pins.
NOTE (5): Includes pins AVDD_A, AVDD_B, AVDD_C, AVDD_SC, AVDD_ADC, AVDD_RPLL_33, AVDD_LV_33, AVDD_OUT_LV_33, and VDDA33_LBADC.
NOTE (6): Maximum current figures are provided for the purposes of selecting a power supply circuit.

5.2 Preliminary AC Characteristics

All timing is measured to a 1.5V logic-switching threshold. The minimum and maximum operating conditions used were: TDIE = 0 to 125° C, Vdd = 2.35 to 2.65V, Process = best to worst, CL = 16pF for all outputs.

Table 21: Max Speed of Operation

Clock Domain	Max Speed of Operation
Main Input Clock (T_CLK)	24 MHz (19.6608 MHz recommended)
ADC Clock (S_CLK)	165 MHz
Input Clock (IP_CLK)	135 MHz
Reference Clock (R_CLK)	240 MHz
On-Chip Microcontroller Clock (OCM_CLK)	100 MHz
Display Clock (D_CLK)	135 MHz

Figure 40: Digital Input Port Timing Diagram

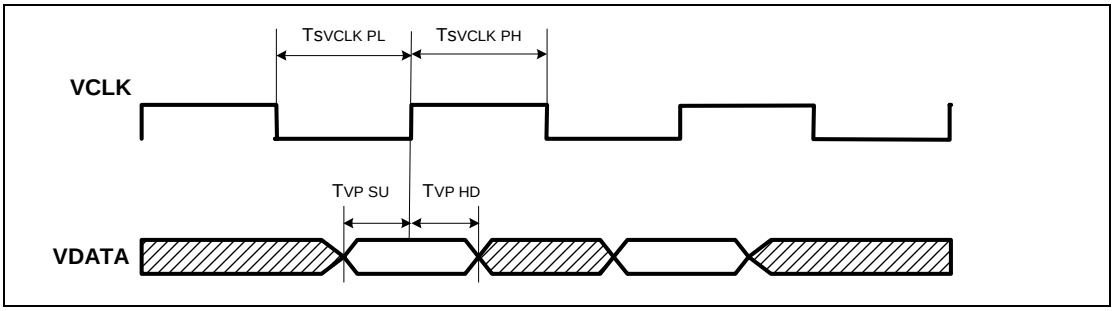


Table 22: ITU656 Video Port Input Timing

Symbol	Parameter	Min	Max	Units
T_{VP_SU}	Setup time for data signals valid before VCLK edge. VCLK edge is programmable to be either rising or falling.	2		nsec.
T_{VP_HD}	Hold time for data/control signals to remain valid after VCLK edge.	3.2		nsec
T_{VCLK_PH}	VCLK high pulse width period	3		nsec
T_{VCLK_PL}	VCLK low pulse width period	3		nsec
F_{VCLK}	VCLK maximum operating frequency.		135	MHz

Figure 41: OCM ROM Interface Timing Diagram

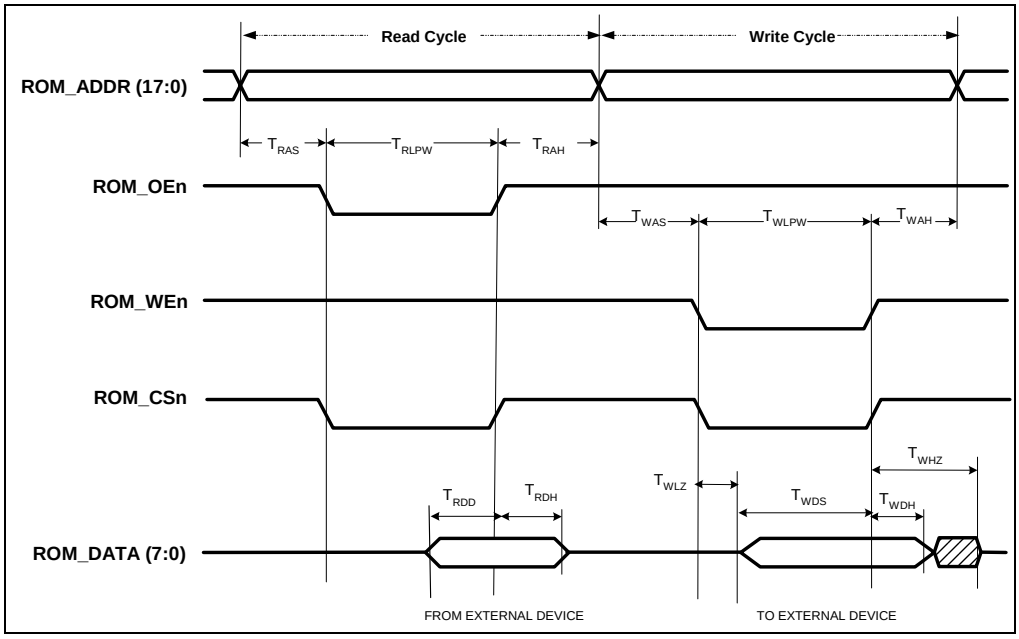


Table 23: OCM ROM Interface Timing

Symbol	Parameter	Min	Max	Units
T_{OCMCLK}	On chip OCM clock period.	10		ns
T_{WAS}	Address setup time provided to falling edge of OCM_WR.	$K1(T_{OCMCLK}) - 3$		ns
T_{WAH}	Address hold time provided from rising edge of OCM_WR.	$T_{OCMCLK} - 3$		ns
T_{WLPW}	OCM_WR active low pulse width	$K2\ (T_{OCMCLK})$		ns

Symbol	Parameter	Min	Max	Units
T_{WDS}	OCM_DATA valid time to OCM_WR rising edge (data set-up time provided)	$K2(T_{OCMCLK}) - 3$		ns
T_{WDH}	OCM_DATA held valid from OCM_WR rising edge. (data hold time provided)	$T_{OCMCLK} - 3$		ns
T_{WLZ}	OCM_DATA Low-Z after OCM_WEn falling edge.	-2	3	ns
T_{WHZ}	OCM_DATA Hi-Z after OCM_WEn rising edge.	$T_{OCMCLK} - 3$	$T_{OCMCLK} + 3$	ns
T_{RAS}	Address setup time provided to falling edge of OCM_RD.	0		ns
T_{RAH}	Address hold time provided from rising edge of OCM_RD.	$T_{OCMCLK} - 3$		ns
T_{RLPW}	OCM_RD low pulse width	$K3 (T_{OCMCLK})$		ns
T_{RDD}	Read data valid before OCM_RD rising edge.	10		ns
T_{RDH}	Read data hold after OCM_RD rising edge.	0		ns

NOTE: Conditions: For ROMC the C_{LOAD} = 16 pF. For ROM_ADDR[17:0] and ROM_DATA[7:0] the C_{LOAD} = 32 pF.

NOTE: K1, K2 and K3 are programmable in units of OCM_CLK.

Table 24: SPI Interface Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
F_{CLK}	Serial Clock frequency		50	MHZ
T_{SCKH}	Serial Clock High Time	5		ns
T_{SCKL}	Serial Clock Low Time	5		ns
T_{SCKR}	Serial Clock Rise Time		5	ns
T_{SCKF}	Serial Clock Fall Time		5	ns
T_{CES}	CE# active Setup time	10		ns
T_{CEH}	CE# active Hold time	10		ns
T_{CHS}	CE# Not active Setup time	10		ns
T_{CHH}	CE# Not active Hold time	10		ns
T_{CPH}	CE# High time	100		ns
T_{CHZ}	CE# High to High-Z output		20	ns
T_{CLZ}	SCK Low to Low-Z Output	0		ns
T_{DS}	Data In Setup Time	5		ns
T_{DH}	Data In Hold Time	5		ns
T_{OH}	Output Hold from SCK change	0		ns
T_V	Output Valid from SCK		20	ns
T_{SE}	Sector Erase		25	ms
T_{BE}	Block Erase		25	ms
T_{SCE}	Chip Erase		100	ms
T_{BP}	Byte Program		20	µs

Figure 42: FLI8125 SPI Output or Serial Interface SPI ROM Input Timing

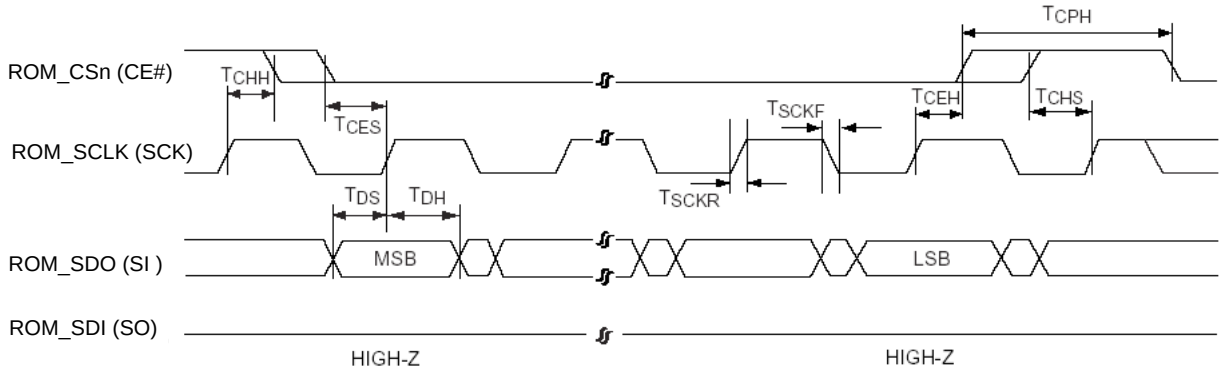
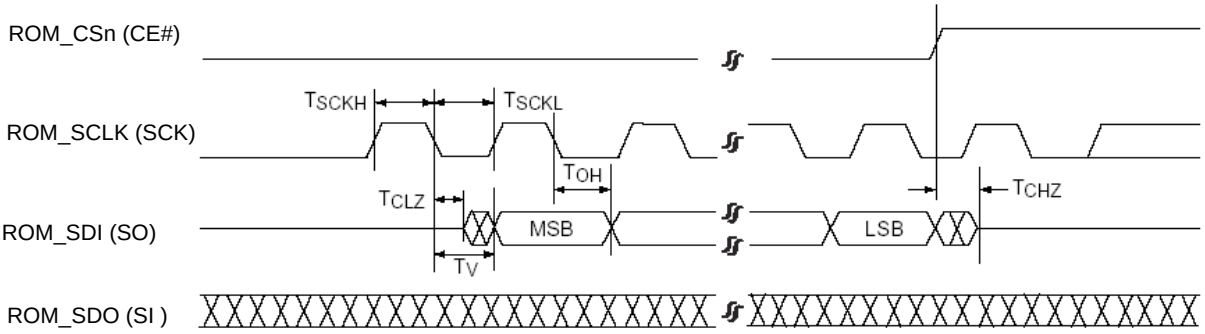


Figure 43: FLI8125 SPI Input or Serial Interface SPI ROM Output Timing

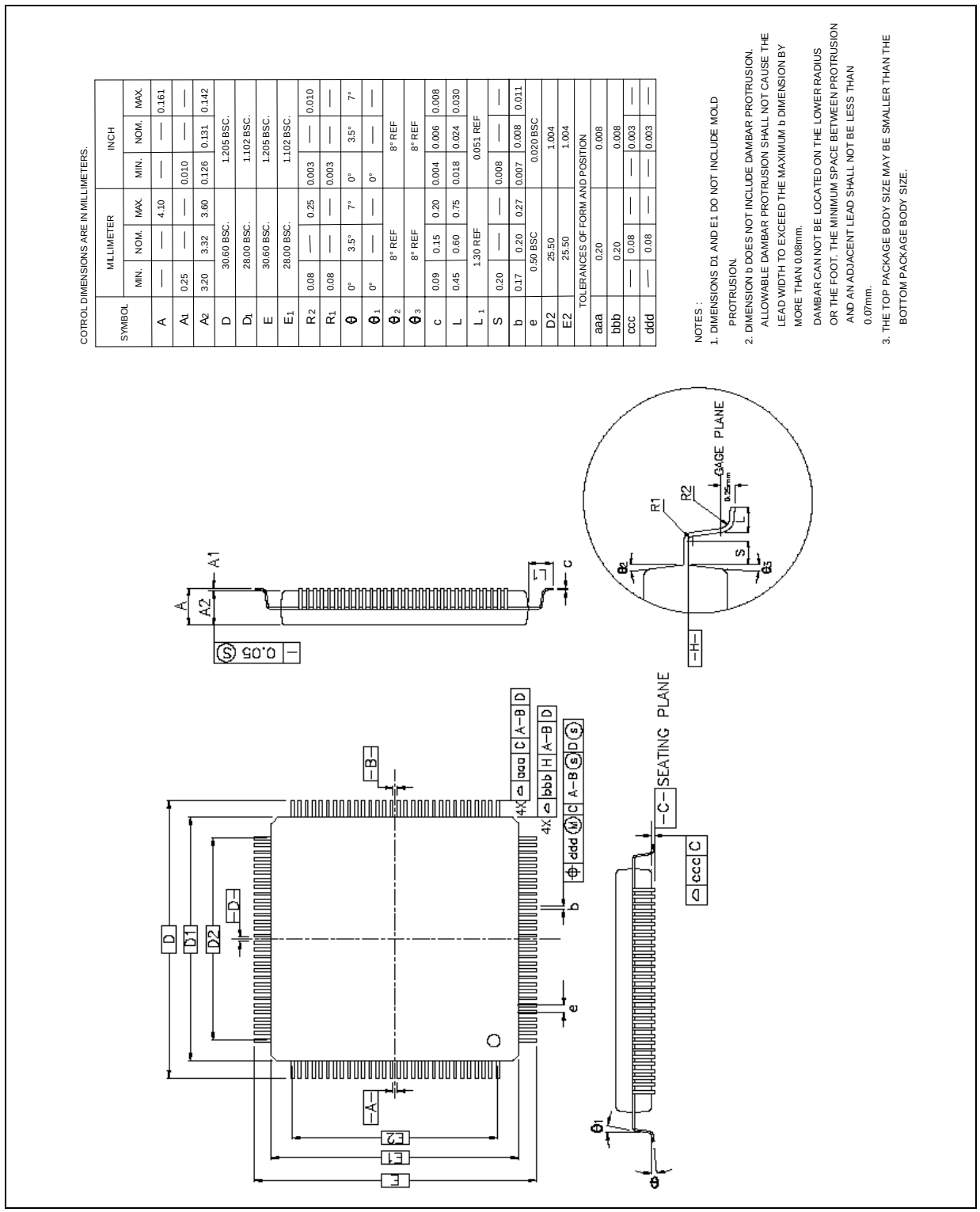


6 Ordering Information

Order Code	Application	Package	Temperature Range
FLI8125-BC	SXGA	208-pin PQFP	0-70°C
FLI8125 LF-BC	SXGA	208-pin PQFP Lead-free	0-70°C

7 Package Specification

Figure 44: FLI8125 208 Pin PQFP Package Drawing

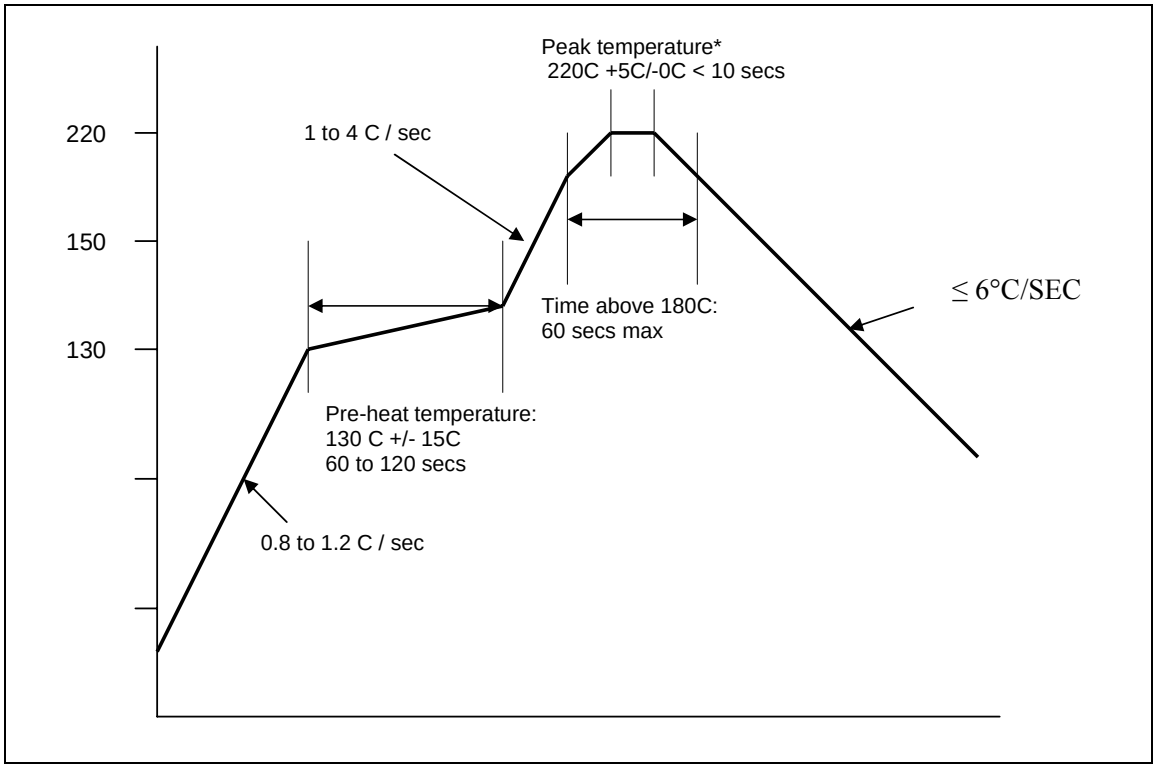


8 Solder Profiles

8.1 Regular QFP Reflow Profile

The following is the recommended solder reflow profile for Genesis Microchip regular QFP devices.

Figure 45: Regular QFP Solder Reflow Profile



8.2 Lead-Free QFP Reflow Profile

The following is the recommended solder reflow profile for Genesis Microchip lead free QFP devices.

Figure 46: Lead free QFP Solder Reflow Profile