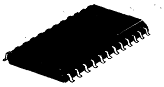


M5M5117FP, -15

16384-BIT (2048-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5117FP series of 2048-word by 8-bit asynchronous silicon gate CMOS static RAM operates on a single 5V power supply and is designed for easy use in applications requiring battery backup.

A chip select input, $\overline{S}$, is available to provide the minimum standby current with battery back-up while an output enable input, $\overline{OE}$, enables high-speed memory access.

The series features pin compatibility with the M5L2716K 16K EPROM and M58725P 16K static RAM, and it is packaged in a small 24-pin plastic DIL flat package.

FEATURES

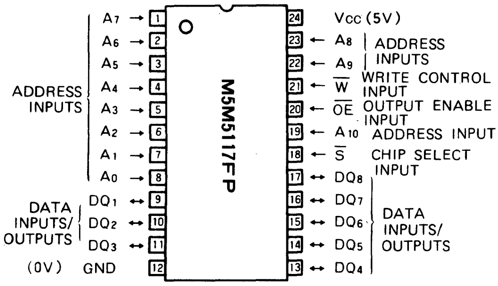
Type name	Access time (max)	$\overline{OE}$ access time (max)	Current consumption	
			Active (max)	Stand-by (max)
M5M5117FP-15	150ns	80ns	50mA	15μA
M5M5117FP	200ns	100ns		

- Single 5V power supply.
- External clock and refresh operation not required.
- Data can be held with 2V supply voltage.
- All inputs, and outputs are directly TTL compatible.
- All outputs are 3-state with OR-tie capability.
- Easy expansion of memory capacity with chip select signal.
- Common input/output for data pins.
- Pin compatibility with M5L2716K 16K EPROM and M58725P 16K static RAM.

APPLICATIONS

Battery drive, small-capacity memory units with battery back-up

PIN CONFIGURATION (TOP VIEW)



Outline 24P2W

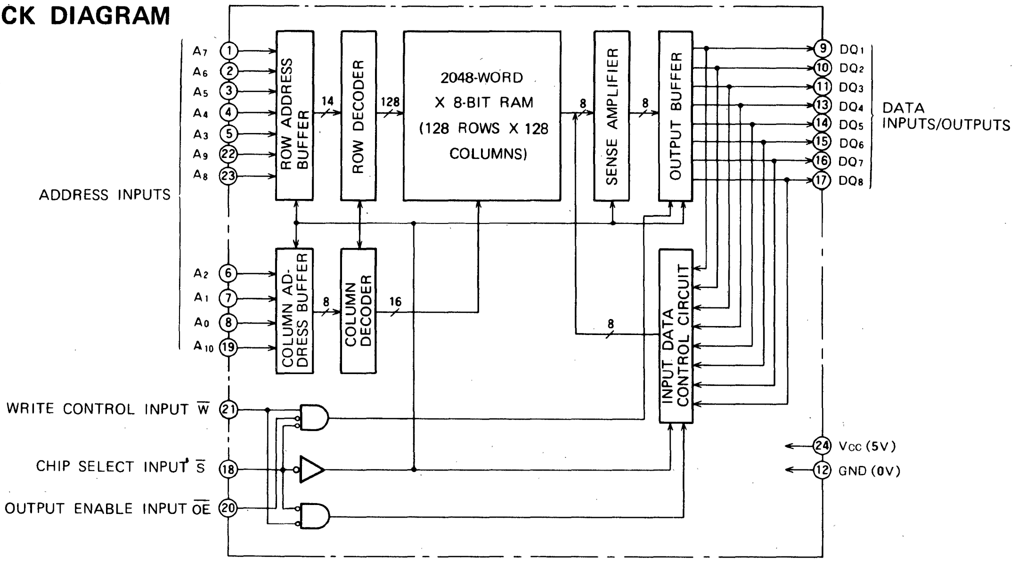
FUNCTION

The M5M5117FP series has a 2048-word by 8-bit configuration. It operates on a single 5V supply and its inputs/outputs are directly TTL compatible. Its completely static circuitry obviates the need for external clock and refresh operations and makes it very easy to use.

The data of the DQ pin are written when the address is designated by address signals $A_0 \sim A_{10}$, the $\overline{S}$ signals turns low-level, and the $\overline{W}$ signal is set low.

When for the reading operation the $\overline{W}$ signal is set high, the $\overline{S}$ and $\overline{OE}$ signals are set low, pin DQ is set to the output mode and the address is designated by signals $A_0 \sim A_{10}$, the data of the designated address are output to pin DQ.

BLOCK DIAGRAM



When signal $\overline{S}$ is set high, the chip is set to a non-select status in which neither reading nor writing is possible. Since the output floats (high-impedance state), OR-tie is possible with the other chip output pins. When the $\overline{OE}$ signal is set high, the output is put in the floating state. When $\overline{OE}$ is set high during writing for use with an I/O bus system, bus contention between the input and output data can be avoided.

The standby mode is established when signal $\overline{S}$ is set to V_{CC}. The supply current is now reduced to the very low level of 15μA (max) and the data in the memory are retained even if the supply voltage falls to 2V, permitting power-down during non-operation or battery back-up during power failures.

OPERATION MODES

$\overline{S}$	$\overline{OE}$	$\overline{W}$	Mode	DQ	I_{CC}
H	X	X	Non-select	High impedance	Standby
L	X	L	Write	D_{IN}	Active
L	L	H	Read	D_{OUT}	Active
L	H	H	Output disable	High impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to GND	$-0.3 \sim 7$	V
V_I	Input voltage		$-0.3 \sim V_{CC}+0.3$	V
V_O	Output voltage		$0 \sim V_{CC}$	V
Pd	Power dissipation	$T_a=25°C$	700	mW
Topr	Operating free-air ambient temperature		$0 \sim 70$	°C
Tstg	Storage temperature		$-65 \sim 150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a=0 \sim 70°C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	Low-level input voltage	−0.3		0.8	V
V_{IH}	High-level input voltage	2.2		$V_{CC}+0.3$	V

ELECTRICAL CHARACTERISTICS ($T_a=0 \sim 70°C$, $V_{CC}=5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.2		$V_{CC}+0.3$	V
V_{IL}	Low-level input voltage			−0.3		0.8	V
V_{OH}	High-level output voltage		$I_{OH}=-1mA$	2.4			V
V_{OL}	Low-level output voltage		$I_{OL}=2.1mA$			0.4	V
I_I	Input current		$V_I=0 \sim V_{CC}$			±1	μA
I_{OZH}	Off-state high-level output current		$\overline{S}$ or $\overline{OE}=V_{IH}$, $V_O=2.4V \sim V_{CC}$			1	μA
I_{OZL}	Off-state low-level output current		$\overline{S}$ or $\overline{OE}=V_{IH}$, $V_O=0V$			−1	μA
I_{CC1}	Supply current	**M5M5117FP-15**	$V_I(\overline{S})=0V$ Output pin open Other inputs $=V_{CC}$			45	mA
		M5M5117FP			30	45	mA
I_{CC2}	Supply current	**M5M5117FP-15**	$V_I(\overline{S})=V_{IL}$ Output pin open Other inputs $=V_{IH}$			50	mA
		M5M5117FP			35	50	mA
I_{CC3}	Standby supply current		$\overline{S}=V_{CC}-0.2V$, Other inputs $=0 \sim V_{CC}$			15	μA
I_{CC4}	Standby supply current		$\overline{S}=V_{IH}$, Other inputs $=0 \sim V_{CC}$			2	mA
Ci	Input capacitance ($T_a=25°C$)		$V_I=GND$, $V_i=25mVrms$, $f=1MHz$			6	pF
Co	Output capacitance ($T_a=25°C$)		$V_O=GND$, $V_O=25mVrms$, $f=1MHz$			8	pF

Note 1: Current flowing into an IC shall be positive (no sign).
2: Typical values: $V_{CC}=5V$, $T_a=25°C$.

SWITCHING CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

READ CYCLE

Symbol	Parameter	M5M5117FP-15			M5M5117FP			Unit
		Limits			Limits			
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	150			200			ns
$t_{a\,(A)}$	Address access time			150			200	ns
$t_{a\,(S)}$	Chip select access time			150			200	ns
$t_{a\,(OE)}$	Output enable access time			80			100	ns
$t_{dis\,(S)}$	Output disable time from S			50			60	ns
$t_{dis\,(OE)}$	Output disable time from OE			50			60	ns
$t_{en\,(S)}$	Output enable time from S	15			15			ns
$t_{en\,(OE)}$	Output enable time from OE	15			15			ns
$t_{v\,(A)}$	Data valid time from address	20			20			ns

TIMING REQUIREMENTS (Ta=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

WRITE CYCLE

Symbol	Parameter	M5M5117FP-15			M5M5117FP			Unit
		Limits			Limits			
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	150			200			ns
$t_{w(W)}$	Write pulse width	90			120			ns
$t_{su\,(A)}$	Address set-up time	0			0			ns
$t_{su\,(S)}$	Chip select set-up time	90			120			ns
$t_{su\,(D)}$	Data set-up time	40			60			ns
$t_{h\,(D)}$	Data hold time	0			0			ns
$t_{rec\,(W)}$	Write recovery time	10			10			ns
$t_{su\,(OE)}$	Output enable set-up time	40			40			ns
$t_{dis\,(OE)}$	Output disable time from OE			50			60	ns
$t_{dis\,(W)}$	Output disable time from write			50			60	ns
$t_{en\,(W)}$	Output enable time from write	15			15			ns

POWER-DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC\,(PD)}$	Power-down supply voltage		2			V
$V_{I\,(S)}$	Chip select input voltage	$2.2V \leqq V_{CC\,(PD)}$	2.2			V
		$2V \leqq V_{CC\,(PD)} \leqq 2.2V$		$V_{CC\,(PD)}$		V
$I_{CC\,(PD)}$	Power-down supply current	V_{CC}=3V, Other inputs =3V			10	μA

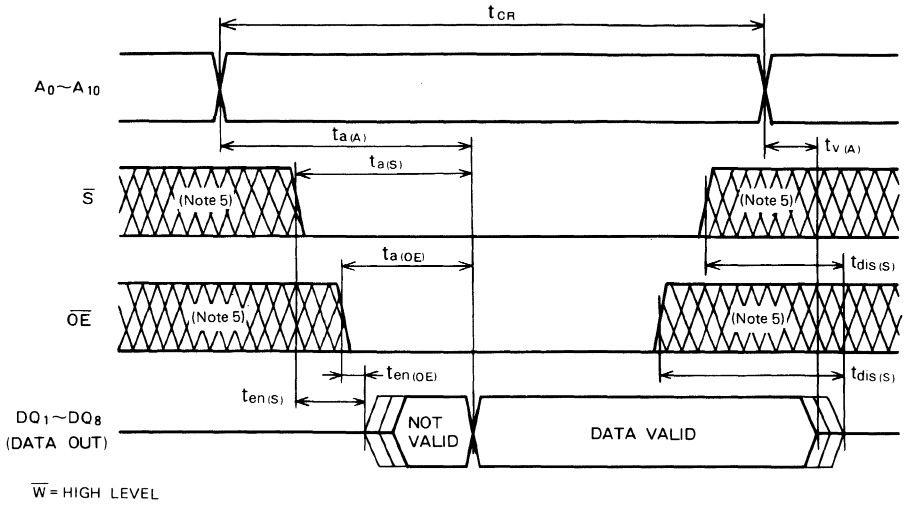
Note 3: When $\overline{S}$ is operated at 2.2V (V_{IH} min), the supply current at which $V_{CC\,(PD)}$ is between 4.5V and 2.4V, is specified by I_{CC4}.

TIMING REQUIREMENTS (Ta=0~70°C, unless otherwise noted)

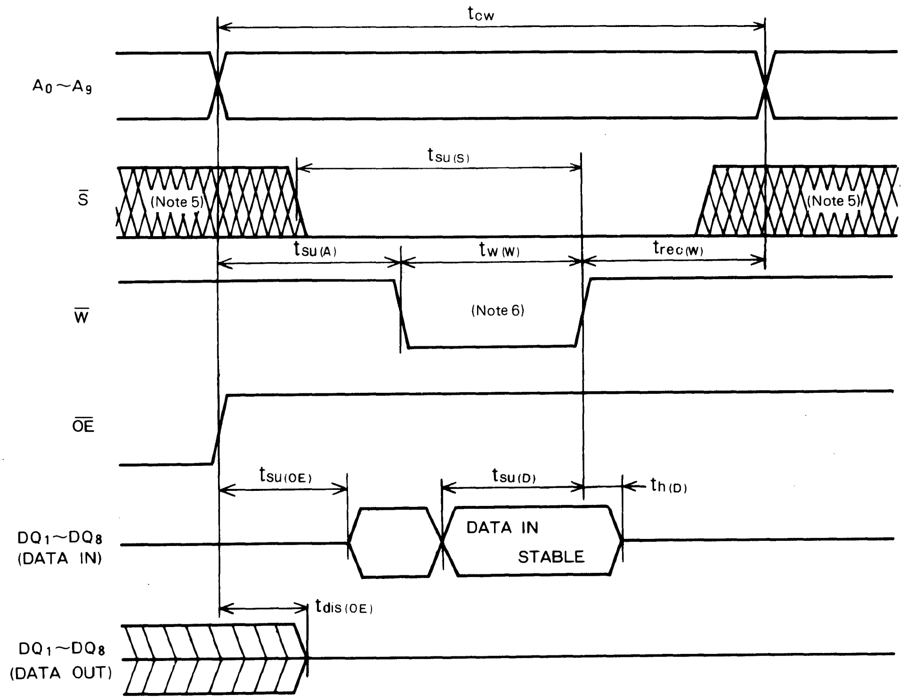
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\,(PD)}$	Power-down set-up time		0			ns
$t_{rec\,(PD)}$	Power-down recovery time		t_{CR}			ns

TIMING DIAGRAM

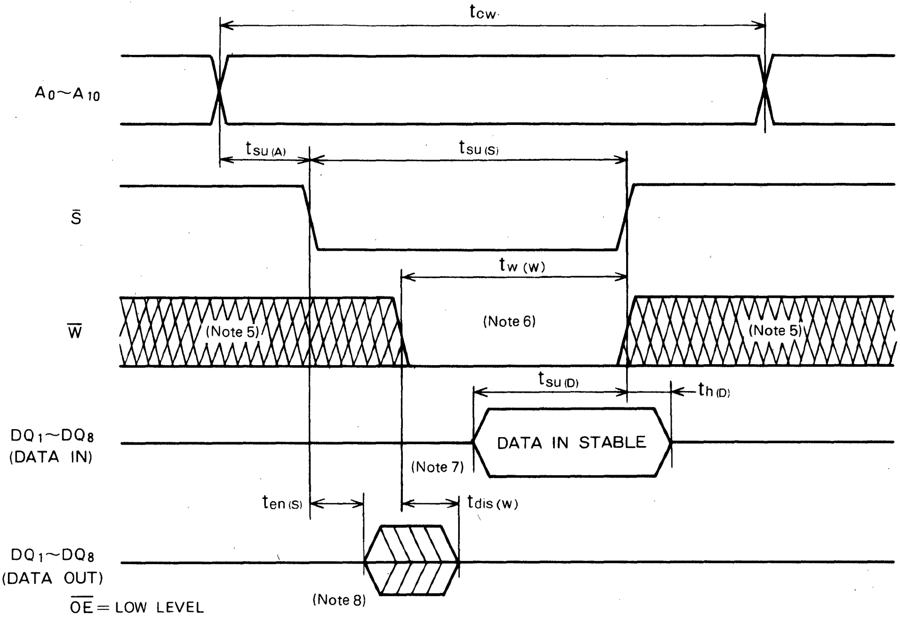
Read cycle



Write cycle (W̄ control)



Write cycle ($\overline{S}$ control)



Note 4: Test conditions
Input pulse level: 0.4 ~ 2.4V
Input pulse risetime and falltime: 10ns
Load: 1TTL, C_L = 100pF
Reference level: 1.5V

Note 5: Hatching indicates the don't care inputs.
6: Writing is performed while $\overline{S}$ and $\overline{W}$ are in the low-level overlap period.
7: The output is kept in the high-impedance state when $\overline{W}$ falls simultaneously with, or before, the $\overline{S}$ falls.
8: A reverse phase signal should not be supplied when DQ is in the output mode.

POWER-DOWN CHARACTERISTICS