Discontinued Product

OKI Semiconductor

MSM60808

PCI to PCMCIA R2.1/CardBus Controller (PPCC)

FEATURES

- PCI Local Bus Specification Rev. 2.1 Compliant
- PC Card Standard 95 Compliant
- PC Card auto-detect configuration
- 2-socket multifunction PCI device
- Intel 82365 register-compatible
- Power supply voltage +3.0~+3.6 V (core)
  +3.0~+3.6 V, +4.5~+5.5 V (I/O)
- Maximum operating frequency: 33 MHz
- Serial interface with power control IC TI TPS2202AI
- ZV port mode supported
- Clock control (CLKRUN#) supported
- Package: 208-pin plastic LQFP (LQFP208-P-2828-0.50-K) (Product name : MSM60808GS-K)

Table of Contents

1. General Description

The MSM60808 is a bridge chip to interface a PCI bus and a two-socket PC Card bus. The PCI bus interface is based on the PCI 2.1 standard. The PC Card interface works with 16-bit cards and 32-bit CardBus cards based on the PCMCIA 2.1/JEIDA 4.2 standard. This new PC Card standard enables high-speed data transfer at a maximum clock frequency of 33 MHz, with a data width of 8 bits or 16 bits for 16-bit PC Cards and a data width of 32 bits for CardBus PC Cards.

When a PC Card is inserted in a socket, the MSM60808 automatically detects the card type and the power supply voltage requested by the card. After it detects card type and power supply voltage, the MSM60808 automatically switches to 16-bit PC Card mode or CardBus PC Card mode depending on the type of card inserted. In 16-bit PC Card mode, the MSM60808 operates as a target device on the PCI bus, and in CardBus PC Card mode, the MSM60808 operates as a PCI-to-PCI bridge. After this, software will configure the MSM60808's internal control registers, and data transfer from the PCI bus to the card can begin.

After the card's power supply voltage has been confirmed, the MSM60808 performs serial data access to the TPS2202AI voltage control chip and applies voltage to the card using the TPS2202AI. When the card is removed, the MSM60808 automatically stops applying voltage to the socket.

After a card is inserted, it will have numerous status changes and request service routines, which will generate various interrupts. These interrupts can be made on the ISA bus IREQ signal or the PCI bus INT# signal.

1.1 PCI Interface

The MSM60808 is a multifunction PCI device that supports PC Cards in two sockets.

When a CardBus card is inserted in a socket, the MSM60808 will operate as a PCI-to-PCI bridge. When a 16-bit card is inserted, the MSM60808 will operate as a PCI target device. Table 1.1 shows each of the bus commands supported by the MSM60808 for different cards. When MSM60808 is a target, the response speed of DEVSEL# is medium speed.

Table 1.1 PCI Bus Commands For Different Cards

C/BE[3:0]#	Command Type	16-Bit Cards	Target CardBus Cards	Master CardBus Cards	Buffer Control
0000	Interrupt Acknowledge	Not Supported	Not Supported	Not Supported	—
0001	Special Cycle	Not Supported	Not Supported	Not Supported	—
0010	IO Read	Supported	Supported	Supported	No
0011	IO Write	Supported	Supported	Supported	No
0100	Reserved	—	—	—	—
0101	Reserved	—	—	—	—
0110	Memory Read	Supported	Supported	Supported	Yes
0111	Memory Write	Supported	Supported	Supported	Yes
1000	Reserved	—	—	—	—
1001	Reserved	—	—	—	—
1010	Configuration Read	Supported	Supported	Not Supported	No
1011	Configuration Write	Supported	Supported	Not Supported	No
1100	Memory Read Multiple	Supported	Supported	Supported	No
1101	Dual Address Cycle	Not Supported	Not Supported	Not Supported	—
1110	Memory Read Line	Supported	Supported	Supported	No
1111	Memory Write Invalidate	Supported	Supported	Supported	No

Data transfers from PCI to CardBus and from CardBus to PCI are performed as delayed transactions for configuration read/write cycles, IO read/write cycles, and memory read cycles, and are performed as posted writes for memory write cycles. For 16-bit cards, this applies to transfers from PCI to the card.

The MSM60808 can also control the depth of the internal FIFO used for data transfers (memory read/write cycles). This control enables switching between single transfers and burst transfers.

The PCI lock function and bus parking function are not supported.

1.2 CardBus Card Interface

The maximum operating frequency between the PCI bus and the MSM60808 is 33 MHz. The CardBus clock outputs the PCI system clock as is, so the CardBus maximum operating frequency is also 33 MHz. When a CardBus card is inserted, the MSM60808 operates as a PCI-to-PCI bridge. Applicable bus commands are shown in Table 1.1.

Configuration write cycles also issue special cycles.

The MSM60808 has an internal counter to measure the number of retries received, so when a target card returns a retry the MSM60808 will issue commands to the card until the counter finishes. It transfers target aborts and master aborts generated by the CardBus to the PCI bus in accordance with the bridge control register settings.

For master cards, data transfers are processed as delayed transactions and posted writes, identical to the PCI interface. The response speed of CDEVSEL# is also medium speed.

1.3 16-Bit Card Interface

The MSM60808 uses a data width of 32 bits to transfer data between itself and the PCI bus, and a data width of either 8 bits or 16 bits to transfer data between itself and a 16-bit PC Card. Applicable bus commands are shown in Table 1.1.

When a 16-bit card is inserted, the MSM60808's 16-bit card control logic will be selected. The card interface will be Intel 82365 compatible. The 16-bit card control logic transfers data by converting the 32-bit data of the PCI bus to the 8-bit or 16-bit data requested by the PC Card. Memory write commands are performed as posted writes and all other commands use delayed transactions, so this conversion does not have a large effect on the transfer efficiency of the PCI bus. As a result data can be transferred without degrading system transfer speed.

The MSM60808 supports the READY/BUSY# signal of memory cards and INPACK# signal of I/O cards.

1.4 Configuration

The MSM60808 is a CardBus controller for two sockets, so it has two independent configuration spaces. As shown in Table 1.2, Function 0 is used for Socket A and Function 1 is used for Socket B. In order to access the configuration of a CardBus card, MSM60808 decodes the Function Number Field, sets CAD[1:0] to 00b, and issues a configuration on the CardBus.

When the bus number of a Type 1 configuration command matches MSM60808's CardBus number (CBBUSN), MSM60808 responds to the configuration cycle and generates a Type 0 configuration cycle on the CardBus. If the bus number is greater than the CardBus number (CBBUSN), and if it is less than or equal to the subordinate bus number (SUBBUSN), then MSM60808 will forward the Type 1 configuration cycle.

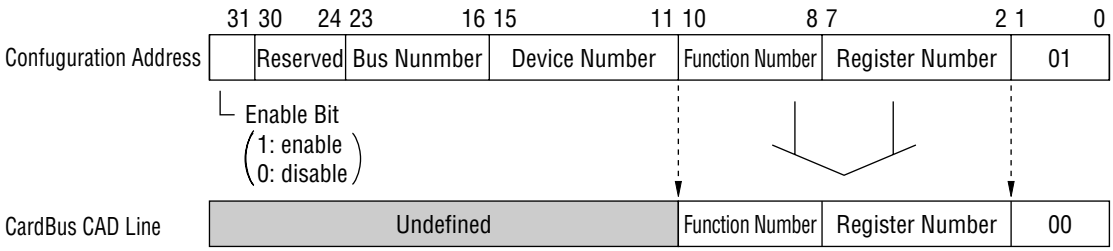


Figure 1.1 Configuration Type 1 → Type 0 Conversion

Table 1.2 Slot Selected by Function Number

Function Number	Selected socket
0h	Socket A
1h	Socket B
2h~3h	Reserved

1.5 PC Card Registers

In order to control PC Cards in two sockets, MSM60808 has CardBus card registers and 16-bit card registers for each socket.

The CardBus registers are configured from two types of registers (CardBus Socket Status Register and Clock Control Register). These registers are mapped to memory space by the PC Card Socket Status Address Register (PCCBADR) and can be directly accessed.

The 16-bit card registers are configured from four types of registers (Setup Register, Interrupt Control Register, IO Mapping Control Register, and Memory Mapping Control Register). These registers can be mapped to both memory space and IO space. When mapped to memory space, they can be directly accessed using the PC Card Socket Status Address Register (PCCBADR), similarly to the CardBus registers. In this case the 16-bit card registers are located in the upper 2 Kbytes of the 4 Kbytes saved by the PC Card Socket Status Address Register (PCCBADR). When mapped to IO space, they can be indirectly accessed using the Index/Data Register at the address pointed to by the R21 Register Base Address (R21BADR).

1.6 Determining Card Types

MSM60808 decodes the CVS[2:1] and CCD[2:1] pins as shown in Table 1.3, determines the card type and voltage to apply, and then reflects the result in MSM60808's internal Socket Present Register. After MSM60808 has checked the card, it switches its internal control logic to conform to the type of card inserted. The types of cards that may be inserted into the sockets correspond to the cases shown in Figure 1.2.

Table 1.3 CCD#[2:1]/CVS[2:1] and PC Card Interface

CCD2#	CCD1#	CVS2	CVS1	Key	InterFace	Voltage
Ground	Ground	Open	Open	5V	16bit PC Card	5V
Ground	Ground	Open	PD	5V	16bit PC Card	5V and 3.3V
Ground	Ground	Ground	PD	5V	16bit PC Card	5V and 3.3V
Ground	Ground	Open	Ground	LV	16bit PC Card	3.3V
Ground	Connect to CVS1	Open	Connect to CCD1#	LV	CardBus PC Card	3.3V
Ground	Ground	Ground	Ground	LV	16bit PC Card	3.3V and X.XV
Connect to CVS2	Ground	Connect to CCD2#	Ground	LV	CardBus PC Card	3.3V and X.XV
Connect to CVS1	Ground	Ground	Connect to CCD2#	LV	CardBus PC Card	3.3V, X.XV and Y.YV
Ground	Ground	Ground	Open	LV	16bit PC Card	X.XV
Connect to CVS2	Ground	Connect to CCD2#	Open	LV	CardBus PC Card	X.XV
Ground	Connect to CVS2	Connect to CCD1#	Open	LV	CardBus PC Card	X.XV and Y.YV
Connect to CVS1	Ground	Open	Connect to CCD2#	LV	CardBus PC Card	Y.YV
Ground	Connect to CVS1	Ground	Connect to CCD1#	Reserved		
Ground	Connect to CVS2	Connect to CCD1#	Ground	Reserved		

Note: X.XV and Y.YV have not been standardized and are not supported.

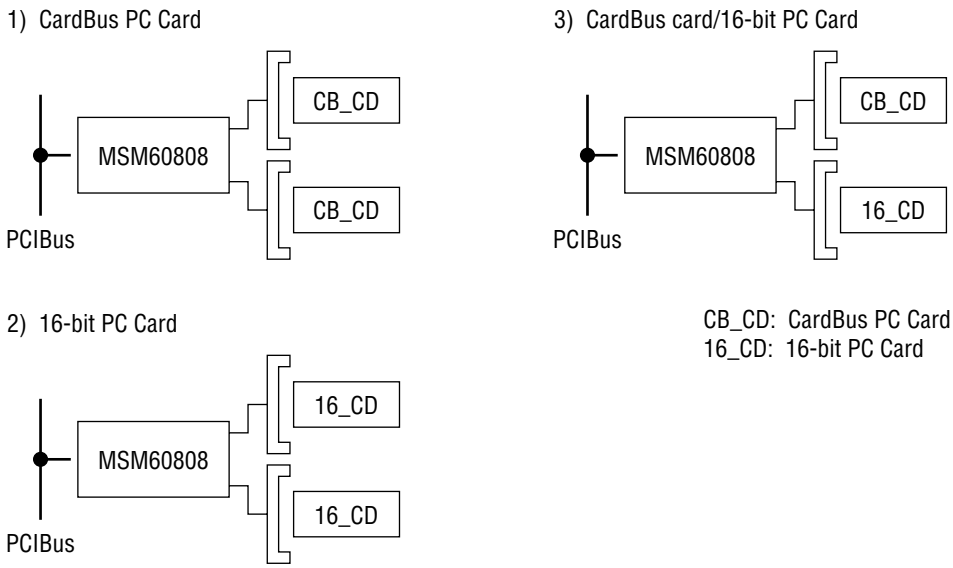


Figure 1.2 Card Combinations

1.7 Address Decoding

The MSM60808's Base Registers and Limit Registers (MEMBASE0/1, MEMLIMIT0/1, IOBASE0/1L, IOBASE0/1H, IOLIMIT0/1L) define the address window for forwarding transactions from the PCI bus to the CardBus.

Two address windows, a memory window and IO window, can be opened. The range of these windows can be set up to 4 GB for memory and 64 KB for IO in 4 KB units. The windows can be placed at any position in the 4 GB space with these registers.

These registers are used and decoded when transactions are data transfers forwarded from the CardBus to the PCI bus to determine MSM60808's CardBus address range. Figure 1.3 shows MSM60808's address decode method when a CardBus card is inserted.

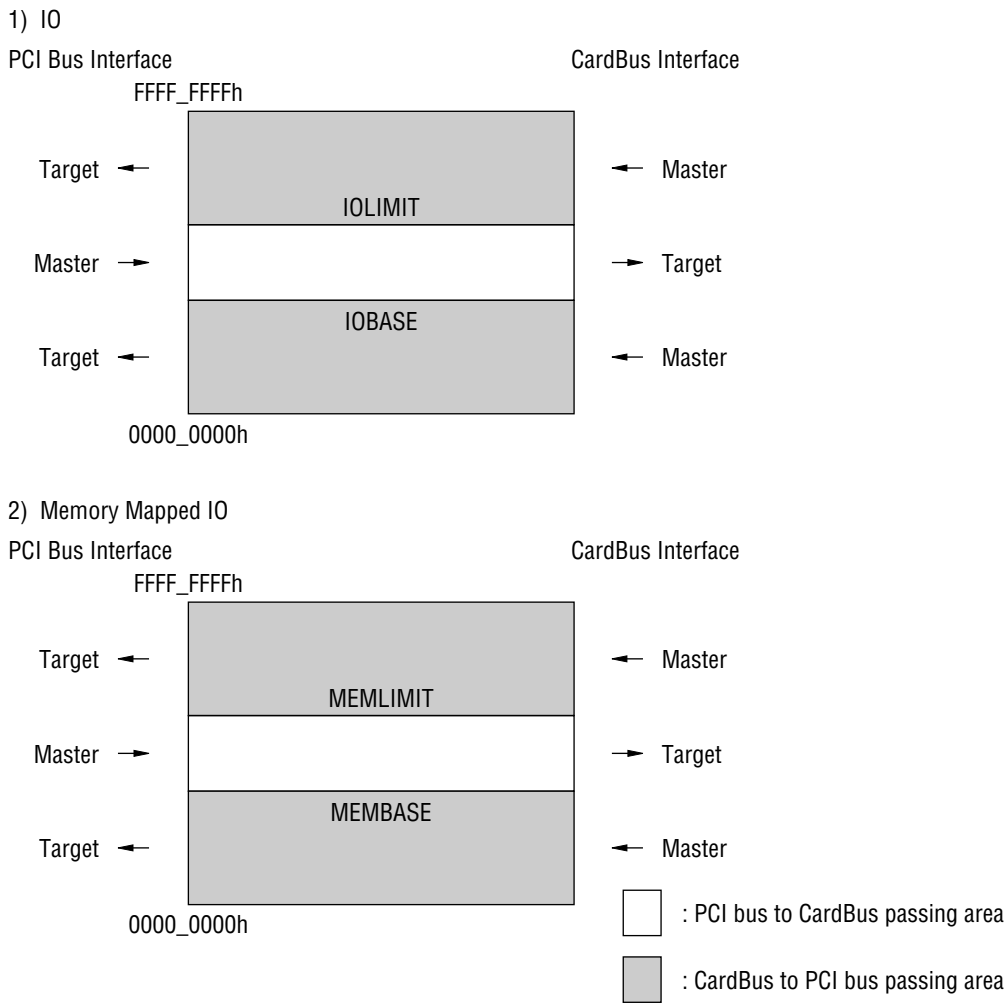


Figure 1.3 Address Decoding Method (CardBus PC Card)

When a 16-bit card is inserted, the IO mapping control registers (IOCREG, IOSL[1:0], IOSH[1:0], IOSTL[1:0], IOSTH[1:0]) or memory mapping registers (SML[4:0], SMH[4:0], SMSTL[4:0], SMSTH[4:0]) determine whether or not a PCI cycle will be transferred to the card. Up to two windows in IO space and five windows in memory space can be opened with a 16-bit card. For memory cards the offset registers (OFFL[4:0], OFFH[4:0]) are used to convert PCI addresses to card addresses. Figure 1.4 shows the relationship of PCI and 16-bit cards.

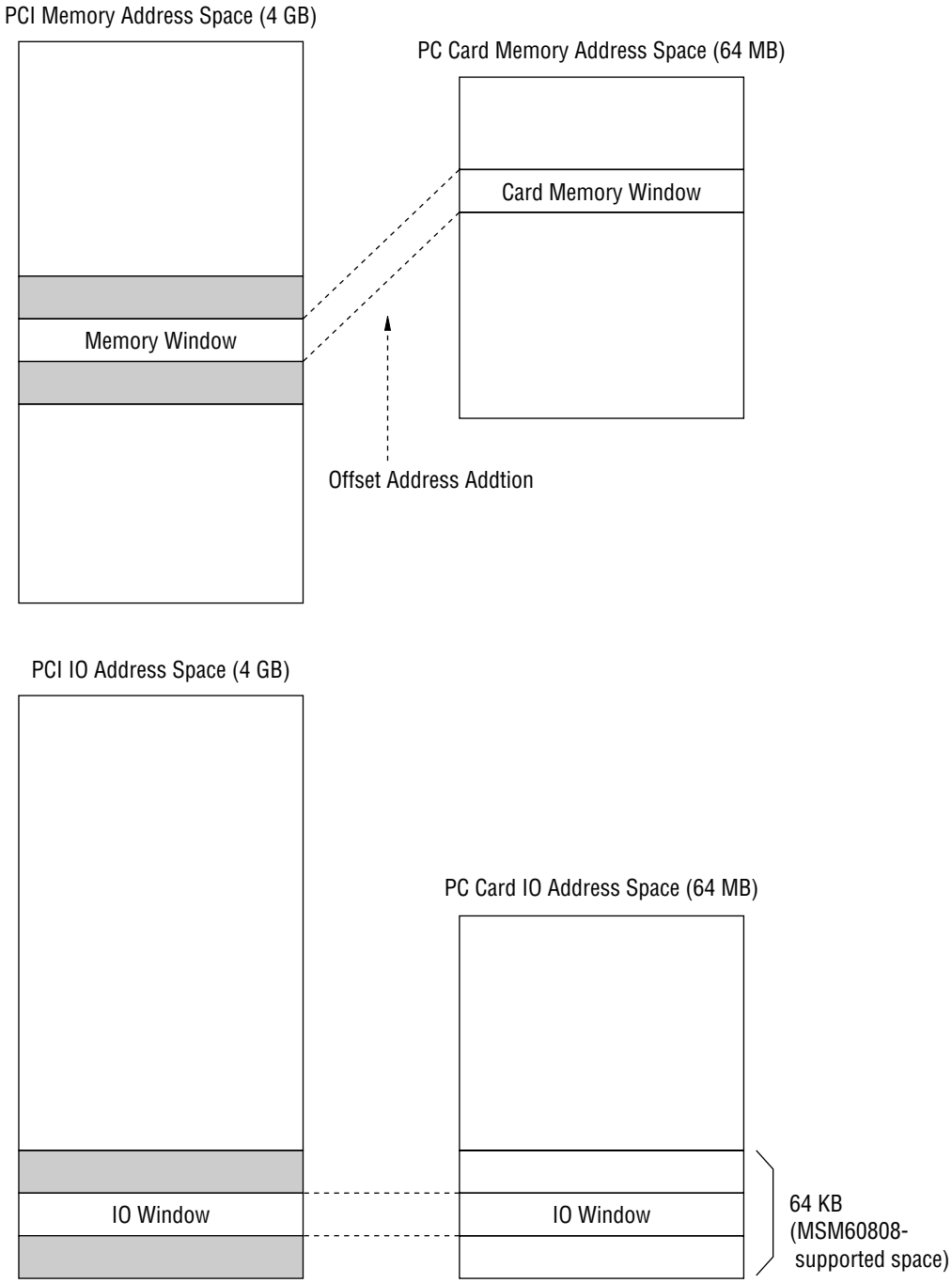


Figure 1.4 Address Decoding Method (16-bit PC Card)

1.8 Interrupts

Interrupts are used to inform the system of card status changes like card detect pin transitions, battery discharge, and ready transitions, and of interrupt service requests from the PC Card to the system. For card status changes, 16-bit memory cards will generate interrupts when a bit in the Card Status Change Register (CSTCH) changes, and CardBus cards will generate interrupts when a bit in the Event Register (EVENT) changes. Generation of these card status change interrupts can be controlled by setting bits in the Card Status Change Interrupt Configuration Register (CSCICR) for 16-bit cards or the Interrupt Mask Register (MASK) for CardBus cards. For service requests, cards will generate interrupts to the system when card pin signal transitions are received (IREQ for 16-bit IO cards or CINT for CardBus cards). Table 1.4 lists the PC Card interrupt types and descriptions.

The MSM60808 supports ten ISA-compatible direct system interrupts (IREQ) and PCI interrupts (INTA/B#).

For PCI interrupts INTA# is assigned to Socket A and INTB# is assigned to Socket B. The ISA and PCI lines are multiplexed on the same pins, with the signals switched by setting bits in the Bridge Control Register (BRGCTL) and Card Control Register (CDCTL).

System interrupts can be executed without modification on ISA-compatible platforms. PC Card interrupts can be directly connected to the IREQ line. Edge-triggered system interrupt signals are supported with 16-bit cards.

Table 1.4 PC Card Interrupts

Card Type	Event	Interrupt Type	Signal Line	Description
16-bit memory	Battery status change	CSC	BVD1	Notification of battery status chante by BVD1 signal
		CSC	BVD2	Notification of battery status chante by BVD2 signal
	Card ready	CSC	READY	Notification PC Card can accept data transfers
16-bit IO	Card status change	CSC	STSCHG#	Notification of card status change from PC Card
	Interrupt request	FUNC	IREQ#	Interrupt service request from PC Card
CardBus	Card status change	CSC	CSTSCHG	Notification of card status change from PC Card
	Interrupt request	FUNC	CINT#	Interrupt service request from PC Card
	Power cycle done	CSC	—	Notification to system of power cycle completion
All cards	Card insertion/removal	CSC	CD1#/CCD1# CD2#/CCD2#	Notification of card insertion/ removal by CD pin change

1.9 Socket Power Control

The MSM60808 has functions to control power. It performs socket power control through its internal Socket Present Register (PRESENT), Socket Control Register (CONTROL), CCD#[2:1], and CVS[2:1].

Power-up of both 16-bit cards and CardBus cards is done after card detection by software reading the PRESENT register and writing the contents to the CONTROL register. The MSM60808 uses the contents to output signals directly to the TI TPS2202AI, a socket power control IC.

The TI TPS2202AI has three control lines (clock, data, latch) with which MSM60808 performs serial data transfers. Transfer speed is the clock from dividing the PCI bus clock by 16. Figure 1.5 and Table 1.5 show the serial data transfer protocol and contents. For details on the TI TPS2202AI, please refer to the TI TPS2202AI data sheet.

When PCIRST# is generated, register power is reset, prompting power-down. Power-down is performed automatically, without software writes to registers. For card removal power-down, data will be transferred only to the socket from which the card was removed. However, when reset by PCIRST#, the D8 bit (shutdown bit) will output low and both sockets will power down (at other times the D8 bit will always output high).

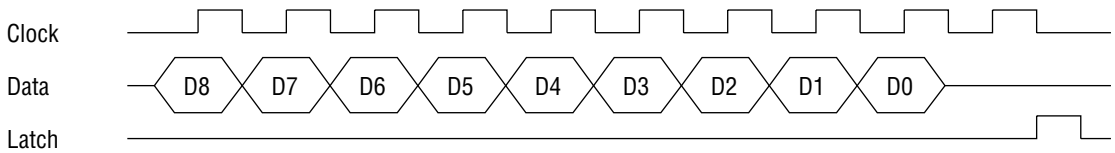


Figure 1.5 Control Output Signals For Power Control IC

Table 1.5 Control Output Signals For Power Control IC

	Socket B						Socket A					
SHDN	VCC	D7	D6	VPP	D5	D4	VPP	D3	D2	VCC	D1	D0
1	0V	1	1	Hi-Z	1	1	0V	1	1	Hi-Z	1	1
1	5V	1	0	12V	1	0	5V	1	0	12V	1	0
1	3.3V	0	1	VCC	0	1	3.3V	0	1	VCC	0	1
1	0V	0	0	0V	0	0	0V	0	0	0V	0	0
0	X	X	X	X	X	X	X	X	X	X	X	X

1.10 Clock Control

The MSM60808 has two clock control methods for reducing power to PC Cards as well as the MSM60808 itself.

The MSM60808's own clock will stop supplying MSM60808 internally when the SUSPEND# pin of the Card Control Register (CDCTL) is asserted low.

The clock to the card can be controlled by setting the Clock Control Register. However, just setting these bits will not stop the clock supply to the card. The MSM60808 communicates with the card using the CCLKRUN# pin, and it will stop the clock if that pin's state allows it.

In clock control the suspend mode has higher precedence than clock run mode. Therefore, care is needed in the sequence of events when stopping the clock supply. Figure 1.6 shows the transitions between each mode.

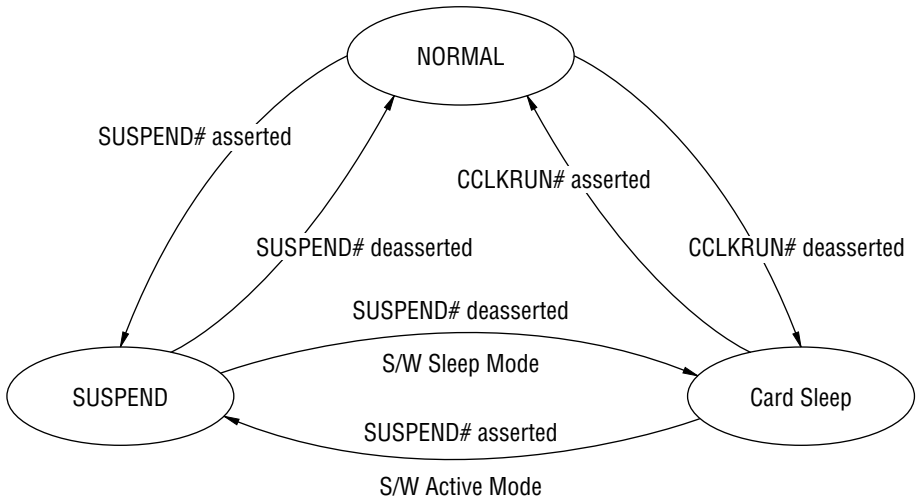


Figure 1.6 MSM60808 Power Management Transition Diagram

1.11 Reset

The MSM60808 will generate a reset signal to a card during the following states.

1) During a power cycle generated when the card is inserted or removed.

2) When the CRST# bit of the Bridge Control Register is set.
(Note: Software reset is not supported for 16-bit cards.)

1.12 ZV Port

The MSM60808 can also be used for a ZV port. When a ZV card is inserted, the ZV Mode Enable Bit of the Card Control Register (CDCTL) will be set. In ZV port mode the address lines A[25:4] are used by the card, so MSM60808 will put these pins in a Hi-Z state. Figure 1.7 shows a system configuration example of a ZV port using the MSM60808.

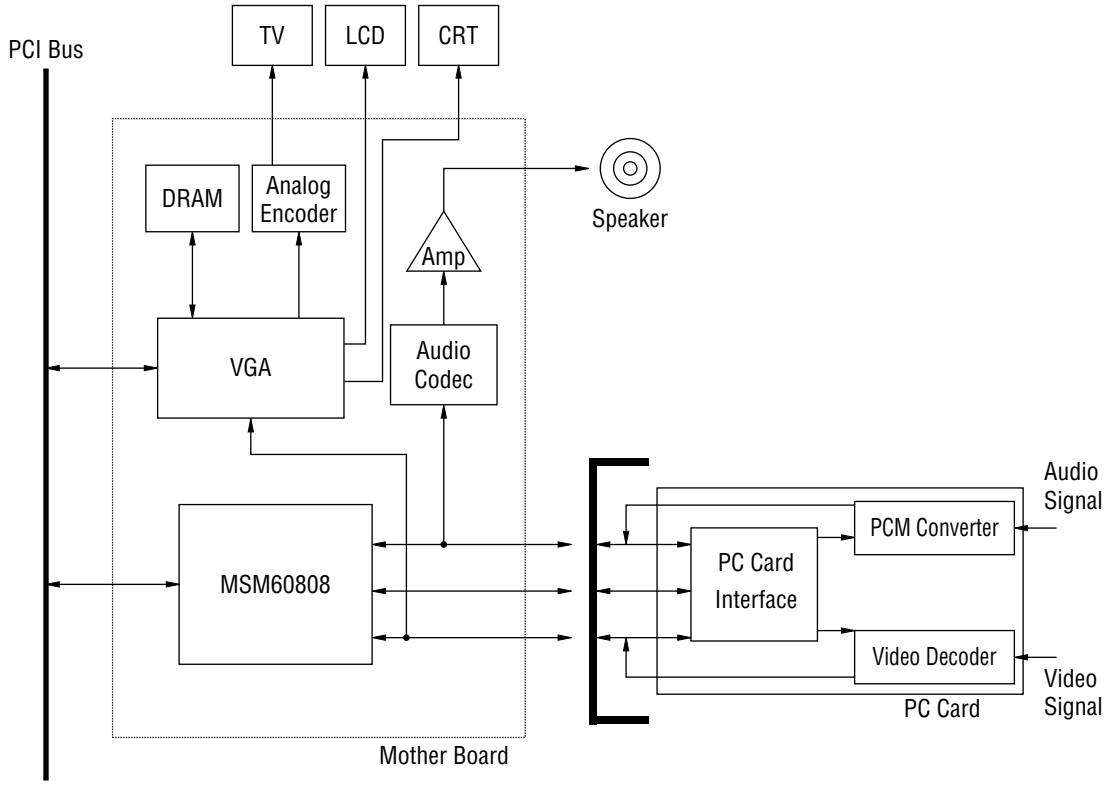


Figure 1.7 ZV Port System Example

1.13 Restrictions

The MSM60808 does not support the following functions.

- 68-pin IDE interface mode
- DMA transfers
- PCI LOCK#
- Multifunction cards
- Serial IREQ

2. Block Diagram

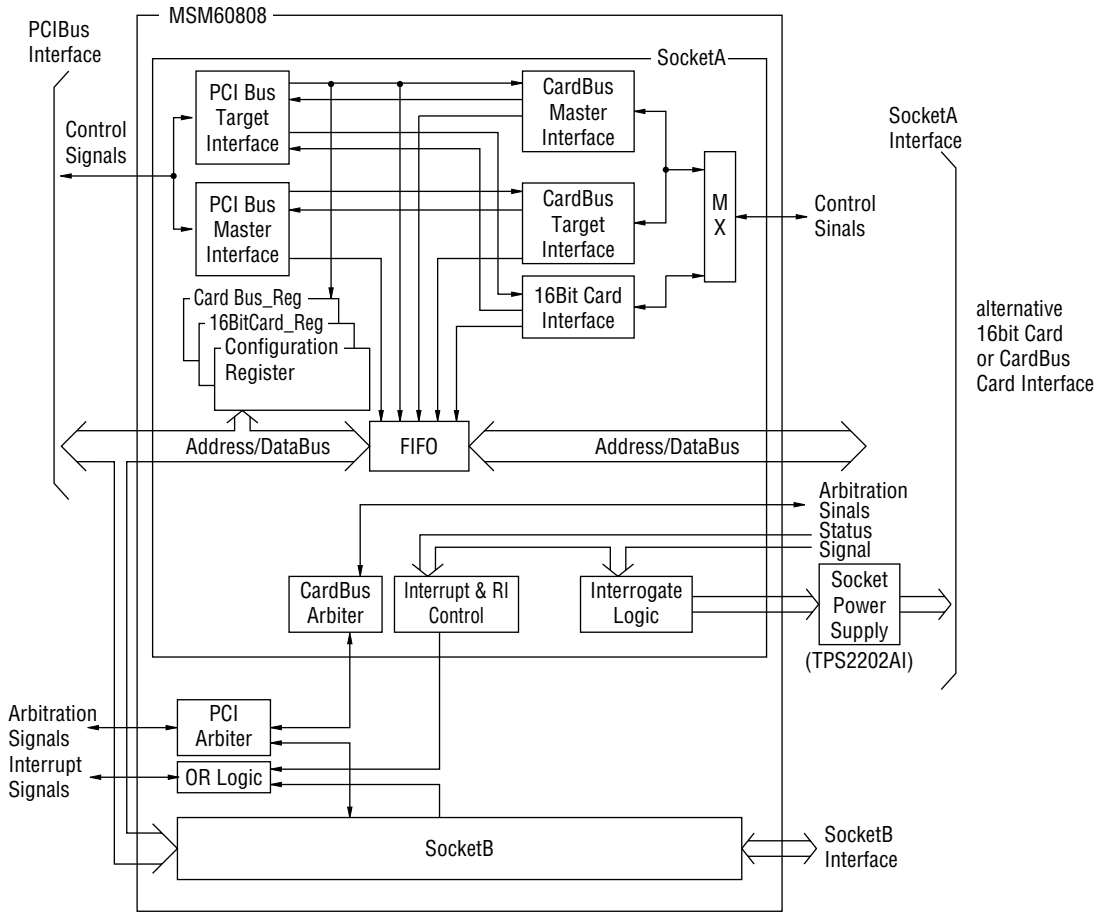


Figure 2. Block Diagram

3. System Configuration Example

Figure 3.1 shows a configuration example of a system using the MSM60808.

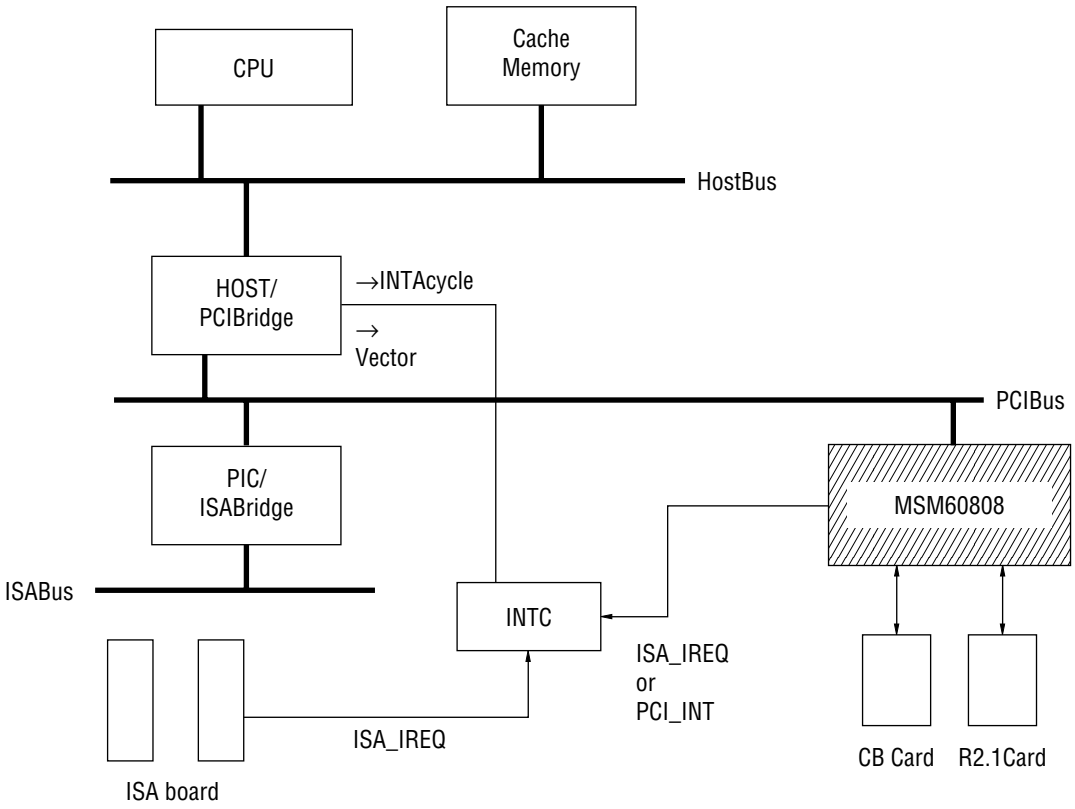


Figure 3.1 System Configuration Example

4. Pin Descriptions

4.1 Signal Types

IN	Standard input signal.
OUT	Totem pole output signal.
O/D	Open drain output signal.
T/S	Bi-directional tri-state signal.
T/S/O	Tri-state output signal.
S/T/S	Active-low sustained tri-state signal driven by only one agent at a time. The agent that drives an S/T/S signal low must drive it high for at least one clock before letting it float. A new agent cannot start driving the S/T/S signal any sooner than one clock after the previous owner tri-states it. When no agent is driving the S/T/S signal, an external pull-up must be supplied by the central resource to sustain the inactive state.

4.2 PCI Bus Interface Signals

If a 16-bit card is inserted, then the MSM60808 converts the PCI interface to a PCMCIA interface. If a CardBus card is inserted, then the MSM60808 interfaces between the PCI local bus and the CardBus.

Table 4.1 PCI Bus Interface Signals

Signal Name	I/O	Description
PCLK	IN	PCI system clock signal. All PCI signals except RSTIN#, INTA#, and INTB# are synchronized to the rising edge of PCLK. The MSM60808 is designed to operate up to 33 MHz.
RSTIN#	IN	PCI system reset signal. When RSTIN# goes active, all MSM60808 internal functions are reset and all MSM60808 internal registers are set to their default values. RSTIN# operates asynchronously with PCLK. Also, the socket will enter a power-down state when RSTIN# is active.
AD[31:0]	T/S	Address/data bus signals. Addresses and data are multiplexed on the same PCI pins. During the first clock of a transaction AD[31:0] carry a physical address (32 bits). During the following clocks AD[31:0] carry data.
C/BE#[3:0]	T/S	Command and byte enable signals. During the address phase of a transaction C/BE#[3:0] define the bus command. During the data phase C/BE#[3:0] are used as byte enables.
PAR	T/S	Parity signal. PAR provides even parity across AD[31:0] and C/BE#[3:0]. Address parity is driven by the master that started the bus cycle one clock after the address phase. In the data phase, the master calculates parity and drives PAR for write cycles, and the target does so for read cycles. Just like the address phase, in the data phase parity for data is output delayed by one clock.
FRAME#	S/T/S	Cycle frame signal. FRAME# is driven by the master to indicate the start and duration of a bus cycle. FRAME# is asserted to indicate the start of a bus cycle. Bus cycles continue while FRAME# stays asserted. FRAME# is deasserted to indicate that the next data phase is the final data phase.
DEVSEL#	S/T/S	Device select signal. When the MSM60808 is the target, it will respond to bus cycles where DEVSEL# is asserted. When the MSM60808 is the master, it monitors DEVSEL# to determine whether or not the target has responded.
IRDY#	S/T/S	Initiator ready signal. IRDY# indicates that the master is ready to perform a transfer. IRDY# is used in conjunction with TRDY#. Data transfers are timed to execute when both IRDY# and TRDY# are asserted. During write cycles IRDY# indicates that valid data is on AD[31:0]. During read cycles IRDY# indicates that the device is ready to accept read data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.

Table 4.1 PCI Bus Interface Signals (continued)

Signal Name	I/O	Description
TRDY#	S/T/S	Target ready signal. TRDY# indicates that the target is ready to perform a transfer. TRDY# is used in conjunction with IRDY#. Data transfers are timed to execute when both IRDY# and TRDY# are asserted. During read cycles TRDY# indicates that valid data is on AD[31:0]. During write cycles TRDY# indicates that the device is ready to accept write data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	S/T/S	Stop signal. STOP# is used by the target to request that the master stop the current transaction.
IDSEL	IN	Initialization device select signal. IDSEL is used as a chip select signal during configuration cycles.
PERR#	S/T/S	Parity error signal. PERR# reports only data parity errors during all transactions except special cycles.
SERR#	O/D	System error signal. SERR# reports address parity errors and other fatal system errors.
REQ#	T/S/O	Request signal. The MSM60808 asserts REQ# when the CardBus master requests use of the PCI bus.
GNT#	IN	Grant signal. The PCI arbiter asserts GNT# to indicate the arbiter the MSM60808 bus usage rights.

4.3 CardBus Interface Signals

Table 4.2 CardBus Interface Signals

Signal Name	I/O	Description
CCLK	OUT	CardBus clock signal. All CardBus signals except CRST#, CCLKRUN#, CINT#, CSTSCHG, CAUDIO, CCD1#, CCD2#, CVS1#, and CVS2# are synchronized to the rising edge of CCLK. The CardBus clock is 33 MHz, but the clock can also be stopped by driving it low.
CCLKRUN#	T/S	CardBus clock run signal. A CardBus card asserts CCLKRUN# to request the MSM60808 clock. The MSM60808 asserts CCLKRUN# while it outputs the clock, and puts the pin in high impedance if it stops the clock.
CRST#	OUT	CardBus reset signal. CRST# operates asynchronously to CCLK.
CAD[31:0]	T/S	CardBus address/data bus signals. Address and data are multiplexed on the same pins. During the first clock of a transaction CAD[31:0] carry a physical address (32 bits). During the following clocks CAD[31:0] carry data.
CC/BE#[3:0]	T/S	Command and byte enable signals. During the address phase of a transaction CC/BE#[3:0] define the bus command. During the data phase CC/BE#[3:0] are used as byte enables.
CPAR	T/S	CardBus parity signal. CPAR provides even parity across CAD[31:0] and CC/BE#[3:0]. Address parity is driven by the master that started the bus cycle one clock after the address phase. In the data phase, the master calculates parity and drives CPAR for write cycles, and the target does so for read cycles. Just like the address phase, in the data phase parity for data is output delayed by one clock.
CFRAME#	S/T/S	CardBus cycle frame signal. CFRAME# is driven by the master to indicate the start and duration of a bus cycle. CFRAME# is asserted to indicate the start of a bus cycle. Bus cycles continue while CFRAME# stays asserted. CFRAME# is deasserted to indicate that the next data phase is the final data phase.
CDEVSEL#	S/T/S	CardBus device select signal. When the MSM60808 is the target, it will respond to bus cycles where CDEVSEL# is asserted. When the MSM60808 is the master, it monitors CDEVSEL# to determine whether or not the target has responded.
CIRDY#	S/T/S	CardBus initiator ready signal. CIRDY# indicates that the master is ready to perform a transfer. CIRDY# is used in conjunction with CTRDY#. Data transfers are timed to execute when both CIRDY# and CTRDY# are asserted. During write cycles CIRDY# indicates that valid data is on CAD[31:0]. During read cycles CIRDY# indicates that the device is ready to accept read data. Wait cycles are inserted until both CIRDY# and CTRDY# are asserted together.

Table 4.2 CardBus Interface Signals (continued)

Signal Name	I/O	Description
CTRDY#	S/T/S	CardBus target ready signal. CTRDY# indicates that the target is ready to perform a transfer. CTRDY# is used in conjunction with CIRDY#. Data transfers are timed to execute when both CIRDY# and CTRDY# are asserted. During read cycles CTRDY# indicates that valid data is on CAD[31:0]. During write cycles CTRDY# indicates that the device is ready to accept write data. Wait cycles are inserted until both CIRDY# and CTRDY# are asserted together.
CSTOP#	S/T/S	CardBus Stop signal. CSTOP# is used by the target to request that the master stop the current transaction.
CBLOCK#	S/T/S	CardBus block signal. CBLOCK# is an optional signal used when the bus master executes a fatal access. The MSM60808 does not support this signal.
CPERR#	S/T/S	CardBus parity error signal. CPERR# reports only data parity errors during all transactions except special cycles.
CSERR#	O/D	CardBus system error signal. CSERR# reports address parity errors and other fatal system errors.
CREQ#	IN	CardBus request signal. CREQ# is asserted when the CardBus master requests use of the PCI bus. When cards are inserted in two slots, the MSM60808's internal arbiter function will respond to request for asserting CGNT# for one or the other card.
CGNT#	T/S/O	CardBus grant signal. CGNT# asserted by the MSM60808 indicates that the CardBus master has been granted PCI bus usage rights.
CINT#	IN	CardBus interrupt signal. CINT# is used to request an interrupt from a CardBus card. CardBus interrupts are level sensitive.
CSTSCHG	IN	CardBus card status change signal. CSTSCHG is used to inform the system when a CardBus card's ready state, write protect state, or battery state changes.
CAUDIO	IN	CardBus card audio signal. CAUDIO is a digital audio output signal from the CardBus card to a system speaker. This signal is output to the system from the MSM60808's SPKROUT# pin.
CCD1# CCD2#	IN	CardBus card detect signals. CCD1# and CCD2# are used in conjunction with the CardBus voltage sense signals to determine the card type and voltage of a CardBus card.
CVS1# CVS2#	T/S	CardBus voltage sense signals. CVS1# and CVS2# are used in conjunction with the CardBus card detect signals to determine the card type and voltage of a CardBus card.

4.4 16-Bit Card Interface Signals

Table 4.3 16-bit Card Interface Signals

Signal Name	I/O	Description
RESET	OUT	Reset signal.
A[25:0]	T/S/O	Address signals. A25 is the most significant bit.
D[15:0]	T/S	Data signals. D15 is the most significant bit.
CE1# CE2#	T/S/O	Card enable signals. CE1# is used to enable even bytes, and CE2# is used to enable odd bytes.
REG#	T/S/O	Attribute memory select signals. A high level on REG# indicates an access to common memory space. A low level indicates an access to attribute memory space or IO space.
WE#	T/S/O	Write enable signal. WE# is asserted when write data is output to a memory card.
OE#	T/S/O	Output enable signal. OE# is asserted when memory read data is read from a memory card.
IOWR#	T/S/O	IO write signal. IOWR# is asserted when data is written to a card's IO space.
IORD#	T/S/O	IO read signal. IORD# is asserted when data is read from a card's IO space.
INPACK#	IN	Input acknowledge signal. INPACK# is asserted by a PC Card when it responds to an IO read access.
WAIT#	IN	Wait signal. WAIT# is asserted by a PC Card when it wants to delay completion of a bus cycle in progress.
READY (IREQ#)	IN	Ready signal. For memory cards, when READY is driven low it indicates that the card is in a busy state. When READY is high it indicates that the card is prepared to accept a new data transfer command. For IO cards, this signal is used as an interrupt request signal (IREQ#).
WP (IOS16#)	IN	Write protect signal. For memory cards, WP reflects the state of the write protect switch. For IO cards, this signal is asserted low by the card when 16-bit access is allowed (IOS16#).
BVD1 (STSCHG#/RI)	IN	Battery voltage detect signal 1. For memory cards, BVD1 is used in conjunction with BVD2 by to indicate the battery state of the PC Card. When both BVD1 and BVD2 are high, the battery is good. When BVD1 is high but BVD2 goes low, the battery enters a warning state. When BVD1 goes low, the battery cannot supply operating voltage regardless of the state of BVD2. For IO cards, this signal is used to indicate a change to the card's ready state, write protect state, battery state, or (for modem cards) ringing indicator (STSCHG#/RI).
BVD2 (SPKER#)	IN	Battery voltage detect signal 2. For memory cards, BVD1 is used in conjunction with BVD2 by to indicate the battery state of the PC Card. When both BVD1 and BVD2 are high, the battery is good. When BVD1 is high but BVD2 goes low, the battery enters a warning state. When BVD1 goes low, the battery cannot supply operating voltage regardless of the state of BVD2. For IO cards, this signal is used as a binary audio signal from the card (SPKR#). This signal will be output to the system from the MSM60808's SPKROUT# pin.

Table 4.3 16-bit Card Interface Signals (continued)

Signal Name	I/O	Description
CD1# CD2#	IN	Card detect signals. CD1# and CD2# are used in conjunction with the voltage sense signals to determine the card type and voltage of a card.
VS1# VS2#	T/S	Card voltage sense signals. VS1# and VS2# are used in conjunction with the card detect signals to determine the card type and voltage of a card.

4.5 Interrupt Signals

Table 4.4 Interrupt Signals

Signal Name	I/O	Description
IREQ3/INTA# IREQ4/INTB#	OUT	Interrupt request signals 3 and 4. These pin connect to PCI or ISA interrupts.
IREQ5 IREQ7 IREQ9 IREQ10 IREQ12 IREQ14	T/S	Interrupt request signals 5, 7, 9, 10, 11, 12, and 14. These signals are ISA interrupts.
IREQ15 /RI_OUT	OUT	Interrupt request signal 15. This signal is used as either an interrupt line or as an output pin for a modem's ring indicator.

4.6 Audio Signals

Table 4.5 Audio Signals

Signal Name	I/O	Description
SPKROUT# /SVSPEND#	IN/OUT	Speaker out signal. SPKROUT# outputs the digital audio signal from a PC Card to the system speaker. When the suspend mode bit : bit 1 of the card control register (CDCTL) is enabled, this pin is used as the suspend # input signal.

4.7 PC Card Power Switch Signals (TPS2202AI Interface)

Table 4.6 PC Card Power Switch Signals

Signal Name	I/O	Description
LATCH	OUT	Power switch latch signal. LATCH is asserted to indicate that data on the DATA line is valid.
CLOCK	OUT	Power switch clock signal. Data on the DATA line is sampled on the rising edge of CLOCK. The maximum frequency value is 2 MHz.
DATA	OUT	Power switch data signal. DATA serially transmits socket power control information.

4.8 Voltage Supply Signals

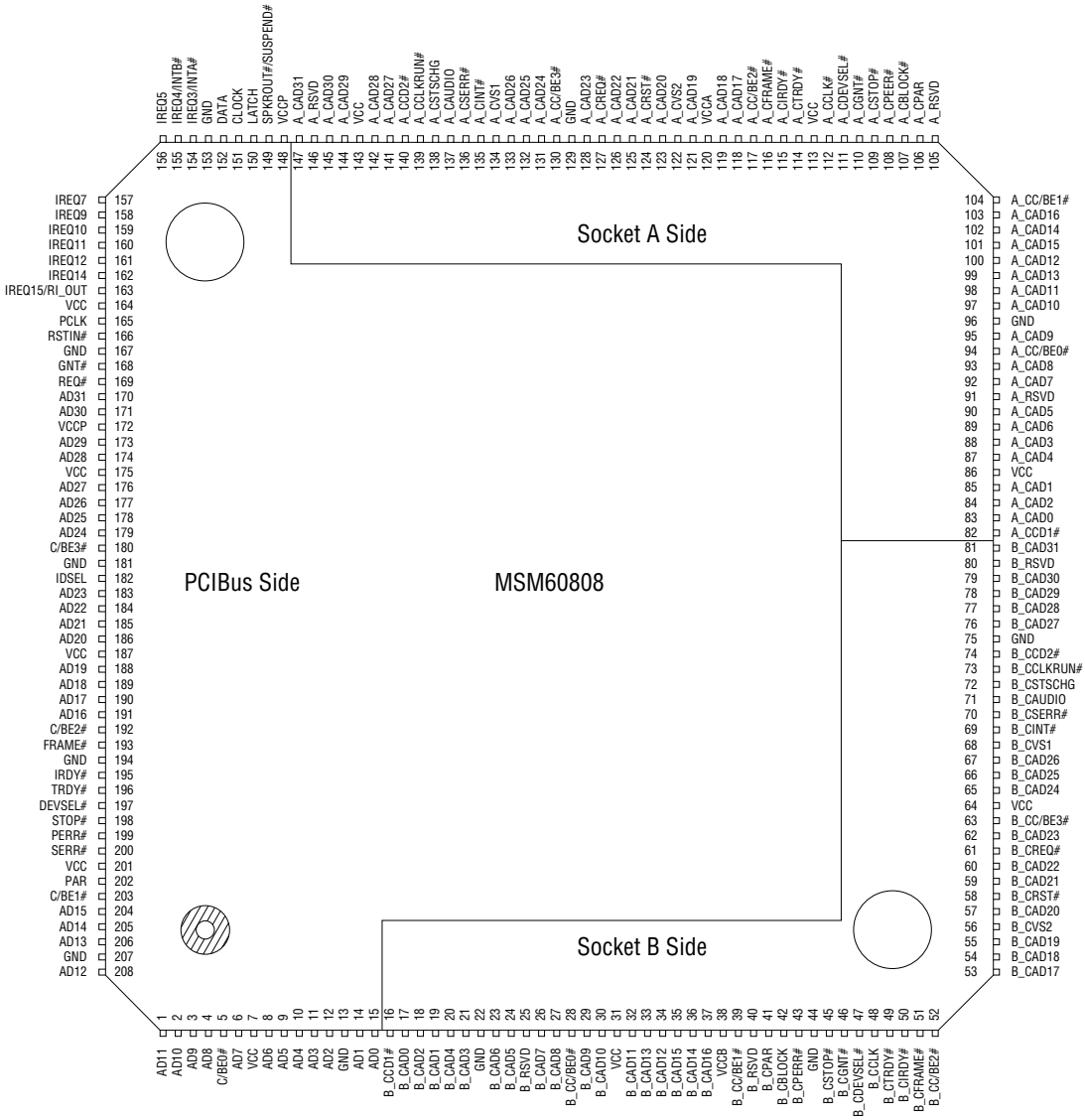
Table 4.7 Voltage Supply Signals

Signal Name	I/O	Description
GND	IN	Device ground.
VCCA	IN	PC Card A voltage supply. 5V or 3.3V may be supplied.
VCCB	IN	PC Card B voltage supply. 5V or 3.3V may be supplied.
VCCP	IN	PCI interface voltage supply. 5V or 3.3V may be supplied.
VCC	IN	Core logic voltage supply. Fixed at 3.3V.

4.9 Pinout

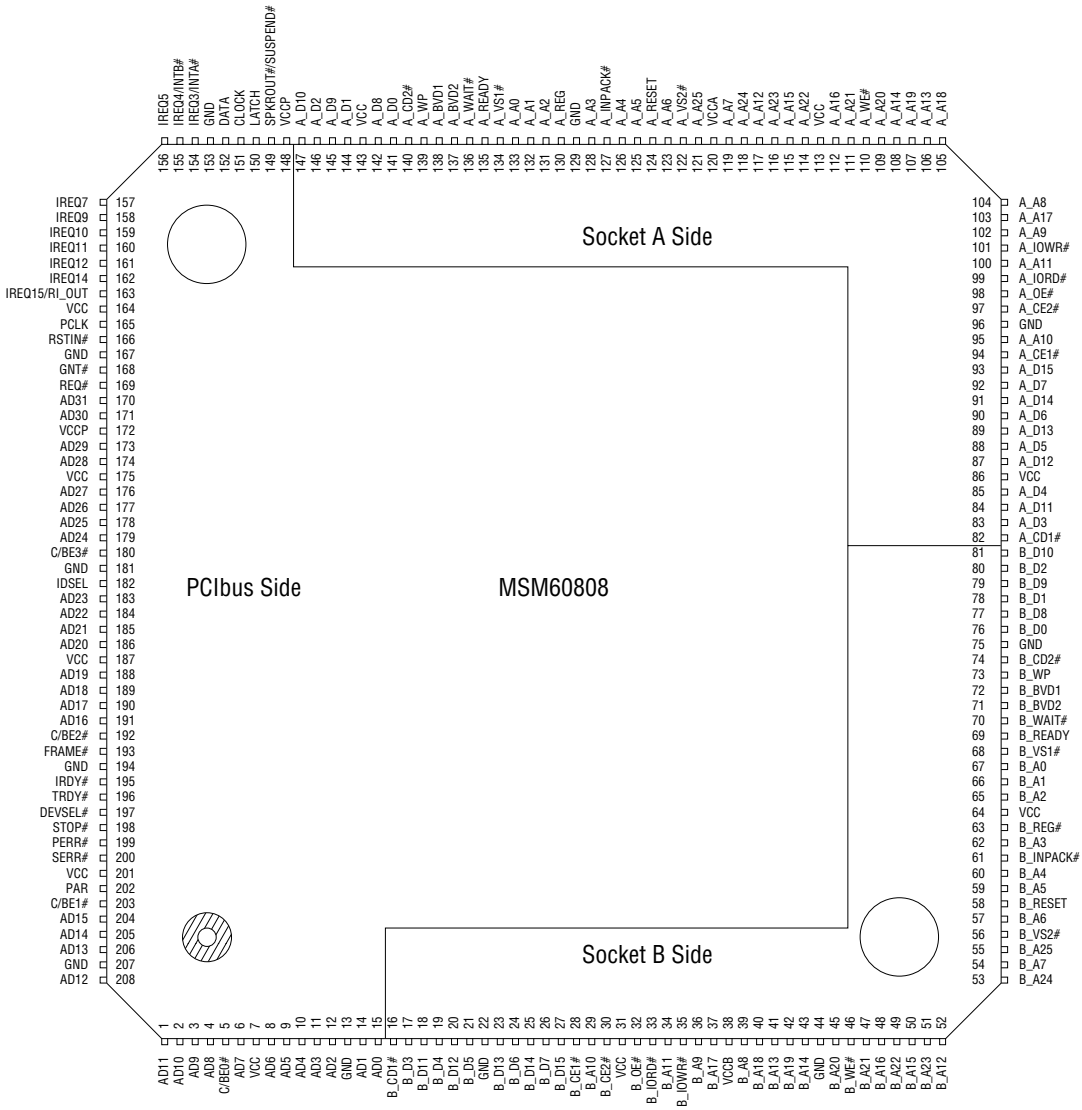
4.9.1 PCI Bus - CardBus Pinout

208-Pin Plastic LQFP



4.9.2 PCI Bus - 16-Bit Pinout

208-Pin Plastic LQFP



5. Registers

5.1 Configuration Registers

Configuration registers determine the basic operation of the MSM60808 bridge.

Addr				
00h	DeviceID		VendID	
04h	PCI Status		PCI Command	
08h	CCODE			REVID
0Ch	Reserved	HTYPE	LTCTM	Reserved
10h	PCCDBADR			
14h	CBSTS		Reserved	
18h	CBLTCTM	SUBUSN	CBBUSN	PCIBUSN
1Ch	MEMBASE0			
20h	MEMLIMIT0			
24h	MEMBASE1			
28h	MEMLIMIT1			
2Ch	IOBASE0U		IOBASE0L	
30h	IOLIMIT0U		IOLIMIT0L	
34h	IOBASE1U		IOBASE1L	
38h	IOLIMIT1U		IOLIMIT1L	
3Ch	BRGCTL		INTPIN	INTLIN
40h	SubSystemID		SubSystem VendorID	
44h	R21BADR			
48 - 8Ch	Reserved			
90h	BFFCTL	DVCTL	CDCTL	RTYCTL
94 - FFh	Reserved			

Figure 5.1 Configuration Register Space

5.1.1 Vendor ID Register (Vend ID)

Register offset : 00h
Default value : 1021h
Access : Read-only
Size : 16-bit

1021h indicates the OKI product.

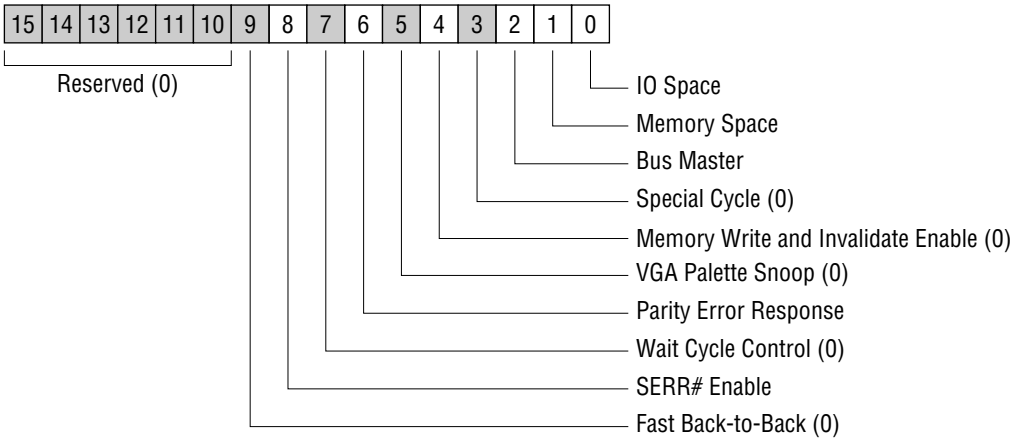
5.1.2 Device ID Register (Device ID)

Register offset : 02h
Default value : 3002h
Access : Read-only
Size : 16-bit

3002h indicates the specific ID of the MSM60808 device.

5.1.3 PCI Command Register (PCI Command)

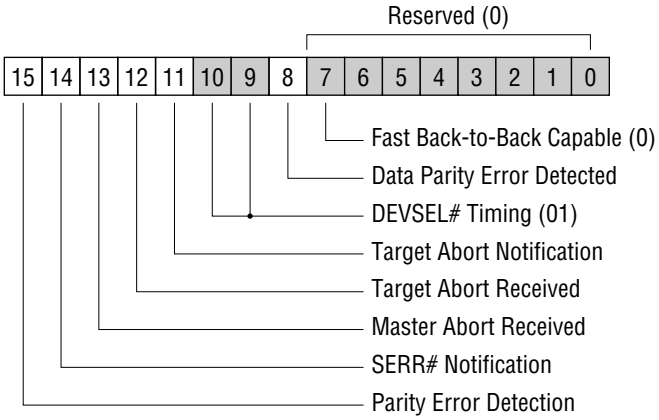
Register offset : 04h
Default value : 0000h
Access : Read/write
Size : 16-bit



Bit	Description
Bit [15:10]	These reserved bits always read as 0.
Bit 9	The MSM60808 does not support the Fast Back-to-Back function. This bit will always read as 0.
Bit 8	The SERR# Enable bit determines whether or not to report system errors. If 1, then system errors will be reported. If 0, then SERR# will not be reported even when errors occur.
Bit 7	The Wait Cycle Control bit's function is not supported by the MSM60808. This bit will always read as 0.
Bit 6	The Parity Error Response bit controls whether or not a parity error will be reported if a one is detected.
Bit 5	The VGA Palette Snoop bit's function is not supported by the MSM60808. This bit will always read as 0.
Bit 4	The Memory Write and Invalidate Enable bit's function is not supported by the MSM60808. This bit will always read as 0.
Bit 3	The MSM60808 will not respond to the command of a Special Cycle bit. This bit will always read as 0.
Bit 2	The Bus Master bit controls whether or not the MSM60808 will operate as the bus master. If set to 1, the card will operate as the bus master. If 0, then the card will be recognized as a target device.
Bit 1	The Memory Space bit controls whether or not to respond to memory accesses on the PCI bus. If this bit is 0, then the MSM60808 will not respond to memory commands. If 1, then it will respond.
Bit 0	The IO Space bit controls whether or not to respond to IO accesses on the PCI bus. If this bit is 0, then the MSM60808 will not respond to IO commands. If 1, then it will respond.

5.1.4 PCI Status Register (PCI Status)

Register offset : 06h
Default value : 0000h
Access : Read/write
Size : 16-bit



Bit	Description
Bit 15	The Parity Error Detected bit is set to 1 when a parity error is detected. Writing 1 to this bit clears it. Writing 0 has no effect.
Bit 14	The SERR# Notification bit is set to 1 when the bridge reports a system error. Writing 1 to this bit clears it. Writing 0 has no effect.
Bit 13	The Master Abort Received bit is set to 1 when a master abort is received. Writing 1 to this bit clears it. Writing 0 has no effect.
Bit 12	The Target Abort Received bit is set to 1 when a target abort is received by the MSM60808 during a PCI bus access. Writing 1 to this bit clears it. Writing 0 has no effect.
Bit 11	The Target Abort Notification bit is set to when this MSM60808 device reports a target abort. Writing 1 to this bit clears it. Writing 0 has no effect.
Bit [10:9]	The DEVSEL# Timing bits are encoded with the device response time. Since the MSM60808 is medium speed, these bits are encoded with 01b. These bits are read-only.
Bit 8	Only bus masters need to implement the Data Parity Error Detected bit. The MSM60808 has been implement for master cards. This bit is set to 1 when a data parity error is detected on the PCI bus. Writing 1 to this bit clears it. Writing 0 has no effect.
Bit 7	The MSM60808 does not support the Fast Back-to-Back Capable function. This bit always reads as 0.
Bit [6:0]	These reserved bits always read as 0.

5.1. 5 Revision ID Register (REVID)

Register offset : 08h
Default value : 01h
Access : Read-only
Size : 8-bit

This register contains the revision number of the device. The MSM60808's revision level is 01h.

5.1.6 Class Code Programming Interface Byte Register (CCPIB)

Register offset : 09h
Default value : 00h
Access : Read-only
Size : 8-bit

There is no specific register-level programming for this class code (indicated by the CCCB register). Therefore, the value of this field is 00h.

5.1.7 Class Code Sub-Class Code Byte Register (CCCB)

Register offset : 0Ah
Default value : 0607h
Access : Read-only
Size : 16-bit

Bits [15:8] : 06h indicate a bridge function. Bits [7:0] : 07h indicate the PCI-CardBus bridge function.

5.1.8 Latency Timer Register (LTCTM)

Register offset : 0Dh
Default value : 00h
Access : Read/write
Size : 8-bit

This register is used only for the PCI bus interface. When the MSM60808 is the master, GNT # is deasserted, and the MSM60808 will complate data transfers after the latency timer expires.

Bit	Description
Bit [7:;0]	Timer setting. 0h : Do not start latency timer. 1h : 8 clocks 2h : 16 clocks 3h : 24 clocks 4h : 32 clocks 5h : 40 clocks 6h : 48 clocks 7h : 56 clocks 8h : 64 clocks 9h~FFh : Reserved

5.1.9 Header Type Register (HTYPE)

Register offset : 0Eh
Default value : 82h
Access : Read-only
Size : 8-bit

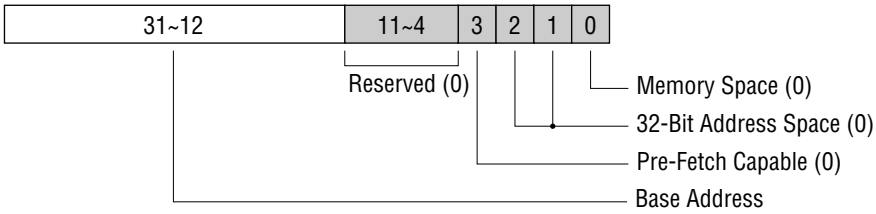
The MSM60808 is a multifunction bridge device, so the value of this register is 82h. This register is read-only.

5.1.10 PC Card Socket Status Base Address Register (PCCDBADR)

Register offset : 10h
Default value : 0000 0000h
Access : Read/write
Size : 32-bit

This register stores the base address of CardBus registers and 16-bit card registers. The address pointed to by this register is mapped into memory space.

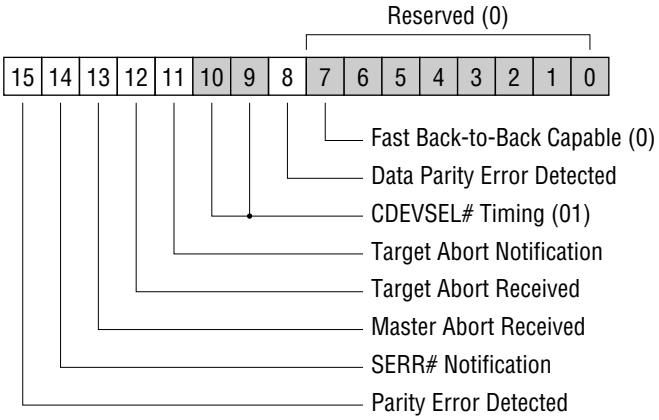
Bits 31~12 are read/write. Bits 11~0 are read-only, and will output 0, when read.



Bit	Description
Bit [31:12]	The Base Address determines the starting address of PC Card socket status control registers mapped into system memory space.
Bit [11:4]	Reserved (0). All bits are fixed 0 and read-only.
Bit 3	Pre-Fetch Capable bit is fixed 0. Pre-fetch reads cannot be performed.
Bit [2:1]	These bits are fixed 00 to indicate that a 32-bit address space is used.
Bit 0	The Memory Space indicator bit is fixed 0 to indicate that there is mapped in the memory space.

5.1.11 CardBus Status Register (CBSTS)

Register offset : 16h
Default value : 0000h
Access : Read/Write
Size : 16-bit



Bit	Description
Bit 15	The Parity Error Detected bit is set to 1 when a parity error is detected.
Bit 14	The SERR# Notification bit is set to 1 when the bridge reports a system error. Writing 1 to this bit clears it. This bit is 0 after reset.
Bit 13	The Master Abort Received bit is set to 1 when a master abort is received
Bit 12	The Target Abort Received bit is set to 1 when a target abort is received by the MSM60808 during a CardBus access. Writing 1 to this bit clears it. Writing 0 has no effect. This bit is 0 after reset.
Bit 11	The Target Abort Notification bit is set to 1 when this MSM60808 device reports a target abort. Writing 1 to this bit clears it. Writing 0 has no effect. This bit is 0 after reset.
Bit [10:9]	The CDEVSEL# Timing bits are encoded with the device response time. Since the MSM60808 is medium speed, these bits are encoded with 01b. These bits are read-only.
Bit 8	Only bus masters need to implement the Data Parity Error Detected bit. The MSM60808 has been implement for master cards. This bit is set to 1 when a data parity error is detected.
Bit 7	The MSM60808 does not support the Fast Back-to-Back Capable function. This bit always reads as 0.
Bit [6:0]	These reserved bits always read as 0.

5.1.12 PCI Bus Number (PCIBUSN)

Register offset : 18h
Default value : 00h
Access : Read/write
Size : 8-bit

This read/write register is used to store the number of the PCI bus connected to the MSM60808. It is set by configuration or socket services software.

5.1.13 CardBus Bus Number (CBBUSN)

Register offset : 19h
Default value : 00h
Access : Read/write
Size : 8-bit

This read/write register is used to store the number of the CardBus bus connected to the MSM60808. The PCIBIOS writes a value to this register. The MSM60808 uses this register to determine whether or not to respond to Type 1 configuration cycles on the PCI bus. If it does respond, the MSM60808 will generate a Type 0 configuration cycle on the CardBus interface.

5.1.14 Subordinate Bus Number (SUBUSN)

Register offset : 1Ah
Default value : 00h
Access : Read/write
Size : 8-bit

This read/write register stores the maximum bus number of the CardBus. The PCIBIOS writes a value to this register. The MSM60808 uses this register along with CBBUSN to determine whether or not to forward Type 1 configuration cycles on the CardBus.

5.1.15 CardBus Latency Timer Register (CBLTCTM)

Register offset : 1Bh
Default value : 00h
Access : Read/write
Size : 8-bit

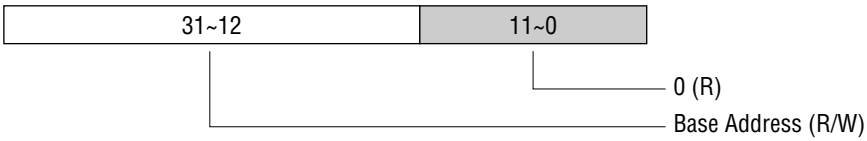
This register is used only for the CardBus interface. When the MSM60808 is the master, it will complete data transfers after the latency timer expires.

Bit	Description
Bit [7:;0]	Timer setting.
	0h : Do not start latency timer.
	1h : 8 clocks
	2h : 16 clocks
	3h : 24 clocks
	4h : 32 clocks
	5h : 40 clocks
	6h : 48 clocks
	7h : 56 clocks
	8h : 64 clocks
	9h~FFh : Reserved

5.1.16 Memory Base Register 0 (MEMBASE0)

Register offset : 1Ch
Default value : 0000 0000h
Access : Read/write
Size : 32-bit

The Memory Base Register defines the base address of a memory mapped IO address range that is used by the MSM60808 to determine whether or not to forward memory transactions from one interface to the other. This window is enabled by bit 1 of the Command Register.

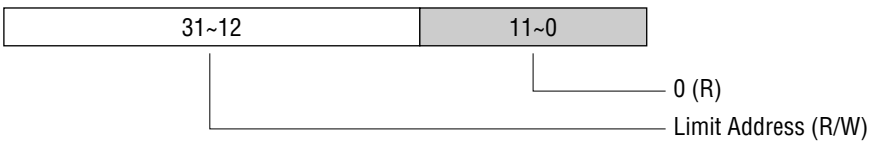


Bit	Description
Bit [31:12]	The Base Address corresponds to AD[31:12]. It is read/write.
Bit [11:0]	All bits AD[11:0] are 0 (4 KB window). These bits are read-only and always return 0.

5.1.17 Memory Limit Register 0 (MEMLIMIT0)

Register offset : 20h
Default value : 0000 0000h
Access : Read/write
Size : 32-bit

The Memory Limit Register defines the highest address of a memory mapped IO address range that is used by the MSM60808 to determine whether or not to forward memory transactions from one interface to the other. This window is enabled by bit 1 of the Command Register.

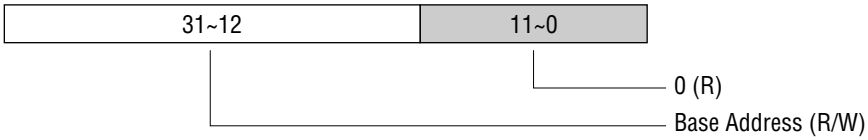


Bit	Description
Bit [31:12]	The Limit Address corresponds to AD[31:12]. It is read/write.
Bit [11:0]	All bits AD[11:0] are 0 (4 KB window). These bits are read-only and always return 0.

5.1.18 Memory Base Register 1 (MEMBASE1)

Register offset : 24h
Default value : 0000 0000h
Access : Read/write
Size : 32-bit

The Memory Base Register defines the base address of a memory mapped IO address range that is used by the MSM60808 to determine whether or not to forward memory transactions from one interface to the other. This window is enabled by bit 1 of the Command Register.

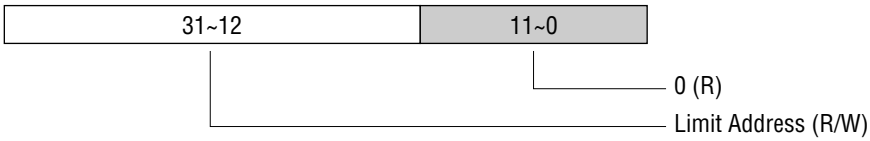


Bit	Description
Bit [31:12]	The Base Address corresponds to AD[31:12]. It is read/write.
Bit [11:0]	These bits are read-only and always return 0.

5.1.19 Memory Limit Register 1 (MEMLIMIT1)

Register offset : 28h
Default value : 0000 0000h
Access : Read/write
Size : 32-bit

The Memory Limit Register defines the highest address of a memory mapped IO address range that is used by the MSM60808 to determine whether or not to forward memory transactions from one interface to the other. This window is enabled by bit 1 of the Command Register.



Bit	Description
Bit [31:12]	The Limit Address corresponds to AD[31:12]. It is read/write.
Bit [11:0]	All bits AD[11:0] are 0 (4 KB window). These bits are read-only and always return 0.

5.1.20 IO Base Register 0L (IOBASE0L)

Register offset : 2Ch
Default value : 0000h
Access : Read/write
Size : 16-bit

The IO Base Register defines the bottom of the address range that is used by the MSM60808 to determine whether or not to forward IO transactions to the CardBus. This register's bits correspond to AD[15:0]. Bits [1:0] are read-only, and always return 0. When the address is decoded, only AD[15:12] are decoded; AD[11:2] are ignored. The minimum IO address range will be 4 KB.

5.1.21 IO Base Register 0U (IOBASE0U)

Register offset : 2Eh
Default value : 0000h
Access : Read/write
Size : 16-bit

This register's bits correspond to AD[31:16]. This register is used to specify the location of the IO address block which is specified by the IO Base Register 0L and IO Limit Register 0L.

5.1.22 IO Limit Register 0L (IOLIMIT0L)

Register offset : 30h
Default value : 0000h
Access : Read/write
Size : 16-bit

The IO Limit Register defines the top of the address range that is used by the MSM60808 to determine whether or not to forward IO transactions to the CardBus. This register's bits correspond to AD[15:0]. When the address is decoded, only AD[15:12] are decoded; AD[11:0] are ignored.

5.1.23 IO Limit Register 0U (IOLIMIT0U)

Register offset : 32h
Default value : 0000h
Access : Read/write
Size : 16-bit

This register's bits correspond to AD[31:16]. This register has no relation to address decoding. It will return 0 when read.

5.1.24 IO Base Register 1L (IOBASE1L)

Register offset : 34h
Default value : 0000h
Access : Read/write
Size : 16-bit

The IO Base Register defines the bottom of the address range that is used by the MSM60808 to determine whether or not to forward IO transactions to the CardBus. This register's bits correspond to AD[15:0]. Bits [1:0] are read-only, and always return 0. When the address is decoded, only AD[15:12] are decoded; AD[11:2] are ignored. The minimum IO address range will be 4 KB.

5.1.25 IO Base Register 1U (IOBASE1U)

Register offset : 36h
Default value : 0000h
Access : Read/write
Size : 16-bit

This register's bits correspond to AD[31:16]. This register is used to specify the location of the IO address block which is specified by The IO Base Register 1L and IO Limit Register 1L.

5.1.26 IO Limit Register 1L (IOLIMIT1L)

Register offset : 38h
Default value : 0000h
Access : Read/write
Size : 16-bit

The IO Limit Register defines the top of the address range that used by the MSM60808 to determine whether or not to forward IO transactions to the CardBus. This register's bits correspond to AD[15:0]. When the address is decoded, only AD[15:12] are decoded; AD[11:0] are ignored.

5.1.27 IO Limit Register 1U (IOLIMIT1U)

Register offset : 3Ah
Default value : 0000h
Access : Read/write
Size : 16-bit

This register's bits correspond to AD[31:16]. This register has no relation to address decoding. It will return 0 when read.

5.1.28 Interrupt Line Register (INTLIN)

Register offset : 3Ch
Default value : 00h
Access : Read/write
Size : 8bit

Bits [7:0]: the value of this register is recognized as the level of an interrupt request from the system interrupt controller connected to the MSM60808's interrupt pins.

5.1.29 Interrupt Pin Register (INTPIN)

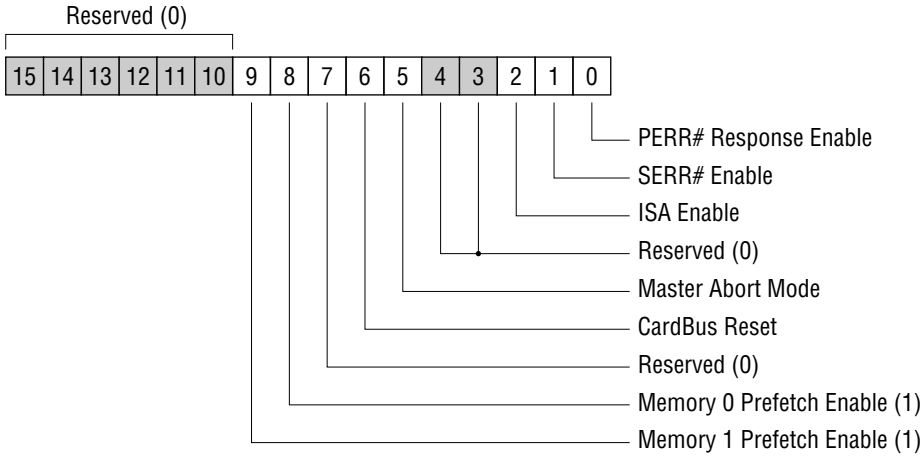
Register offset : 3Dh
Default value : 00h
Access : Read-only
Size : 8bit

Bits [7:0]: the bits in this register define the PCI bus interrupt lines used by the MSM60808. The MSM60808 assigns INTA# to Socket A and INTB# to Socket B.

01h : INTA#, 02h : INTB#

5.1.30 Bridge Control Register (BRGCTL)

Register offset : 3Eh
Default value : 0340h
Access : Read/write
Size : 16-bit



Bit	Description
Bit [15:10]	These reserved bits always read as 0.
Bit 9	When the Memory 1 Prefetch Enable bit is 1, reads from the memory window defined by the Memory Base 1 Register (MEMBASE1) and the Memory Limit 1 Register (MEMLIMIT1) will be prefetched. This bit is fixed to 1.
Bit 8	When the Memory 0 Prefetch Enable bit is 1, reads from the memory window defined by the Memory Base 0 Register (MEMBASE0) and the Memory Limit 0 Register (MEMLIMIT0) will be prefetched. This bit is fiexed to 1.
Bit 7	Reserved. This bit outputs 0, when read.
Bit 6	When the CardBus Reset bit is 1, MSM60808 will assert CRST#. When 0, MSM60808 will deassert CRST#.
Bit 5	The Master Abort Mode bit controls MSM60808 operation when MSM60808 is master and a master abort occurs on the PCI bus or CardBus. When this bit is 0, reads will return all 1 data and writes will discard the data. When this bit is 1, MSM60808 will return a target abort for reads and non-posted writes if the bus that did not terminate with a master abort has not completed processing. When the bus has completed porcessing (when posted write), the MSM60808 asserts SERR# on the PCI bus interface if the SERR# enable bit of PCI command register has been set.
Bit [4:3]	These reserved bits always read as 0.

Bit	Description
Bit 2	The ISA Enable bit applies only to addresses enabled by the IO Base Register and IO Limit Register and are in the first 64 KB of PCI IO space. When this bit is 1, the MSM60808 will block forwarding from PCI to CardBus of IO transaction addressing the last 768 bytes in each 1 KB block. IO transactions addressing the last 768 bytes in the reverse direction will be forwarded. This bit will be 0 after reset.
Bit 1	The SERR# Enable bit controls whether or not the assertion of SERR# on the CardBus will be forwarded. When this bit is 1, SERR# on the CardBus will be forwarded. When 0, it will not. This bit will be 0 after reset.
Bit 0	The PERR# Response Enable bit controls whether or not the MSM60808 will respond to parity errors on the CardBus. When this bit is 1, the MSM60808 will check and report parity errors. When 0, it will ignore parity errors. This bit will be 0 after reset.

5.1.31 Subsystem Vendor ID Register (Subsystem Vendor ID)

Register offset : 40h
Default value : 0000h
Access : Read-only
Size : 16-bit

The MSM60808 does not support this function.
This register always outputs as 0000h, when read.

5.1.32 Subsystem ID Register (Subsystem ID)

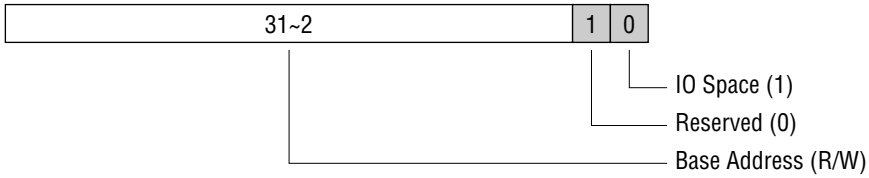
Register offset : 42h
Default value : 0000h
Access : Read-only
Size : 16-bit

The MSM60808 does not support this function.
When read, always outputs as 0000h.

5.1.33 R21 Legacy Register Base Address Register (R21BADR)

Register offset : 44h
Default value : 0000 0000h
Access : Read/write
Size : 32-bit

This register points to address of the Index/Data register that exists at the MSM60808's IO address 3E0h/3E1h. It determine the start address of a 16-bit card's Index/Data register. The Index/Data register can also be mapped to any location in as a double-word in the 4-Gbyte IO space.

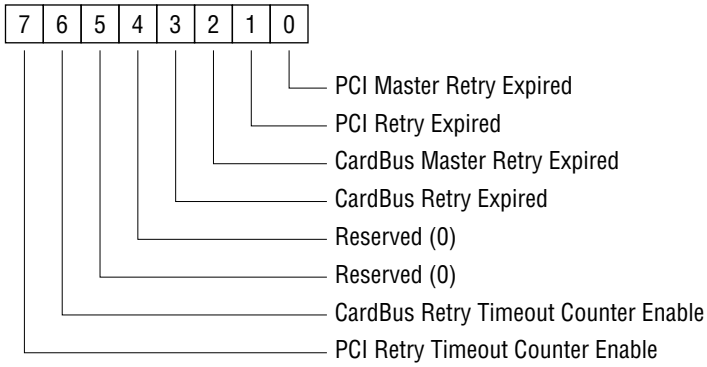


Bit	Description
Bit [31:12]	The Base Address determines the start address of the Index/Data Socket Configuration Register for 16-bit PC Cards. The 16-bit cards Index/Data register provides 82365-compatible window access of 16-bit card registers. It is actually defined with the Index as an 8-bit IO port located at the base address and the Data as an 8-bit IO port located at the base address plus one. Access to the base address plus two or plus three is not permitted. Such access may generate an error to which the system will not respond.
Bit 1	These reserved bits always read as 0.
Bit 0	The IO Space indicator bit is fixed 1. It indicates IO space.

5.1.34 Retry Control Register (RTYCTL)

Register offset : 90h
Default value : 00h
Access : Read/write
Size : 8-bit

This register controls PCI bus and CardBus retry operation.

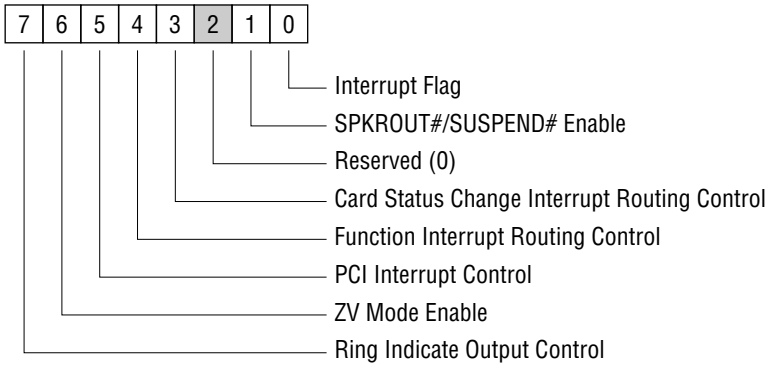


Bit	Description
Bit 7	When the PCI Retry Timeout counter Enable bit is 1, the Retry Counter will operate. When 0, the Retry Counter will not operate.
Bit 6	When the CardBus Retry Timeout counter Enable bit is 1, the Retry Counter will operate. When 0, the Retry Counter will not operate.
Bit 5	Reserved. Always outputs 0 when read.
Bit 4	Reserved. Always outputs 0 when read.
Bit 3	When the CardBus Retry Expired bit is 1, it indicates that retry has expired. Writing 1 to this bit again will clear the bit field.
Bit 2	When the CardBus Master Retry Expired bit is 1, it indicates that retry has expired. Writing 1 to this bit again will clear the bit field.
Bit 1	When the PCI Retry Expired bit is 1, it indicates that retry has expired. Writing 1 to this bit again will clear the bit field.
Bit 0	When the PCI Master Retry Expired bit is 1, it indicates that retry has expired. Writing 1 to this bit again will clear the bit field.

5.1.35 Card Control Register (CDCTL)

Register offset : 91h
Default value : 00h
Access : Read/write
Size : 8-bit

This register is used to control cards independently for Socket A and Socket B.

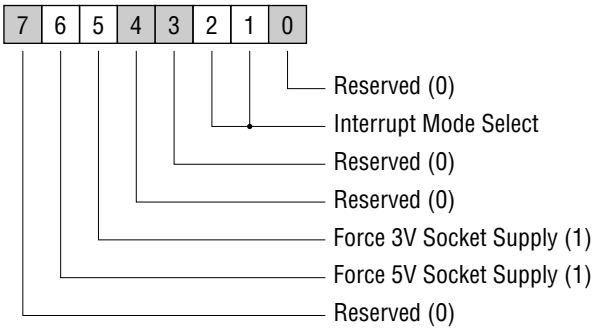


Bit	Description
Bit 7	The Ring Indicate Output Control bit controls the state of the IREQ15/RI_OUT pin. When 1, the pin operates as RI_OUT. When 0, the pin operates as IREQ15.
Bit 6	When the ZV Mode Enable bit is 0, the card will always be in 16-bit card mode. When 1, the card will be in ZV mode. This bit will be 0 after reset.
Bit 5	When the PCI Interrupt Control bit is 1, PCI interrupts (INTA#/INTB#) are enabled. When 0, PCI interrupts are disabled.
Bit 4	The Function Interrupt Routing Control bit controls whether or not IREQ/CINT# will be routed to PCI interrupts. When 1, it will be routed to a PCI interrupt (but only if bit 5 is also 1). When 0, it will not be routed.
Bit 3	The Card Status Change Interrupt Routing Control bit controls whether or not card status change interrupts will be routed as PCI interrupts. When 1, they will be routed to a PCI interrupt (but only if bit 5 is also 1). When 0, they will not be routed.
Bit 2	This reserved bit always reads as 0.
Bit 1	When the SPKROUT#/SUSPEND# bit is 1, SPKROUT# will be enabled. When 0, SUSPEND# will be enabled.
Bit 0	Writing 1 to the Interrupt Flag bit clears it. When this bit is 1, it indicates that an interrupt was generated from a PC Card. When 0, no interrupt has been generated.

5.1.36 Device Control Register (DEVCTL)

Register offset : 93h
Default value : 60h
Access : Read/write
Size : 8-bit

This register controls Socket A and Socket B.

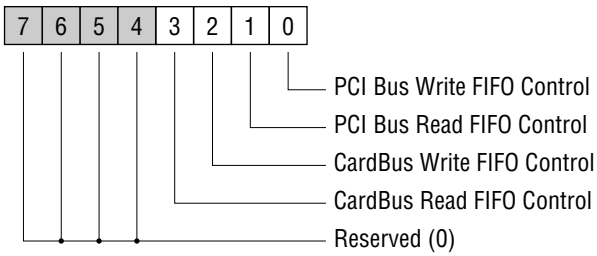


Bit	Description
Bit 7	This reserved bit always reads as 0.
Bit 6	When the Force 5V Socket Supply bit is 1, this function is enabled. This bit is fixed to 1 (enable).
Bit 5	When the Force 3V Socket Supply bit is 1, this function is enabled. This bit is fixed to 1 (enable).
Bit 4	This reserved bit always reads as 0.
Bit 3	This reserved bit always reads as 0.
Bit [2:1]	The Interrupt Mode Select bits are valid when bit 5 of the Card Control Register is enabled. When 00b, no interrupts will be generated. When 01b, the MSM60808 will operate with ISA mode interrupts. Values 10b and 11b are reserved.
Bit 0	This reserved bit always reads as 0. It is used for MSM60808 internal testing.

5.1.37 Buffer Control Register (BFFCTL)

Register offset : 93h
Default value : 00h
Access : Read/write
Size : 8-bit

This register is used to control the depth of FIFO. However, data transfers of configulation commands and I/O commands are not effected by this register setting.



Bit	Description
Bit [7:4]	These reserved bits are fixed to 0h.
Bit 3	The CardBus Read FIFO Control bit controls the depth of the FIFO when reading from the master CardBus card. When this bit is 0, data can be transferred up to the maximum depth of the FIFO. When 1, 4-byte transfers (4-byte signal transfer only) are allowed. This bit will be 0 after reset.
Bit 2	The CardBus Write FIFO Control bit controls the depth of the FIFO when writing from the master CardBus card. When this bit is 0, data can be transferred up to the maximum depth of the FIFO. When 1, 4-byte transfers (4-byte signal transfer only) are allowed. This bit will be 0 after reset.
Bit 1	The PCI Bus Read FIFO Control bit controls the depth of the FIFO when the PCI bus master reads data from a card. When this bit is 0, data can be transferred up to the maximum depth of the FIFO. When 1, 4-byte transfers (4-byte signal transfer only) are allowed. This bit will be 0 after reset.
Bit 0	The PCI Bus Write FIFO Control bit controls the depth of the FIFO when writing from the PCI bus. When this bit is 0, data can be transferred up to the maximum depth of the FIFO. When 1, 4-byte transfers (4-byte signal transfer only) are allowed. This bit will be 0 after reset.

5.2 16-Bit Card Registers

The 16-bit registers control 16-bit cards. These registers consist of setup registers, interrupt control registers, IO mapping control registers, and memory mapping control registers. They can be placed in either IO space or memory space.

When located in IO space, these registers can be indirectly accessed using the Index/Data Register pointed to by the R21 Legacy Register Base Address (R21BADR). When located in memory space, these registers can be directly accessed in the 2 KB of addresses (the addresses added to the memory offset address of Figure 5.2) after the base address from the PC Card Socket Status Address Register (PCCBADR).

Mem Off Addr	Index Addr					
800h	00h	IGENC	PCTRL	ISTAT	IDREG	Setup Registers
804h	04h	IOCREG	ADWEN	CSCICR	CSTCH	Interrupt Registers
808h	08h	IOSTH0	IOSTL0	IOSH0	IOSL0	IO Mapping Control Registers
80Ch	0Ch	IOSTH1	IOSTL1	IOSH1	IOSL1	
810h	10h	SMSTH0	SMSTL0	SMH0	SML0	Memory Mapping Control Registers
814h	14h	Reserved	GRCTL	OFFH0	OFFL0	
818h	18h	SMSTH1	SMSTL1	SMH1	SML1	
81Ch	1Ch	Reserved	GLBCTL	OFFH1	OFFL1	
820h	20h	SMSTH2	SMSTL2	SMH2	SML2	
824h	24h	Reserved	Reserved	OFFH2	OFFL2	
828h	28h	SMSTH3	SMSTL3	SMH3	SML3	
82Ch	2Ch	Reserved	Reserved	OFFH3	OFFL3	
830h	30h	SMSTH4	SMSTL4	SMH4	SML4	
834h	34h	Reserved	Reserved	OFFH4	OFFL4	

MemOffAddr: Memory Offset Address
IndexAddr: Index Address

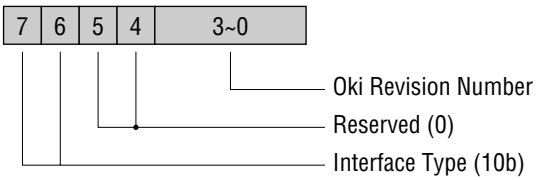
Figure 5.2 16-Bit Card Register Space

5.2.1 Setup Registers

5.2.1.1 Identification Register (IDREG)

Index : 00h
Default value : 80h
Access : Read-only
Size : 8-bit

This register is used by system software to determine the types of PC Cards supported by the sockets.

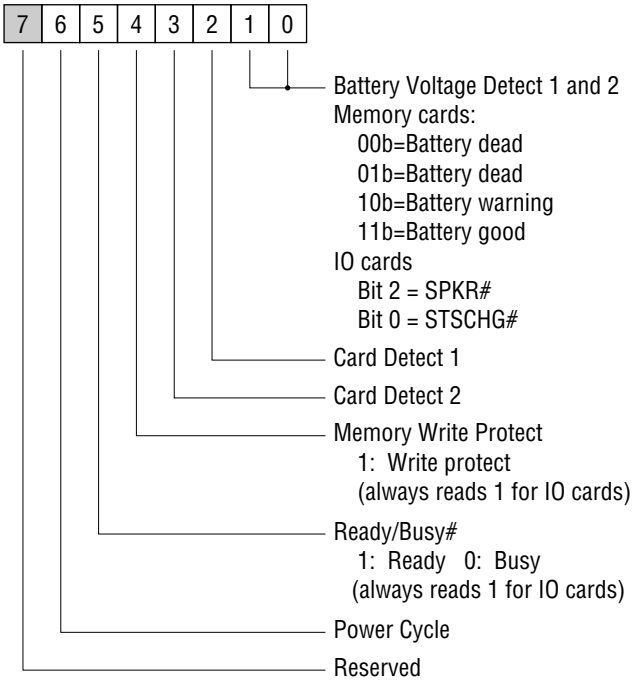


Bit	Description
Bit [7:6]	The Interface Type bits are fixed to 10b. They indicate a memory and IO interface.
Bit [3:0]	This is the Oki Revision Number.

5.2.1.2 Interface Status Register (ISTAT)

Index : 01h
Default value : 3Fh
Access : Read-only
Size : 8-bit

This register provides the current states of the PC Card socket interface signals.

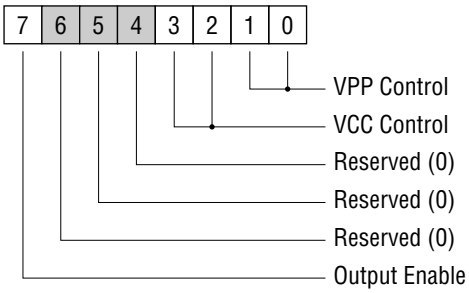


Bit	Description
Bit 7	Reserved (0).
Bit 6	When the Power Cycle bit has been set to 1, it indicates that the interface has powered up. When cleared to 0, it indicates that the interface has powered down. This bit is updated by an adapter that transmits the state of power-up/power-down requests. It is equivalent to the CardBus Preset State Register's Power Cycle bit (bit 3).
Bit 5	The Read/Busy# bit is set to 1 to indicate that the PC Card is ready to perform a data transfer, and set to 0 to indicate that the card is busy completing an operation and cannot accept new data or commands.
Bit 4	The Memory Write Protect bit returns the logic level of the memory PC Card interface's WP signal. However, memory write access is blocked only when the Write Protect bit in the Card Memory Offset High Byte Register is set to 1.
Bit 3	The Card Detect 2 bit returns the state of the CD2# pin. A 1 indicates that CD2# is high (a card is not inserted), and a 0 indicates that CD2# is low (a card is inserted). This bit is equivalent to the CardBus Preset State Register's CCD2# bit (bit 2).
Bit 2	The Card Detect 1 bit returns the state of the CD1# pin. A 1 indicates that CD1# is high (a card is not inserted), and a 0 indicates that CD1# is low (a card is inserted). This bit is equivalent to the CardBus Preset State Register's CCD1# bit (bit 1).
Bit [1:0]	For memory cards, the Battery Voltage Detect bits return battery status. For IO cards, bit 0 returns the state of the STSCHG signal from the PC Card. Bit 1 returns the stale of the SRKR signal from the PC card. Refer to the description of the General Interrupt Register (IGENC) bit 7 for details

5.2.1.3 Voltage Control Register (PCTRL)

Index : 02h
Default value : 00h
Access : Read/write
Size : 8-bit

This register controls the voltages supplied to the PC Card. Voltages to the socket can also be controlled by the CardBus Socket Control Register. Supply voltages are controlled by either this register or the Socket Control Reg. (There is no need to set both registers.)

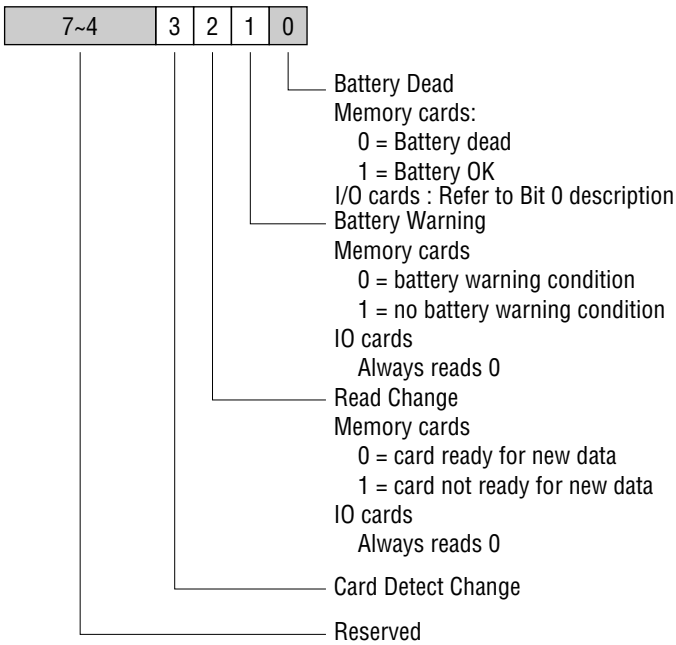


Bit	Description
Bit 7	When the Output Enable bit is 0, MSM60808 output signals directly connected to the socket will be tri-stated. When 1, the signals will not be tri-stated.
Bit 6	This reserved bit always reads as 0.
Bit 5	This reserved bit always reads as 0.
Bit 4	This reserved bit always reads as 0.
Bit [3:2]	VCC Control bit: 00b = requested VCC voltage: power-off 01b = reserved 10b = requested VCC voltage: 5.0 V 11b = requested VCC voltage: 3.3 V
Bit [1:0]	VPP Control bit: 00b = requested VPP voltage: power-off 01b = requested VCC voltage: 5.0 V 10b = requested VCC voltage: 12.0 V 11b = reserved

5.2.1.4 Card Status Change Register (CSTCH)

Index : 04h
Default value : 00h
Access : Read/write
Size : 8-bit

This register contains the status of card status change sources. These sources can be enabled to generating a card status change interrupt by setting the corresponding bit in the Card Status Change Interrupt Configuration Register (CSCICR). A bit in the Card Status Change Register will read as 0 when the corresponding bit in the Card Status Change Interrupt Configuration Register is 0.

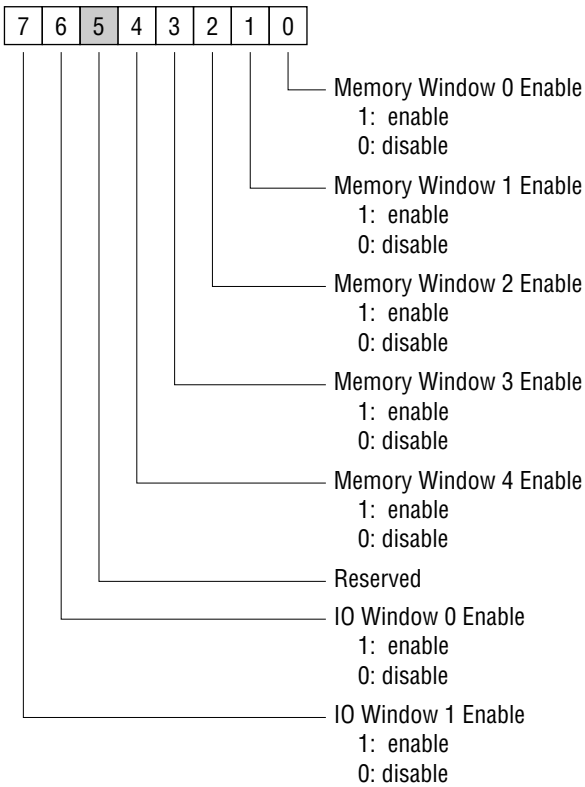


Bit	Description
Bit [7:4]	These reserved bits always read 0.
Bit 3	The Card Detect Change bit is set to 1 when a change in the CD1# or CD2# signal is detected. (It is also set when bits 1 and 2 of the CardBus Socket Event Register change.)
Bit 2	The Ready Change bit is set to 1 when a low-to-high transition occurs on the Ready/Busy# signal, indicating that the PC Card can accept a new data transfer. For IO cards this bit always reads 0.
Bit 1	The Battery Warning bit is set to 1 when a battery warning condition is detected. For IO cards this bit always reads 0.
Bit 0	The Battery Dead bit is set to 1 when a battery dead condition is detected. When the battery dead condition is cleared, this bit will return to 0. For IO cards this bit is set to 1 when the STSCHG# signal from the IO card has been asserted low.

5.2.1.5 Address Window Enable Register (ADWEN)

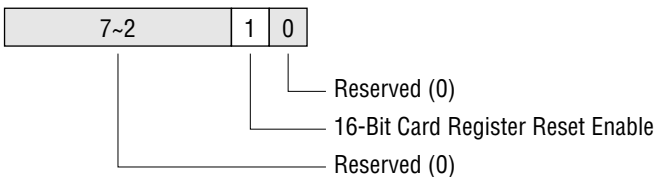
Index : 06h
Default value : 00h
Access : Read/write
Size : 8-bit

This register controls enabling/disabling of memory and IO mapping to PC Card memory and IO space.



5.2.1.6 General Control Register (GRCTL)

Index : 16h
Default value : 00h
Access : Read/write
Size : 8-bit



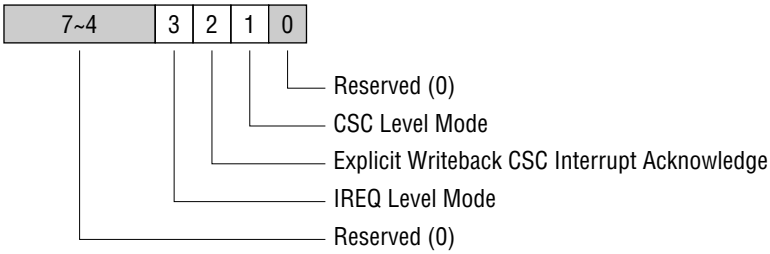
Bit	Description
Bit [7:2]	These reserved bits always read 0.
Bit 1	The default value of the 16-Bit Card Register Reset Enable is 0. When set to 0, 16-bit card register reset from card detection is disabled. When set to 1 and both the CD1# and CD2# inputs for a particular slot go high, a reset pulse will be generated to reset the 16-bit card registers.
Bit 0	This reserved bit always reads 0.

Index	Register Name
03	General Interrupt Control
06	Address Window Enable
07	IO Control
08	IO Address 0 Start Low Byte
09	IO Address 0 Start High Byte
0A	IO Address 0 Stop Low Byte
0B	IO Address 0 Stop High Byte
0C	IO Address 1 Start Low Byte
0D	IO Address 1 Start High Byte
0E	IO Address 1 Stop Low Byte
0F	IO Address 1 Stop High Byte
10	Memory Address Mapping Window 0 Start Low Byte
11	Memory Address Mapping Window 0 Start High Byte
12	Memory Address Mapping Window 0 Stop Low Byte
13	Memory Address Mapping Window 0 Stop High Byte
14	Card Memory Offset Address 0 Low Byte
15	Card Memory Offset Address 0 High Byte
18	Memory Address Mapping Window 1 Start Low Byte
19	Memory Address Mapping Window 1 Start High Byte
1A	Memory Address Mapping Window 1 Stop Low Byte
1B	Memory Address Mapping Window 1 Stop High Byte
1C	Card Memory Offset Address 1 Low Byte
1D	Card Memory Offset Address 1 High Byte

Index	Register Name
20	Memory Address Mapping Window 2 Start Low Byte
21	Memory Address Mapping Window 2 Start High Byte
22	Memory Address Mapping Window 2 Stop Low Byte
23	Memory Address Mapping Window 2 Stop High Byte
24	Card Memory Offset Address 2 Low Byte
25	Card Memory Offset Address 2 High Byte
28	Memory Address Mapping Window 3 Start Low Byte
29	Memory Address Mapping Window 3 Start High Byte
2A	Memory Address Mapping Window 3 Stop Low Byte
2B	Memory Address Mapping Window 3 Stop High Byte
2C	Card Memory Offset Address 3 Low Byte
2D	Card Memory Offset Address 3 High Byte
30	Memory Address Mapping Window 4 Start Low Byte
31	Memory Address Mapping Window 4 Start High Byte
32	Memory Address Mapping Window 4 Stop Low Byte
33	Memory Address Mapping Window 4 Stop High Byte
34	Card Memory Offset Address 4 Low Byte
35	Card Memory Offset Address 4 High Byte

5.2.1.7 Global Control Register (GLBCTL)

Index : 1Eh
Default value : 00h
Access : Read/write
Size : 8-bit



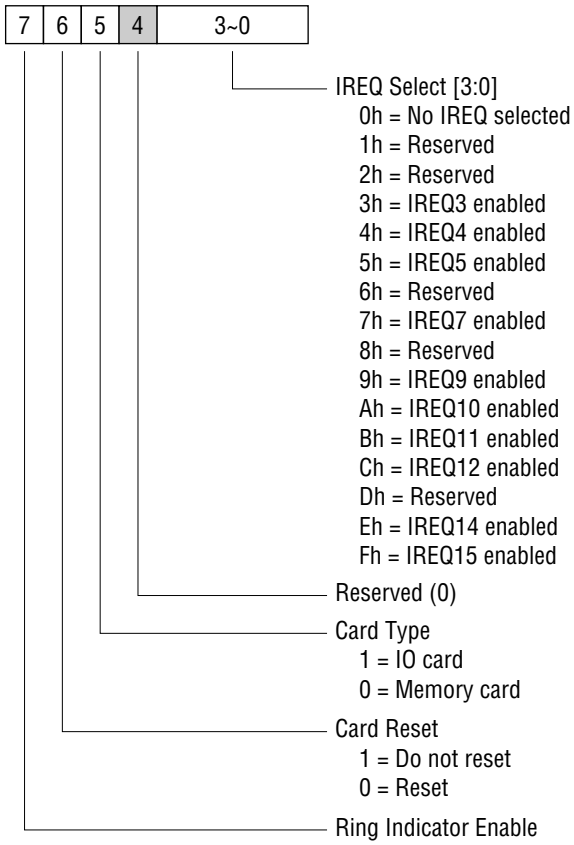
Bit	Description
Bit [7:4]	These reserved bits always read 0.
Bit 3	When the IREQ Level Mode bit is 1, interrupts generated through the PC Cards IREQ signal will be set to level mode. When 0, edge mode will become effective.
Bit 2	Setting the Explicit Writeback CSC Interrupt Acknowledge bit to 1 will clear an interrupt by writing 1 to the bit in the Card Status Change Register corresponding to the interrupt source. When set to 0, card status change interrupts will be recognized and cleared by reading the Card Status Change Register.
Bit 1	Setting the CSC Level Mode bit to 1 will set level mode for card status change interrupts. When set to 0, edge mode interrupts will become effective.
Bit 0	This reserved bit always reads 0.

5.2.2 Interrupt Registers

5.2.2.1 General Interrupt Register (IGENC)

Index : 03h
Default value : 00h
Access : Read/write
Size : 8-bit

This register selects card type and controls PC Card IO interrupts.

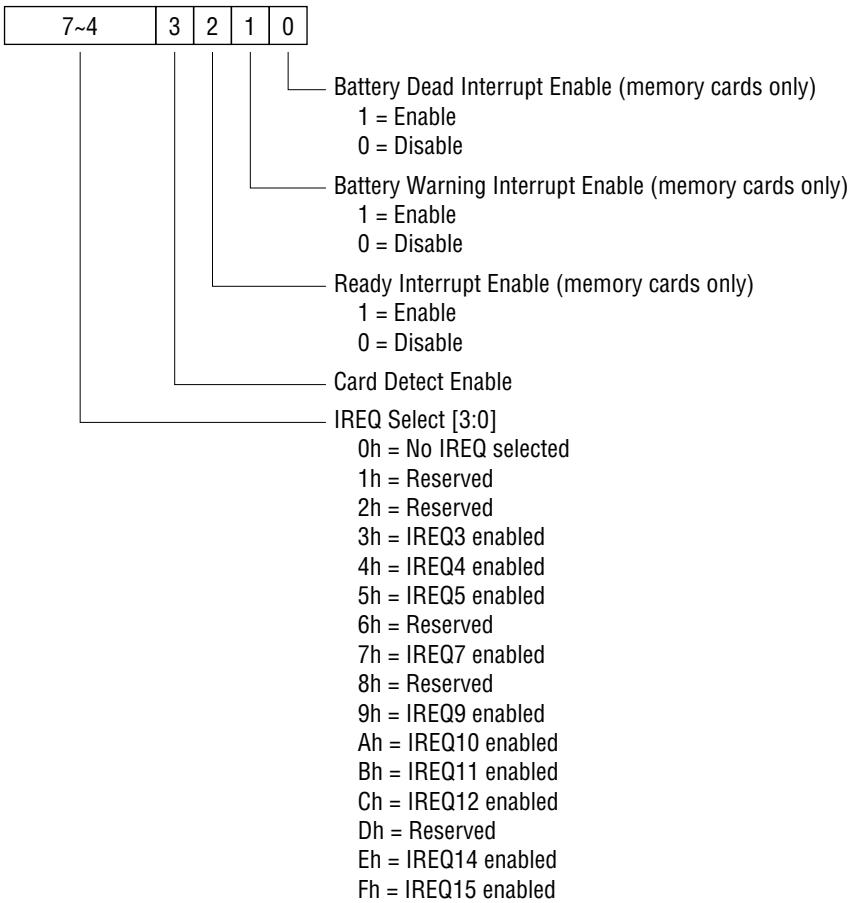


<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>Bit 7</td><td>When both the Ring Indicator Enable bit and the PC Card Type bit (bit 5) are set to 1, the STSCHG#/RI# signal from the card will be handled as the ring indicator signal (RI#), and will be output from the MSM60808's RI_OUT output pin. When the Ring Indicator Enable bit is 0 and the PC Card Type bit is 1, the STSCHG#/RI# signal from the card will be used as the status change signal (STSCHG#). This signal is used as a card status change interrupt source, and its state can be read from the Interface Status Register. When the PC Card Type bit is 0 (for memory cards), the Ring Indicator Enable bit has no function.
<table>
<tr><th>Bit 7</th><th>Bit 5</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>No function</td></tr>
<tr><td>0</td><td>1</td><td>STSCHG#</td></tr>
<tr><td>1</td><td>0</td><td>No function</td></tr>
<tr><td>1</td><td>1</td><td>RI# → RI_OUT#</td></tr>
</table>
</td></tr>
<tr><td>Bit 6</td><td>Setting the Card Reset bit to 0 resets the PC Card by asserting the reset signal to the card.</td></tr>
<tr><td>Bit 5</td><td>Setting the Card Type bit to 1 selects an IO card. The status bit of the Interface Status Register differ for IO cards and memory cards.</td></tr>
<tr><td>Bit 4</td><td>This reserved bit always reads 0.</td></tr>
<tr><td>Bit [3:0]</td><td>The IREQ Select bits select the routing of IO card interrupts.</td></tr>
</table>

5.2.2.2 Card Status Change Interrupt Configuration Register (CSCICR)

Index : 05h
Default value : 00h
Access : Read/write
Size : 8-bit

This register controls card status change interrupts and interrupt pin enables. Other status change interrupt control is performed by the CardBus Socket Mask Register (MASK).



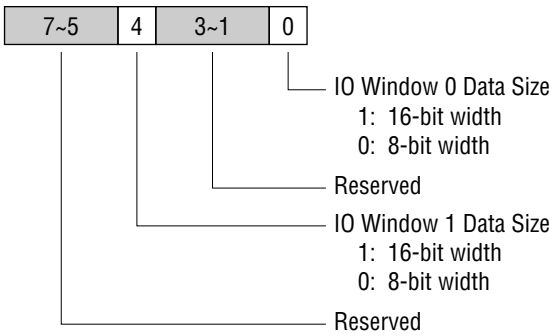
Bit	Description
Bit [7:4]	The IREQ Select bits select the assignment of card status change interrupts.
Bit 3	Setting the Card Detect Enabled bit to 1 enables card status change interrupts when a change to the CD1# or CD2# signal is detected. Setting to 0 disables these interrupts.
Bit 2	Setting the Ready Enable bit to 1 enables status change interrupts when the Ready/Busy# signal transitions from low to high. Setting to 0 disables these interrupts.
Bit 1	Setting the Battery Warning Enable bit to 1 enables status change interrupts when a battery warning condition is detected. Setting to 0 disables these interrupts.
Bit 0	Setting the Battery Dead Enable bit to 1 enables status change interrupts when a battery dead condition is detected. Setting to 0 disables these interrupts.

5.2.3 IO Mapping Control Registers

5.2.3.1 IO Control Register (IOCREG)

Index : 07h
Default value : 00h
Access : Read/write
Size : 8-bit

This register enables/disables IO mapping to the PC Card's IO space. This register controls the data width of IO windows 0 and 1.



5.2.3.2 IO Address 0 Start Low Byte Register (IOSL0)

Index : 08h
Default value : 00h
Access : Read/write
Size : 8-bit

This register stores the low byte of the start address of IO Address Window 0. If the start address and stop address are the same, then this register will provide a minimum 1-byte IO address window.

5.2.3.3 IO Address 0 Start High Byte Register (IOSH0)

Index : 09h
Default value : 00h
Access : Read/write
Size : 8-bit

This register stores the high byte of the start address of IO Address Window 0. If the start address and stop address are the same, then this register will provide a minimum 1-byte IO address window.

5.2.3.4 IO Address 0 Stop Low Byte Register (IOSTL0)

Index : 0Ah
Default value : 00h
Access : Read/write
Size : 8-bit

This register stores the low byte of the stop address of IO Address Window 0. If the start address and stop address are the same, then this register will provide a minimum 1-byte IO address window.

5.2.3.5 IO Address 0 Stop High Byte Register (IOSTH0)

Index : 0Bh
Default value : 00h
Access : Read/write
Size : 8-bit

This register stores the high byte of the stop address of IO Address Window 0. If the start address and stop address are the same, then this register will provide a minimum 1-byte IO address window.

5.2.3.6 IO Address 1 Start Low Byte Register (IOSL1)

Index : 0Ch
Default value : 00h
Access : Read/write
Size : 8-bit

This register stores the low byte of the start address of IO Address Window 1. If the start address and stop address are the same, then this register will provide a minimum 1-byte IO address window.

5.2.3.7 IO Address 1 Start High Byte Register (IOSH1)

Index : 0Dh
Default value : 00h
Access : Read/write
Size : 8-bit

This register stores the high byte of the start address of IO Address Window 1. If the start address and stop address are the same, then this register will provide a minimum 1-byte IO address window.

5.2.3.8 IO Address 1 Stop Low Byte Register (IOSTL1)

Index : 0Eh
Default value : 00h
Access : Read/write
Size : 8-bit

This register stores the low byte of the stop address of IO Address Window 1. If the start address and stop address are the same, then this register will provide a minimum 1-byte IO address window.

5.2.3.9 IO Address 1 Stop High Byte Register (IOSTH1)

Index : 0Fh
Default value : 00h
Access : Read/write
Size : 8-bit

This register stores the high byte of the stop address of IO Address Window 1. If the start address and stop address are the same, then this register will provide a minimum 1-byte IO address window.

5.2.4 Memory Mapping Control Registers

5.2.4.1 Memory Address Mapping Window 0/1/2/3/4 Start Low Byte Register (SML0/1/2/3/4)

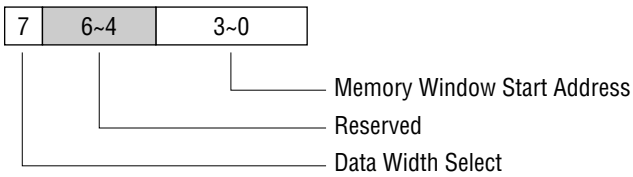
Index : 10h/18h/20h/28h/30h
Default value : 00h
Access : Read/write
Size : 8-bit

These registers store the low byte of the corresponding memory address mapping window's start address. These registers also correspond to PCI memory address A[19:12], and are used to determine whether or not memory accesses are valid.

5.2.4.2 Memory Address Mapping Window 0/1/2/3/4 Start High Byte Register (SMH0/1/2/3/4)

Index : 11h/19h/21h/29h/31h
Default value : 00h
Access : Read/write
Size : 8-bit

These registers store the high byte of the corresponding memory address mapping window's start address. These registers also correspond to PCI memory address A[23:20], and are used to determine whether or not memory accesses are valid. The data width of the corresponding window is controlled by bits in these registers also.



Bit	Description
Bit 7	Data Width Select 1 = 16-bit data width 0 = 8-bit data width
Bit [6:4]	These reserved bits always read 0.
Bit [3:0]	Memory Window Start Address

5.2.4.3 Memory Address Mapping Window 0/1/2/3/4 Stop Low Byte Register (SMSTL0/1/2/3/4)

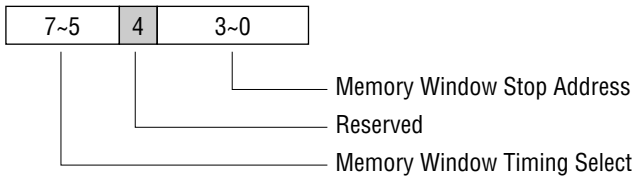
Index : 12h/1Ah/22h/2Ah/32h
Default value : 00h
Access : Read/write
Size : 8-bit

These registers store the low byte of the corresponding memory address mapping window's stop address. These registers also correspond to PCI memory address A[19:12], and are used to determine whether or not memory accesses are valid.

5.2.4.4 Memory Address Mapping Window 0/1/2/3/4 Stop High Byte Register (SMSTH0/1/2/3/4)

Index : 13h/1Bh/23h/2Bh/33h
Default value : 00h
Access : Read/write
Size : 8-bit

These registers store the high byte of the corresponding memory address mapping window's stop address. These registers also correspond to PCI memory address A[23:20], and are used to determine whether or not memory accesses are valid. The 16-bit access cycle time of the corresponding window is controlled by bits in these registers also.



Bit	Description
Bit [7:5]	Memory Window Timing Select 000b = Reserved 001b = 80 ns 010b = 100 ns 011b = 150 ns 100b = 200 ns 101b = 250 ns 110b = 600 ns 111b = Reserved
Bit 4	This reserved bit always reads 0.
Bit [3:0}	Memory Window Stop Address

5.2.4.5 Card Memory Offset Address 0/1/2/3/4 Low Byte Register (OFFL0/1/2/3/4)

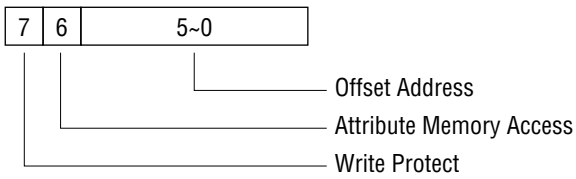
Index : 14h/1Ch/24h/2Ch/34h
Default value : 00h
Access : Read/write
Size : 8-bit

These registers store the low byte added to system address A[19:12] to obtain the PC Card memory address.

5.2.4.6 Card Memory Offset Address 0/1/2/3/4 High Byte Register (OFFH0/1/2/3/4)

Index : 15h/1Dh/25h/2Dh/35h
Default value : 00h
Access : Read/write
Size : 8-bit

Bits[5:0] of these registers are added to PCI memory address A[23:20] to obtain the PC Card memory address. These registers also control PC Card memory software write protect of the corresponding system memory window, and select mapping to common memory or to attribute memory of PC Card.



Bit	Description
Bit 7	Write Protect 1 = Write protect 0 = Do not write protect When the Write Protect bit is set to 1, write operations to the PC Card through the corresponding system memory window are inhibited. When set to 0, write operations are permitted. Even if the write protect switch sets the Interface Status Register's Write Protect bit, that alone will not inhibit memory write cycles.
Bit 6	When the Attribute Memory Access bit is set to 1, accesses to the system memory window will access the PC Card's attribute memory by asserting REG# low, and will access the PC Card's common memory by driving REG# high.
Bit [5:0]	The Offset Address bits are added to PCI memory address bits A[23:20] to obtain the PC Card memory address.

5.3 CardBus Registers

CardBus registers show socket status and control the clock.

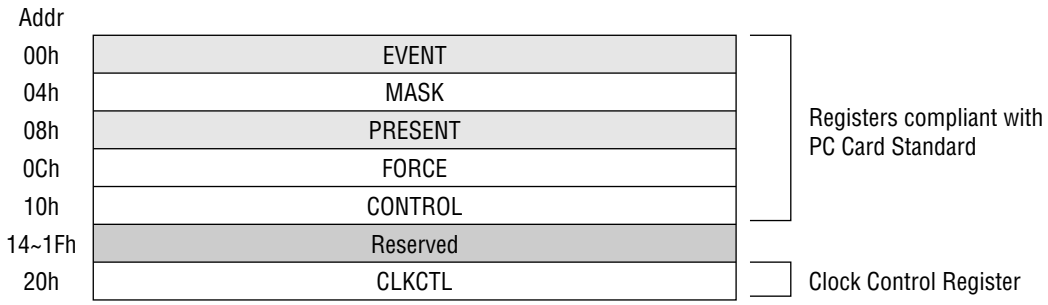
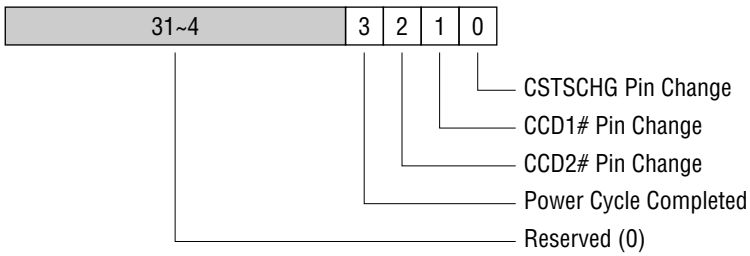


Figure 5.3 CardBus Register Space

5.3.1 Socket Event Register (EVENT)

Offset : 00h
Default value : 0000 0000h
Access : Read/write
Size : 32-bit

MSM60808 uses the Socket Event Register to generate status changed interrupts. The fields in this register indicate that a change in socket status has occurred.
Card service must read this register and present status register to detect the source of interrupt. Card service should be responsible to clear the verified field after the source detection of static change interrupt.

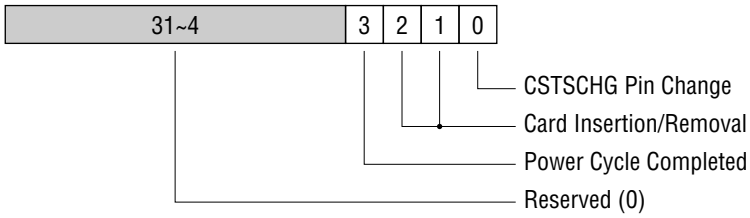


Bit	Description
Bit 3	The Power Cycle Completed field is set to 1 by the MSM60808 when it detects that a power cycle is complete. Note that the Present State Register must be read to see whether or not power-up is successful. Writing 1 to this field will clear it. The state will be 0 after reset.
Bit 2	The CCD2# Pin Change field is always set to 1 when the state of CCD2# in the Present State Register changes. Writing 1 to this field will clear it. The state will be 0 after reset.
Bit 1	The CCD1# Pin Change field is always set to 1 when the state of CCD1# in the Present State Register changes. Writing 1 to this field will clear it. The state will be 0 after reset.
Bit 0	The CSTSCHG Pin Change field is always set to 1 when the state of CSTSCHG in the Present State Register changes. Writing 1 to this field will clear it. The state will be 0 after reset.

5.3.2 Interrupt Mask Register (MASK)

This register gives software the ability to control which events cause status changed interrupts to be generated. It inhibits the corresponding fields in the Socket Event Register from causing status changed interrupts.

Offset : 04h
Default value : 0000 0000h
Access : Read/write
Size : 32-bit

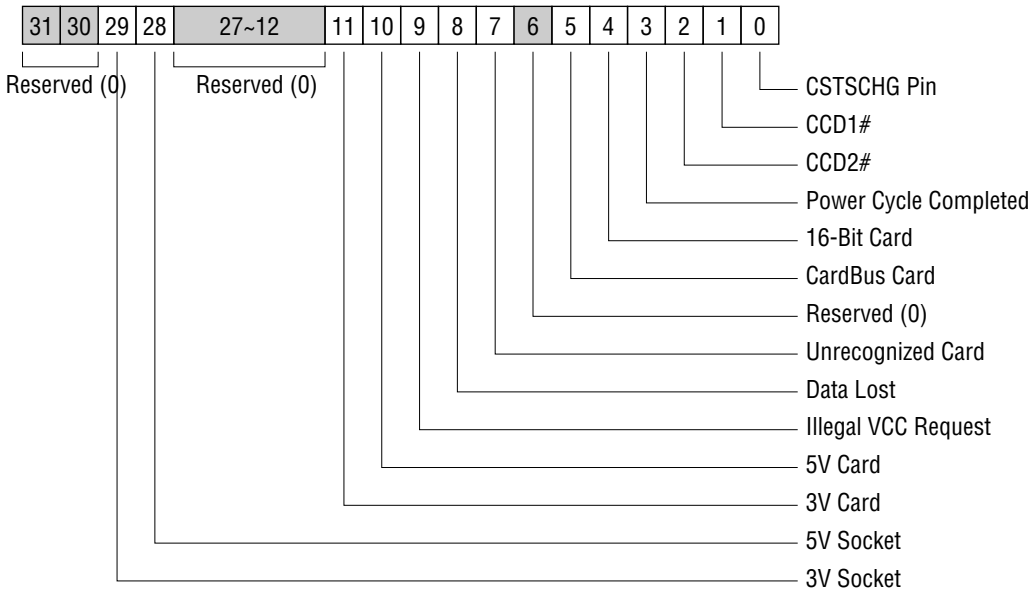


Bit	Description
Bit [31:4]	These reserved fields always read 0.
Bit 3	When the Power Cycle Completed field is cleared to 0, the status changed event signaling that a power cycle is complete will not generate a status changed interrupt even if the Power Cycle field in the Event register has been set. Writing 1 to this field will set it.
Bit [2:1]	The Card Insertion/Removal field masks the Event Register's CCD1# and CCD2# fields so that card insertion and removal events will not cause status changed interrupts to occur. Note that the Event Register's CCD1# and CCD2# fields will still be set. The meaning of the bits is as follows: 00: Mask Event Register's CCD1# and CCD2# fields. Insertion and removal events will not cause status changed interrupts. This is MSM60808's reset value. 01: Not applicable. 10: Not applicable. 11: Do not mask Event Register'S CCD1# and CCD2# fields. Insertion and removal events will cause status changed interrupts.
Bit 0	When the CSCCHG Pin Change field is cleared to 0, assertion of CSTSCHG by the card will not cause a status changed interrupt to occur even if the Event Register's CSTSCHG field has been set. Writing 1 to this field will set it. It is cleared whenever the PC Card inserted in the socket is removed or the MSM60808 is reset.

5.3.3 Present State Register (PRESENT)

This read-only register reflects the current state of the socket. Some bits indicate states related to status changed events and some reflect card interface signals.

Offset : 08h
Default value : 0000 0000h
Access : Read-only
Size : 32-bit



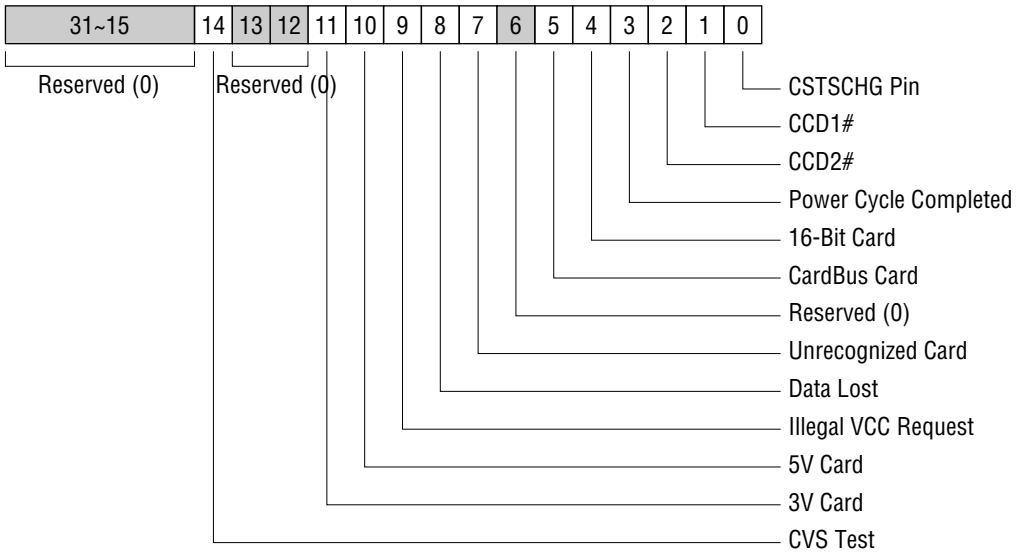
Bit	Description
Bit [31:30]	Reserved
Bit 29	When the 3V Socket field is 1, the socket can provide a 3.3V voltage. When 0, it cannot provide 3.3V
Bit 28	When the 3V Socket field is 1, the socket can provide a 5V voltage. When 0, the socket cannot provide 5V.
Bit [27:12]	Reserved
Bit 11	When the 3V Card field is set to 1, the inserted card can operate with 3.3V. When cleared to 0, the inserted card cannot operate with 3.3V. This field's value is determined using CVS[2:1] and CCD[2:1].
Bit 10	When the 5V Card field is set to 1, the inserted card can operate with 5V. When cleared to 0, the inserted card cannot operate with 5V. This field's value is determined using CVS[2:1] and CCD[2:1]. When a CardBus card is inserted, the MSM60808 does not permit the socket to apply 5V.

Bit	Description
Bit 9	When the Illegal VCC Request field is set to 1, it indicates that software attempted to apply a VCC voltage outside the range detected by using CVS[2:1] and CCD[2:1].
Bit 8	When the Data Lost field is set to 1, it indicates that a PC Card removal event may have caused lost data either because a transaction had not completed or because data remained in the MSM60808's internal buffer.
Bit 7	When the Unrecognized Card field is set to 1, it indicates that the type of card inserted could not be determined. This value will not be updated until a recognizable card (CardBus card or 16-bit card) is inserted.
Bit 6	Reserved
Bit 5	When the CardBus Card field is set to 1, it indicates that the inserted card is a CardBus card. This value will not be updated until a non-CardBus card is inserted. When set, the MSM60808 will configure the socket interface for CardBus card use.
Bit 4	When the 16-Bit Card field is set to 1, it indicates that the inserted card is a 16-bit card. This value will not be updated until a non-16-bit card is inserted. When set, the MSM60808 will configure the socket interface for 16-bit card use.
Bit 3	When the Power Cycle field is set to 1, it indicates that the interface is powered up. When 0, it indicates that the interface is powered down or that power up was not successful. This field is updated by the MSM60808 to communicate the status of power up/power down requests.
Bit 2	The CCD2# field indicates the current state of the CCD2# pin on the interface. 1 indicates that CCD2# is high (card is not present in socket). 0 indicates that CCD2# is low (card is present in socket). The CCD2# pin may be shorted to the CVS1 or CVS2 pin, so the value stored in this field is for when the CVS pins are low.
Bit 1	The CCD1# field indicates the current state of the CCD1# pin on the interface. 1 indicates that CCD1# is high (card is not present in socket). 0 indicates that CCD2# is low (card is present in socket). The CCD1# pin may be shorted to the CVS1 or CVS2 pin, so the value stored in this field is for when the CVS pins are low.
Bit 0	The CSTSCHG field reflects the current state of the CSTSCHG pin on the interface. 1 indicates that CSTSCHG is asserted, and 0 indicates that it is deasserted.

5.3.4 Force Event Register (FORCE)

The CardBus can simulate events for debug purposes by forcing values in the Socket Event Register and Present State Register. Note that this register is not physically implemented. Instead it is an address at which the Present State Register can be written. The result of writing to this address will be reflected in the Present State Register and Socket Event Register. However, other events may alter those registers before they can be read.

Offset : 0Ch
Default value : 0000 0000h
Access : Read/write
Size : 32-bit



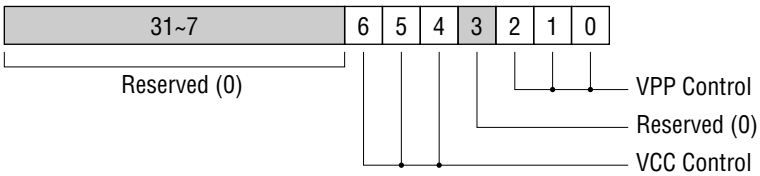
Bit	Description
Bit [31:15]	Reserved.
Bit 14	When 1 is written to the CVS Test bit, the MSM60808 will again interrogate the CVS[2:1] and CCD#[2:1] states and update the Present State Register's nV Card fields. This operation enables the socket to power up VCC again if the nV Card fields are forced.
Bit [13:12]	Reserved
Bit 11	Writing the 3V Card field in this register writes to the 3V Card field in the Present State Register. Even if this field is set to 1, the socket cannot power up VCC until the CVS Test field is set.
Bit 10	Writing the 5V Card field in this register writes to the 5V Card field in the Present State Register. Even if this field is set to 1, the socket cannot power up VCC until the CVS Test field is set.

Bit	Description
Bit 9	Writing the Illegal VCC Request field in this register writes to the Illegal VCC Request field in the Present State Register.
Bit 8	Writing the Data Lost field in this register writes to the Data Lost field in the Present State Register.
Bit 7	Writing the Unrecognized Card field in this register writes to the Unrecognized Card field in the Present State Register. Writes to this field are ignored if a card is inserted in the socket.
Bit 6	Reserved.
Bit 5	Writing the CardBus Card field in this register writes to the CardBus Card field in the Present State Register. Writes to this field are ignored if a card is inserted in the socket.
Bit 4	Writing the 16-Bit Card field in this register writes to the 16-Bit Card field in the Present State Register. Writes to this field are ignored if a card is inserted in the socket.
Bit 3	Writing the Power Cycle field in this register sets the Power Cycle field in the Event Register to 1, which can simulate a successful power cycle completion. However, writing 1 to this field will not affect the Power Cycle field in the Present State Register. Writing 0 to this field has no meaning.
Bit 2	Writing the CCD2# field in this register sets the CCD2# field in the Event Register to 1. However, writing 1 to this field will not affect the CCD2# field in the Present State Register. Writing 0 to this field has no meaning.
Bit 1	Writing the CCD1# field in this register sets the CCD1# field in the Event Register to 1. However, writing 1 to this field will not affect the CCD1# field in the Present State Register. Writing 0 to this field has no meaning.
Bit 0	Writing the CSTSCHG field in this register sets the CSTSCHG field in the Event Register to 1. However, writing 1 to this field will not affect the CSTSCHG field in the Present State Register. Writing 0 to this field has no meaning.

5.3.5 Socket Control Register (CONTROL)

This register controls the VCC and VPP voltages applied to the socket.

Offset : 10h
Default value : 0000 0000h
Access : Read/write
Size : 32-bit

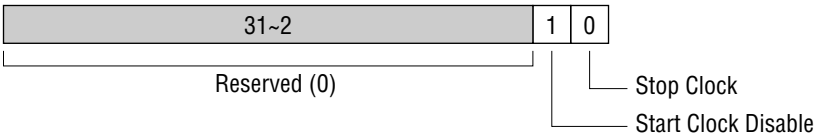


Bit	Description
Bit [31:7]	These reserved bits always read 0.
Bit [6:4]	VCC Control 000b : Power off request 001b : Reserved 010b : 5V VCC voltage request 011b : 3.3V VCC voltage request 100b~111b : Reserved
Bit 3	These reserved bits always read 0.
Bit [2:0]	VPP Control 000b : Power off request 001b : 12V VPP voltage request 010b : 5V VPP voltage request 011b : 3.3V VPP voltage request 100b~111b : Reserved

5.3.6 CardBus Clock Control Register (CLKCTL)

This register is used to control the CardBus clock.

Offset : 20h
Default value : 0000 0000h
Access : Read-only
Size : 32-bit



Bit	Description
Bit [31:2]	These reserved bits always read 0.
Bit 1	When the Start Clock Disable bit is 0, CCLK will be output on the CardBus and CCLKRUN# will be asserted. If this bit is set to 1, then the clock supply to the CardBus will stop when CCLKRUN# from the CardBus is not asserted.
Bit 0	When the Clock Stop bit is set to 1, the MSM60808 will drive CCLKRUN# high. Then the clock will stop after 4 clocks.

6. Electrical Specifications

6.1 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings

Item	Symbol	Condition	Rated Value	Unit
Power supply voltage	VDD	Referenced to ground	–0.3 to +6.5	V
Input voltage	V_{IN}		–0.5 to VDD+0.5	V
Output voltage	V_{OUT}		–0.5 to VDD+0.5	V
Storage temperature	T_{STG}	—	–65 to +150	°C

6.2 Recommended Operating Conditions

Table 6.2 Recommended Operating Conditions

Item	Symbol	Range	Unit
Power supply voltage	VDD	3 to 5.5	V
Operating temperature	Top	0 to 70	°C
Trangistor junction temprature	Tj	85 max.	°C
Input rise time/fall time	tr, tf	1 to 20	ns

6.3 DC Characteristics

Table 6.3 PCI Bus Interface

Item	Symbol	Operating voltage	Min.	Typ.	Max.	Unit
Core power supply voltage	VCC	3.3	3.0	3.3	3.6	V
PCI bus power supply voltage	VCCP	5.0	4.5	5.0	5.5	V
		3.3	3.0	3.3	3.6	
Input voltage	V_{IN}	5.0	0	—	VCCP	V
		3.3	0	—	VCCP	
Output voltage	V_{OUT}	5.0	0	—	VCCP	V
		3.3	0	—	VCCP	
Input high voltage	V_{IH}	5.0	2	—	—	V
		3.3	0.7VCC	—	—	
Input low voltage	V_{IL}	5.0	—	—	0.8	V
		3.3	—	—	0.3VCC	

Table 6.4 PC Card Interface

Item	Symbol	Operating voltage	Min.	Typ.	Max.	Unit
Core power supply voltage	VDD_C	3.3	3.0	3.3	3.6	V
PC Card supply voltage	VCCA/B	5.0	4.5	5	5.5	V
		3.3	3.0	3.3	3.6	
Input voltage	V_{IN}	5.0	0	—	VCCA/B	V
		3.3	0	—	VCCA/B	
Output voltage	V_{OUT}	5.0	0	—	VCCA/B	V
		3.3	0	—	VCCA/B	
Input high voltage	V_{IH}	5.0	2.4	—	—	V
		3.3	2.0	—	—	
Input low voltage	V_{IL}	5.0	—	—	0.8	V
		3.3	—	—	0.8	

Table 6.5 Other DC Characteristics

Item	Symbol	Interface	Operating voltage	Condition	Min.	Max.	Unit
Output high voltage	V_{OH}	PCI	5V	IOH=–2mA	2.4		V
			3.3V	IOH=–2mA	0.9×VDD		
		PC Card	5V	IOH=4mA	2.4		
			3.3V	IOH=4mA	0.9×VDD		
Output low voltage	VOL	PCI	5V	IOH=6mA		0.55	V
			3.3V	IOH=6mA		0.1VDD	
		PC Card	5V	IOH=4mA		0.55	
			3.3V	IOH=4mA		0.1VDD	
3-State output leak current	IOZH			VOH=VDD		1	µA
	IOZL			VOL=GND		–1	
Input high current	IIH			VI=VDD		–1	µA
Input low current	IIL			VI=GND		1	µA

6.4 AC Characteristics

6.4.1 PCI Bus AC Characteristics

Table 6.6 Clock Signal Specifications

Item	Symbol	Min.	Typ.	Max.	Unit
Clock cycle time	tcycp	30	—	∞	ns
Clock high time	t_{HWP}	12	—	—	ns
Clock low time	t_{LWP}	12	—	—	ns
Clock rise time/fall time	trp, tfp	1	—	4	V/ns

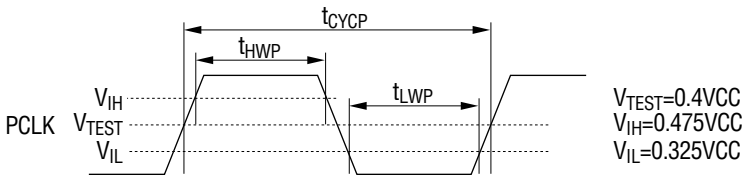


Figure 6.1 PCI Bus Clock Waveform

Table 6.7 Input Timing

Item	Symbol	Min.	Typ.	Max.	Unit
Valid output delay from clock	t_{VALP}	2	—	11	ns
Hi-Z to active drive delay time	t_{ONP}	2	—	—	ns
Active drive to Hi-Z delay time	t_{OFFP}	—	—	28	ns
Setup time to clock	t_{SUP}	7	—	—	ns
Hold time from clock	t_{HOP}	0	—	—	ns

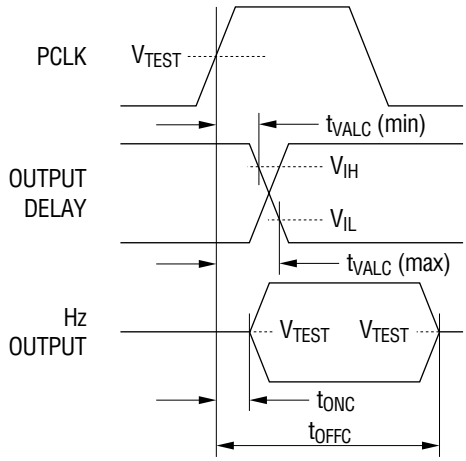
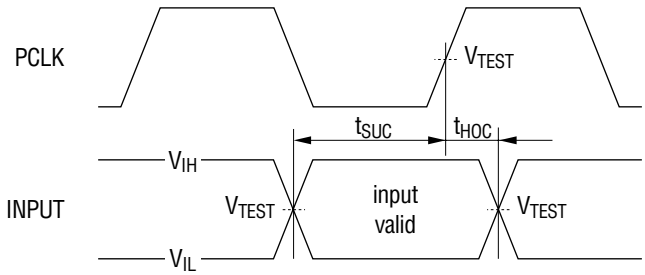


Figure 6.2 PCI Bus Output Timing



V_{TEST}=0.4VCC
V_{IH}=0.475VCC
V_{IL}=0.325VCC

Figure 6.3 PCI Bus Input Timing

6.4.2 CardBus AC Characteristics

Table 6.8 Clock Signal Specifications

Item	Symbol	Min.	Typ.	Max.	Unit
Clock cycle time	tcycc	30	—	∞	ns
Clock high time	thwc	12	—	—	ns
Clock low time	tlwc	12	—	—	ns
Clock rise time/fall time	trc, tfc	1	—	4	V/ns

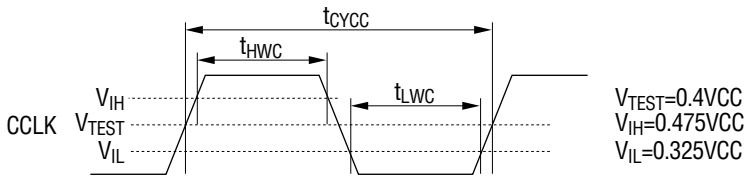


Figure 6.4 CardBus Clock Waveform

Table 6.9 Input Timing

Item	Symbol	Min.	Typ.	Max.	Unit
Valid output delay from clock	t_{VALC}	2	—	11	ns
Hi-Z to active drive delay	t_{ONC}	2	—	—	ns
Active drive to Hi-Z delay	t_{OFFC}	—	—	28	ns
Setup time to clock	t_{SUC}	7	—	—	ns
Hold time from clock	t_{HOC}	0	—	—	ns

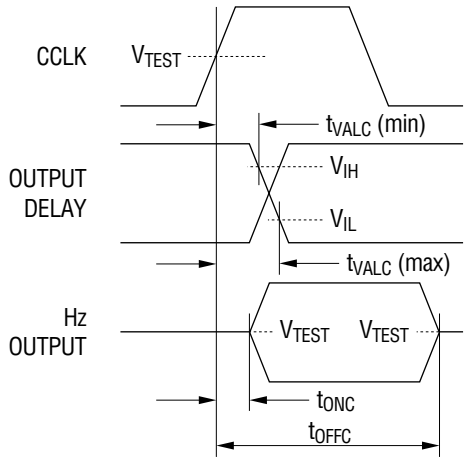
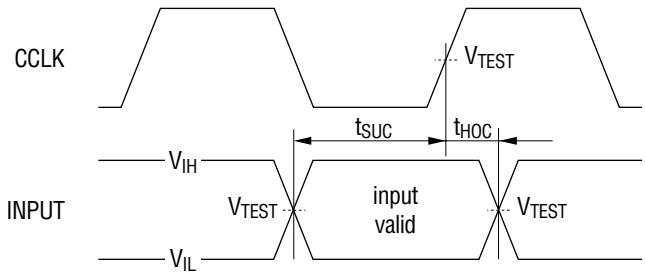


Figure 6.5 CardBus Output Timing



V_{TEST}=0.4VCC
V_{IH}=0.475VCC
V_{IL}=0.325VCC

Figure 6.6 CardBus Input Timing

6.4.3 16-Bit Card AC Characteristics

6.4.3.1 Memory Timing

Table 6.10 Common Memory Read Timing

Item	Symbol	600ns		250ns		200ns		150ns		100ns	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Read cycle time	tcR	600		250		200		150		100	
Address access time	ta (A)		600		250		200		150		100
Card enable access time	ta (CE)		600		250		200		150		100
Output enable access time	ta (OE)		300		125		100		75		50
Output disable time from OE#	tdis (OE)		150		100		90		75		50
Output disable time from CE#	ten (CE)	5		5		5		5		5	
Address change to data valid	tv (A)	0		0		0		0		0	
Address setup time	tsu (A)	100		30		20		20		10	
Address hold time	th (A)	35		20		20		20		15	
Card enable setup time	tsu (CE)	0		0		0		0		0	
Card enable Hold time	th (CE)	35		20		20		20		15	
WAIT# valid from OE#	tv (WT-OE)		100		35		35		35		35
WAIT# pulse width	tw (WT)		12µs		12µs		12µs		12µs		12µs
Data setup time from WAIT# release	tv (WT)	0		0		0		0		0	

Note: All unmarked units are ns.

Table 6.11 Common Memory Write Timing

Item	Symbol	600ns		250ns		200ns		150ns		100ns	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Write cycle time	tcW	600		250		200		150		100	
Write pulse width	tw (WE)	300		150		120		80		60	
Address setup time	tsu (A)	50		30		20		20		10	
Address setup time to WE#	tsu (A-WEH)	350		180		140		100		70	
Card enable setup time to WE#	tsu (CE-WEH)	300		180		140		100		70	
Data setup time to WE#	t (D-WEH)	150		80		60		50		40	
Data hold time	th (D)	70		30		20		20		15	
Write recovery time	trc (WE)	70		30		30		20		15	
Output disable time from WE#	tdis (WE)		150		100		90		75		50
Output disable time from OE#	tdis (OE)		150		100		90		75		50
Output enable time from WE#	ten (WE)	5		5		5		5		5	
Output enable time from WE#	ten (OE)	5		5		5		5		5	
Output enable setup time from WE#	tsu (OE-WE)	35		10		10		10		10	
Output enable hold time from WE#	th (OE-WE)	35		10		10		10		10	
Card enable setup time	tsu (CE)	0		0		0		0		0	
Card enable hold time	th (CE)	35		20		20		20		15	
WAIT# valid from WE#	tv (WT-WE)		100		35		35		35		35
WE# pulse width	wt (WT)		12µs		12µs		12µs		12µs		12µs
WE# deasserted from WAIT# release	tv (WT)	0		0		0		0		0	

Note: All unmarked units are ns.

Table 6.12 Attribute Memory Read Timing

Item	Symbol	300ns		600ns	
		Min.	Max.	Min.	Max.
Read cycle time	tcR	300		600	
Address access time	ta (A)		300		600
Card enable access time	ta (CE)		300		600
Output enable access time	ta (OE)		150		300
Output disable time from OE# deasserted	tdis (OE)		100		150
Output enable time from OE# asserted	ten (OE)	5		5	
Address change to data valid	tv (A)	0		0	
Address setup time	tsu (A)	30		100	
Address hold time	th (A)	20		35	
Card enable setup time	tsu (CE)	0		0	
Card enable hold time	th (CE)	20		35	
WAIT# valid from OE# asserted	tv (WT-OE)		35		100
WAIT# pulse width	tw (WT)		12µs		12µs
Data setup time from WAIT# release	tv (WT)	0		0	

Note: All unmarked units are ns.

* Attribute write timing follows 250 ns SRAM timing for 5V operation and 600 ns timing for 3.3V operation.

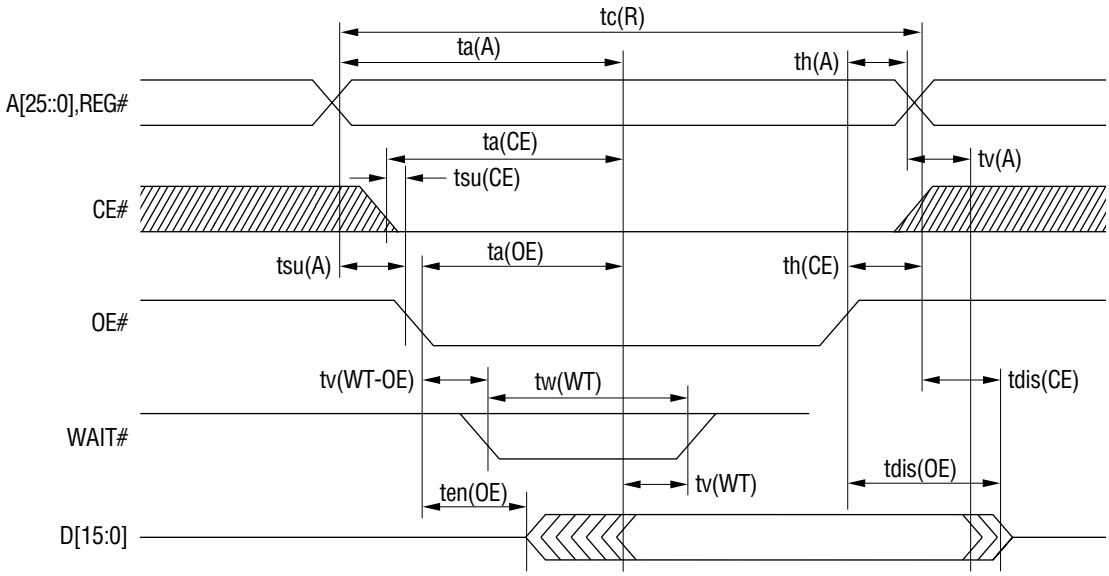


Figure 6.7 Memory Read Timing

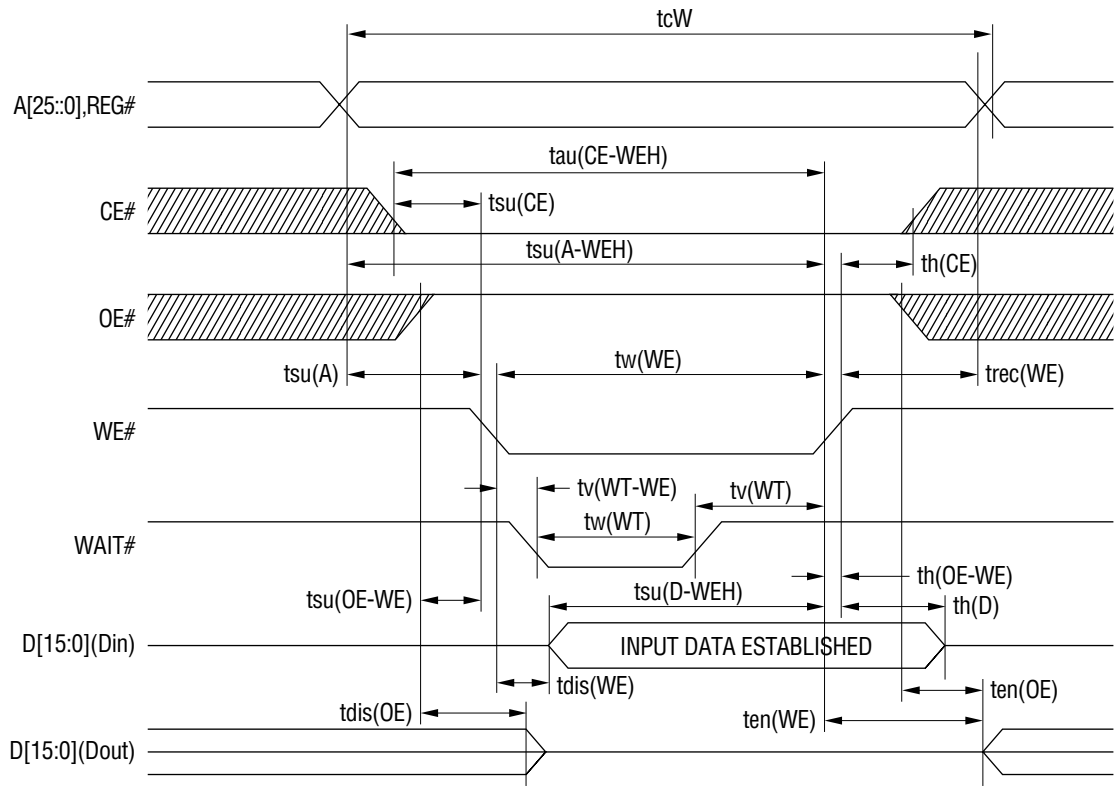


Figure 6.8 Memory Write Timing

Table 6.13 IO Read Timing

Item	Symbol	Min.	Max.
Data delay time from IORD# asserted	td (IORD)		100
Data hold time after IORD# deasserted	th (IORD)	0	
IORD# pulse width	twIORD	165	
Address setup time before IORD# asserted	tsuA (IORD)	70	
Address hold time after IORD# deasserted	thA (IORD)	20	
CE# setup time before IORD# asserted	tsuCE (IORD)	5	
CE# hold time after IORD# deasserted	thCE (IORD)	20	
REG# setup time before IORD# asserted	tsuREG (IORD)	5	
REG# hold time after IORD# deasserted	thREG (IORD)	0	
INPACK# fall delay time from IORD# asserted	tdfINPACK (IORD)	0	45
INPACK# rise delay time from IORD# deasserted	tdrINPACK (IORD)		45
IOIS16# fall delay time from address change	tdfIOIS16 (ADR)		35
IOIS16# rise delay time from address change	tdrIOIS16 (ADR)		35
WAIT# fall delay time from IORD# asserted	tdfWT (IORD)		35
Data delay time from WAIT# rise	tdr (WT)		0
WAIT# pulse width	tw (WT)		12,000

Note: All units are ns.

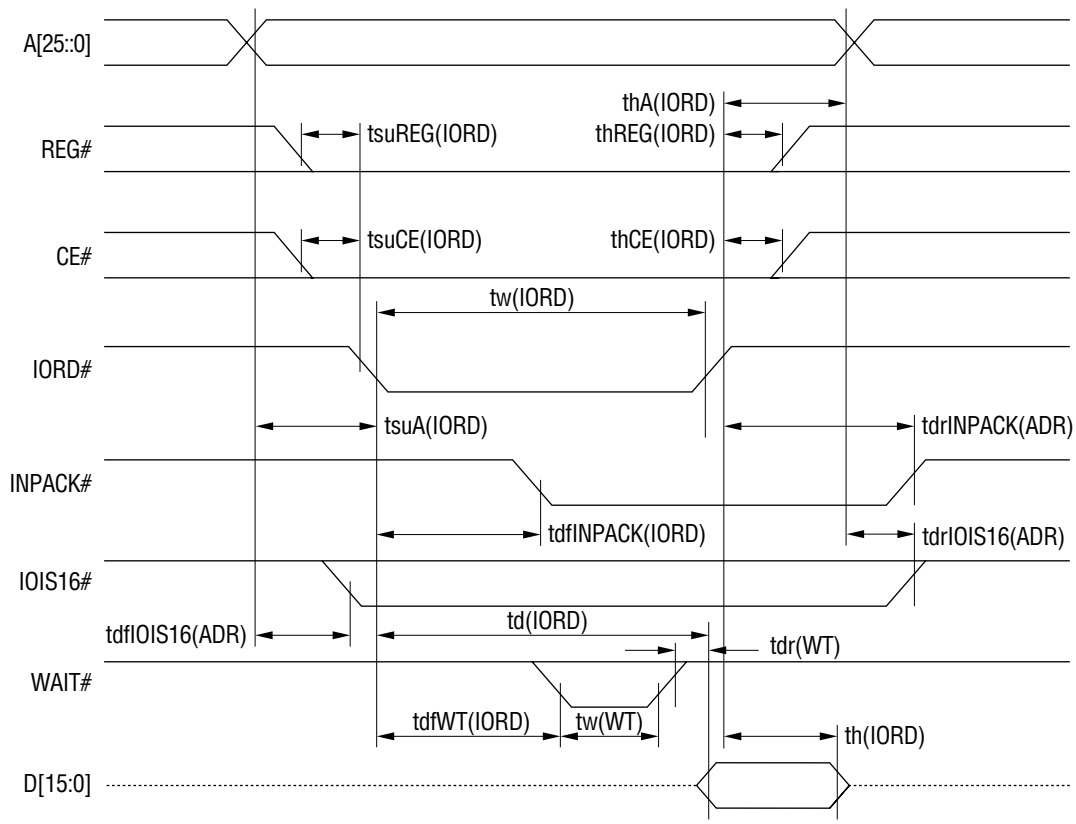


Figure 6.9 IO Read Timing

Table 6.14 IO Write Timing

Item	Symbol	Min.	Max.
Data setup time from IOWR# asserted	tsu (IOWR)	60	
Data hold time after IOWR# deasserted	th (IOWR)	30	
IOWR# pulse width	twIOWR	165	
Address setup time before IOWR# asserted	tsuA (IOWR)	70	
Address hold time after IOWR# deasserted	thA (IOWR)	20	
CE# setup time before IOWR# asserted	tsuCE (IOWR)	5	
CE# hold time after IOWR# deasserted	thCE (IOWR)	20	
REG# setup time before IOWR# asserted	tsuREG (IOWR)	5	
REG# hold time after IOWR# deasserted	thREG (IOWR)	0	
IOIS16# fall delay time from address change	tdfIOIS16 (ADR)		35
IOIS16# rise delay time from address change	tdrIOIS16 (ADR)		35
WAIT# fall delay time from IOWR# asserted	tdfWT (IOWR)		35
WAIT# pulse width	tw (WT)		12,000
	tdrIOWR (WT)	0	

Note: All units are ns.

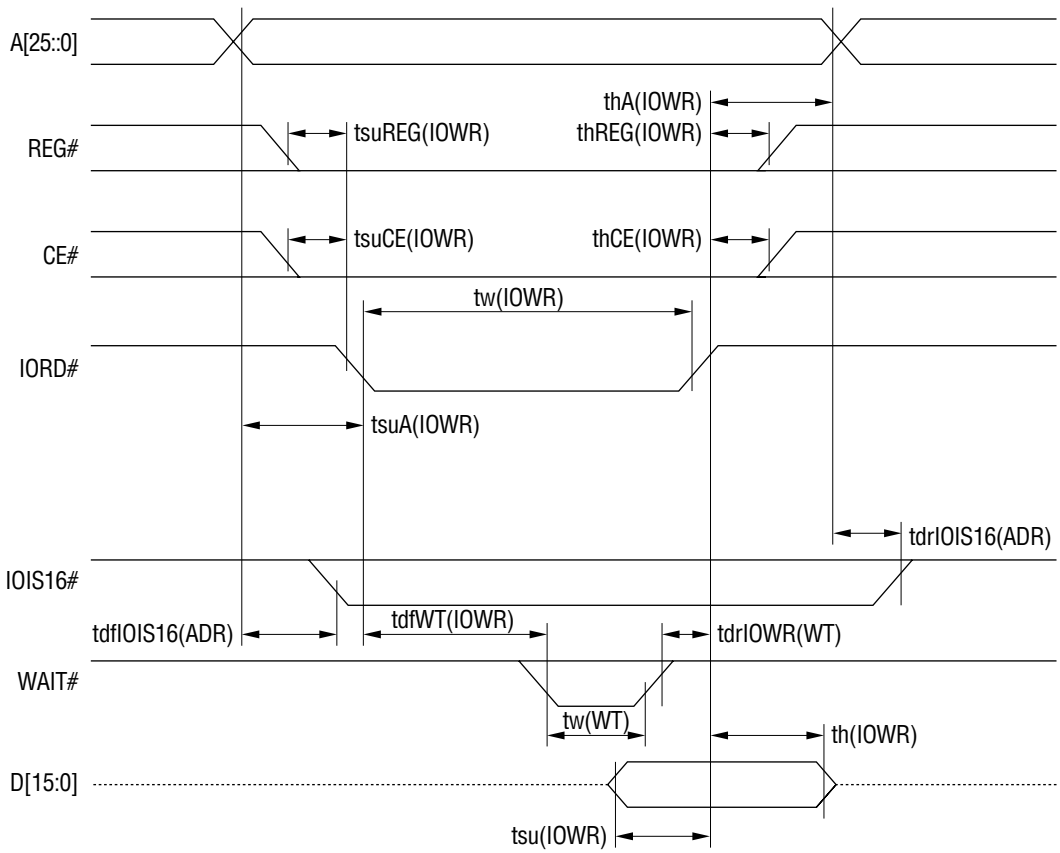


Figure 6.10 IO Write Timing

7. Package Dimentions

208-Pin Plastic LQFP