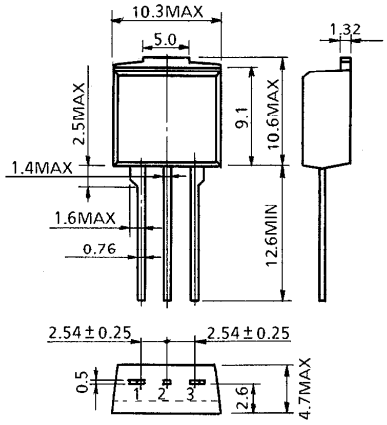
TOSHIBA THYRISTOR SILICON PLANAR TYPE

SF3G48, SF3J48, USF3G48, USF3J48

MEDIUM POWER CONTROL APPLICATIONS.

- Repetitive Peak Off-State Voltage : V_{DRM}
  Repetitive Peak Reverse Voltage : V_{RRM}
  } = 400, 600V
- Average On-State Current : $I_{T(AV)}$ = 3A
- Gate Trigger Current : I_{GT} = 10mA MAX.

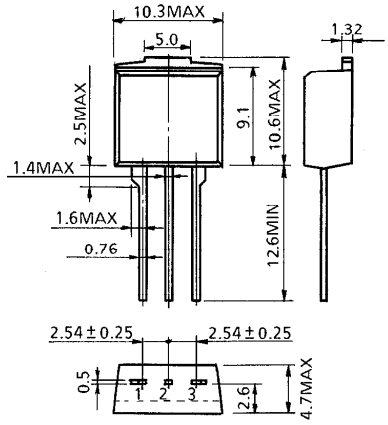
SF3G48·SF3J48



1. CATHODE
2. ANODE
3. GATE

JEDEC	—
EIAJ	—
TOSHIBA	13-10J1B

USF3G48·USF3J48

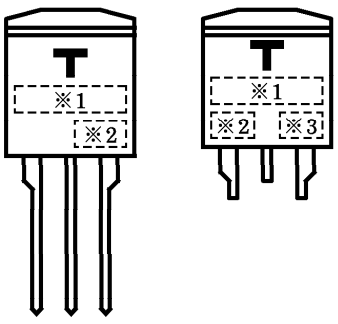


1. CATHODE
2. ANODE (BACK SIDE)
3. GATE

JEDEC	—
EIAJ	—
TOSHIBA	13-10J2B

Weight : 1.7 g

MARK



※ 1	MARK	F3G48	TYPE NAME	SF3G48, USF3G48
		F3J48		SF3J48, USF3J48
※ 2	Lot Number □ □ ←Month (Starting from Alphabet A) ↑ Year (Last Number of the Christian Era)			

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MAXIMUM RATINGS

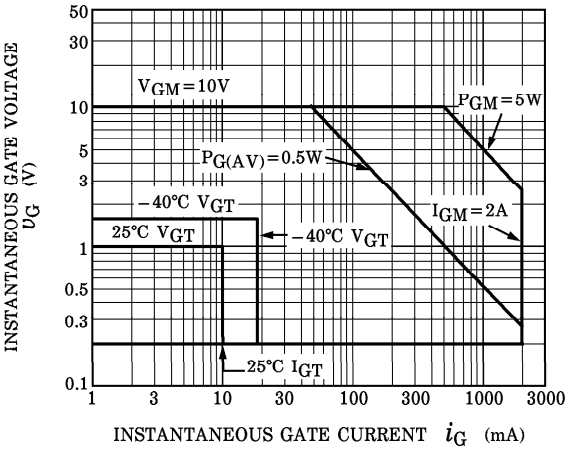
CHARACTERISTICS		SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage and Repetitive Peak Reverse Voltage	SF3G48 USF3G48	V_{DRM} V_{RRM}	400	V
	SF3J48 USF3J48		600	
Non-Repetitive Peak Reverse Voltage (Non-Repetitive < 5ms, T_j = 0~125°C)	SF3G48 USF3G48	V_{RSM}	500	V
	SF3J48 USF3J48		720	
Average On-State Current		$I_{T(AV)}$	3	A
R. M. S On-State Current		$I_{T(RMS)}$	4.7	A
Peak One Cycle Surge On-State Current (Non-Repetitive)		I_{TSM}	50 (50Hz)	A
			55 (60Hz)	
I^2t Limit Value (t = 1~10ms)		I^2t	18	A^2s
Critical Rate of Rise of On-State Current (Note 1)		di / dt	100	A / μs
Peak Gate Power Dissipation		P_{GM}	5	W
Average Gate Power Dissipation		$P_{G(AV)}$	0.5	W
Peak Forward Gate Voltage		V_{FGM}	10	V
Peak Reverse Gate Voltage		V_{RGM}	−5	V
Peak Forward Gate Current		I_{GM}	2	A
Junction Temperature		T_j	−40~125	°C
Strage Temperature Range		T_{stg}	−40~125	°C

Note 1: $V_{DRM} = 0.5 \times$ Rated
$I_{TM} \leqq 12A$
$t_{gw} \geqq 10\mu s$
$t_{gr} \leqq 250ns$
$i_{gp} = I_{GT} \times 2.0$

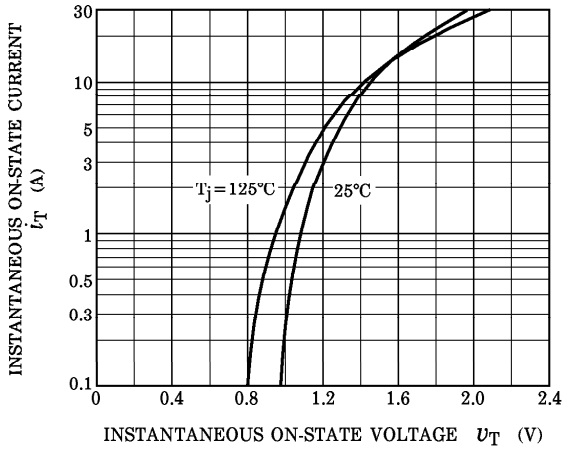
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Repetitive Peak Off-State Current and Repetitive Peak Reverse Current	I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM}$ = Rated	—	—	10	μA
Peak On-State Voltage	V_{TM}	I_{TM} = 12A	—		1.5	V
Gate Trigger Voltage	V_{GT}	V_D = 6V, R_L = 10Ω	—	—	1.0	V
Gate Trigger Current	I_{GT}		—	—	10	mA
Gate Non-Trigger Voltage	V_{GD}	V_D = Rated × 2 / 3, Tc = 125°C	0.2	—	—	V
Critical Rate of Rise of Off-State Voltage	dv /dt	V_{DRM} = Rated, Tc = 125°C Exponential Rise	—	50	—	V / μs
Holding Current	I_H	V_D = 6V, I_{TM} = 1A	—	—	40	mA
Latching Current	I_L	V_D = 6V, f = 50Hz t_{gw} = 50μs, i_G = 30mA	—	—	50	mA
Thermal Resistance	$R_{th(j-c)}$	Junction to Case, DC	—	—	3.6	°C / W

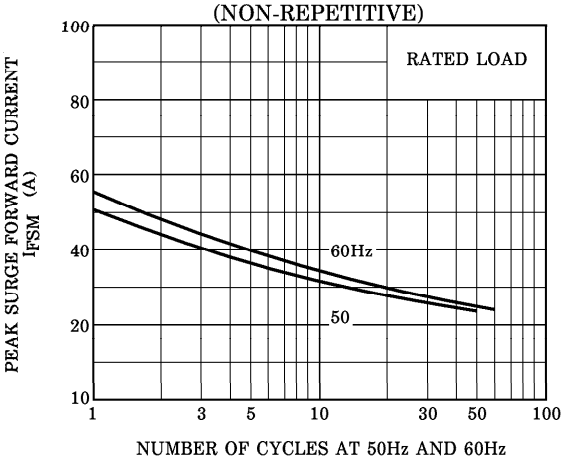
GATE TRIGGER CHARACTERISTIC



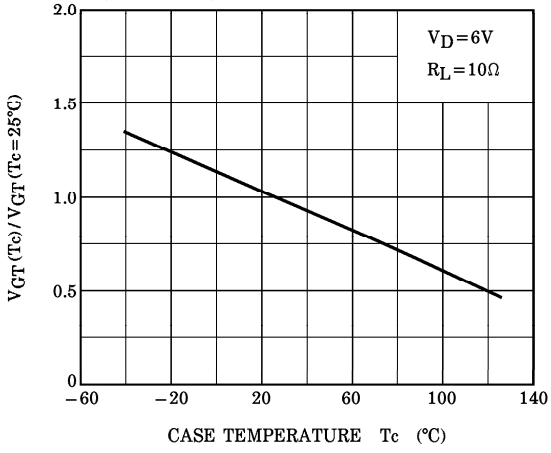
$i_T - v_T$



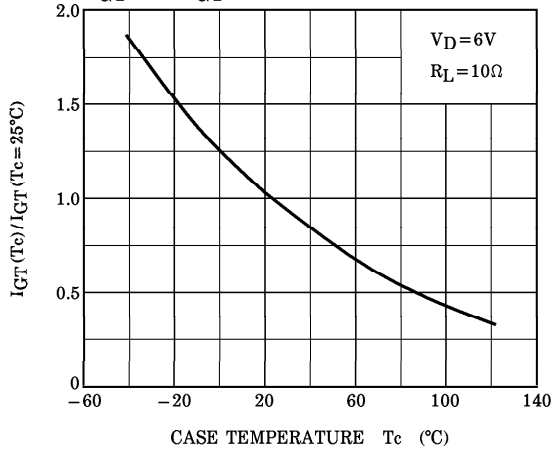
SURGE ON-STATE CURRENT
(NON-REPETITIVE)



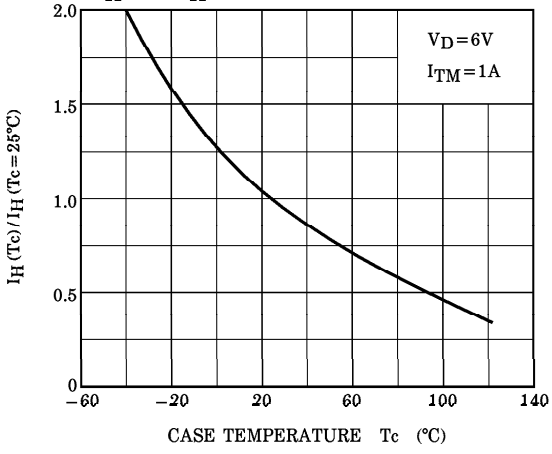
V_{GT} (Tc) / V_{GT} (Tc = 25°C) − Tc (TYPICAL)



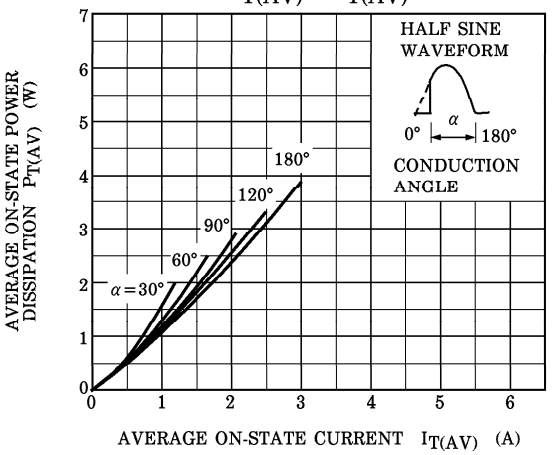
I_{GT} (Tc) / I_{GT} (Tc = 25°C) − Tc (TYPICAL)



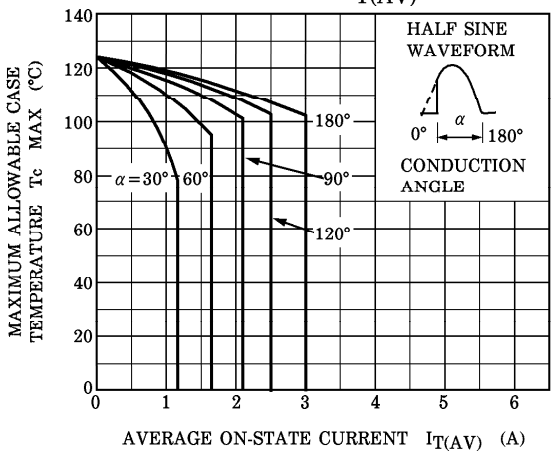
I_H (Tc) / I_H (Tc = 25°C) − Tc (TYPICAL)



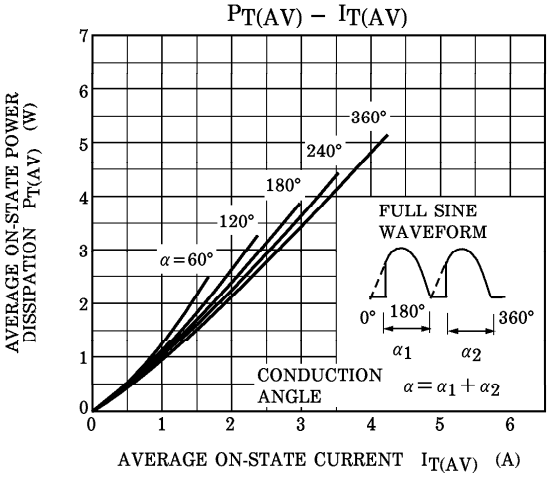
$P_{T(AV)} - I_{T(AV)}$



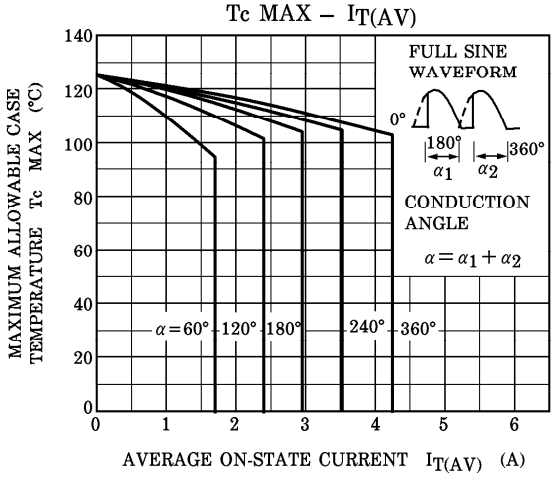
T_C MAX – $I_{T(AV)}$



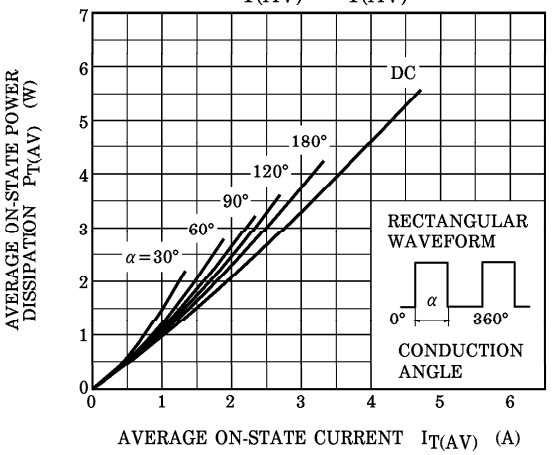
$P_{T(AV)} - I_{T(AV)}$



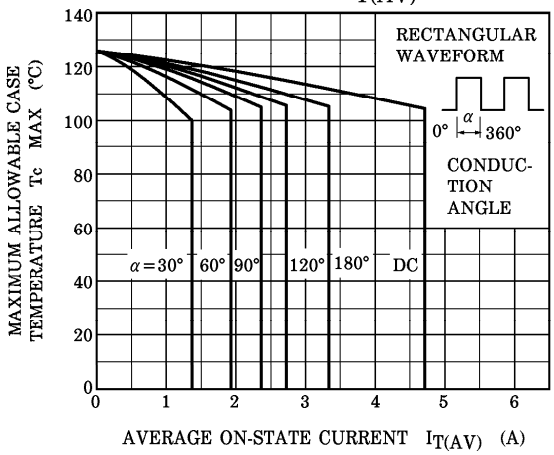
T_C MAX – $I_{T(AV)}$



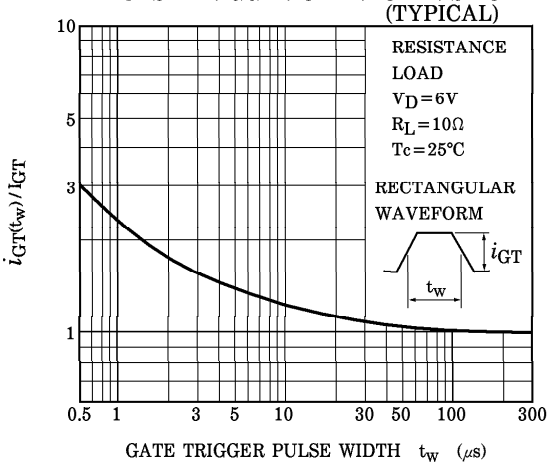
$P_{T(AV)} - I_{T(AV)}$



T_C MAX – $I_{T(AV)}$



PULSE TRIGGER CHARACTERISTIC
(TYPICAL)



TRANSIENT THERMAL IMPEDANCE
(JUNCTION TO CASE)