Digitally programmable 65 and 81 multiplex rate LCD Controller and Driver

Features

- Slim IC for COG, COF and COB technologies
- I^2C & Serial bus interface
- Internal display data RAM
- 2 digitally programmable multiplex rates :
  - 81 rows x 102 columns
  - 65 rows x 118 columns
- LCD supply voltage internally generated and digitally programmable from 4.5V to 11V
- Low operating current consumption: 140µA (typ)
- No external components needed except one V_{LCD} and one VDD capacitor
- On chip
  - 4 intermediate bias voltages generation
  - Oscillator for LCD refresh (no external components required)
- High noise immunity on inputs
- Row and column drivers mirroring for COG or COF connections flexibility
- Partial display mode with 17 active rows for current consumption reduction
- Sleep mode for a nearly zero current consumption
- Wide V_{DD} supply voltage from 2.4V to 3.3V
- Wide temperature range: -40°C to +85°C

Description

The EM6126 is a bit map controller and driver for full dot matrix monochrome STN LCD displays. The driving capability is 81 rows x 102 columns (10 rows of characters + one row of icons) or 65 rows x 118 columns (8 rows of characters + one row of icons). There is a one to one relation between LCD pixels and bits of the Display Data RAM.
The EM6126 is an extremely low power consumption LCD controller and driver product. The typical current consumption is about 140µA with no external component except the capacitors connected to V_{LCD} and VDD. One important feature on EM6126 is the partial display mode, which enables important current consumption reduction. With this function selected, only 17 rows remain active, needed V_{LCD} decreases and the commutation frequencies of row and column drivers are also decreased. These three effects of partial display mode reduce drastically current consumption.

Typical Applications

- Mobile phones
- Smart cards
- Portable, battery operated products
- Balances and scales, utility meters

Typical Operating Configuration

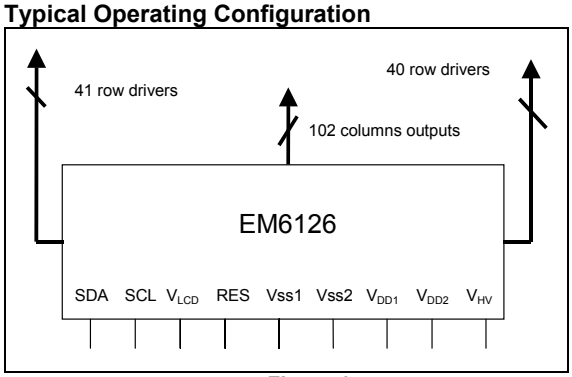


Figure 1

Pin Configuration

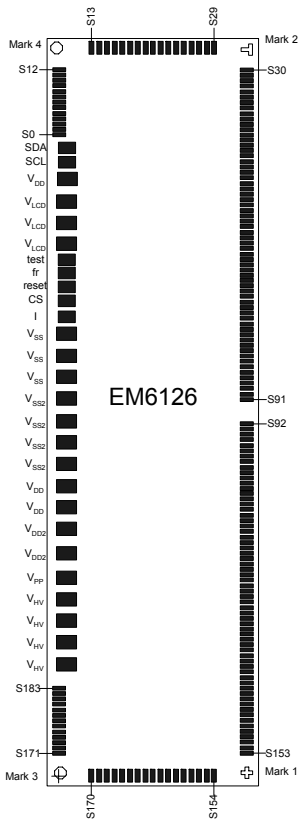


Figure 2

1 Absolute Maximum Ratings

Parameter	Symbol	Conditions
Supply voltage range	$V_{DD1,2}$	-0.3V to +3.6V
Supply voltage range	V_{HV}	-0.3V to +3.6V
Supply voltage range	V_{LCD}	V_{HV}-0.3V to +12V
All input voltages	V_{LOGIC}	-0.3V to $V_{DD1,2}$+0.3V
Voltages at S_0 to S_{184}	$V_{DISPLAY}$	-0.3V to V_{LCD} + 0.3V
Storage temperature range	T_{STO}	-65°C to +150 °C
Maximum soldering conditions	T_{SMAX}	250°C × 10 s

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified electrical characteristics may affect device reliability or cause malfunction.

2 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

3 Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	
Operating temperature	T_A	-40		+85	°C
Logic supply voltage	$V_{DD1,2}$	2.4	2.5	3.3	V
High voltage generator supply voltage	V_{HV}	2.4	2.5	3.3	V
LCD supply voltage	V_{LCD}	4.5	8	11	V

4 Electrical Characteristics

$V_{SS1,2}$ = 0V, V_{DD1} = V_{DD2} = 2.4V, V_{HV} = 2.4V, unless otherwise specified. T_A = -40°C to +85 °C unless otherwise specified.
Minimum required capacitor: 1µF on V_{LCD}, 100nF on $V_{DD1,2}$ and V_{HV}.

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
Supply Current						
Sleep mode	I_{DD}	T_A = 25°C, Sleep = 1		100		nA
Sleep mode	I_{HV}	T_A = 25°C, Sleep = 1		0.8		µA
Normal LCD refresh mode	I_{DD}	T_A = 25°C, (note 1)		17	22	µA
Normal LCD refresh mode	I_{HV}	T_A = 25°C, (note 2)		124	180	µA
Partial LCD refresh mode	I_{HV}	T_A = 25°C, (note 3)		50	90	µA
Control Input Signals						
Input leakage	I_{IN}	V_i = V_{ss1} or V_{DD1}	-1		1	µA
Low level input voltage	V_{IL}				0.3xV_{DD1}	V
High level input voltage	V_{IH}		0.7xV_{DD1}			V
Low Level Output Current SDA	I_{OL_SDA}	V_{OL_SDA} = 0.4V		1.6		mA
LCD Outputs						
Internally generated LCD supply voltage	T_A = 25°C, V_{LCD} 00101011b (Hex: 2B)			4.53		V
	T_A = 25°C, V_{LCD} 10001110b (Hex: 8E)			8.02		V
V_{LCD} step between 2 consecutive programmed V_{LCD} Level	V_{LCD} step			35.2		mV
V bias tolerance	V bias tol.	(note 4)	-80		80	mV
Typical load	C_{LOAD}			1.2		pF/pixel

Note 1: Measured on V_{DD1} + V_{DD2}, all outputs open, SDA and SCL at V_{SS}, RES at V_{DD1}, multiplex rate 81, x5 voltage multiplier, V_{LCD} = 10001110b, DDRAM loaded with checker pattern

Note 2: Measured on V_{HV}, same conditions as (note 1).

Note 3: Measured on V_{HV}, all outputs open, SDA and SCL at V_{SS}, RES at V_{DD1}, partial display mode, ×2 voltage multiplier, V_{LCD} = 00101011b, DDRAM loaded with checker pattern.

Note 4: V_1, V_2, V_3 and V_4 bias levels measured with V_{LCD} = 7V, on 1 LCD row driver output and 1 LCD column driver output, multiplex rate 81, T_A = 25 °C, load = ±10µA, I_{load} = 10µA to V_{SS} or V_{LCD}
V bias_tol is: ½(Vbias_$_{+10µA}$ + Vbias_$_{-10µA}$) – Vbias_$_{theor}$

(Vbias_$_{theor}$: see § 8.8; e.g. for V1: 0.9xV_{LCD} at Mux=81)

5 Timing Characteristics

$V_{SS1,2}$ = 0V, V_{DD1}= V_{DD2} = 2.4V, V_{HV} = 2.4V, T_A = -40°C to +85 °C unless otherwise specified.

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
Internal frame frequency for LCD refresh	f_{FR}	(note 1)		75 x mux		Hz
Minimum reset pulse width	t_{RW}		1			us
I2C timing characteristics						
SCL frequency	f_{I2C}				1600	kHz
SCL low period	t_{LOW}		350			ns
SCL high period	t_{HIGH}		100			ns
SDA setup time	t_{SUDAT}		10			ns
SDA hold time	t_{HDDAT}		20			ns
SCL and SDA rise time	t_R				200	ns
SCL and SDA fall time	t_F				200	ns
Setup time for a repeated start condition	t_{SUSTA}		20			ns
Hold time for a start condition	t_{HDSTA}		20			ns
Setup time for a stop condition	t_{SUSTO}		20			ns
Spike width on SCL and SDA	t_{SW}				10	ns
Time before a new transmission can start	t_{BUF}		100			ns
Capacitive bus line load	C_b				400	pF
Serial bus timing characteristics						
SCL frequency	f_{SER}				4	MHz
SCL low period	t_{CL}		80			ns
SCL high period	t_{CH}		130			ns
SDA setup time	t_{DS}		20			ns
SDA hold time	t_{DH}		70			ns
SCL rise time	t_{CR}				200	ns
SCL fall time	t_{CF}				200	ns
CS setup time	t_{SUCS}		10			ns
CS hold time	t_{HDCS}		130			ns
Time before a new transmission can start, CS minimum high time.	t_{BUFCS}		70			ns

Note 1: Measured on pad FR.

5.1 Timing Waveforms

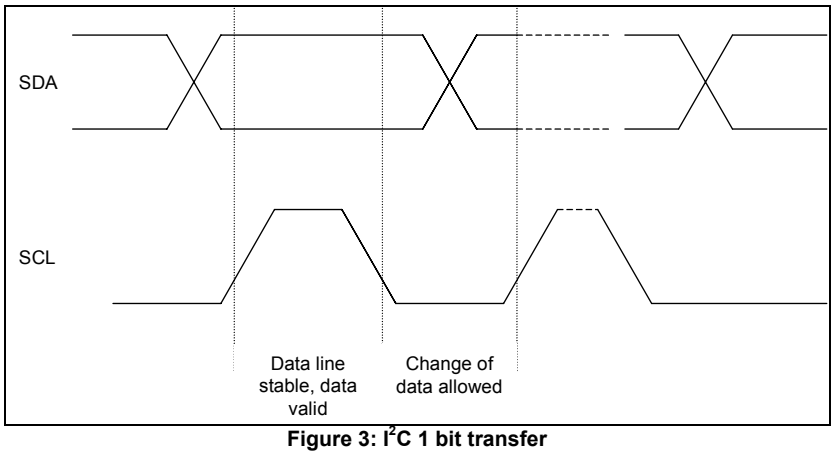


Figure 3: I²C 1 bit transfer

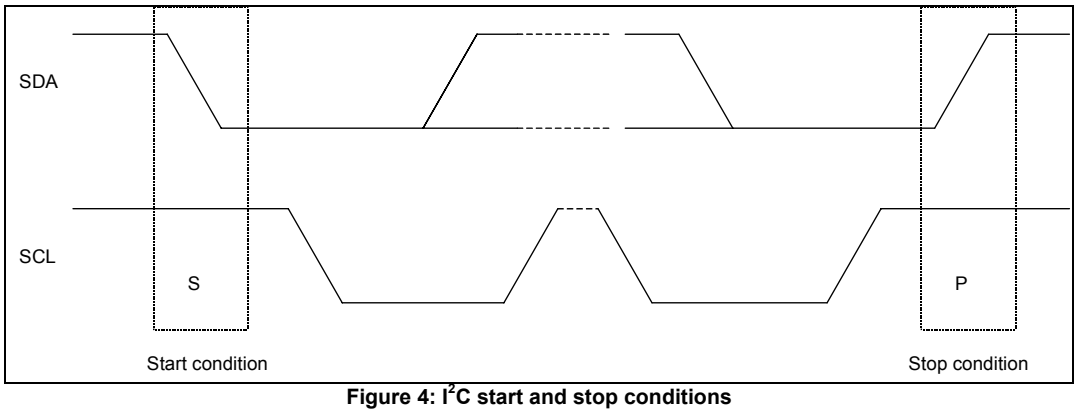


Figure 4: I²C start and stop conditions

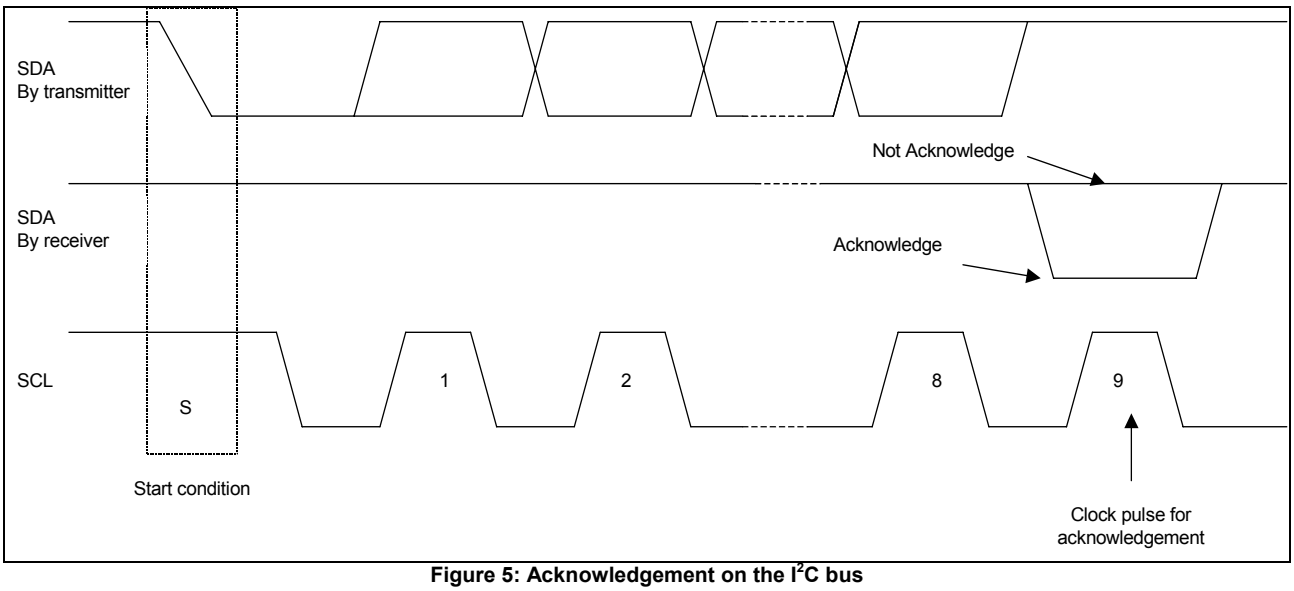


Figure 5: Acknowledgement on the I²C bus

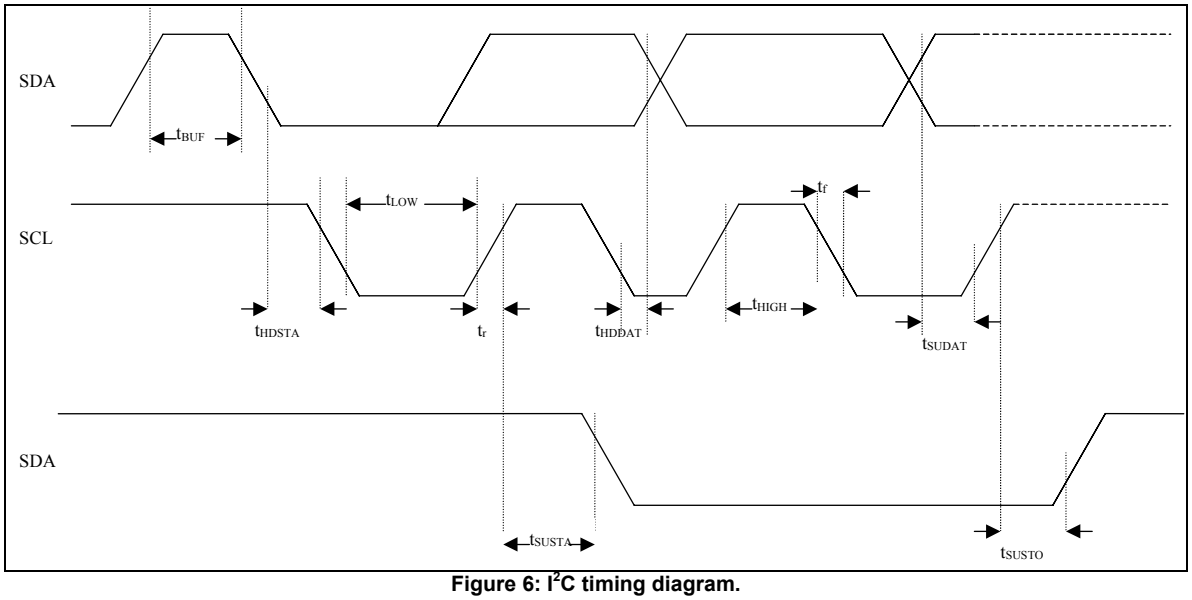


Figure 6: I²C timing diagram.

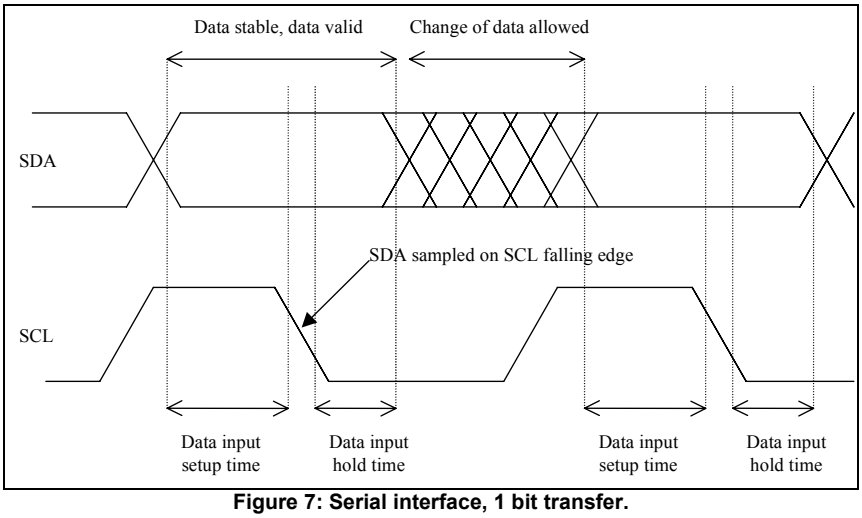


Figure 7: Serial interface, 1 bit transfer.

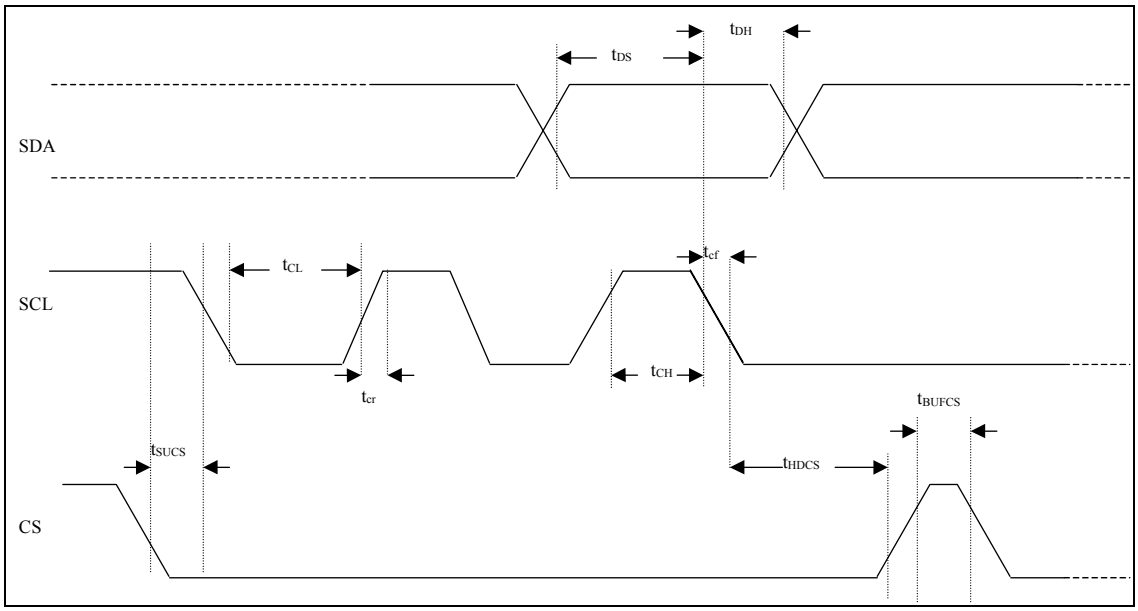


Figure 8: Serial interface timing diagram.

6 Block diagram

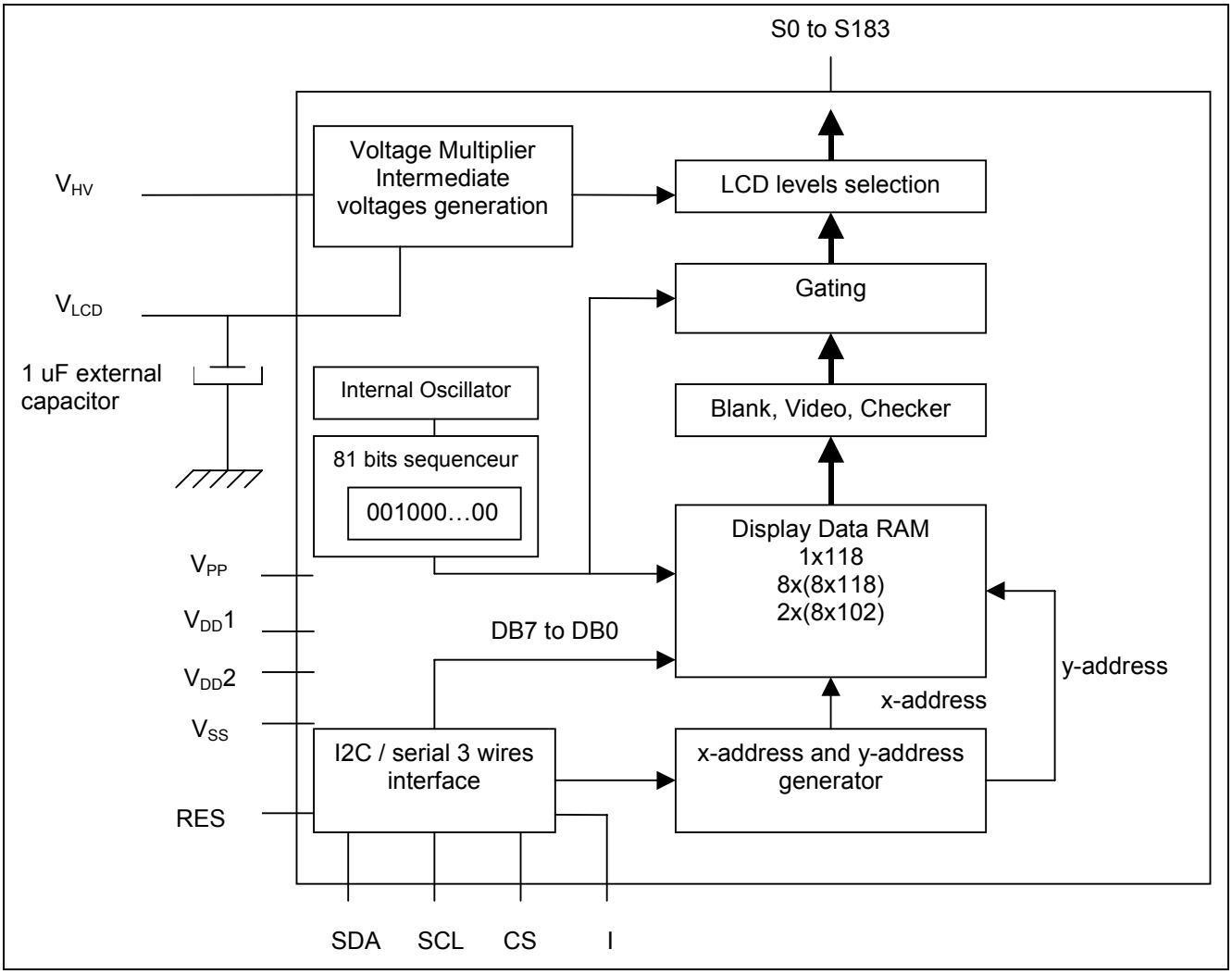


Figure 9: Block diagram.

7 Pin description

Symbol	Pad Type	Description
S_0 to S_{183}	Output	LCD driver outputs
S_0 to S_{32} and S_{151} to S_{183}	Output	LCD row driver outputs $S_0 = S_{183}$
S_{33} to S_{40} and S_{143} to S_{150}	Output	LCD row driver outputs when multiplex rate 81 is selected LCD column driver outputs when multiplex rate 65 is selected
S_{41} to S_{142}	Output	LCD column driver outputs
V_{HV}	Positive power supply	Supply voltage for internal voltage multiplier
$V_{DD1,2}$	Positive power supply	Supply voltage for logical and analog parts
V_{PP}	Positive power supply	Supply voltage for OTP
$V_{SS1,2}$	Ground power supply	Ground power supply
I	Input	Interface protocol selection input
RES	Input	External reset input, active low
CS	Input	Chip select input
FR	Input/output	Frame frequency input/output
TEST	Input/output	Test
SDA	Input/output	Serial data input
SCL	Input	Serial clock
V_{LCD}	Positive power supply	LCD supply voltage

Table 1: Pin description

S0 to S183: Connected to LCD electrodes, it should be left open if not used. S0 and S183 are internally connected together.

V_{HV}: Supply voltage for internal voltage multiplier, it could be a different voltage value than for $V_{DD1,2}$.

$V_{DD1,2}$ V_{PP}: Logic and analog power supplies. V_{DD1}, V_{DD2} and V_{PP} are not connected inside EM6126but have to be connected outside to the same potential. For chip on glass application, it is advised to keep V_{DD1} and V_{DD2} separated until their connection to 1 µF capacitor.

$V_{SS1,2}$: Ground supply for logic and high voltage generator. V_{SS1} is connected to substrate. Same precautions than for $V_{DD1,2}$ should be taken to connect these pads.

I: Selects the chosen interface protocol. For chip on glass applications, it can be directly connected to V_{SS1} or V_{DD1} on glass.

RES: External reset, a reset cycle must be applied at power on (reset at low level when power on).

Note that the outputs $S_0 = S_{183}$ are at VLCD level when reset is active. If this static state is applied during long time the LCD could be damaged.

CS: Active low chip select, when serial interface is used it enables data transfer. If I^2C is used, it must be connected at V_{SS1} or V_{DD1} pads.

FR: Outputs LCD refresh frame frequency, used for test. It must be left open.

TEST: Test pad, it must be left open.

SDA: Serial data input used for I^2C interface as for 3 wires serial interface.

SCL: Serial clock input used to latch SDA for I^2C interface as for 3 wires serial interface.

V_{LCD}: LCD voltage supply (generation of LCD waveforms applied to S0 to S183). It is normally internally generated from V_{HV} supply voltage. 1 µF capacitor is required between V_{LCD} and V_{SS}. A forward biased diode is connected between V_{HV} and V_{LCD}, therefore V_{LCD} must be programmed higher than V_{HV}.

External power supply is also possible; in this configuration, V_{LCD} must be programmed at its lowest value and V_{HV} connected to V_{SS2}.

8 Functional description

8.1 Selection of interface type

There are two different serial interfaces available on EM6126. Selection depends on logical value applied on input I.

- If I = 0, serial interface is selected: 3 wires with Chip Select CS, Serial Clock SCL and Serial Data SDA.
- If I = 1, I^2C protocol is selected: 2 wires with Serial Clock SCL and Serial Data SDA. CS must be connected to V_{SS} or V_{DD1}.

I	Interface
0	3 wires serial interface
1	I^2C

Table 2: Interface selection

8.2 Serial interface

The serial interface consists of 3 wires: Chip Select CS, Serial Clock SCL and Serial Data SDA. The information is exchanged byte-wide and is shifted serially in the LCD driver at SCL falling edge.

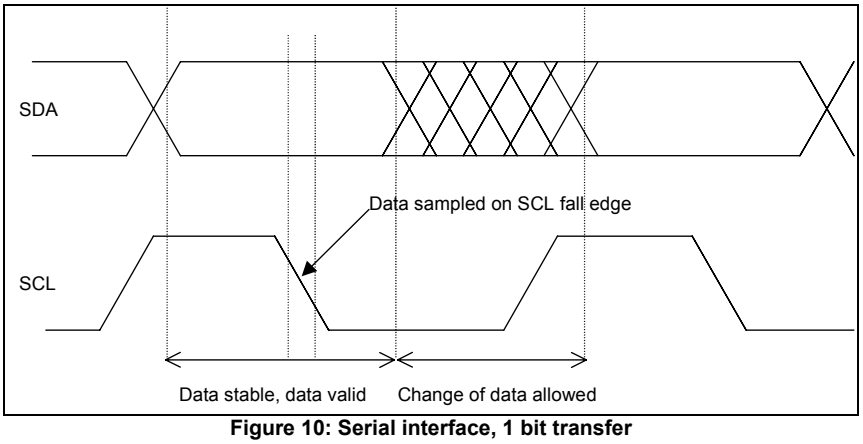


Figure 10: Serial interface, 1 bit transfer

Transfer data direction is from microcontroller to EM6126. When CS is activated at low level, the communication is enabled and CS must stay low for the rest of the transmission. Data transfer begins with one control byte. This control byte is transfered MSB first; it consists in:

MSB							LSB
C0	DC	Test[2]	Test[1]	Test[0]	Ini[2]	Ini[1]	Ini[0]

C_0 is the continuation bit:

- If C_0 = 1, the control byte is followed by 1 data byte only, the next byte is a new control byte.
- If C_0 = 0, all the following bytes are data bytes until data transfer is stopped.

DC selects data bytes or command bytes to be sent after the control byte:

- If DC = 1, the following data byte(s) is (are) written into the Display Data RAM. First data byte is stored at the address specified by the x-address and y-address pointers. Data pointers are automatically updated for each byte written in the DDRAM (see DDRAM description).
- IF DC = 0, the following data byte is a command byte. It enables initialization of functions (multiplex rate, number of voltage multiplier stages, V_{LCD} programming, partial display settings…).

Bytes ini2, ini1 and ini0 select the initialization register which will be set by the following command byte (see Table 4: EM6126 instructions).

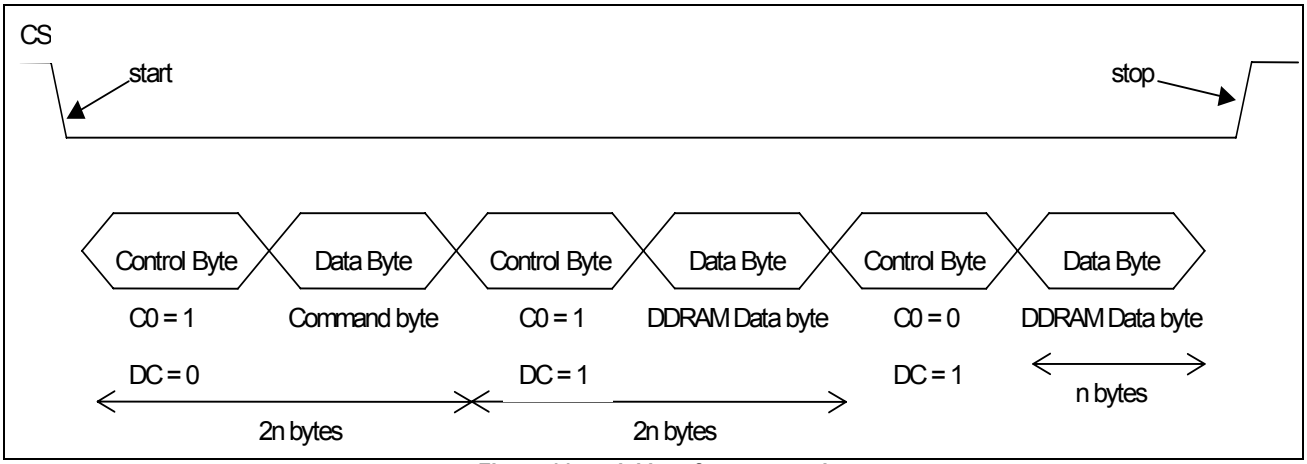
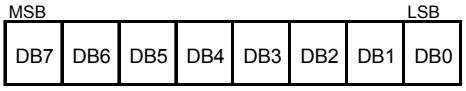


Figure 11: serial interface protocol

Data byte is transfered with MSB bit first, LSB bit last:



If CS goes high during a byte transfer, this byte is invalid, but all previously transmitted data are valid. While CS is high, the serial interface is kept in reset and data transfer is disabled. To prevent transmission errors, CS should be at high level when transfer is stopped.

8.3 I²C interface

The EM6126 can be interfaced with a slave I²C protocol (see description I2C protocol). The I²C bus consists in 2 wires: SCL (Serial Clock Line) and SDA (Serial Data Line). Both lines must be connected to $V_{DD1,2}$ via pull up resistors. EM6126 pad SCL is input, pad SDA is bi-directional with open drain NMOS driver. EM6126 supports initialization and RAM write and status read access.

8.3.1 Start and stop conditions

Data transfer begins by a falling edge on SDA when SCL is at high level, this is the start condition (S), initiated by the I²C bus master. It is stopped with a rising edge on SDA when SCL isat high level, this is the stop condition (P) (see Figure 4: I2C start and stop conditions).

8.3.2 Bit transfer

One data bit is transfered by each SCL pulse. The data on the SDA line must remain stable during the high period of SCL pulses, as any changes at this time would be interpreted as start or stop conditions. Data is always transfered with MSB first.

8.3.3 Acknowledge

After a start condition, data bits are transfered to EM6126. Each byte is followed by an acknowledge bit: the transmitter lets the SDA line at high level (by pull up resistor) and generates an SCL pulse; if transfer concerns the EM6126 slave receiver and has performed correctly, EM6126 generates a low SDA level (NMOS activated). SDA remains stable during the high period of the acknowledge related SCL pulse. After acknowledge, EM6126 lets SDA line free, enabling the transmitter to continue transfer or to generate a stop condition.

8.4 I²C protocol

The EM6126 has the slave address coded on 7 bits: 0000000.

After a start condition, the slave address + RW bit must be sent first. If the slave address does not match with the EM6126 one, there is no acknowledge from LCD driver and the following data transfer will not affect the EM6126.

If the slave address corresponds to EM6126 slave address, it will acknowledge (pull SDA down to logical low level) and data transfer is enabled.

The 8th bit RW sets the chip in write mode or read status mode, it is read for data transfer.

8.4.1 Write mode

If RW = 0, data are written into EM6126 by the microcontroller.

Data transfer bytes can be either control bytes or data bytes. Data transfer always begins with a control byte (described in fig.12). It sets bits C0, DC, ini2, ini1 and ini0

C0 is the continuation bit:

- If C_0 = 1, the control byte is followed by 1 data byte only, the next byte is a new control byte.
- If C_0 = 0, all the following bytes are data bytes until data transfer is stopped.

DC selects data bytes or command bytes to be sent after the control byte:

- If DC = 1, the following data byte(s) is (are) written into the Display Data RAM. First data byte is stored at the address specified by the x-address and y-address pointers. Data pointers are automatically updated for each byte written in the DDRAM (see DDRAM description).
- IF DC = 0, the following data byte is a command byte. It enables initialization of functions (multiplex rate, number of voltage multiplier stages, V_{LCD} programming, partial display settings…).

Bytes ini2, ini1 and ini0 select the initialization register to be set by the following command byte (see Table 4: EM6126 instructions).

8.4.2 Read Mode (RW = 1)

EM6126 will output one status byte after slave address. This status byte consists in 8 initialization bits previously set by command bytes or the reset cycle (see Table 4: EM6126 instructions).

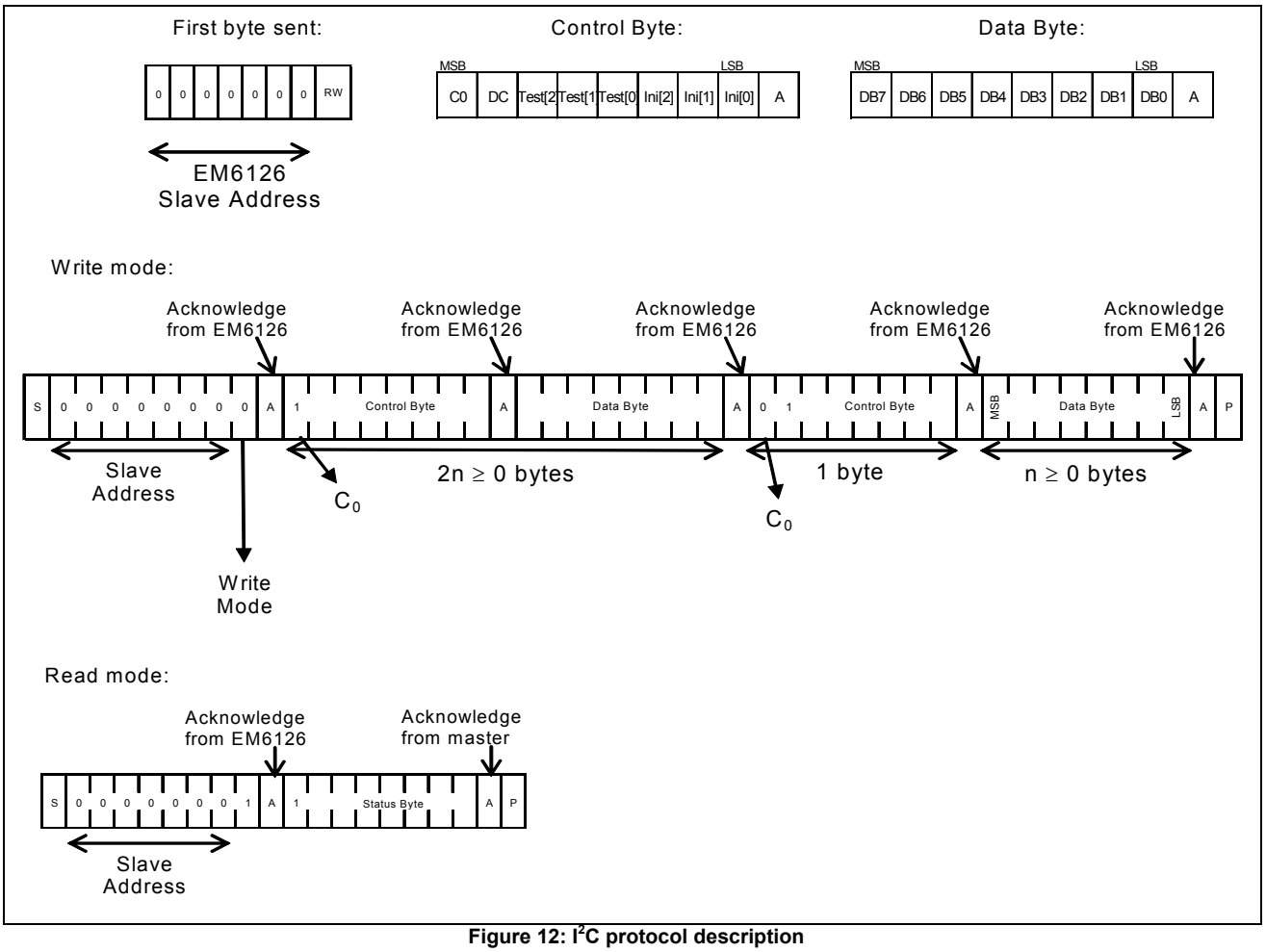


Figure 12: I²C protocol description

8.5 Display Data RAM

The EM6126 contains a RAM, which stores the display data; there is a one to one correspondence between the bit stored in the RAM and one LCD pixel.

8.5.1 DDRAM description

DDRAM consists in:

- 1 bank of 118 bits (row 0)
- 8 banks of 118 bytes (rows 1 to 64)
- 2 banks of 102 bytes (rows 65 to 80)

DDRAM is read row by row for display refresh. Each row corresponds to one row output pad, which is activated when the corresponding row in the DDRAM is read.

DDRAM is accessed via the serial interface. Bytes are stored at the column specified by x-address pointer and the bank specified by y-address pointer. These pointers are set by the corresponding instruction “Initialization 1” and “Initialization 2” and are automatically incremented or decrement after each byte written in the DDRAM (see

DDRAM addressing and Table 5: Internal functions after reset.)

For bank 0 only data byte 7 (DB7) is stored in row 0, DB6 to DB0 are not used. For bank 1 to 10 (y-address = 1 to 10), DBX is stored at row ((8 x y-address)-X).

If Mux Mode = 0, the DDRAM provides a 65 rows and 118 columns matrix.
Bank 9 and 10 are not used for display refresh, the cells can not be addressed.

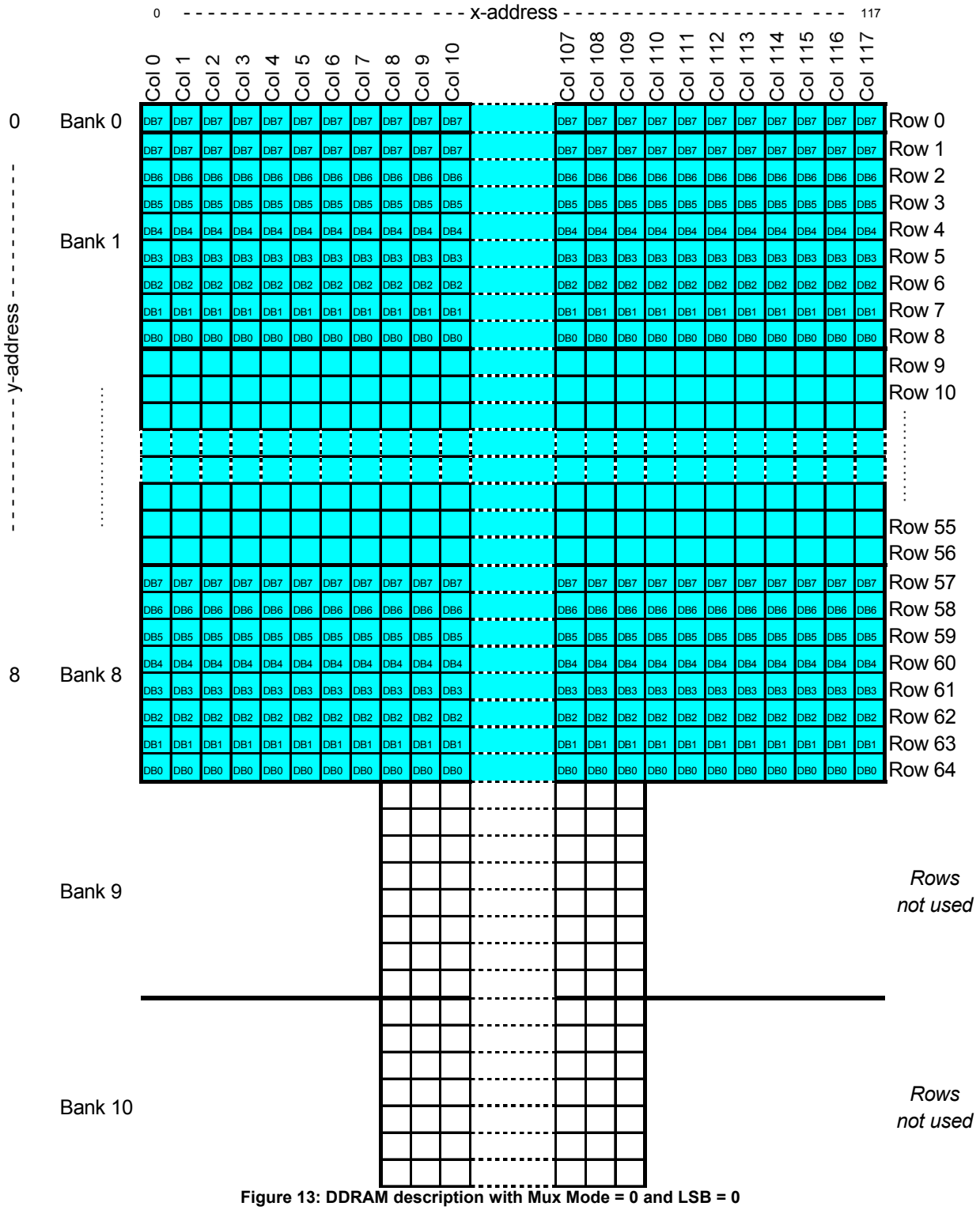


Figure 13: DDRAM description with Mux Mode = 0 and LSB = 0

If Mux Mode = 1, the DDRAM provides a 81 rows and 102 columns matrix.
8 columns on the left + 8 columns on the right are not used for display refresh, the cells can not be addressed.

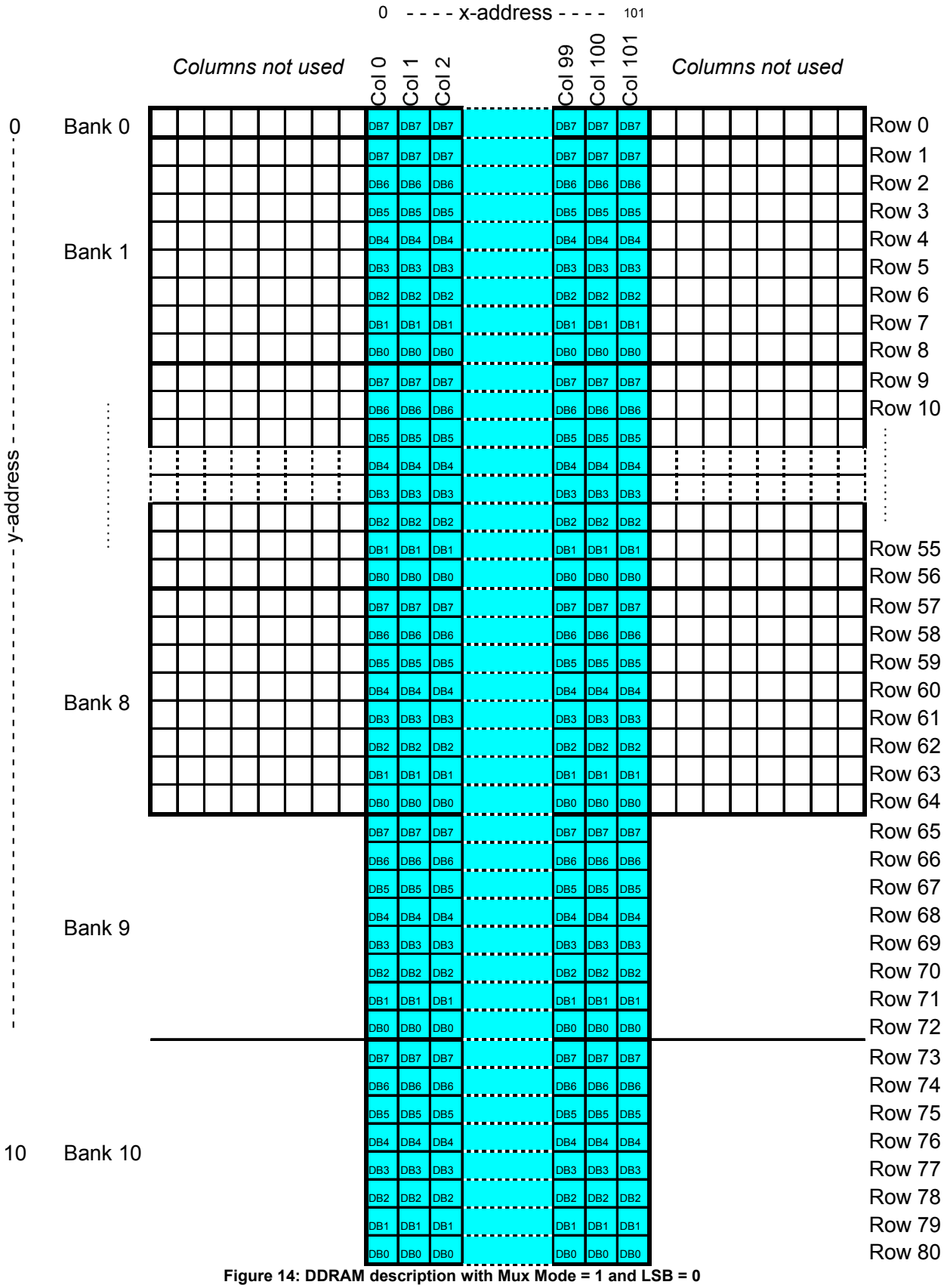


Figure 14: DDRAM description with Mux Mode = 1 and LSB = 0

If Mux Mode = 1 and LSB=1.

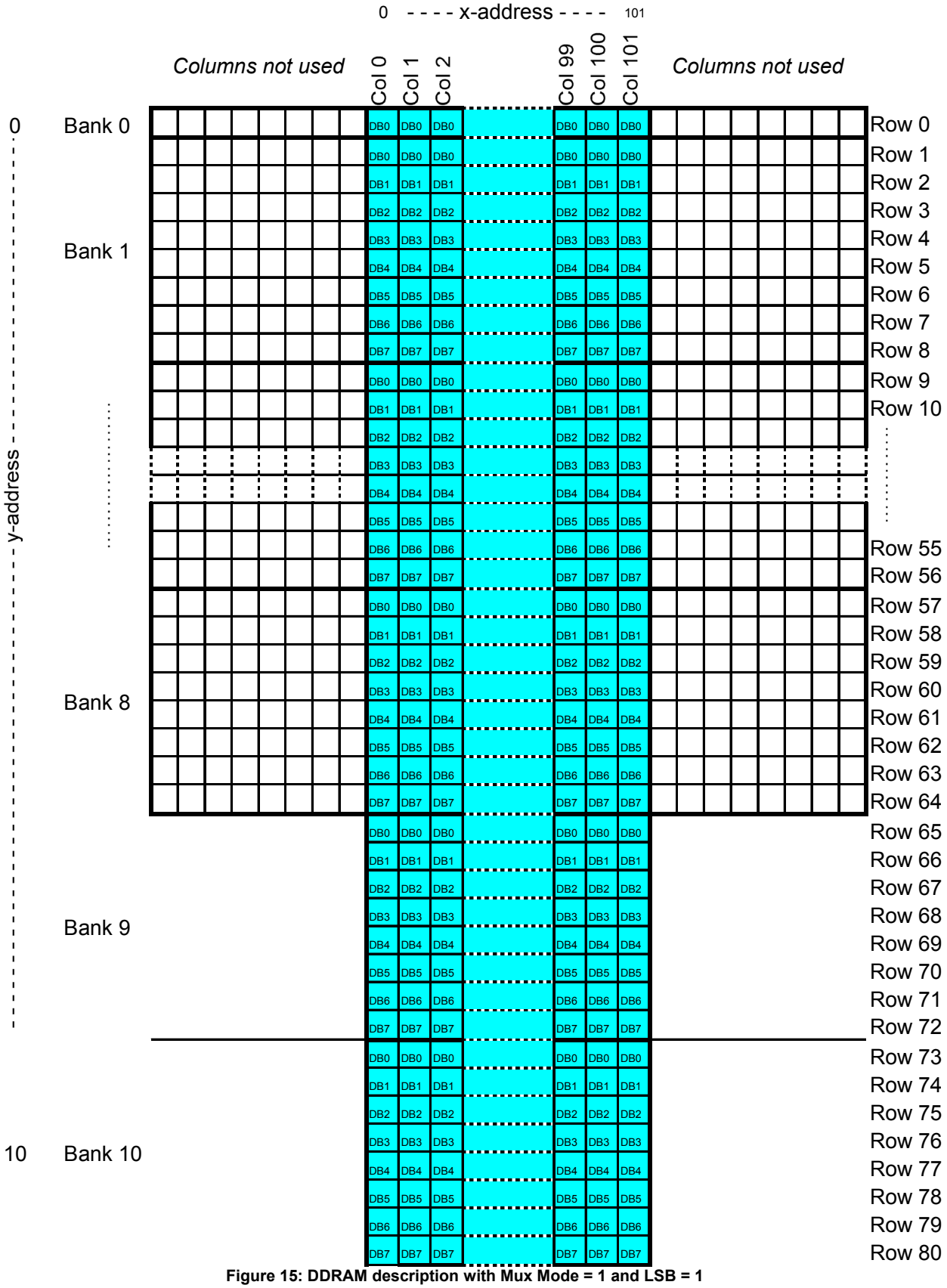


Figure 15: DDRAM description with Mux Mode = 1 and LSB = 1

8.5.2 DDRAM addressing

The x-address and the y-address pointers are used to address RAM cells. They are set by instructions “initialization 1” and “initialization 2”. As EM6126 offers 2 digitally programmable multiplex rates, number of row drivers and number of column drivers are not fixed.

As DDRAM is an image of LCD display, address ranges also depend on multiplex rate (Mux Mode):

- If Mux Mode = 0: $0 \leq$ x-address ≤ 117
  $0 \leq$ y-address ≤ 8
- If Mux Mode = 1: $0 \leq$ x-address ≤ 101
  $0 \leq$ y-address ≤ 10

Addresses outside these ranges are not allowed.

There are three functions that affects the pointers: DEC, V and MX. They are set by instructions “initialization 1” and “initialization 2” (see Table 4: EM6126 instructions).

- Instruction DEC increment or decrement x-address:
  - If DEC = 0, x-address increments after each byte written into the RAM. After the last x-address, x-address is reset to 0 and y-address increments.
  - If DEC = 1, x-address decrements after each byte written to the RAM. After x-address=0, x-address is set back to the highest x-address for the selected mux mode and y-address increments.

  DEC allows writing easily to the RAM in two ways, right and left.

- Instruction V horizontal or vertical mode addressing:
  - If V = 0 (horizontal mode addressing), x-address increments or decrements after each byte written into the RAM. After the last x-address, x-address is reset to 0 or to the highest x-address, and y-address increments.
  - If V = 1 (vertical mode addressing), y-address increments after each byte written to the RAM. After the last y-address, y-address is set back to 0 and x-address increments or decrements.

- Instruction MX mirrored the DDRAM columns:
  - If MX = 0, x-address 0000000b corresponds to DDRAM column 0.
  - If MX = 1, x-address 0000000b corresponds to DDRAM column 117 or 101.

The table below represents the next address selected after pointers are in the last allowed address:

Mux Mode	DEC	Last allowed address		Next address	
		x-address	y-address	x-address	y-address
0	0	117	8	0	0
1	0	101	10	0	0
0	1	0	8	117	0
1	1	0	10	101	0

Table 3

The following tables represent the way that the pointers x-address and y-address are working according to the setting of the instructions Mux Mode, V, MX and DEC.

Mux Mode = 0, V = 0, DEC =0, MX = 0:

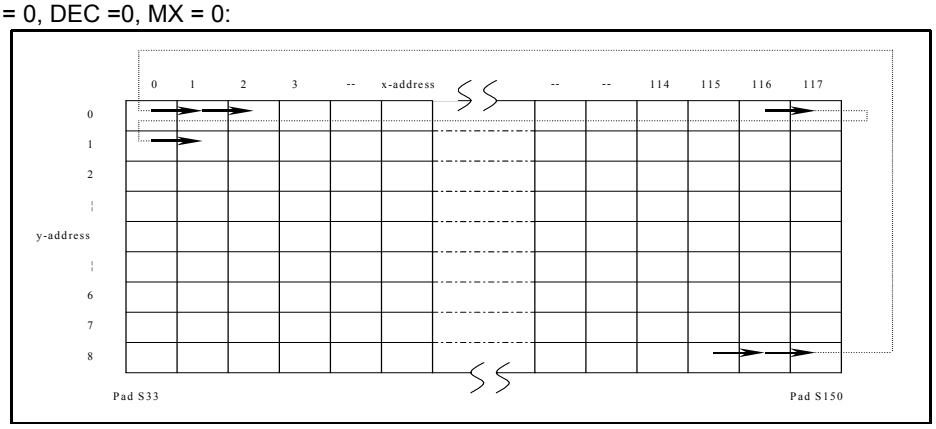


Figure 16

Mux Mode = 0, V = 0, DEC =1, MX = 0:

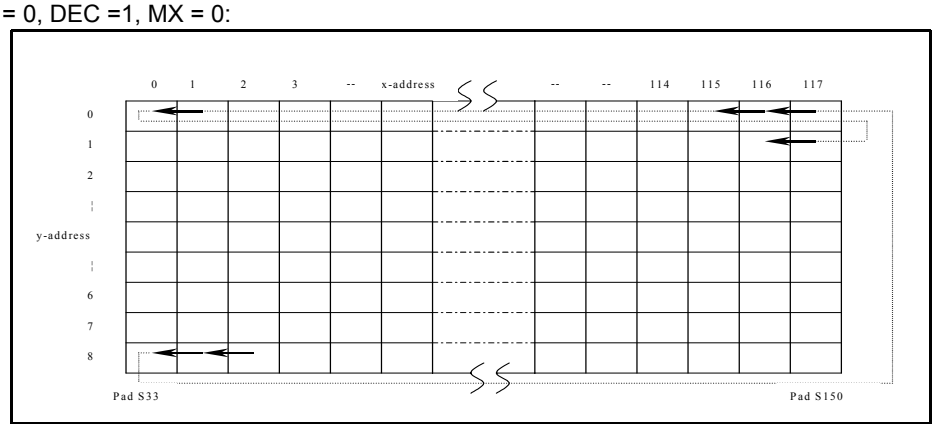


Figure 17

Mux Mode = 1, V = 0, DEC =0, MX = 0:

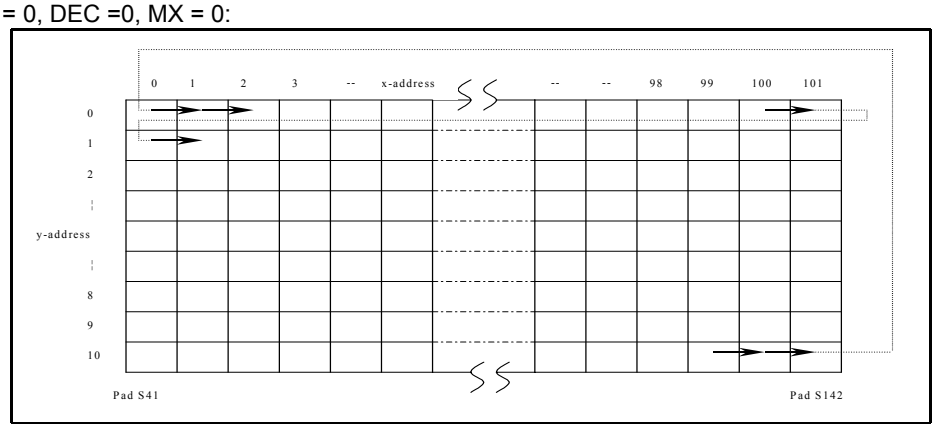


Figure 18

Mux Mode = 1, V = 0, DEC =1, MX = 0:

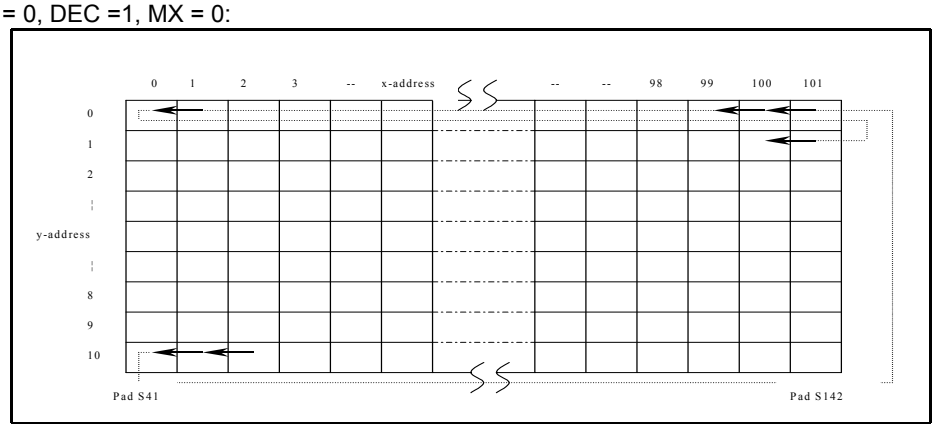


Figure 19

Mux Mode = 0, V = 1, DEC =0,MX = 0:

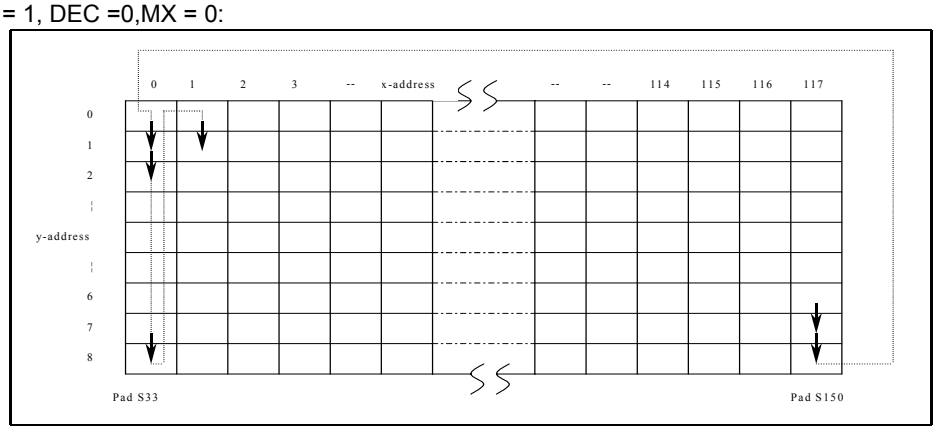


Figure 20

Mux Mode = 0, V = 1, DEC =1,MX = 0:

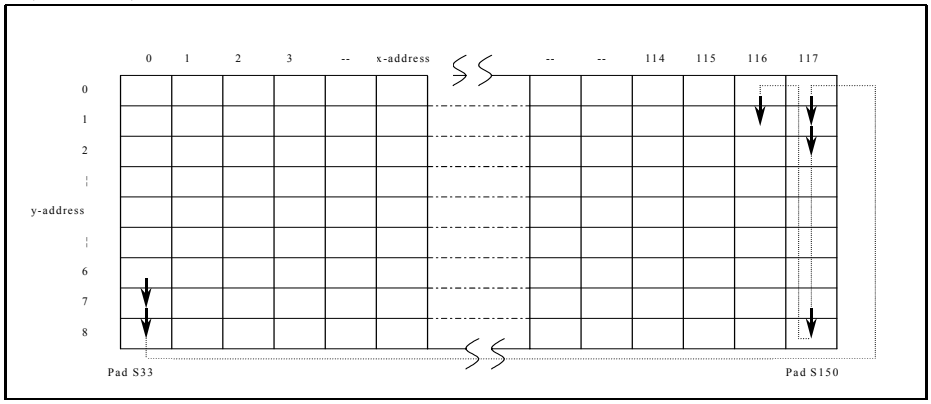


Figure 21

Mux Mode = 1, V = 1, DEC =0, MX = 0:

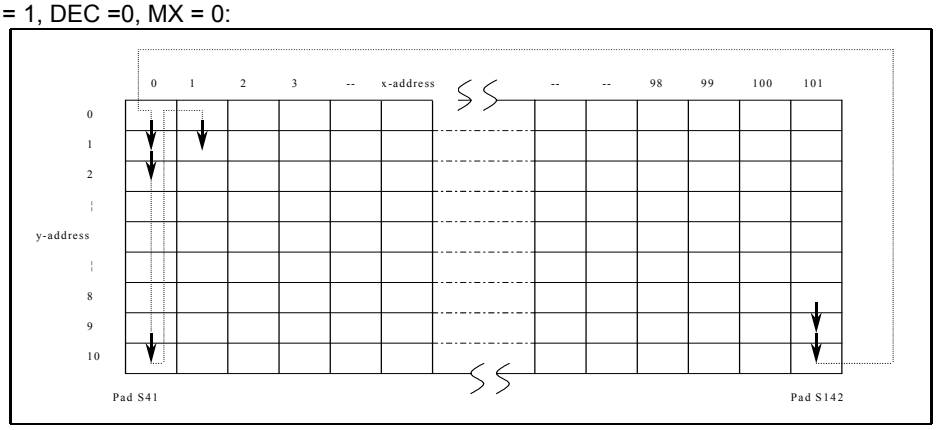


Figure 22

Mux Mode = 1, V = 1, DEC =1, MX = 0:

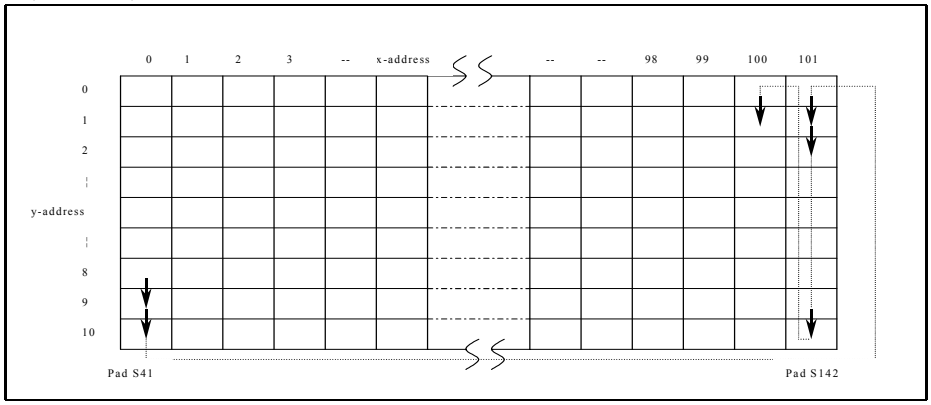


Figure 23

Mux Mode = 0, V = 0, DEC =0, MX = 1:

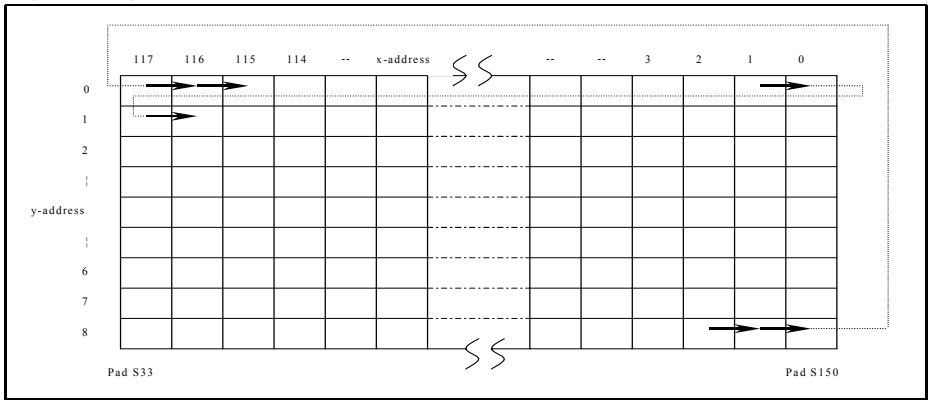


Figure 24

Mux Mode = 0, V = 0, DEC =1, MX = 1:

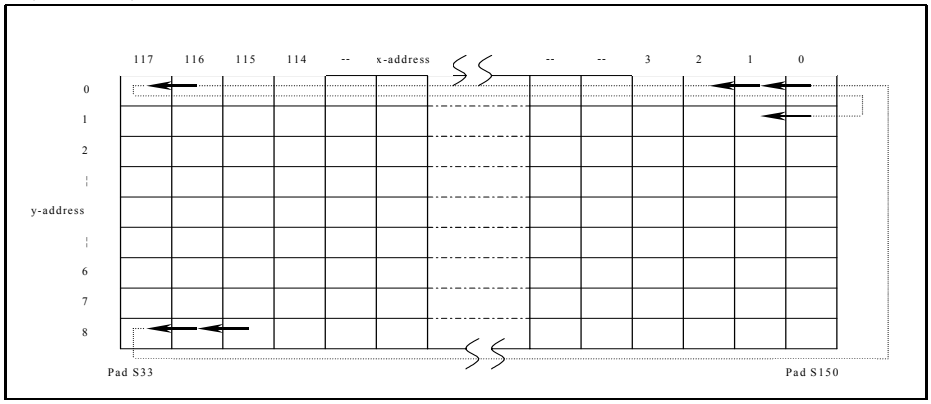


Figure 25

Mux Mode = 1, V = 0, DEC =0, MX = 1:

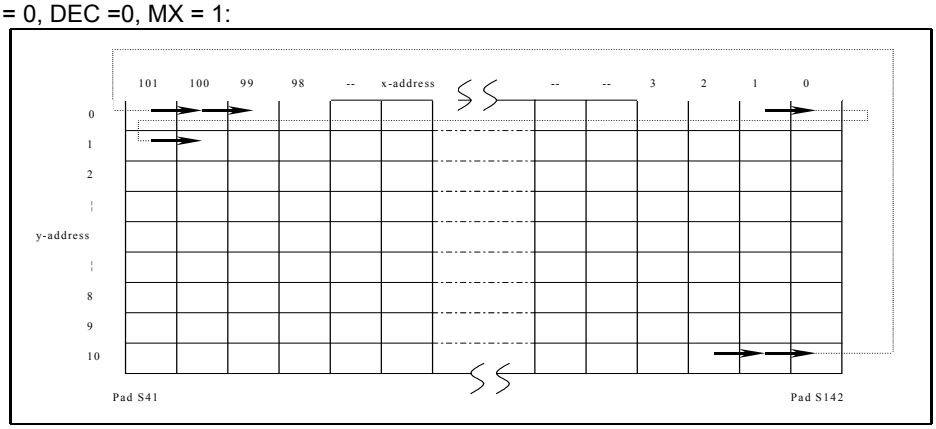


Figure 26

Mux Mode = 1, V = 0, DEC =1, MX = 1:

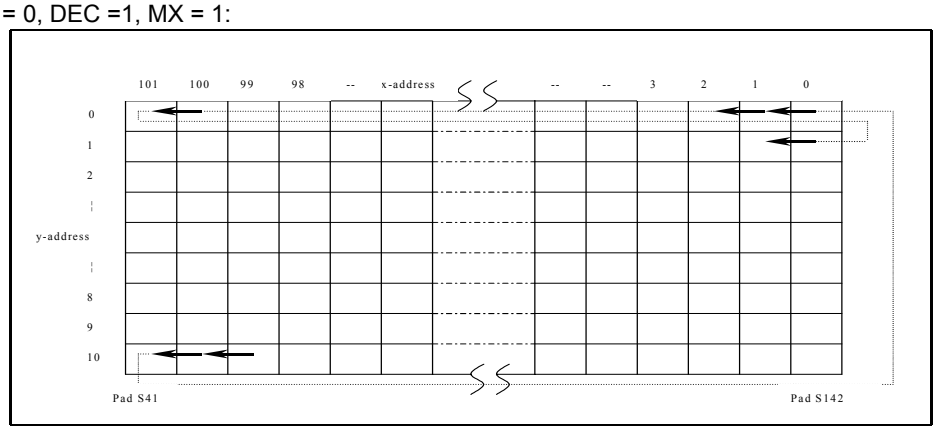


Figure 27

Mux Mode = 0, V = 1, DEC =0,MX = 1:

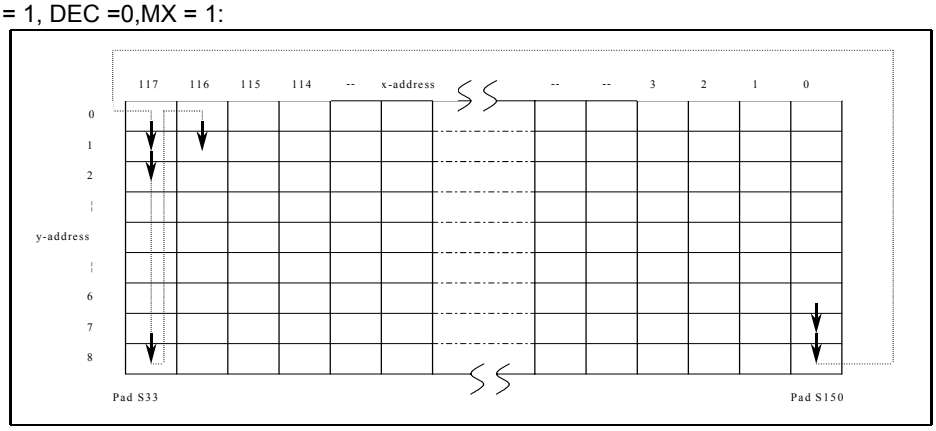


Figure 28

Mux Mode = 0, V = 1, DEC =1,MX = 1:

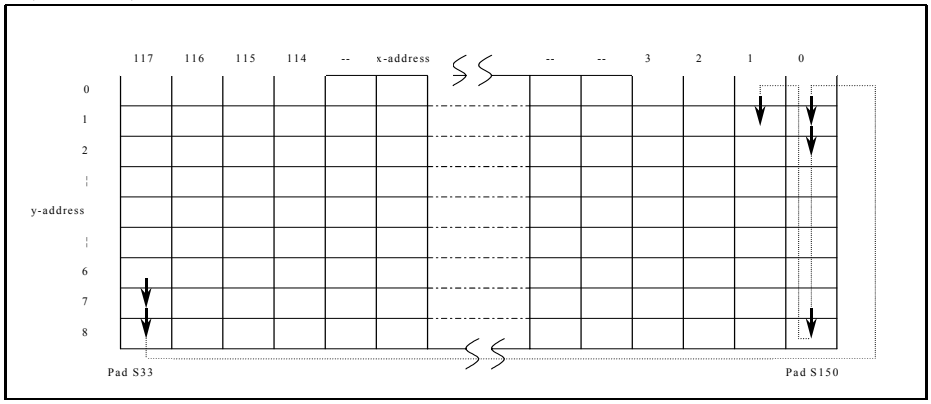


Figure 29

Mux Mode = 1, V = 1, DEC =0, MX = 1:

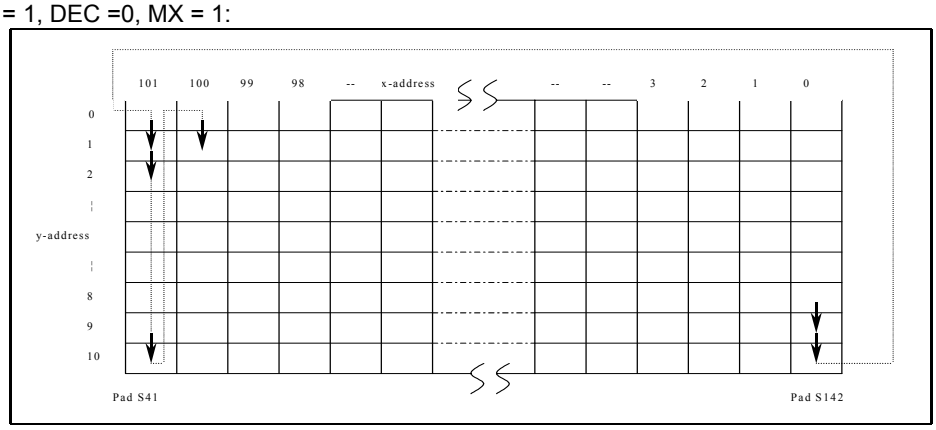


Figure 30

Mux Mode = 1, V = 1, DEC =1, MX = 1:

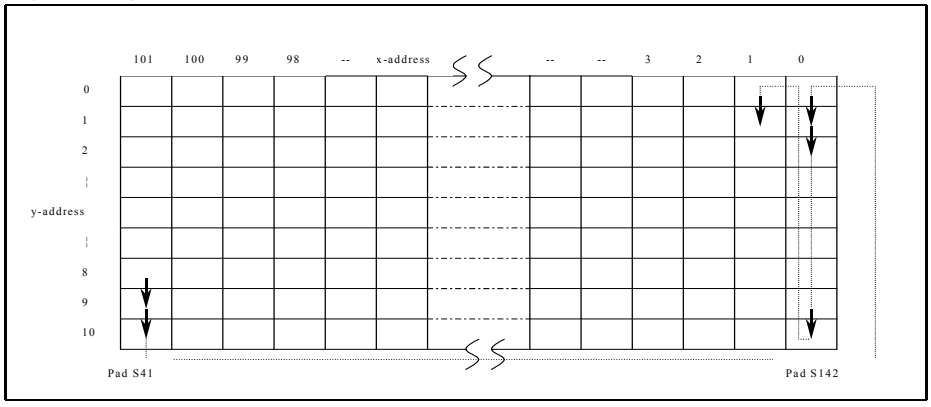


Figure 31

8.6 Initialization of EM6126

Data loaded into EM6126 can be divided in two parts:

- The bits stored in the DDRAM, which are corresponding to LCD pixels.
- The command bits, which are used to set functions of the LCD controller.

The way of addressing these bits is described in table below:

	Instruction	RW	Control Byte								Control Byte								Description
			CO	DC	test[2]	test[1]	test[0]	ini[2]	ini[1]	ini[0]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Initialization of functions	Initialization 0	0	1	0	0	0	0	0	0	0	Mux Mode	TC [1]	TC [0]	Inv. Row	MX	Blank	Checker	Inv. Video	Set functions
	Initialization 1	0	1	0	0	0	0	0	0	1	X[6]	X[5]	X[4]	X[3]	X[2]	X[1]	X[0]	V	Set column adress for DDRAM write access and vertical/horizontal addressing
	Initialization 2	0	1	0	0	0	0	0	1	0	Y[3]	Y[2]	Y[1]	Y[0]	0	Vlcd Dischg	DEC	LSB	Set bank adress for DDRAM write access, increment /decrement pointer and LSB/MSB mode
	Initialization 3	0	1	0	0	0	0	0	1	1	Vlcd Level [7]	Vlcd Level [6]	Vlcd Level [5]	Vlcd Level [4]	Vlcd Level [3]	Vlcd Level [2]	Vlcd Level [1]	Vlcd Level [0]	Programming the internally generated LCD voltage supply V_{LCD}
	Initialization 4	0	1	0	0	0	0	1	0	0	Mult [1]	Mult [0]	Partial Display	First Row PD [3]	First Row PD [2]	First Row PD [1]	First Row PD [0]	Sleep	Number of voltage multiplier stages Partial display parameters Sleep mode
Test	Test 0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	Byte test 0, all bits must be set to 0
	Test 1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	Byte test 1, all bits must be set to 0
	Test 2	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	Byte test 2, all bits must be set to 0
	Test 3	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	Byte test 3, all bits must be set to 0
Write DDRAM	Write 1 byte in DDRAM	0	1/0	1	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Write data byte to the Display Data Ram
Read Status	Read 1 byte in initialization	1	-	-	-	-	-	-	-	-	Mux Mode	TC [1]	TC [0]	Inv. Row	MX	Blank	Checker	Inv. Video	Read Status Byte from EM6126 Status Byte = initialization 0 using I^2C interface

Table 4: EM6126 instructions

Instruction bits from Table 4, active levels and state after reset:

Bits	0	1	State after reset
Mux Mode	Multiplex rate 65	Multiplex rate 81	0
TC[1:0]	Select V_{LCD} Temperature Coefficient		00b
Inv. Row.	Normal row drivers	Mirrored row drivers	0
MX	Normal column drivers	Mirrored column drivers	0
Blank	Display DDRAM content	LCD blanked (all OFF)	0
Checker	Display DDRAM content	LCD = checker board	0
Inv. Video	LCD = DDRAM	LCD = NOT (DDRAM)	0
X[6:0]	x-address pointer. Selects DDRAM columns to be accessed		0000000b
V	Horizontal addressing	Vertical addressing	0
Y[3:0]	y-address pointer. Selects DDRAM bank to be accessed		0000b
V_{LCD} Dischg	Normal Mode	Discharge Capacitor	0b
DEC	x-address pointer incremented	x-address pointer decrement	0
LSB	DB7 copied to the higher row of the selected bank	DB0 copied to the higher row of the selected bank	0
V_{LCD} Level[7:0]	Program the required LCD supply voltage		00000000b
Mult[1:0]	Number of voltage multiplier stages		00b
Partial Display	Mux Mode multiplex rate	17 LCD rows active only	0
First RowPD[3:0]	Position of first active row when partial display mode		0000b
Sleep	Normal mode	Sleep mode: No LCD pixel active, low power consumption	0

Table 5: Internal functions after reset.

8.7 Description of instructions

8.7.1 Initialization 0

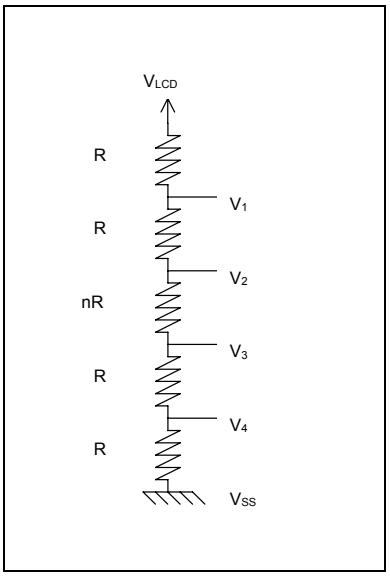
8.7.1.1 Mux Mode

Set the multiplex rate.

Mux Mode	0	1
Multiplex rate (number of row drivers)	65	81
Row drivers	S0 → S32 S151 → S182	S0 → S40 S143 → S182
Number of column drivers	118	102
Column drivers	S33 → S150	S41 → S142
Bias system	1/9	1/10

Table 6

The bias system sets the voltages V_1, V_2, V_3 and V_4 applied to row and column drivers. Assuming these voltages come from a resistive divider, we have:



The value of the corresponding bias system is:
$V_1 / V_{LCD} = 1/(n+4)$.
The value of the RMS voltage, applied to an LCD pixel ON, divided by the RMS voltage, applied to an LCD pixel OFF, $(V_{ON})_{RMS}/(V_{OFF})_{RMS}$, is optimized.

This condition leads to:

$$\frac{1}{(n+4)} = \frac{1}{(1+\sqrt{\text{MultiplexRate}})}$$

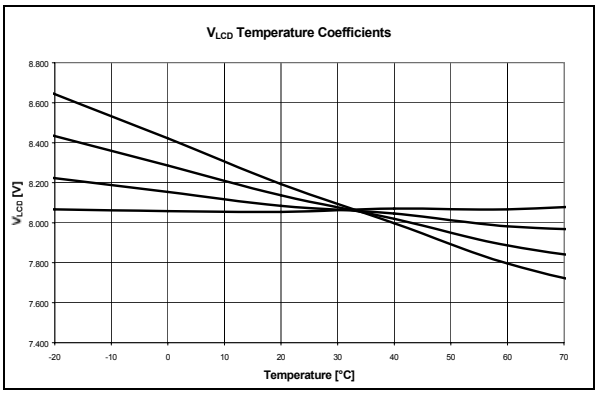
- bias systems ≅ 1/5 for multiplex rate 17 (partial display mode)
- bias systems ≅ 1/9 for multiplex rate 65
- bias systems = 1/10 for multiplex rate 81

8.7.1.2 TC[1:0]

These two bits set the V_{LCD} temperature compensation.
4 temperature coefficients are available for the internally generated voltage supply V_{LCD}. One of these coefficients is selected depending on the LCD display needs. The temperature coefficient is proportional to V_{LCD}.

TC[1]	TC[0]	V_{LCD} Temperature coefficient (mV/°C)
0	0	0
0	1	$-0.39 \times V_{LCD}$
1	0	$-0.86 \times V_{LCD}$
1	1	$-1.34 \times V_{LCD}$

Table 7



8.7.1.3 Inv. Row

Row driver read direction in the DDRAM can be mirrored to give more flexibility for LCD interconnects.
This function acts on the row driver that is activated when a given DDRAM row is read: it becomes active with no need of rewriting the RAM (see Table 8 and Figure 34: LCD output pads configuration in mux 65 depending on Inv. Row and MX).

Read data when Inv. Row=0:

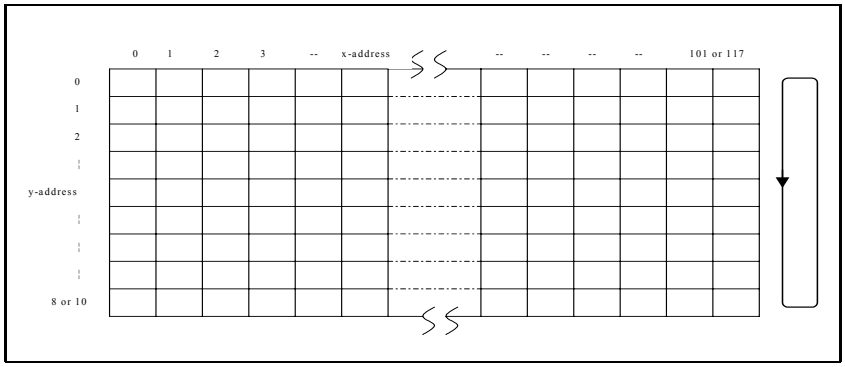


Figure 32

Read data when Inv. Row=1:

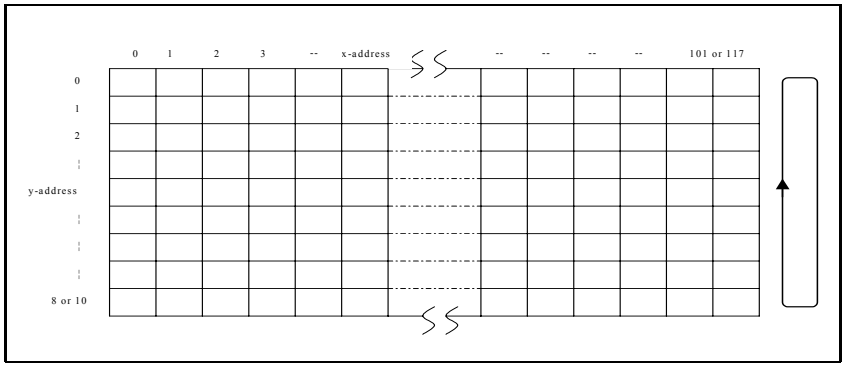


Figure 33

	Inv. Row	0	1	0	1
	Mux Mode	0	0	1	1
Pad name	S0	Row 0	Row 64	Row 0	Row 80
	S1	Row 1	Row 63	Row 1	Row 79
	⋮	⋮	⋮	⋮	⋮
	S32	Row 32	Row 32	Row 32	Row 48
	S33	x-addreess = 0		Row 33	Row 47
	S34	x-addreess = 1		Row 34	Row 46
	S35	x-addreess = 2		Row 35	Row 45
	S36	x-addreess = 3		Row 36	Row 44
	S37	x-addreess = 4		Row 37	Row 43
	S38	x-addreess = 5		Row 38	Row 42
	S39	x-addreess = 6		Row 39	Row 41
	S40	x-addreess = 7		Row 40	Row 40
	S41 to S142	x-addreess = 8 to x-addreess = 109		x-addreess = 0 to x-addreess = 101	
	S143	x-addreess = 110		Row 80	Row 0
	S144	x-addreess = 111		Row 79	Row 1
	S145	x-addreess = 112		Row 78	Row 2
	S146	x-addreess = 113		Row 77	Row 3
	S147	x-addreess = 114		Row 76	Row 4
	S148	x-addreess = 115		Row 75	Row 5
	S149	x-addreess = 116		Row 74	Row 6
	S150	x-addreess = 117		Row 73	Row 7
	S151	Row 64	Row 0	Row 72	Row 8
	S152	Row 63	Row 1	Row 71	Row 9
	⋮	⋮	⋮	⋮	⋮
	S182	Row 33	Row 31	Row 41	Row 39
	S183 = S0	Row 0	Row 64	Row 0	Row 80

Table 8

8.7.1.4 MX

Column driver pads can also be mirrored to give more flexibility for LCD interconnects.

This function changes the x-address pointer to reverse columns of the DDRAM accessed during a write cycle: a rewrite cycle is required to observe changes on outputs (see Figure 34: LCD output pads configuration in mux 65 depending on Inv. Row and MX)

Table 9 shows how the DDRAM is connected to LCD output pads, depending on bits Mux Mode, MX and Inv. Row.

	MX	0	1	0	1
	Mux Mode	0	0	1	1
Pad name	S0	Row 0		Row 0	
	⋮	⋮		⋮	
	S32	Row 32		Row 32	
	S33	x-address = 0	x-address = 117	Row 33	
	S34	x-address = 1	x-address = 116	Row 34	
	S35	x-address = 2	x-address = 115	Row 35	
	S36	x-address = 3	x-address = 114	Row 36	
	S37	x-address = 4	x-address = 113	Row 37	
	S38	x-address = 5	x-address = 112	Row 38	
	S39	x-address = 6	x-address = 111	Row 39	
	S40	x-address = 7	x-address = 110	Row 40	
	S41	x-address = 8	x-address = 109	x-address = 0	x-address = 101
	S42	x-address = 9	x-address = 108	x-address = 1	x-address = 100
	S43	x-address = 10	x-address = 107	x-address = 2	x-address = 99
	S44 to S139	x-address =11 to x-address =106	x-address =106 to x-address =11	x-address =3 to x-address = 98	x-address = 98 to x-address = 3
	S140	x-address = 107	x-address = 10	x-address = 99	x-address = 2
	S141	x-address = 108	x-address = 9	x-address = 100	x-address = 1
	S142	x-address = 109	x-address = 8	x-address = 101	x-address = 0
	S143	x-address = 110	x-address = 7	Row 80	
	S144	x-address = 111	x-address = 6	Row 79	
	S145	x-address = 112	x-address = 5	Row 78	
	S146	x-address = 113	x-address = 4	Row 77	
	S147	x-address = 114	x-address = 3	Row 76	
	S148	x-address = 115	x-address = 2	Row 75	
	S149	x-address = 116	x-address = 1	Row 74	
	S150	x-address = 117	x-address = 0	Row 73	
	S151	Row 64		Row 72	
	⋮	⋮		⋮	
	S182	Row 33		Row 41	
	S183 = S0	Row 0		Row 0	

Table 9: Relation between LCD output pads and row and columns of DDRAM

The combination of Mux Mode, Inv. Row and MX gives the following figures (next page) of output pads.

8.7.1.5 Blank

Sets all the LCD pixels OFF.

Every row driver and column driver is at V_{SS} level.

DDRAM content is not affected by this instruction.

8.7.1.6 Checker

Sets all the LCD pixels in a checker board pattern, LCD displays alternately ON and OFF pixels.

DDRAM content is not affected by this instruction.

8.7.1.7 Inv. Video

Sets an inverse video mode.

- If Inv. Video = 0, a logical 1 level stored in the DDRAM leads to an “ON” pixel displayed on the LCD.
- If Inv. Video = 1, a logical 1 level stored in the DDRAM leads to an “OFF” pixel displayed on the LCD.

DDRAM content is not affected by this instruction.

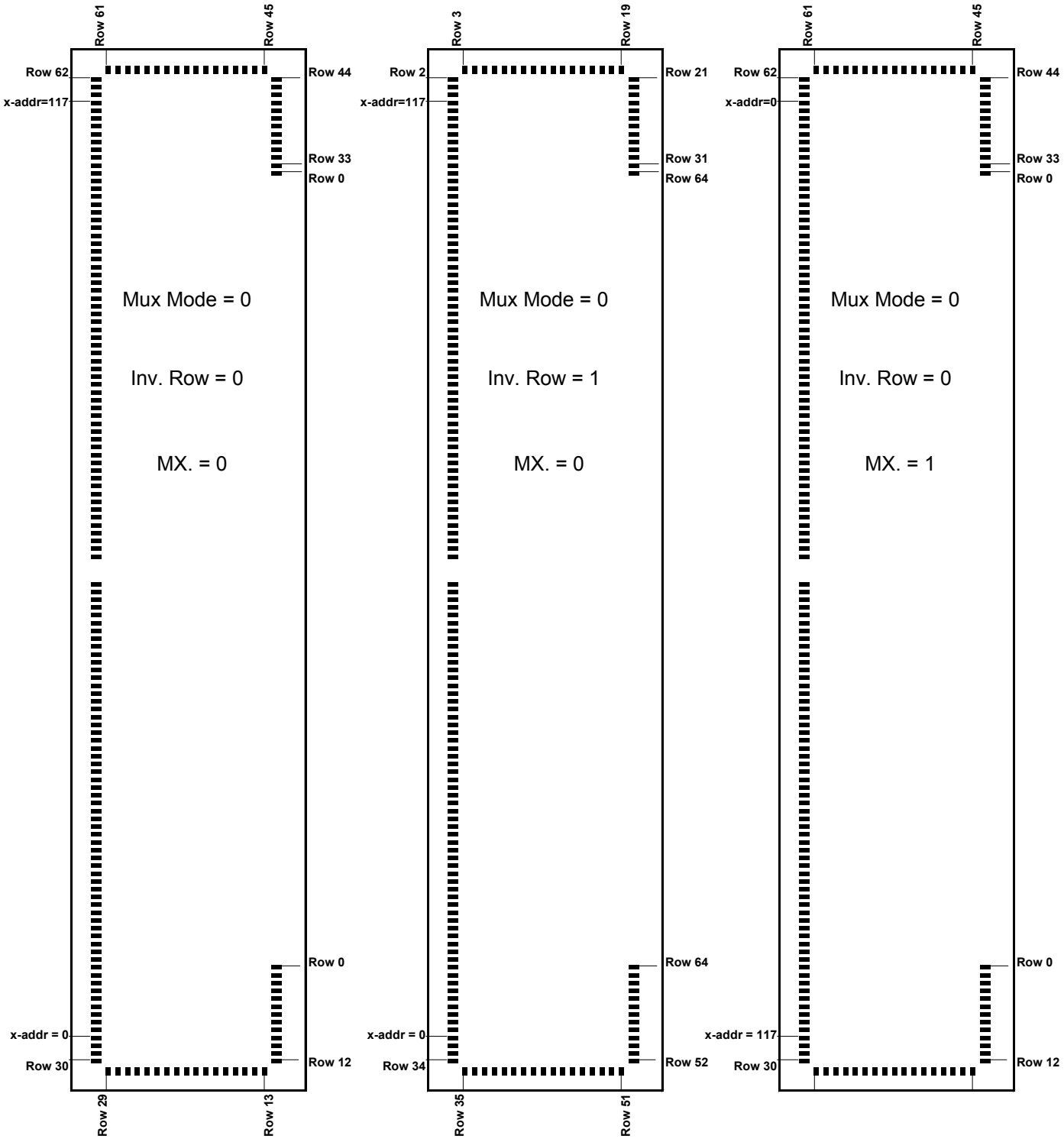


Figure 34: LCD output pads configuration in mux 65 depending on Inv. Row and MX

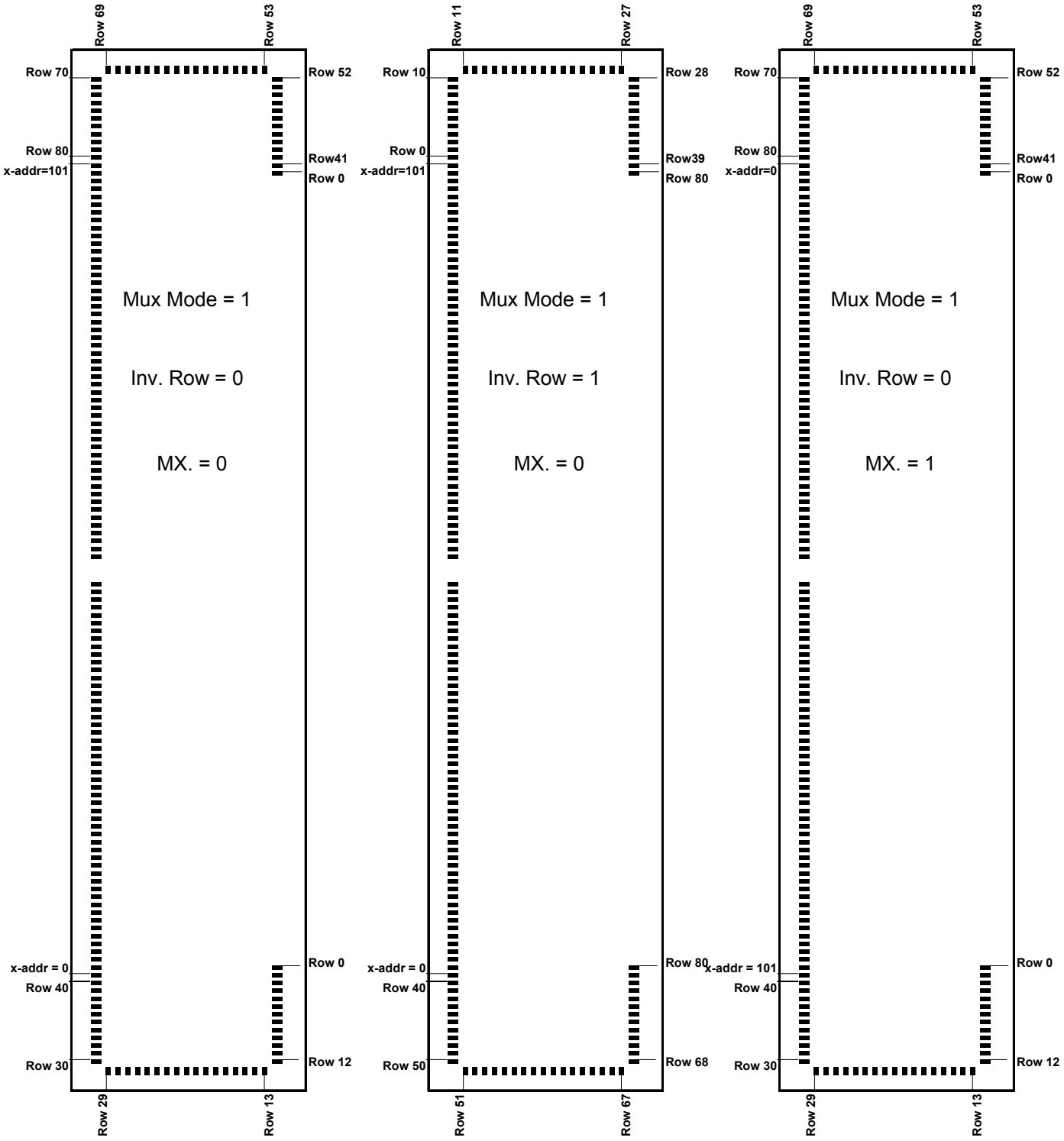


Figure 35: LCD output pads configuration in mux 81 depending on Inv. Row and MX

8.7.2 Initialization 1

8.7.2.1 X[6:0]

These 7 bits set the x-address pointer of the DDRAM.

Data are written into column “x-address” with: X[6] = MSB, X[0] = LSB.

As the number of column drivers depends on the selected multiplex rate, the DDRAM x-address pointer should also satisfy the following conditions:

- If Mux Mode = 0 then 0 ≤ x-address ≤ 1110101b. (117).
- If Mux Mode = 1 then 0 ≤ x-address ≤ 1100101b. (101).

8.7.2.2 V

Vertical addressing:

- If V = 0, DDRAM x-address pointer is incremented or decremented after each data byte sent.
- If V = 1, DDRAM y-address pointer is incremented or decremented after each data byte sent.

8.7.3 Initialization 2

8.7.3.1 Y[3:0]

These 4 bits set the y-address pointer of the DDRAM.

Data are written into bank “y-address” with Y[3]= MSB, Y[0]= LSB.

As the multiplex rate is digitally programmable, the DDRAM y-address pointer should also satisfy the following conditions:

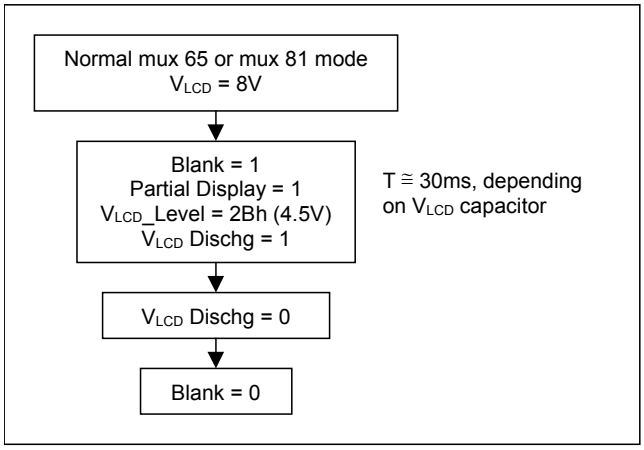
- If Mux Mode = 0 then 0 ≤ y-address ≤ 1000b.
- If Mux Mode = 1 then 0 ≤ y-address ≤ 1010b.

8.7.3.2 Vlcd Dischg.

The V_{LCD} discharge function can discharge the capacitor connected to PAD V_{LCD}. This operation becomes necessary when changing from Mux 65 or 81 mode to Partial Display Mode. In this case, a lower V_{LCD} is required than the voltage used for Mux 65 or 81 operation, the display at beginning of partial mode operation could be completely ‘ON’ until V_{LCD} has decreased to its new correct value.

To avoid this effect, an internal pull down helps the V_{LCD} voltage to drop down and to reach the new optimum value in a short time. This pull down is active until bit *‘Vlcd Dischg’* is reset to low level.

Typical use of *‘Vlcd Dischg’* command:



Using this command with external power supply on V_{LCD} can damage the IC.

8.7.3.3 DEC

DEC controls the DDRAM writing direction:

- If DEC = 0 then x-address pointer increments after each byte written into the DDRAM.
- If DEC = 1 then x-address pointer decrements after each byte written into the DDRAM.

8.7.3.4 LSB

This instruction changes the bytes send to the DDRAM before writing them. For instance, for bank 1 we have:

- If LSB = 0 then DB7 is written on Row 1.
- If LSB = 1 then DB0 is written on Row 1 (see Figure 14 and Figure 15).

8.7.4 Initialization 3

8.7.4.1 Vlcd Level[7:0]

This byte sets the internally generated voltage level.

These 8 bits generate integer “V_{LCD} Level”, V_{LCD} Level [7] = MSB, V_{LCD} Level [0] = LSB.

V_{LCD} is given by the following formula:

$$V_{LCD} = 3.02 + 0.0352 \times V_{LCD}\_Level$$

8.7.5 Initialization 4

8.7.5.1 Mult[1:0]

These two bits set the internal voltage multiplier factor.

These bits should be defined depending on the V_{HV} supply voltage level and the current consumption due to LCD load, to have a correct V_{LCD} voltage.

If low V_{LCD} is required, for instance when partial display mode is enabled, lower voltage multiplier range should be used, resulting in a current consumption reduction (due to better voltage multiplier efficiency at lower multiplication rate).

Mult1	Mult0	Voltage multiplier
0	0	$\times 2$
0	1	$\times 3$
1	0	$\times 4$
1	1	$\times 5$

Table 10

8.7.5.2 Partial Display

Set the partial display configuration of the driver (multiplex ratio 17).

In this configuration, 17 rows are active:

- The row which corresponds to RAM address 0.
- 16 selectable rows, first one is defined by First Row PD [3:0].

Partial Display	Multiplex rate
0	65 or 81 (depending on Mux Mode)
1	17

Table 11

8.7.5.3 First Row PD[3:0]

Partial display mode yields to an LCD with 2 activated banks.

Row 0 is always active, it could be used to drive icons.

The 16 other active rows are selected from 64 or 80 rows, as shown in following table:

Mux Mode	*First Row PD[3]*	*First Row PD[2]*	*First Row PD[1]*	*First Row PD[0]*	First active row (DDRAM)	Last active row (DDRAM)	Activated banks
0 or 1	0	0	0	0	Row 1	Row 16	0,1,2
	0	0	0	1	Row 9	Row 24	0,2,3
	0	0	1	0	Row 17	Row 32	0,3,4
	0	0	1	1	Row 25	Row 40	0,4,5
	0	1	0	0	Row 33	Row 48	0,5,6
	0	1	0	1	Row 41	Row 56	0,6,7
	0	1	1	0	Row 49	Row 64	0,7,8
1	0	1	1	1	Row 57	Row 72	0,8,9
	1	0	0	0	Row 65	Row 80	0,9,10

Table 12

- If Mux Mode = 0, 0 ≤ First_Row PD [3:0] ≤ 0110b.
- If Mux Mode = 1, 0 ≤ First_Row PD [3:0] ≤ 1000b.

Values for “First_Row PD [3:0]” outside these ranges are not allowed.

8.7.5.4 Sleep

This function stops all functionality, internal oscillator and voltage multiplier are off, and LCD is blanked. It yields to a very low current consumption with leakage currents only.

8.7.6 Test 0 to 3

All bits must be set to 0 (see example in typical application page 37).

8.8 LCD outputs

The LCD output signals and voltages are optimized for the best LCD contrast and minimum DC component of voltage applied to the LCD display. Table 13 gives bias voltages referring to V_{LCD}.

Multiplex Rate	V_{LCD}	V_1	V_2	V_3	V_4	V_{SS}
n	1	$1-\left(\frac{1}{\sqrt{n}+1}\right)$	$1-\left(\frac{2}{\sqrt{n}+1}\right)$	$\frac{2}{\sqrt{n}+1}$	$\frac{1}{\sqrt{n}+1}$	0
81 (Mux Mode = 1)	1	0.90	0.80	0.20	0.10	0
65 (Mux Mode = 0)	1	0.89	0.78	0.22	0.11	0
17 (Partial Display = 1)	1	0.80	0.60	0.40	0.20	0

Table 13: Values of intermediate bias voltages

Table 14 gives ratios of V_{LCD} in reference to RMS voltage of an OFF pixel, and the RMS voltage ratios between an ON pixel and an OFF pixel (achievable contrasts). These values correspond to bias voltages described in Table 13.

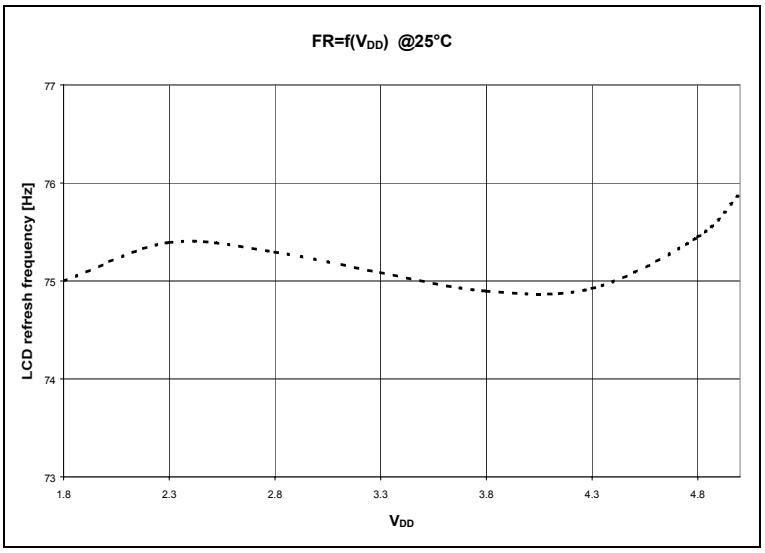
Programmed multiplex rate	LCD Bias configuration	$\frac{V_{LCD}}{V_{OFF}(RMS)}$	$\frac{V_{ON}(RMS)}{V_{OFF}(RMS)}$
81	6 levels	$\sqrt{\frac{\sqrt{n}(\sqrt{n}+1)^2}{2(\sqrt{n}-1)}}=7.500$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}}=1.118$
65	6 levels	$\sqrt{\frac{\sqrt{n}(\sqrt{n}+1)^2}{2(\sqrt{n}-1)}}=6.847$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}}=1.133$
17	6 levels	$\sqrt{\frac{\sqrt{n}(\sqrt{n}+1)^2}{2(\sqrt{n}-1)}}=4.162$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}}=1.281$

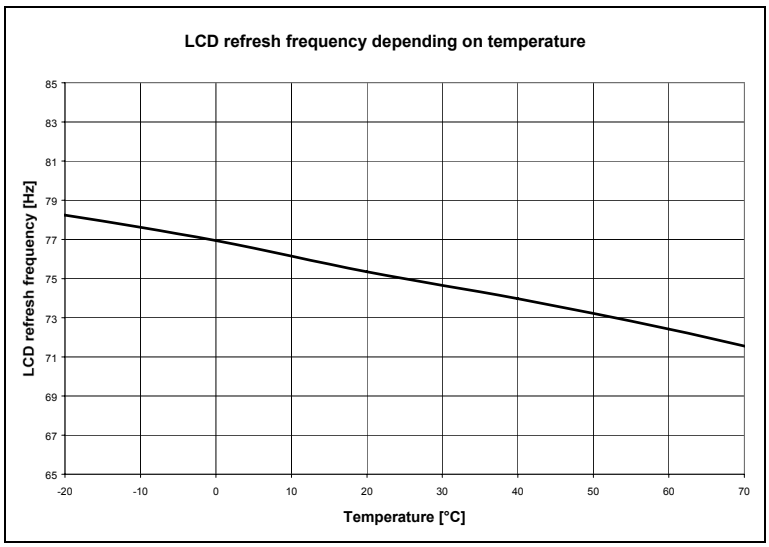
Table 14: Required LCD supply voltage and achieved LCD contrast

The selected LCD display gives the value of $V_{OFF}(RMS)$ and the value of $\frac{V_{LCD}}{V_{OFF}(RMS)}$ gives the needed V_{LCD} voltage supply. The Partial Display mode decreases V_{LCD}, leading to lower power consumption. Lower V_{LCD} decreases consumption because less stages for voltage multiplier can be selected.

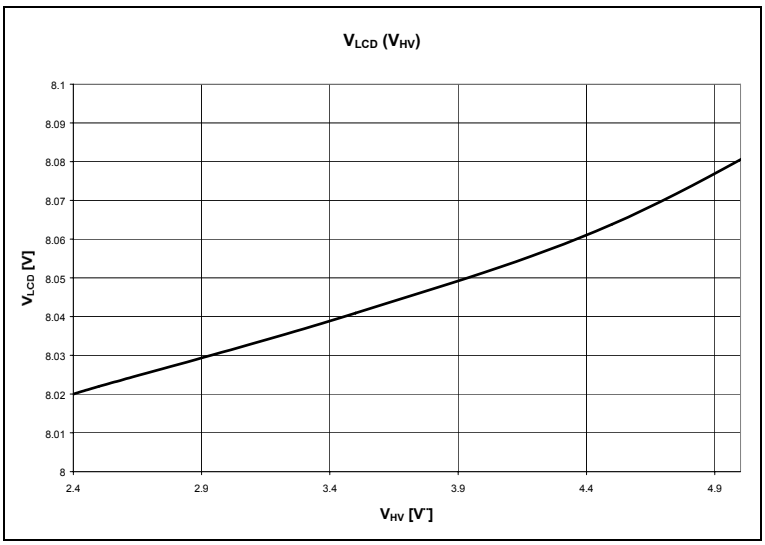
8.9 LCD refresh frequency

LCD refresh frequency depends on an internal RC oscillator. Pad FR outputs this frequency, multiplied by the multiplex rate. Following figures display typical variations depending on V_{DD} power supply and temperature.





8.10 V_{LCD} depending on V_{HV}



8.11 LCD driver waveforms

Row and Column Multiplexing Waveform EM6126 Mux = 81

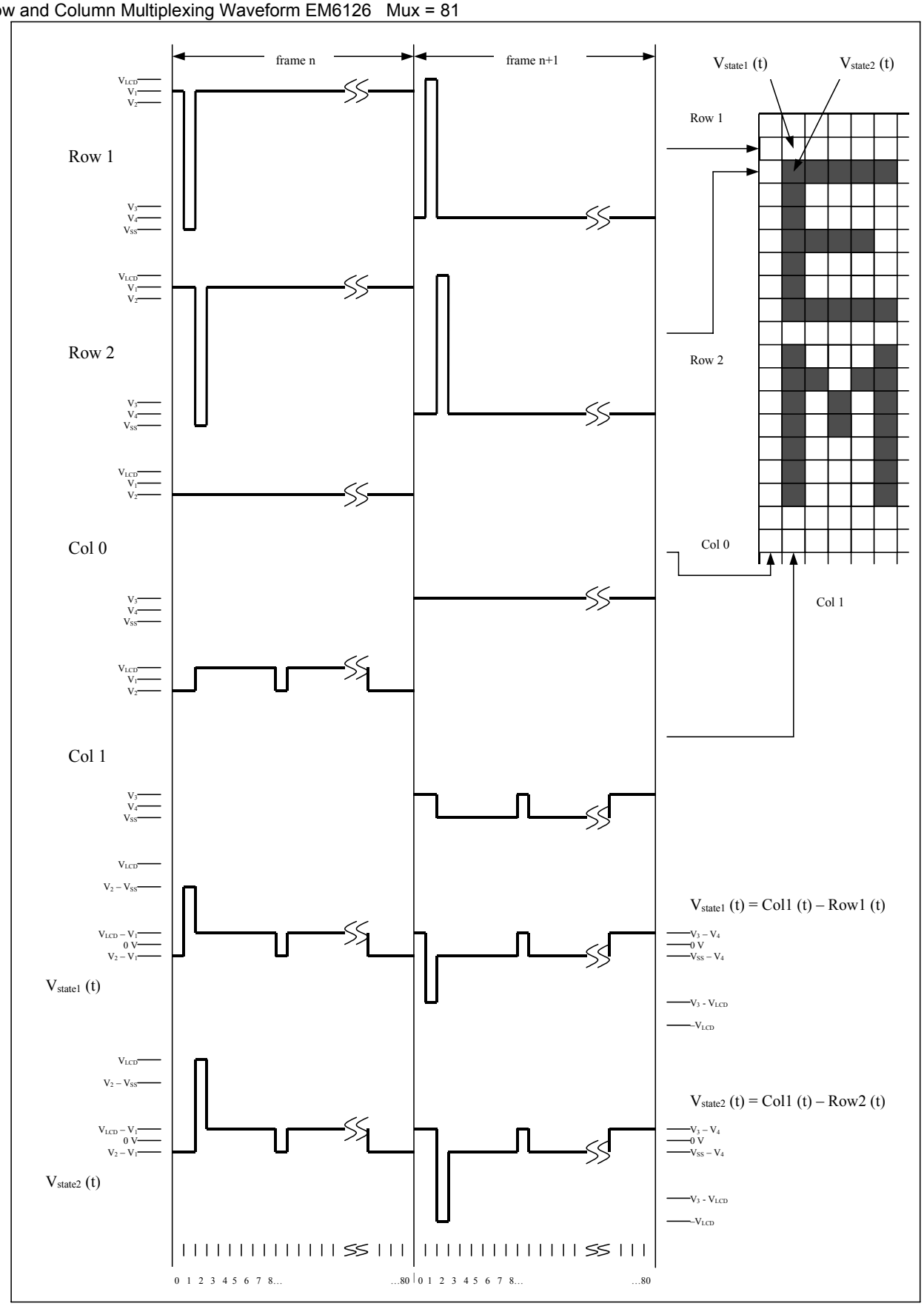


Figure 36

Row and Column Multiplexing Waveform EM6126 Mux = 65

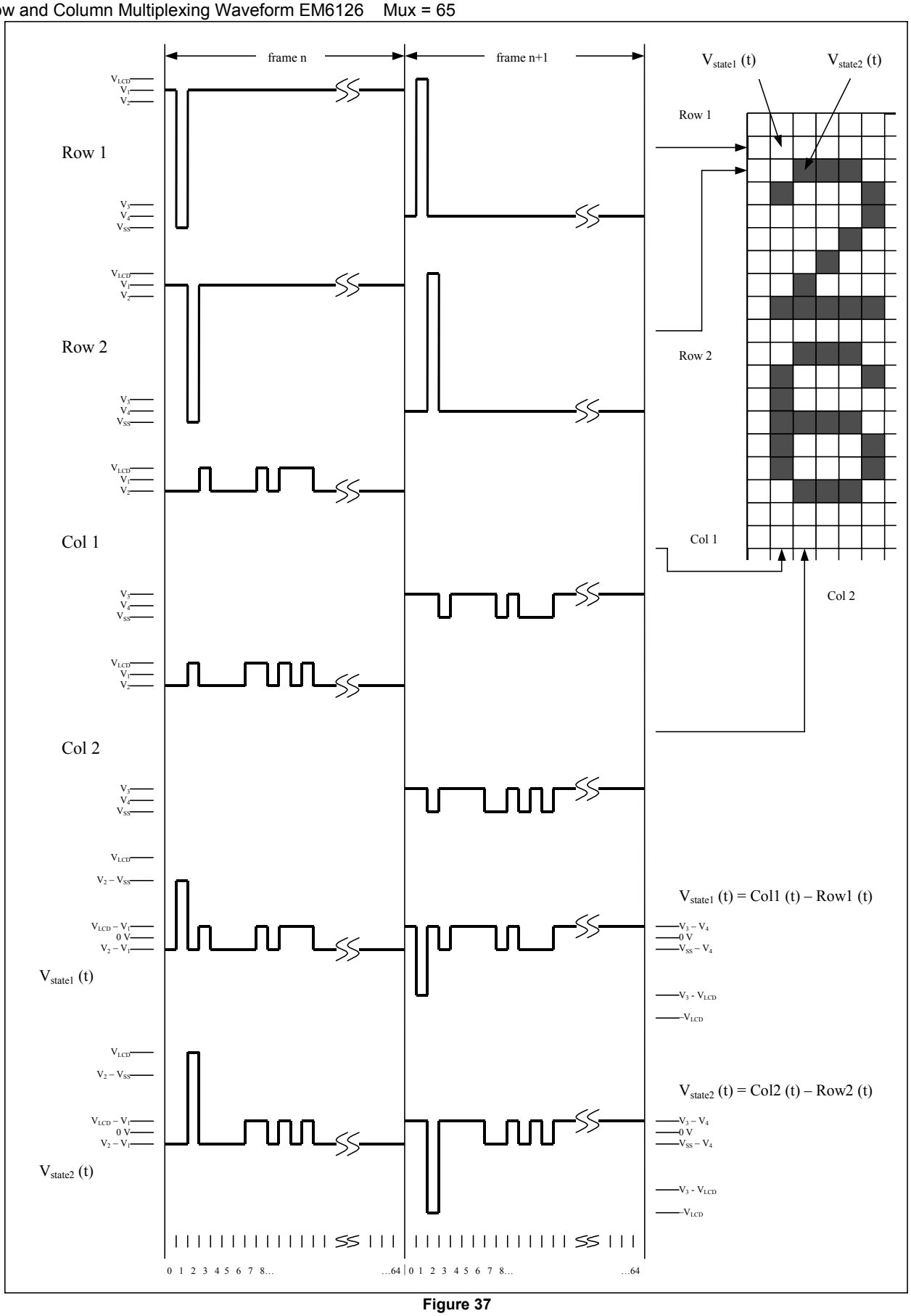


Figure 37

8.11.1 Partial Display

Row and Column Multiplexing Waveform EM6126 Mux = 17

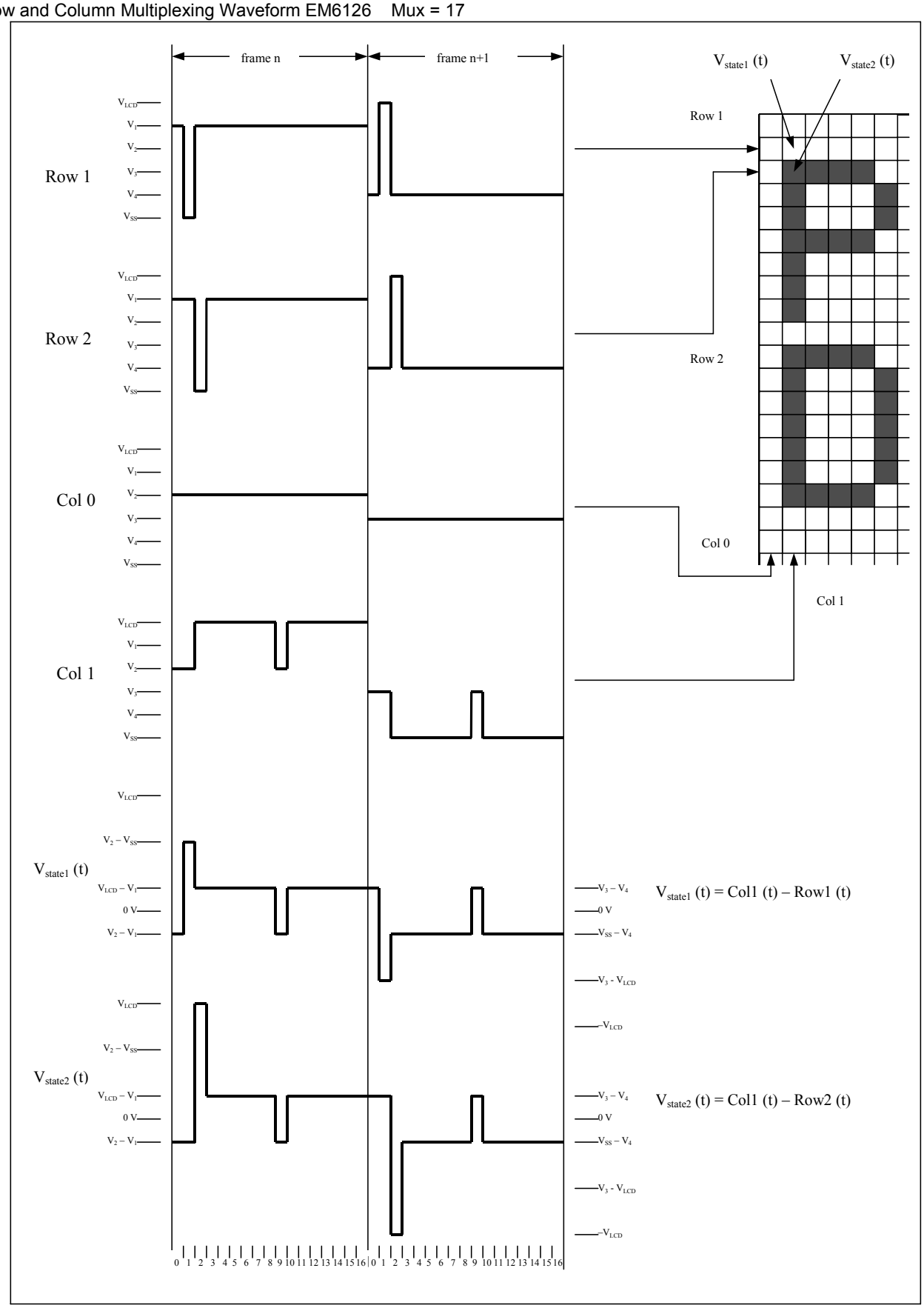


Figure 38

9 Typical Application

9.1 Power supply connection

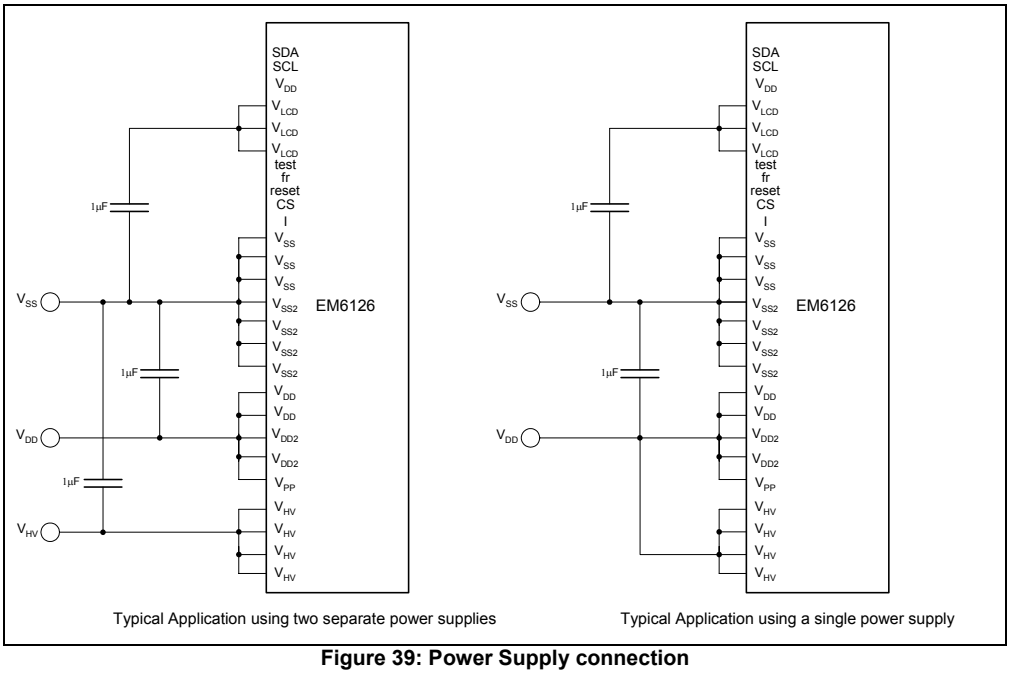


Figure 39: Power Supply connection

9.2 Connection and communication with the display

This example gives typical programming steps for EM6126 with I^2C interface, for serial interface, start and stop conditions should be replaced by CS at 0L and CS at 1L. LCD display is connected as described on Figure 40:

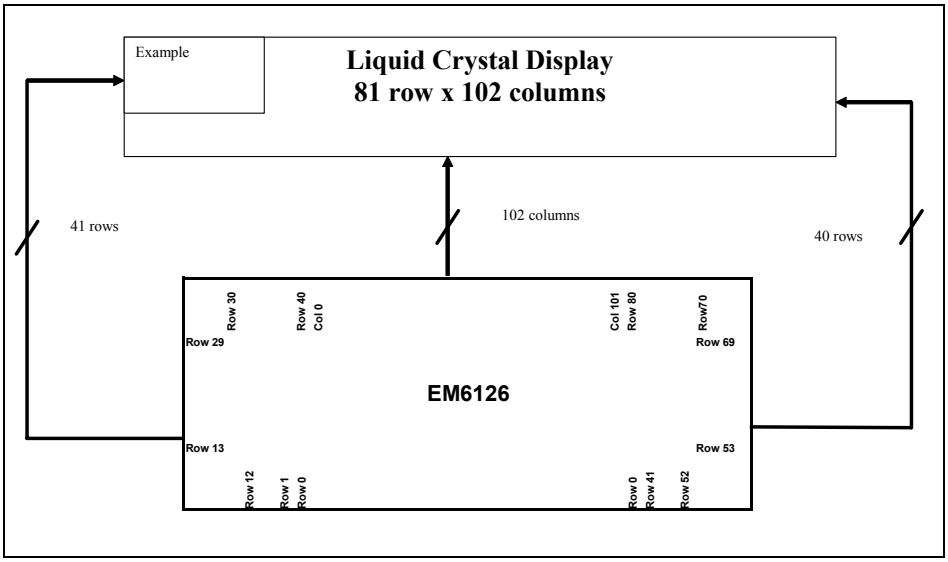
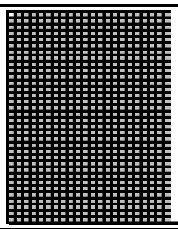
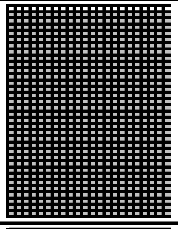
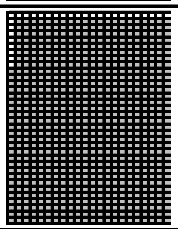
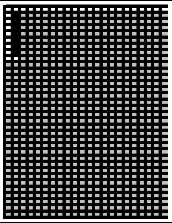
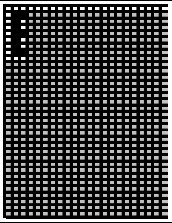
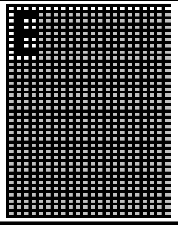
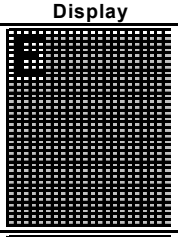
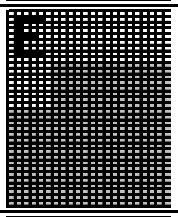
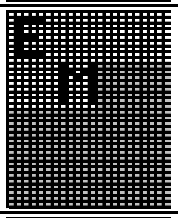
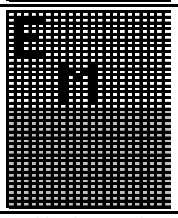
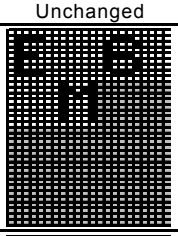
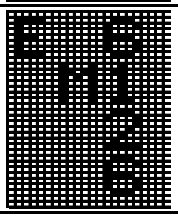
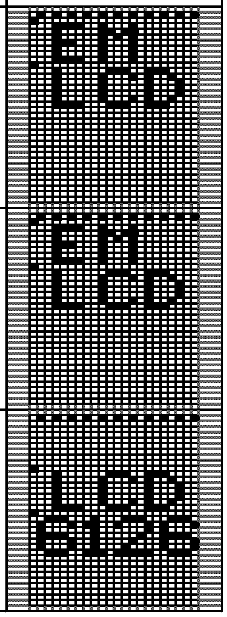


Figure 40: Connection between EM6126 and LCD for the application example

Step	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Comment	Display
1	Power on									Undefined
2	Reset								A reset cycle must always follow the power on	Blank
3	I2C start condition									Blank
4	x	x	x	x	x	x	x	0	EM6126 slave address + write mode	Blank
5	1	0	0	0	0	0	0	0	Control byte for initialization 0	Blank
6	1	0	1	0	0	0	0	0	**Data byte = initialization 0** Multiplex Rate = 81 Vlcd Temperature Coefficient = -0.39 x Vlcd (mV/°C) No row or column mirroring No blank, Checker or Video functions.	Blank
7	1	0	0	0	0	0	1	1	Control byte for initialization 3	Blank
8	1	0	0	0	1	1	1	0	**Data byte = initialization 3** Programmed Vlcd_level = 10001110b (8Eh=142) Vlcd = 3.02 + 142*0.0352 = 8.02V	Blank
9	1	0	0	0	0	1	0	0	Control byte for initialization 4	Blank
10	1	1	0	0	0	0	0	0	**Data byte = initialization 4** x 5 Voltage Multiplier No partial display mode. No sleep mode	Undefined
11	1	0	1	0	0	0	0	0	Control byte for test 0	Undefined
12	0	0	0	0	0	0	0	0	bits test must be set to 0L	
13	1	0	1	0	1	0	0	0	Control byte for test 1	
14	0	0	0	0	0	0	0	0	bits test must be set to 0L	
15	1	0	1	1	0	0	0	0	Control byte for test 2	
16	0	0	0	0	0	0	0	0	bits test must be set to 0L	
17	1	0	1	1	1	0	0	0	Control byte for test 3	
18	0	0	0	0	0	0	0	0	bits test must be set to 0L	

Step	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Comment	Display
19	0	1	0	0	0	0	0	0	Last control byte DDRAM write selected Fisrt DDRAM byte stored at x-address = 0, y-address = 0 Horizontal addressing is selected (state after reset)	Undefined
20	0	x	x	x	x	x	x	x	Only DB7 is stored at row 0 of DDRAM, column 0	
21 to 121	0	x	x	x	x	x	x	x	Only DB7 is stored at row 0, columns 1 to 101	
122	0	0	0	0	0	0	0	0	DB7 to DB0 are stored at column 0, rows 1 to 8	
123	1	1	1	1	1	1	1	0	DB7 to DB0 are stored at column 1, rows 1 to 8	
124	1	0	0	1	0	0	1	0	DB7 to DB0 are stored at column 2, rows 1 to 8	
125	1	0	0	1	0	0	1	0	DB7 to DB0 are stored at column 3, rows 1 to 8	

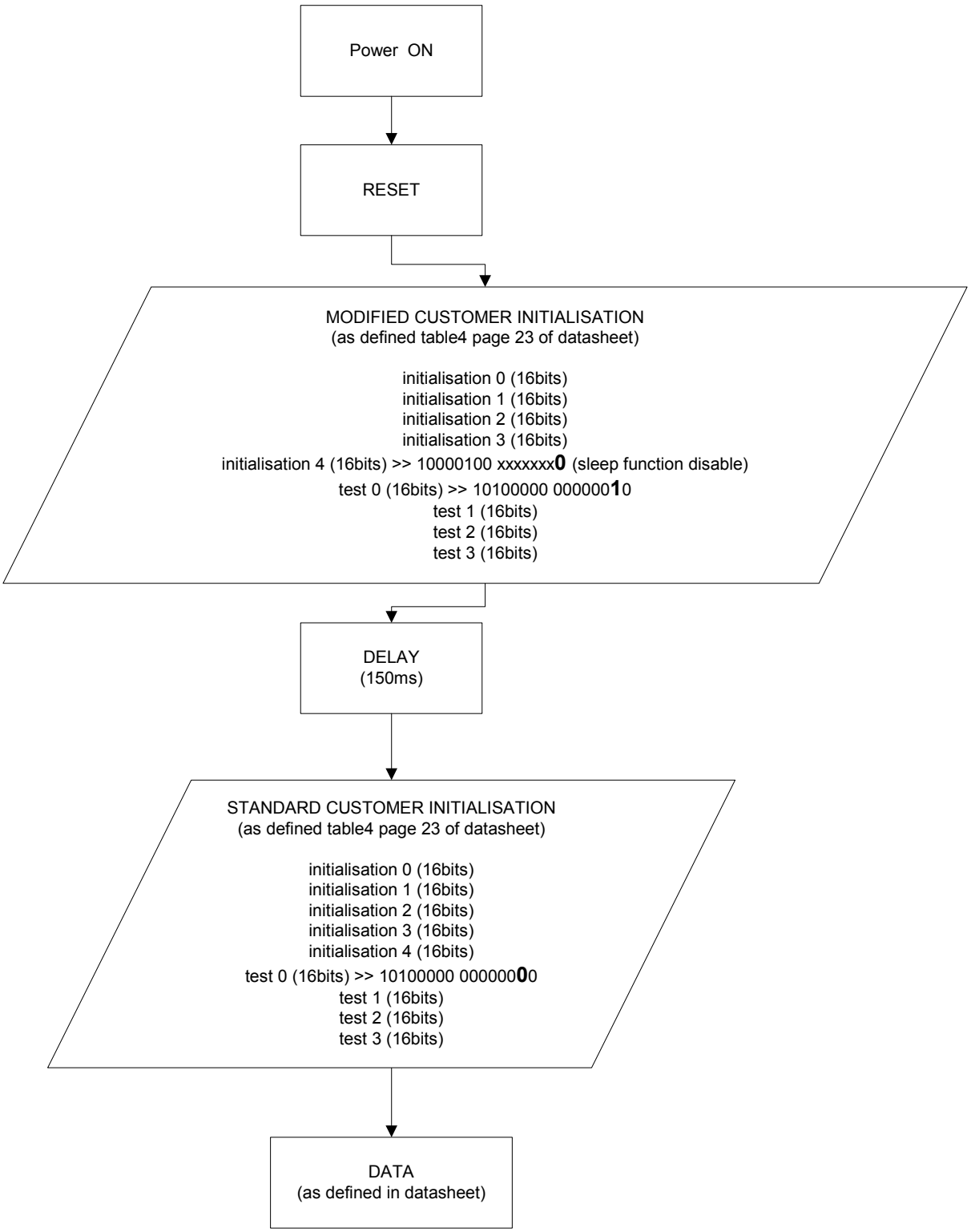
Step	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Comment	Display
126	1	0	0	0	0	0	1	0	DB7 to DB0 are stored at column 4, rows 1 to 8	
127 to 229	0	0	0	0	0	0	0	0	DB7 to DB0 are stored at column 5 to 101, rows 1 to 8 column 0 to 5, rows 9 to 16	
230	0	0	0	0	0	0	0	0	Write letter M	
231	1	1	1	1	1	1	1	0		
232	0	1	0	0	0	0	0	0		
233	0	0	1	0	0	0	0	0		
234	0	1	0	0	0	0	0	0		
235	1	1	1	1	1	1	1	0		
236 to 325	0	0	0	0	0	0	0	0	DB7 to DB0 are stored at column 12 to 101, rows 9 to 16	
326	I2C stop condition + new start condition									Unchanged
327	x	x	x	x	x	x	x	0	EM6126 slave address + write mode	Unchanged
328	1	0	0	0	0	0	0	1	Control byte for initialization 1	Unchanged
329	0	0	0	1	1	0	0	0	x-address = 12 , Horizontal mode addressing	Unchanged
330	1	0	0	0	0	0	1	0	Control byte for initialization 2	Unchanged
331	0	0	0	1	0	0	0	0	y-address = 1	Unchanged
332	0	1	0	0	0	0	0	0	DDRAM write selected	Unchanged
333	0	0	0	0	0	0	0	0	Write 6	
334	0	1	1	1	1	1	0	0		
335	1	0	0	1	0	0	1	0		
336	1	0	0	1	0	0	1	0		
337	1	0	0	1	0	0	1	0		
338	0	1	0	0	1	1	0	0		
339	x	x	x	x	x	x	x	x	Continuation…	

Step	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Comment	Display
1	I2C start condition									Previously set
2	x	x	x	x	x	x	x	0	EM6126 slave address + write mode	Unchanged
3	1	0	0	0	0	0	0	0	Control byte for initialization 0	Unchanged
4	1	0	1	0	0	1	0	0	Blank = 1	All pixels OFF
5	1	0	0	0	0	0	1	1	Control byte for initialization 3	All pixels OFF
6	0	0	1	0	1	0	1	1	Vlcd_level = 2Bh	All pixels OFF
7	1	0	0	0	0	0	1	0	Control byte for initialization 2	All pixels OFF
8	0	0	0	0	0	1	0	0	Vlcd_Dischg = 1	All pixels OFF
9	1	0	0	0	0	1	0	0	Control byte for initialization 4	All pixels OFF
10	1	1	1	0	0	0	0	0	Partial display on banks: 0, 1 and 2	All pixels OFF
Wait 30 ms										
11	1	0	0	0	0	0	1	0	Control byte for initialization 32	All pixels OFF
12	0	0	0	0	0	0	0	0	Vlcd_Dischg = 0	All pixels OFF
13	1	0	0	0	0	0	0	0	Control byte for initialization 0	All pixels OFF
14	1	0	1	0	0	0	0	0	Blank = 0 Partial display on banks: 0, 1 and 2	
15	1	0	0	0	0	1	0	0	Control byte for initialization 4	
16	1	1	1	0	0	0	1	0	Partial display on banks: 0, 2 and 3	

Remark:

This typical application example shows an LCD display 'ON' before the DDRAM is completely written, parts of the LCD are undefined as DDRAM data is undefined at power on. To avoid this effect, blank function can remain active until DDRAM is completed to avoid randomly ON or OFF pixels to appear on the LCD display.

9.3 Power ON recommended flow



10 Pad location

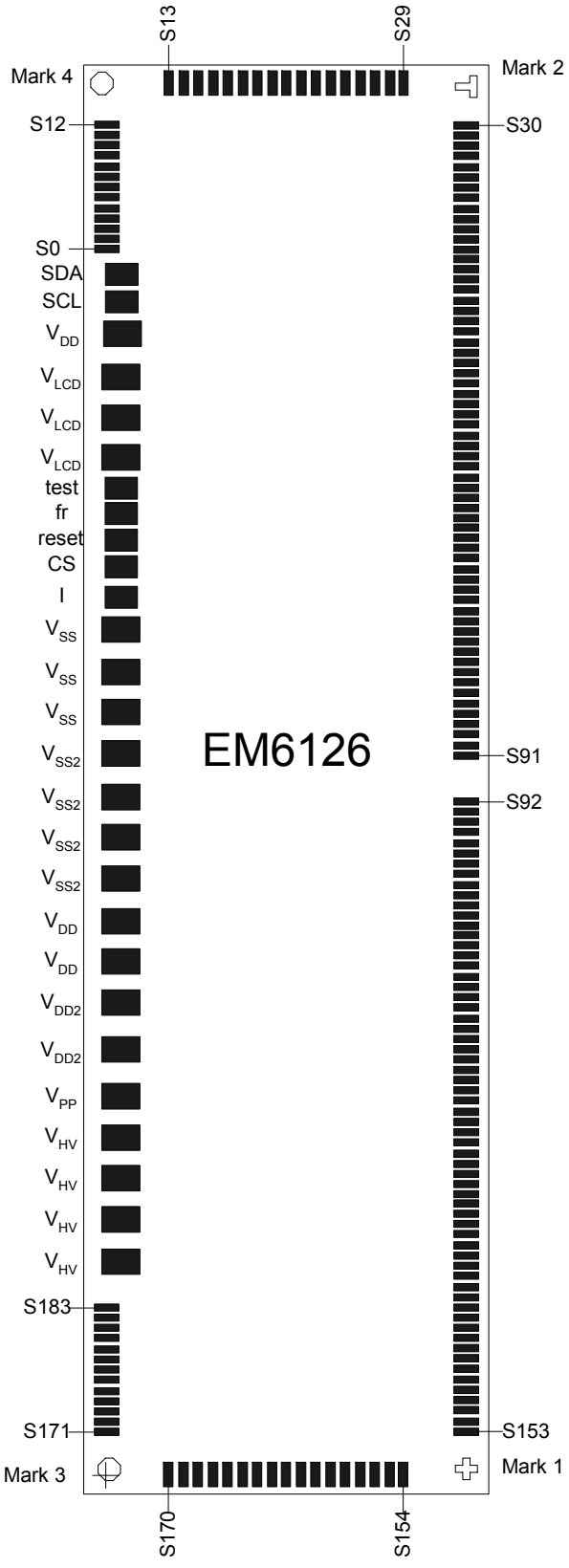
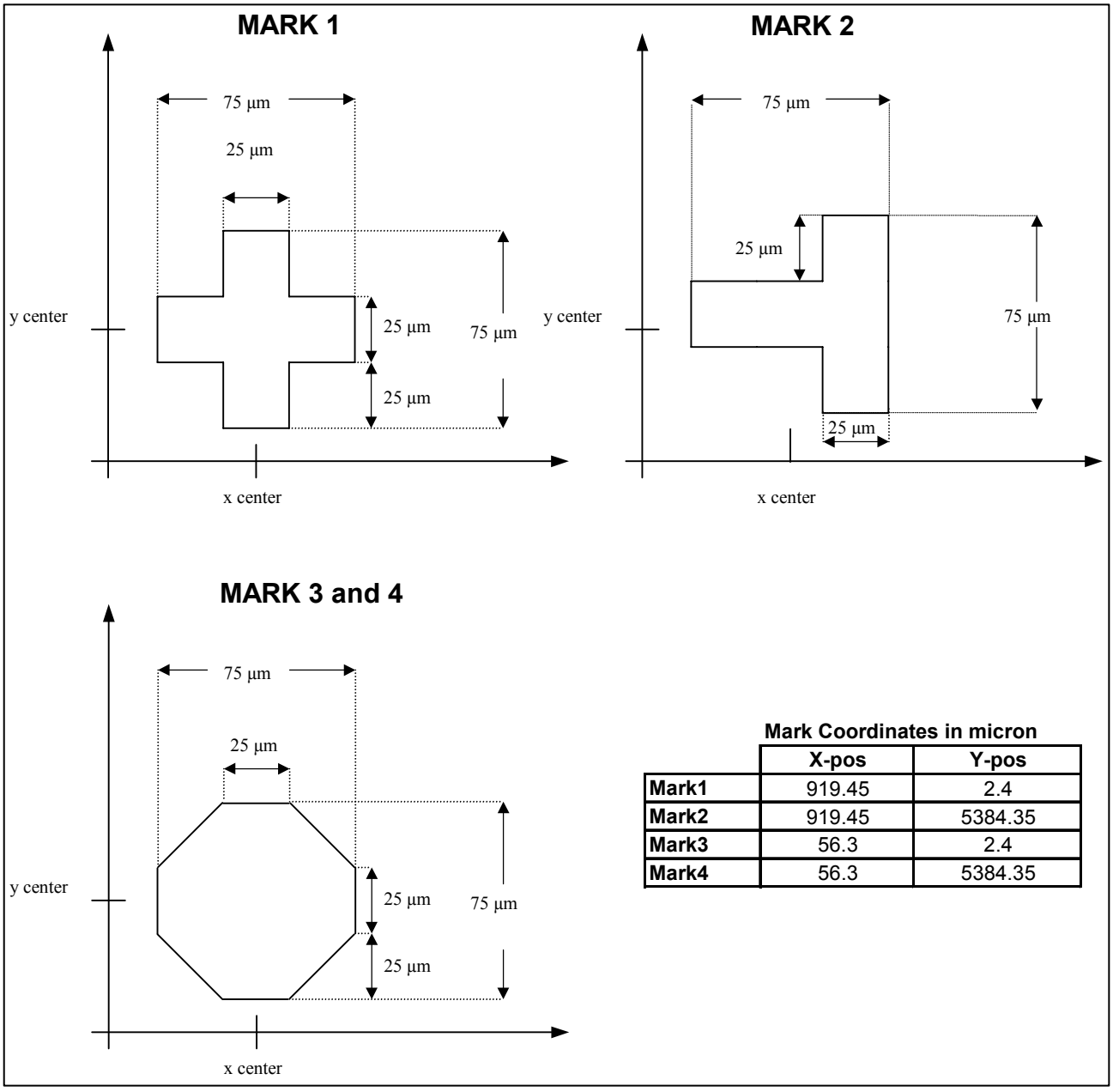


Figure 41

Mechanical Dimensions:

	Typical value	Unit
Minimum pad pitch	40	µm
Bump size pads from S[0] to S[183]	25×74×17.5	µm
Bump size interface pads	85×85×17.5	µm
Bump Size power supply pads	96×85×17.5	µm
Bump hardness	50	Vickers
Chip Size	5591 ×1180	µm



Mark Coordinates in micron

	X-pos	Y-pos
Mark1	919.45	2.4
Mark2	919.45	5384.35
Mark3	56.3	2.4
Mark4	56.3	5384.35

Pad	Serial number	x	y
S171	1	0	167.875
S172	2	0	207.875
S173	3	0	247.875
S174	4	0	287.875
S175	5	0	327.875
S176	6	0	367.875
S177	7	0	407.875
S178	8	0	447.875
S179	9	0	487.875
S180	10	0	527.875
S181	11	0	567.875
S182	12	0	607.875
S183	13	0	647.875
V_{HV}	14	38.5	815.125
V_{HV}	15	38.5	975.125
V_{HV}	16	38.5	1135.125
V_{HV}	17	38.5	1295.125
V_{PP}	18	38.5	1475.125
V_{DD2}	19	38.5	1655.125
V_{DD2}	20	38.5	1815.125
V_{DD}	21	38.5	1975.125
V_{DD}	22	38.5	2135.125
V_{SS2}	23	38.5	2295.125
V_{SS2}	24	38.5	2455.125
V_{SS2}	25	38.5	2615.125
V_{SS2}	26	38.5	2775.125
V_{SS}	27	38.5	2935.125
V_{SS}	28	38.5	3095.125
V_{SS}	29	38.5	3255.125
I	30	38.5	3377.125
CS	31	38.5	3477.125
reset	32	38.5	3577.125
fr	33	38.5	3677.125
test	34	38.5	3777.125
V_{LCD}	35	38.5	3925.125
V_{LCD}	36	38.5	4085.125
V_{LCD}	37	38.5	4245.125
V_{DD}	38	38.5	4415.125
SCL	39	38.5	4537.125
SDA	40	38.5	4637.125
S0	41	0	4738.875
S1	42	0	4778.875
S2	43	0	4818.875
S3	44	0	4858.875
S4	45	0	4898.875
S5	46	0	4938.875
S6	47	0	4978.875
S7	48	0	5018.875
S8	49	0	5058.875
S9	50	0	5098.875
S10	51	0	5138.875
S11	52	0	5178.875
S12	53	0	5218.875
S13	54	167.875	5386.75
S14	55	207.875	5386.75
S15	56	247.875	5386.75
S16	57	287.875	5386.75
S17	58	327.875	5386.75
S18	59	367.875	5386.75
S19	60	407.875	5386.75
S20	61	447.875	5386.75
S21	62	487.875	5386.75
S22	63	527.875	5386.75
S23	64	567.875	5386.75
S24	65	607.875	5386.75

Pad	Serial number	x	y
S25	66	647.875	5386.75
S26	67	687.875	5386.75
S27	68	727.875	5386.75
S28	69	767.875	5386.75
S29	70	807.875	5386.75
S30	71	975.75	5218.875
S31	72	975.75	5178.875
S32	73	975.75	5138.875
S33	74	975.75	5098.875
S34	75	975.75	5058.875
S35	76	975.75	5018.875
S36	77	975.75	4978.875
S37	78	975.75	4938.875
S38	79	975.75	4898.875
S39	80	975.75	4858.875
S40	81	975.75	4818.875
S41	82	975.75	4778.875
S42	83	975.75	4738.875
S43	84	975.75	4698.875
S44	85	975.75	4658.875
S45	86	975.75	4618.875
S46	87	975.75	4578.875
S47	88	975.75	4538.875
S48	89	975.75	4498.875
S49	90	975.75	4458.875
S50	91	975.75	4418.875
S51	92	975.75	4378.875
S52	93	975.75	4338.875
S53	94	975.75	4298.875
S54	95	975.75	4258.875
S55	96	975.75	4218.875
S56	97	975.75	4178.875
S57	98	975.75	4138.875
S58	99	975.75	4098.875
S59	100	975.75	4058.875
S60	101	975.75	4018.875
S61	102	975.75	3978.875
S62	103	975.75	3938.875
S63	104	975.75	3898.875
S64	105	975.75	3858.875
S65	106	975.75	3818.875
S66	107	975.75	3778.875
S67	108	975.75	3738.875
S68	109	975.75	3698.875
S69	110	975.75	3658.875
S70	111	975.75	3618.875
S71	112	975.75	3578.875
S72	113	975.75	3538.875
S73	114	975.75	3498.875
S74	115	975.75	3458.875
S75	116	975.75	3418.875
S76	117	975.75	3378.875
S77	118	975.75	3338.875
S78	119	975.75	3298.875
S79	120	975.75	3258.875
S80	121	975.75	3218.875
S81	122	975.75	3178.875
S82	123	975.75	3138.875
S83	124	975.75	3098.875
S84	125	975.75	3058.875
S85	126	975.75	3018.875
S86	127	975.75	2978.875
S87	128	975.75	2938.875
S88	129	975.75	2898.875
S89	130	975.75	2858.875

Pad	Serial number	x	y
S90	131	975.75	2818.875
S91	132	975.75	2778.875
S92	133	975.75	2607.875
S93	134	975.75	2567.875
S94	135	975.75	2527.875
S95	136	975.75	2487.875
S96	137	975.75	2447.875
S97	138	975.75	2407.875
S98	139	975.75	2367.875
S99	140	975.75	2327.875
S100	141	975.75	2287.875
S101	142	975.75	2247.875
S102	143	975.75	2207.875
S103	144	975.75	2167.875
S104	145	975.75	2127.875
S105	146	975.75	2087.875
S106	147	975.75	2047.875
S107	148	975.75	2007.875
S108	149	975.75	1967.875
S109	150	975.75	1927.875
S110	151	975.75	1887.875
S111	152	975.75	1847.875
S112	153	975.75	1807.875
S113	154	975.75	1767.875
S114	155	975.75	1727.875
S115	156	975.75	1687.875
S116	157	975.75	1647.875
S117	158	975.75	1607.875
S118	159	975.75	1567.875
S119	160	975.75	1527.875
S120	161	975.75	1487.875
S121	162	975.75	1447.875
S122	163	975.75	1407.875
S123	164	975.75	1367.875
S124	165	975.75	1327.875
S125	166	975.75	1287.875
S126	167	975.75	1247.875
S127	168	975.75	1207.875
S128	169	975.75	1167.875
S129	170	975.75	1127.875
S130	171	975.75	1087.875

Pad	Serial number	x	y
S131	172	975.75	1047.875
S132	173	975.75	1007.875
S133	174	975.75	967.875
S134	175	975.75	927.875
S135	176	975.75	887.875
S136	177	975.75	847.875
S137	178	975.75	807.875
S138	179	975.75	767.875
S139	180	975.75	727.875
S140	181	975.75	687.875
S141	182	975.75	647.875
S142	183	975.75	607.875
S143	184	975.75	567.875
S144	185	975.75	527.875
S145	186	975.75	487.875
S146	187	975.75	447.875
S147	188	975.75	407.875
S148	189	975.75	367.875
S149	190	975.75	327.875
S150	191	975.75	287.875
S151	192	975.75	247.875
S152	193	975.75	207.875
S153	194	975.75	167.875
S154	195	807.875	0
S155	196	767.875	0
S156	197	727.875	0
S157	198	687.875	0
S158	199	647.875	0
S159	200	607.875	0
S160	201	567.875	0
S161	202	527.875	0
S162	203	487.875	0
S163	204	447.875	0
S164	205	407.875	0
S165	206	367.875	0
S166	207	327.875	0
S167	208	287.875	0
S168	209	247.875	0
S169	210	207.875	0
S170	211	167.875	0

Table 15: Pad location.

11 Ordering Information

When ordering, please specify the complete part number and package.

Part Number	Die Form & Thickness	Bumping
EM6126WP15E	Waffle pack, 15mils	Gold Bumps

Other delivery form might be available upon request and for a minimum order quantity. Please contact EM sales.