

T2513BK – T2513NK TRIACS

25.0 A 200–800 V
50/50/50/75 mA

The T2513 series isolated TRIAC's are high performance glass passivated PNP devices. These parts are intended for high volume, very high current applications where high gate insensitivity is required.

U. L. Recognized, File Nr. E72763 (M)

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

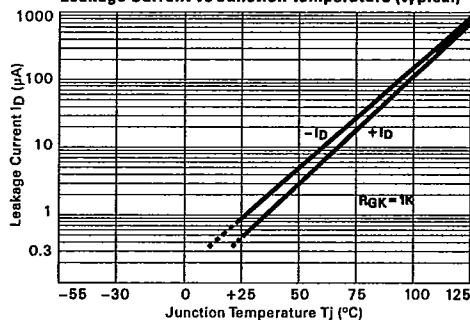
Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	T2513BK T2513DK T2513MK T2513NK	V_{DRM}	200 400 600 800		V	[$T_J = -40^\circ\text{C}$ to 125°C] [$R_{GK} = 1\text{K}\Omega$]
On-State Current		$I_{T(RMS)}$	25		A	
Nonrept. On-State Current		I_{TSM}	210		A	
Nonrept. On-State Current		I_{TSM}	190		A	
Fusing Current		I^2t	180		A^2s	$t = 10\text{ ms}$
Peak Gate Current		I_{GM}	4		A	10 μs max.
Peak Gate Dissipation		P_{GM}	10		W	10 μs max.
Gate Dissipation		$P_{G(AV)}$	1		W	20 ms max.
Isolation Voltage		V_{iso}	2500		VAC	
Operating Temperature		T_J	-40	125	$^\circ\text{C}$	
Storage Temperature		T_{stg}	-40	125	$^\circ\text{C}$	
Soldering Temperature		T_{slid}		250	$^\circ\text{C}$	1.6 mm from case, 10 s max.

Electrical Characteristics

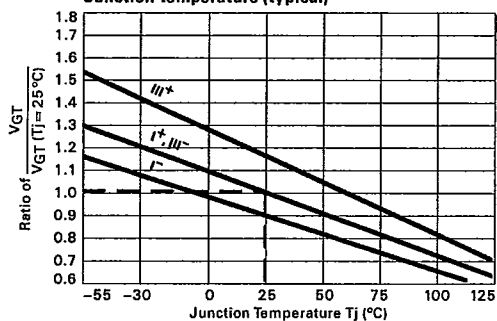
$T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	I_{DRM}		3	mA	$V_D = V_{DRM}$ $R_{GK} = 1\text{K}\Omega$ $T_J = 125^\circ\text{C}$
Off-State Leakage Current	I_{DRM}		10	μA	$V_D = V_{DRM}$ $R_{GK} = 1\text{K}\Omega$ $T_J = 25^\circ\text{C}$
On-State Voltage	V_T		1.4	V	at $I_T = 37.5\text{ A}$, $T_J = 25^\circ\text{C}$
On-State Threshold Voltage	$V_{T(TO)}$		0.85	V	$T_J = 125^\circ\text{C}$
On-State Slope Resistance	r_T		12	m Ω	$T_J = 125^\circ\text{C}$
Gate Trigger Current	$I_{GT\ I+}$ (1)		50	mA	$V_D = 12\text{ V}$
	$I_{GT\ I-}$ (2)		50	mA	$V_D = 12\text{ V}$
	$I_{GT\ III-}$ (3)		50	mA	$V_D = 12\text{ V}$
	$I_{GT\ III+}$ (4)		75	mA	$V_D = 12\text{ V}$
Gate Trigger Voltage	V_{GT}		2.5	V	$V_D = 12\text{ V}$ All Quadrants
Holding Current	I_H		75	mA	$R_{GK} = 1\text{K}\Omega$
Critical Rate of Voltage Rise	dv/dt	500		V/ μs	$V_D = .67 \times V_{DRM}$ $R_{GK} = 1\text{K}\Omega$ $T_J = 125^\circ\text{C}$
Critical Rate of Rise, Off-State	dv/dt_c	5		V/ μs	$I_T = 25\text{ A}$ $T_J = 125^\circ\text{C}$
Thermal Resistance junc. to case	$R_{\theta jc}$		1.5	K/W	

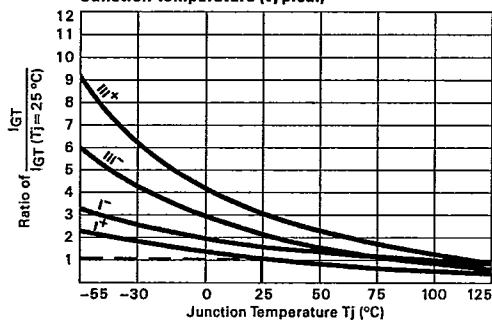
Leakage Current vs Junction Temperature (typical)



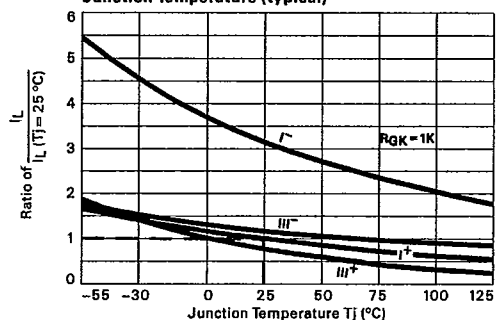
Normalized DC Gate Trigger Voltage vs Junction Temperature (typical)



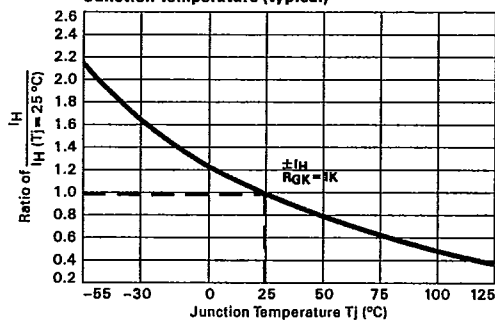
Normalized DC Gate Trigger Current vs Junction Temperature (typical)

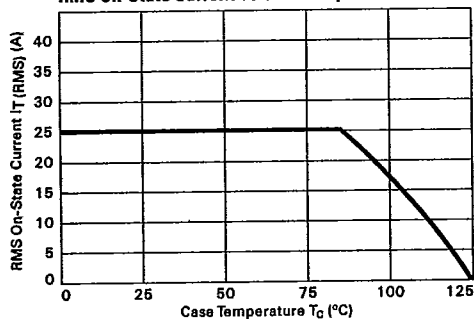
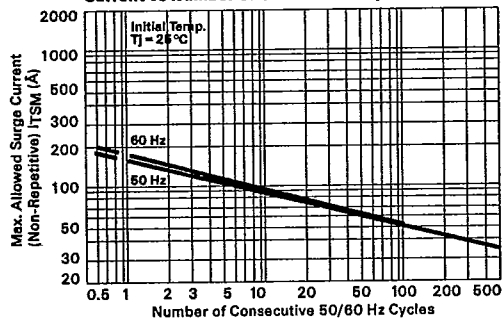
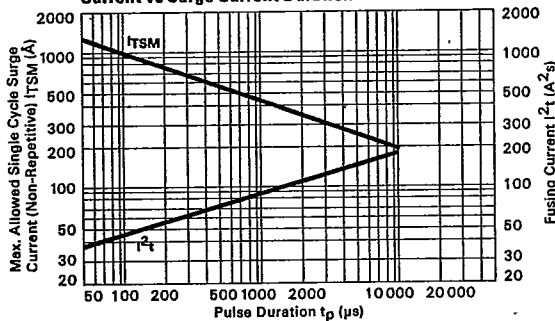
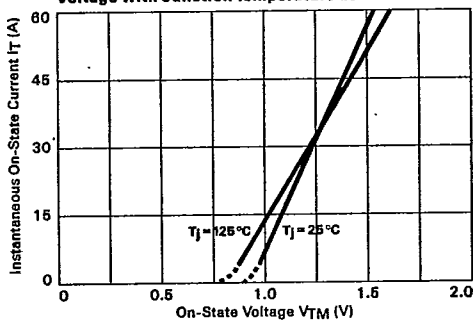
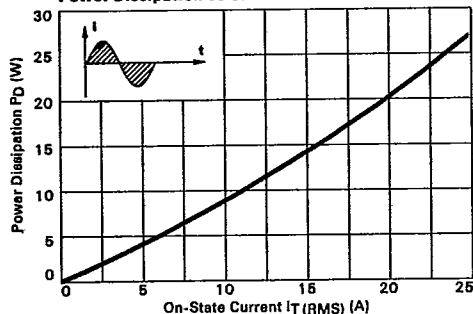


Normalized DC Latching Current vs Junction Temperature (typical)



Normalized DC Holding Current vs Junction Temperature (typical)



RMS On-State Current vs Case Temperature

Max. Allowed Multi Cycle Surge (On-State) Current vs Number of Consecutive Cycles

Max. Allowed Single Cycle Surge (On-State) Current vs Surge Current Duration

Instantaneous On-State Current vs On-State Voltage with Junction Temperature as Parameter

Power Dissipation vs On-State Current

Max. All. Power Dissip. vs Ambient Temp. with given Heatsink Thermal Resistances as Parameter
