Integrated Circuit Systems, Inc.

ICS840031I

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS840031I is an IEEE 1394b Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS840031I uses a 24.576MHz crystal to synthesize 98.304MHz. The ICS840031I has excellent phase jitter performance, from 12KHz – 20MHz integration range. The ICS840031I is packaged in a small 8-pin SOIC, making it ideal for use in systems with limited board space.

FEATURES

- (1) LVCMOS/LVTTL output
- Crystal oscillator interface designed for a 24.576MHz, 18pF parallel resonant crystal
- Output frequency: 98.304MHz (typical)
- VCO range: 490MHz to 640MHz
- RMS phase jitter @ 98.304MHz, using a 24.576MHz crystal (12KHz - 20MHz): 0.75ps (typical)
- RMS phase noise at 98.304MHz (typical)

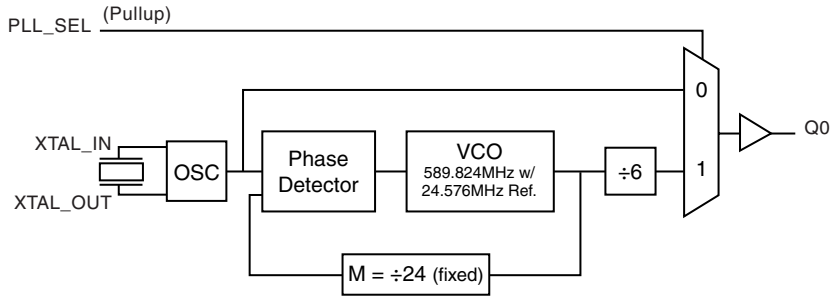
Offset	Noise Power
100Hz	-103.3 dBc/Hz
1KHz	-126.2 dBc/Hz
10KHz	-134.2 dBc/Hz
100KHz	-132.9 dBc/Hz

- 3.3V core/1.8V output operating supply
- Lead-Free fully RoHS compliant
- -40°C to 85°C ambient operating temperature

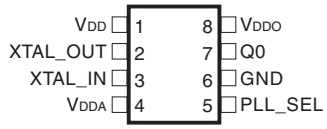
FREQUENCY TABLE

Inputs	Output Frequency (MHz)
Crystal Frequency (MHz)	
24.576	98.304

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS840031I

8-Lead SOIC

3.90mm x 4.90mm x 1.37mm package body

M Package

Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DD}	Power		Core supply pin.
2, 3	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
4	V_{DDA}	Power		Analog supply pin.
5	PLL_SEL	Input	Pullup	PLL select pin. LVCMOS/LVTTL interface levels.
6	GND	Power		Power supply ground.
7	Q0	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
8	V_{DDO}	Power		Output supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	$V_{DD} = V_{DDA} = 3.465V$, $V_{DDO} = 1.89V$		18		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{OUT}	Output Impedance			10		Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 1.8V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.71	1.8	1.89	V
I_{DD}	Power Supply Current				55	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				5	mA

TABLE 3B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 1.8V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	PLL_SEL	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	PLL_SEL	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1			1.5			V
V_{OL}	Output Low Voltage; NOTE 1					0.4	V

NOTE 1: Outputs terminated with 50Ω to $V_{DD}/2$. See Parameter Measurement Information Section, "3.3V/1.8V Output Load Test Circuit".

TABLE 4. CRYSTAL CHARACTERISTICS

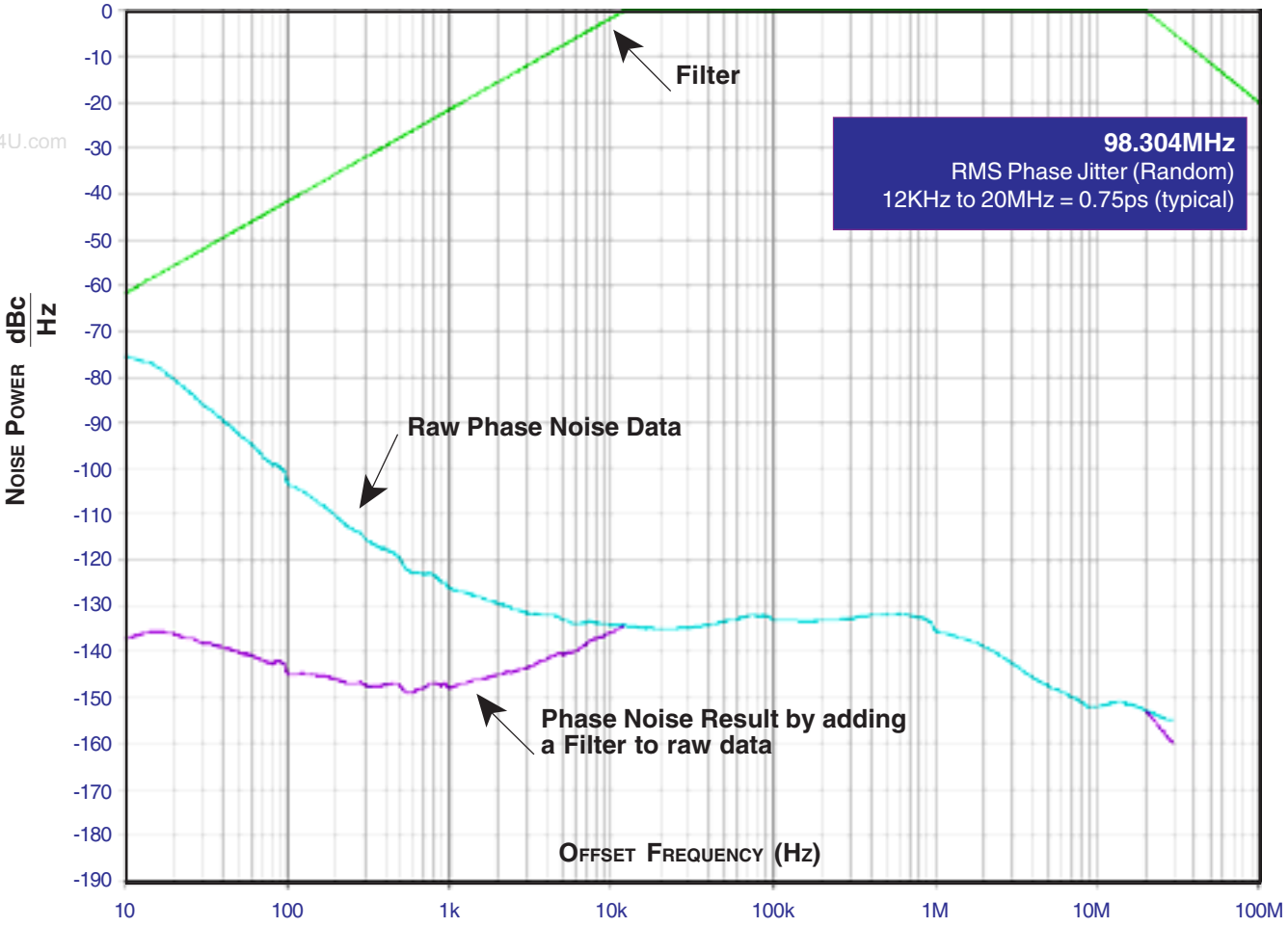
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency	F_SEL = 1	20.417	24.576	26.667	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 1.8V±5\%$, T_A = -40°C TO 85°C

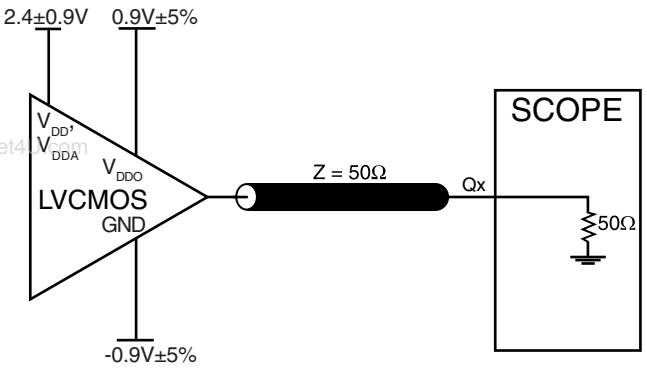
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		81.67	98.304	106.67	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	fOUT = 98.304MHz, (12KHz to 20MHz)		0.75		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	0.2		1	ns
odc	Output Duty Cycle		46		54	%

NOTE 1: Please refer to the Phase Noise Plot.

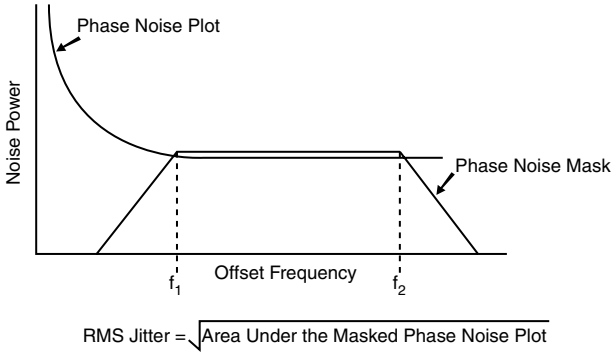
TYPICAL PHASE NOISE AT 98.304MHZ



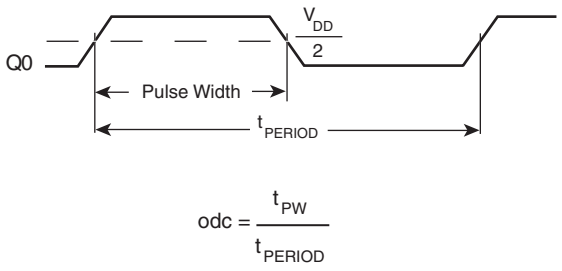
PARAMETER MEASUREMENT INFORMATION



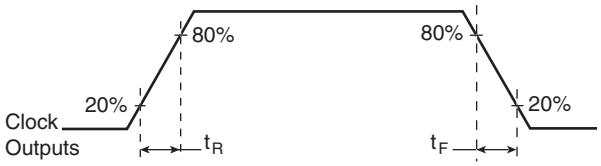
3.3V/1.8V OUTPUT LOAD AC TEST CIRCUIT



RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840031I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

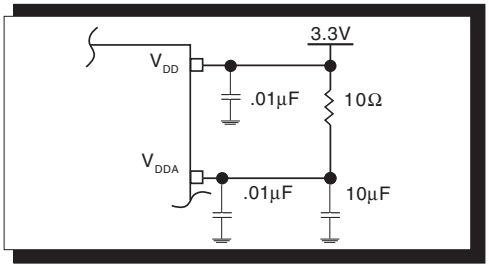


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840031I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 24.576MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

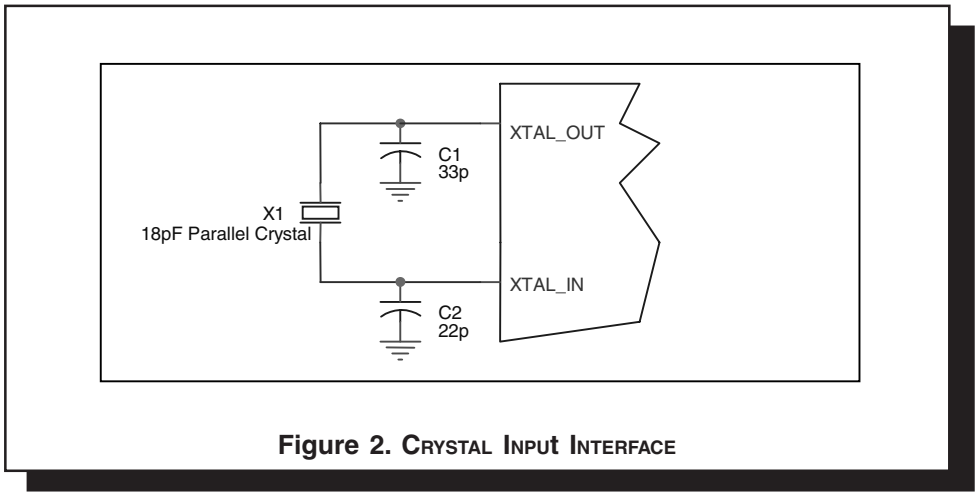


Figure 2. CRYSTAL INPUT INTERFACE

APPLICATION SCHEMATIC EXAMPLE

Figure 3 shows a schematic example of the ICS840031I. In this example, a series termination, one of LVCMOS termination approaches, is shown. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18pF parallel resonant crystal is used. The C1=22pF and C2=33pF are approximate values for frequency accuracy. The C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

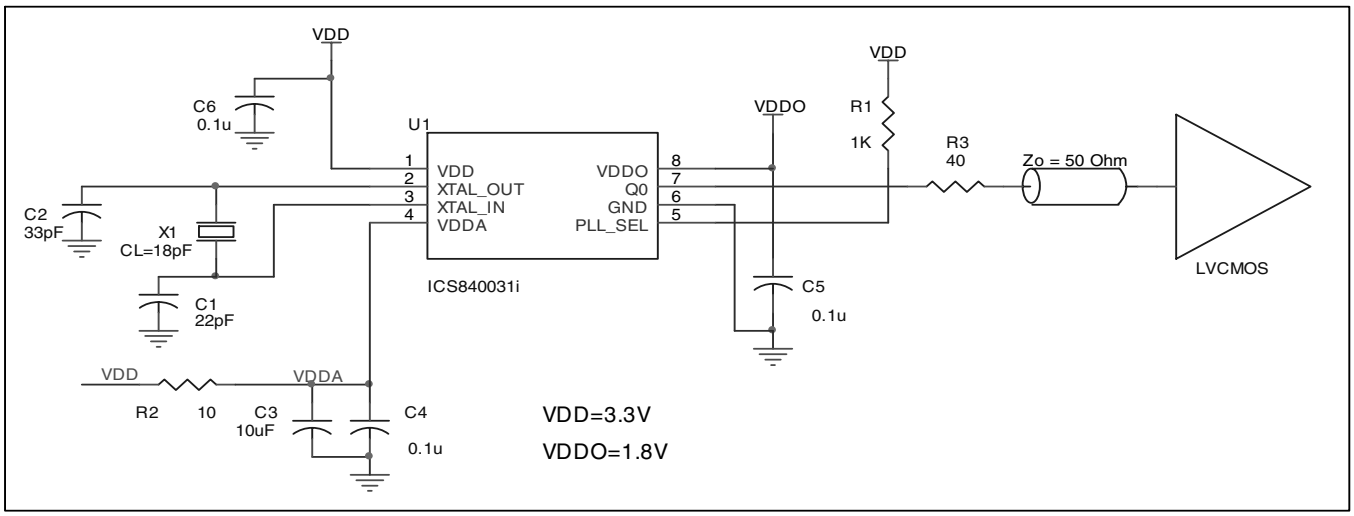


FIGURE 3. ICS840031I APPLICATION SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS840031I is: 1787

PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

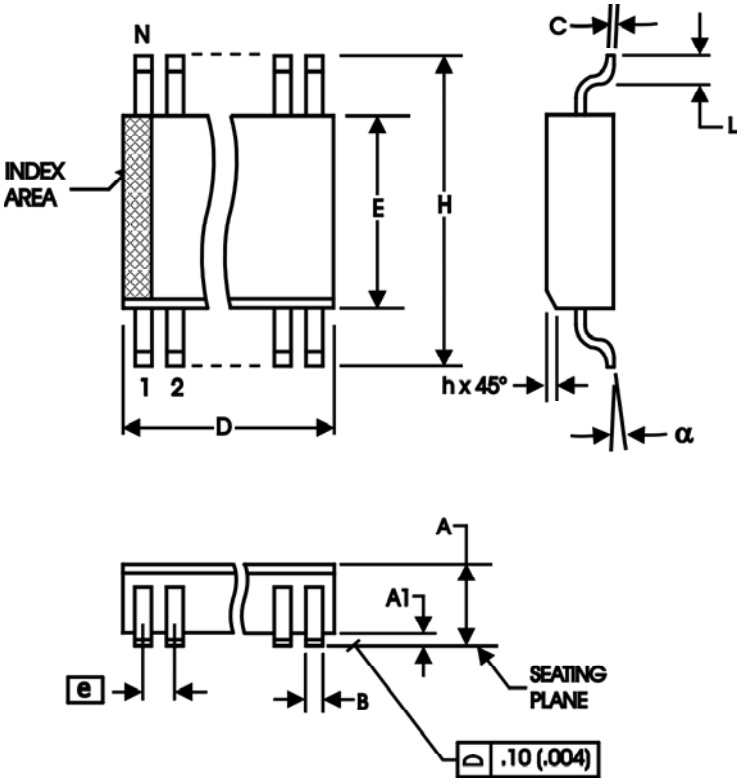


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS840031AMI	840031AI	8 lead SOIC	tube	-40°C to 85°C
ICS840031AMIT	840031AI	8 lead SOIC	2500 tape & reel	-40°C to 85°C
ICS840031AMILF	40031AIL	8 lead "Lead-Free" SOIC	tube	-40°C to 85°C
ICS840031AMILFT	40031AIL	8 lead "Lead-Free" SOIC	2500 tape & reel	-40°C to 85°C