



### GENERAL DESCRIPTION



The ICS84021 is a general purpose, Crystal-to-LVCMOS/LVTTTL High Frequency Synthesizer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS84021 has a selectable TEST\_CLK or crystal input. The VCO operates at a frequency range of 620MHz to 780MHz. The VCO frequency is programmed in steps equal to the value of the input reference or crystal frequency. The VCO and output frequency can be programmed using the serial or parallel interface to the configuration logic. The low phase noise characteristics of the ICS84021 make it an ideal clock source for Gigabit Ethernet, SONET, Fibre Channel 1 and 2, and Infiniband applications.

### FEATURES

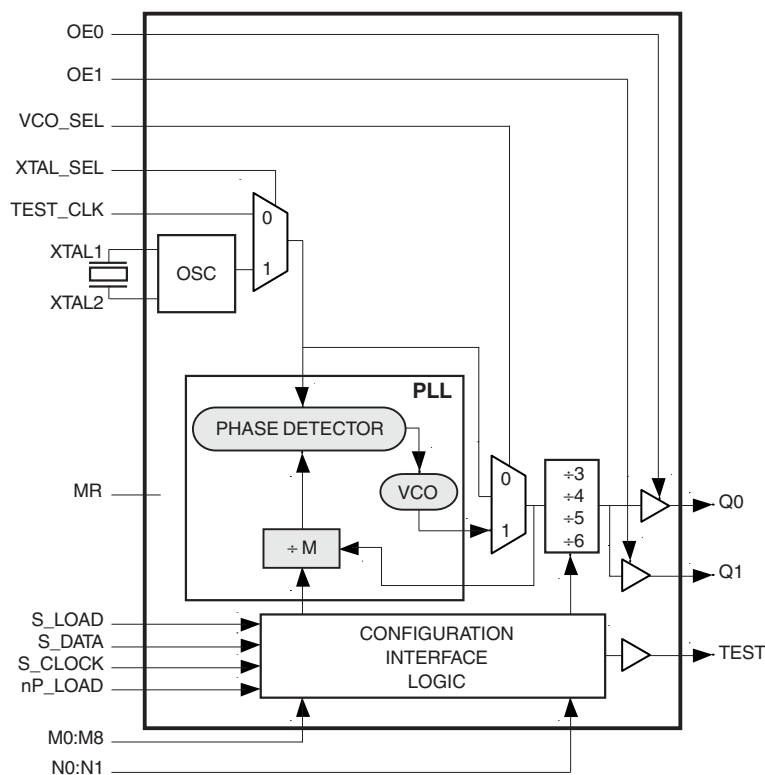
- 2 LVCMOS/LVTTTL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTTL TEST\_CLK
- Output frequency range: 103.3MHz to 260MHz
- Crystal input frequency range: 14MHz to 40MHz
- VCO range: 620MHz to 780MHz
- Parallel or serial interface for programming counter and output dividers
- RMS period jitter: 4.3ps (typical) ( $N \div 4$ ,  $V_{DDO} = 3.3V \pm 5\%$ )
- RMS phase jitter at 155.52MHz, using a 38.88MHz crystal (12KHz to 20MHz): 2.88ps (typical)

Phase noise: 155.52MHz

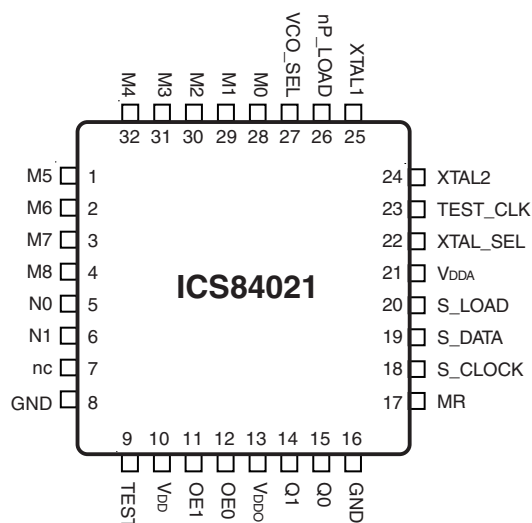
| Offset       | Noise Power   |
|--------------|---------------|
| 100Hz .....  | -93.7 dBc/Hz  |
| 1KHz .....   | -111.3 dBc/Hz |
| 10KHz .....  | -120.4 dBc/Hz |
| 100KHz ..... | -125.1 dBc/Hz |

- Full 3.3V or mixed 3.3V core/2.5V or 1.8V supply voltage
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

### BLOCK DIAGRAM



### PIN ASSIGNMENT



**32-Lead LQFP**  
7mm x 7mm x 1.4mm package body  
**Y Package**  
Top View



## FUNCTIONAL DESCRIPTION

**NOTE:** The functional description that follows describes operation using a 25MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The ICS84021 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is fed into the phase detector. A 25MHz crystal provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 620MHz to 780MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVCMOS output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS84021 support two input modes to program the M divider and N output divider. The two input operational modes are parallel and serial. Figure 1 shows the timing diagram for each mode. In parallel mode, the nP\_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 and N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP\_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP\_LOAD or until a serial event occurs. As a result, the M and N bits can be hardwired to set the

M divider and N output divider to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:  $f_{VCO} = f_{xtal} \times M$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as  $25 \leq M \leq 31$ . The frequency out is defined as follows:  $F_{OUT} = \frac{f_{VCO}}{N} = f_{xtal} \times \frac{M}{N}$

Serial operation occurs when nP\_LOAD is HIGH and S\_LOAD is LOW. The shift register is loaded by sampling the S\_DATA bits with the rising edge of S\_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S\_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S\_LOAD. If S\_LOAD is held HIGH, data at the S\_DATA input is passed directly to the M divider and N output divider on each rising edge of S\_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

| T1 | T0 | TEST Output                  |
|----|----|------------------------------|
| 0  | 0  | LOW                          |
| 0  | 1  | S_DATA, Shift Register Input |
| 1  | 0  | Output of M divider          |
| 1  | 1  | CMOS Fout                    |

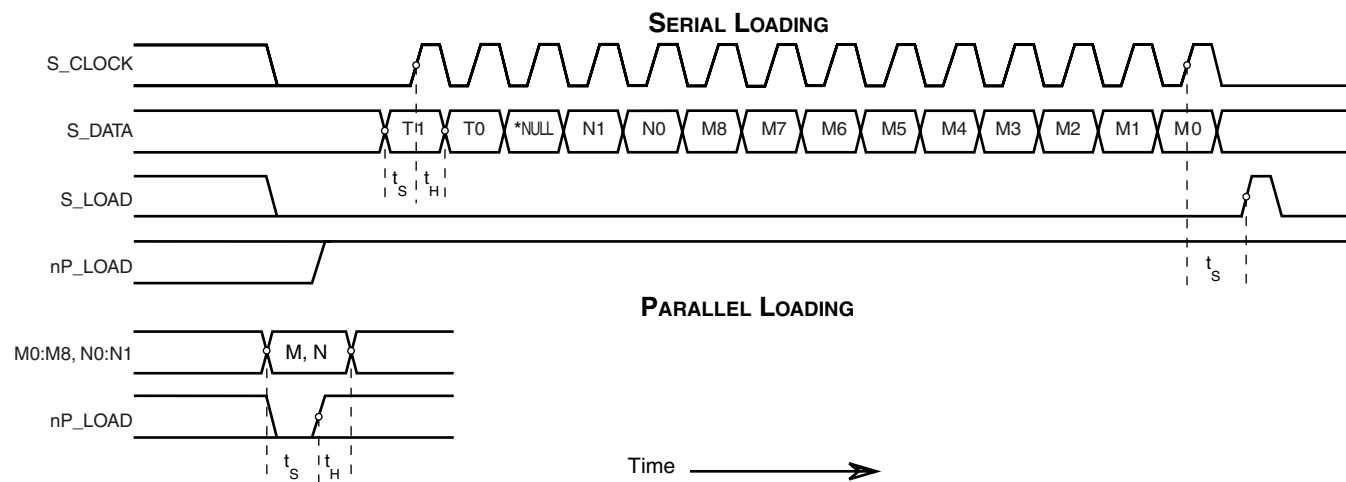


FIGURE 1. PARALLEL & SERIAL LOAD OPERATIONS

**\*NOTE:** The NULL timing slot must be observed.



**TABLE 1. PIN DESCRIPTIONS**

| Number                            | Name                                 | Type   |          | Description                                                                                                                                                                                                                                                               |
|-----------------------------------|--------------------------------------|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                                 | M5                                   | Input  | Pullup   | M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS / LVTTTL interface levels.                                                                                                                                                              |
| 2, 3, 4,<br>28, 29,<br>30, 31, 32 | M6, M7, M8,<br>M0, M1,<br>M2, M3, M4 | Input  | Pulldown |                                                                                                                                                                                                                                                                           |
| 5, 6                              | N0, N1                               | Input  | Pulldown |                                                                                                                                                                                                                                                                           |
| 7                                 | nc                                   | Unused |          |                                                                                                                                                                                                                                                                           |
| 8, 16                             | GND                                  | Power  |          | Power supply ground.                                                                                                                                                                                                                                                      |
| 9                                 | TEST                                 | Output |          | Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS / LVTTTL interface levels.                                                                                                                                        |
| 10                                | V <sub>DD</sub>                      | Power  |          | Core supply pin.                                                                                                                                                                                                                                                          |
| 11, 12                            | OE1, OE0                             | Input  | Pullup   | Output enable. When logic HIGH, the outputs are enabled (default). When logic LOW, the outputs are in Tri-State. See Table 3E, OE Function Table. LVCMOS / LVTTTL interface levels.                                                                                       |
| 13                                | V <sub>DDO</sub>                     | Power  |          | Output supply pin.                                                                                                                                                                                                                                                        |
| 14, 15                            | Q0, Q1                               | Output |          | Clock outputs. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                          |
| 17                                | MR                                   | Input  | Pulldown | Active High Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not effect loaded M, N, and T values. LVCMOS / LVTTTL interface levels. |
| 18                                | S_CLOCK                              | Input  | Pulldown | Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS / LVTTTL interface levels.                                                                                                                                    |
| 19                                | S_DATA                               | Input  | Pulldown | Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS / LVTTTL interface levels.                                                                                                                                                                |
| 20                                | S_LOAD                               | Input  | Pulldown | Controls transition of data from shift register into the dividers. LVCMOS / LVTTTL interface levels.                                                                                                                                                                      |
| 21                                | V <sub>DDA</sub>                     | Power  |          | Analog supply pin.                                                                                                                                                                                                                                                        |
| 22                                | XTAL_SEL                             | Input  | Pullup   | Selects between crystal or test inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects TEST_CLK when LOW. LVCMOS / LVTTTL interface levels                                                                                                            |
| 23                                | TEST_CLK                             | Input  | Pulldown | Test clock input. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                       |
| 24, 25                            | XTAL2, XTAL1                         | Input  |          | Crystal oscillator interface. XTAL1 is the input. XTAL2 is the output.                                                                                                                                                                                                    |
| 26                                | nP_LOAD                              | Input  | Pulldown | Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divider value. LVCMOS / LVTTTL interface levels.                                                                                    |
| 27                                | VCO_SEL                              | Input  | Pullup   | Determines whether synthesizer is in PLL or bypass mode. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.



**TABLE 2. PIN CHARACTERISTICS**

| Symbol         | Parameter                                  | Test Conditions                              | Minimum | Typical | Maximum | Units      |
|----------------|--------------------------------------------|----------------------------------------------|---------|---------|---------|------------|
| $C_{IN}$       | Input Capacitance                          |                                              |         | 4       |         | pF         |
| $C_{PD}$       | Power Dissipation Capacitance (per output) | $V_{DD}, V_{DDA}, V_{DDO} = 3.465V$          |         | 15      |         | pF         |
|                |                                            | $V_{DD}, V_{DDA} = 3.465V, V_{DDO} = 2.625V$ |         | 15      |         | pF         |
|                |                                            | $V_{DD}, V_{DDA} = 3.465V, V_{DDO} = 1.89V$  |         | 20      |         | pF         |
| $R_{PULLUP}$   | Input Pullup Resistor                      |                                              |         | 51      |         | K $\Omega$ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor                    |                                              |         | 51      |         | K $\Omega$ |

**TABLE 3A. PARALLEL AND SERIAL MODE FUNCTION TABLE**

| Inputs |         |      |      |        |         |        | Conditions                                                                                                        |
|--------|---------|------|------|--------|---------|--------|-------------------------------------------------------------------------------------------------------------------|
| MR     | nP_LOAD | M    | N    | S_LOAD | S_CLOCK | S_DATA |                                                                                                                   |
| H      | X       | X    | X    | X      | X       | X      | Reset. Forces outputs LOW.                                                                                        |
| L      | L       | Data | Data | X      | X       | X      | Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.             |
| L      | ↑       | Data | Data | L      | X       | X      | Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs. |
| L      | H       | X    | X    | L      | ↑       | Data   | Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.                   |
| L      | H       | X    | X    | ↑      | L       | Data   | Contents of the shift register are passed to the M divider and N output divider.                                  |
| L      | H       | X    | X    | ↓      | L       | Data   | M divider and N output divider values are latched.                                                                |
| L      | H       | X    | X    | L      | X       | X      | Parallel or serial input do not affect shift registers.                                                           |
| L      | H       | X    | X    | H      | ↑       | Data   | S_DATA passed directly to M divider as it is clocked.                                                             |

NOTE: L = LOW  
H = HIGH  
X = Don't care  
↑ = Rising edge transition  
↓ = Falling edge transition

**TABLE 3B. PROGRAMMABLE VCO FREQUENCY FUNCTION TABLE (NOTE 1)**

| VCO Frequency (MHz) | M Divide | 256 | 128 | 64 | 32 | 16 | 8  | 4  | 2  | 1  |
|---------------------|----------|-----|-----|----|----|----|----|----|----|----|
|                     |          | M8  | M7  | M6 | M5 | M4 | M3 | M2 | M1 | M0 |
| 625                 | 25       | 0   | 0   | 0  | 0  | 1  | 1  | 0  | 0  | 1  |
| •                   | •        | •   | •   | •  | •  | •  | •  | •  | •  | •  |
| 700                 | 28       | 0   | 0   | 0  | 0  | 1  | 1  | 1  | 0  | 0  |
| •                   | •        | •   | •   | •  | •  | •  | •  | •  | •  | •  |
| 775                 | 31       | 0   | 0   | 0  | 0  | 1  | 1  | 1  | 1  | 1  |

NOTE 1: These M divide values and the resulting frequencies correspond to crystal or TEST\_CLK input frequency of 25MHz.



**TABLE 3C. PROGRAMMABLE OUTPUT DIVIDER FUNCTION TABLE (PLL ENABLED)**

| Inputs |    | N Divider Value | Output Frequency (MHz) |         |
|--------|----|-----------------|------------------------|---------|
| N1     | N0 |                 | Minimum                | Maximum |
| 0      | 0  | 3               | 206.7                  | 260     |
| 0      | 1  | 4               | 155                    | 195     |
| 1      | 0  | 5               | 124                    | 156     |
| 1      | 1  | 6               | 103.3                  | 130     |

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**TABLE 3D. COMMONLY USED CONFIGURATION FUNCTION TABLE**

| Input         |                 |                 | Output Frequency (MHz) |
|---------------|-----------------|-----------------|------------------------|
| Crystal (MHz) | M Divider Value | N Divider Value |                        |
| 19.44         | 32              | 4               | 155.52                 |
| 19.53125      | 32              | 4               | 156.25                 |
| 25            | 25              | 4               | 156.25                 |
| 25            | 25              | 5               | 125                    |
| 25.50         | 25              | 3               | 212.50                 |
| 25.50         | 25              | 4               | 159.375                |
| 25.50         | 25              | 6               | 106.25                 |
| 38.88         | 16              | 4               | 155.52                 |

**TABLE 3E. OUTPUT ENABLE & CLOCK ENABLE FUNCTION TABLE**

| Control Inputs |     | Output  |         |
|----------------|-----|---------|---------|
| OE0            | OE1 | Q0      | Q1      |
| 0              | 0   | Hi-Z    | Hi-Z    |
| 0              | 1   | Hi-Z    | Enabled |
| 1              | 0   | Enabled | Hi-Z    |
| 1              | 1   | Enabled | Enabled |



#### ABSOLUTE MAXIMUM RATINGS

|                                          |                           |
|------------------------------------------|---------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                      |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$  |
| Outputs, $V_O$                           | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W (0 lfpm)         |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C            |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

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**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD}=V_{DDA}=3.3V\pm5\%$ ,  $V_{DDO}=3.3V\pm5\%$ ,  $2.5V\pm5\%$  OR  $1.8V\pm5\%$ ,  $T_A=0^\circ\text{C}$  TO  $70^\circ\text{C}$**

| Symbol    | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDA}$ | Analog Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
|           |                       |                 | 2.375   | 2.5     | 2.625   | V     |
|           |                       |                 | 1.71    | 1.8     | 1.89    | V     |
| $I_{DD}$  | Power Supply Current  |                 |         |         | 140     | mA    |
| $I_{DDA}$ | Analog Supply Current |                 |         |         | 25      | mA    |
| $I_{DDO}$ | Output Supply Current |                 |         |         | 5       | mA    |



**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD}=V_{DDA}=3.3V\pm5\%$ ,**

$V_{DDO}=3.3V\pm5\%$ ,  $2.5V\pm5\%$  OR  $1.8V\pm5\%$ ,  $T_A=0^\circ\text{C}$  TO  $70^\circ\text{C}$

| Symbol   | Parameter                   |                                                                                 | Test Conditions                      | Minimum         | Typical | Maximum        | Units         |
|----------|-----------------------------|---------------------------------------------------------------------------------|--------------------------------------|-----------------|---------|----------------|---------------|
| $V_{IH}$ | Input High Voltage          | VCO_SEL, XTAL_SEL, MR, S_LOAD, nP_LOAD, S_DATA, S_CLOCK, OE0, OE1, N0:N1, M0:M8 |                                      | 2               |         | $V_{DD} + 0.3$ | V             |
|          |                             | TEST_CLK                                                                        |                                      | 2               |         | $V_{DD} + 0.3$ | V             |
| $V_{IL}$ | Input Low Voltage           | VCO_SEL, XTAL_SEL, MR, S_LOAD, nP_LOAD, S_DATA, S_CLOCK, OE0, OE1, N0:N1, M0:M8 |                                      | -0.3            |         | 0.8            | V             |
|          |                             | TEST_CLK                                                                        |                                      | -0.3            |         | 1.3            | V             |
| $I_{IH}$ | Input High Current          | M0-M4, M6-M8, N0, N1, MR, S_CLOCK, TEST_CLK, S_DATA, S_LOAD, nP_LOAD            | $V_{DD} = V_{IN} = 3.465V$           |                 |         | 150            | $\mu\text{A}$ |
|          |                             | M5, OE0, OE1, XTAL_SEL, VCO_SEL                                                 | $V_{DD} = V_{IN} = 3.465V$           |                 |         | 5              | $\mu\text{A}$ |
| $I_{IL}$ | Input Low Current           | M0-M4, M6-M8, N0, N1, MR, S_CLOCK, TEST_CLK, S_DATA, S_LOAD, nP_LOAD            | $V_{DD} = 3.465V$ ,<br>$V_{IN} = 0V$ | -5              |         |                | $\mu\text{A}$ |
|          |                             | M5, OE0, OE1, XTAL_SEL, VCO_SEL                                                 | $V_{DD} = 3.465V$ ,<br>$V_{IN} = 0V$ | -150            |         |                | $\mu\text{A}$ |
| $V_{OH}$ | Output High Voltage; NOTE 1 |                                                                                 | $V_{DDO} = 3.3V \pm 5\%$             | 2.6             |         |                | V             |
|          |                             |                                                                                 | $V_{DDO} = 2.5V \pm 5\%$             | 1.8             |         |                | V             |
|          |                             |                                                                                 | $V_{DDO} = 1.8V \pm 5\%$             | $V_{DDO} - 0.3$ |         |                | V             |
| $V_{OL}$ | Output Low Voltage; NOTE 1  |                                                                                 | $V_{DDO} = 3.3V \pm 5\%$             |                 |         | 0.5            | V             |
|          |                             |                                                                                 | $V_{DDO} = 2.5V \pm 5\%$             |                 |         | 0.5            | V             |
|          |                             |                                                                                 | $V_{DDO} = 1.8V \pm 5\%$             |                 |         | 0.4            | V             |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See *Parameter Measurement Section*, "Load Test Circuit Diagrams".

**TABLE 5. INPUT FREQUENCY CHARACTERISTICS,  $V_{DD}=V_{DDA}=V_{DDO}=3.3V\pm5\%$ ,  $T_A=0^\circ\text{C}$  TO  $70^\circ\text{C}$**

| Symbol   | Parameter       |                      | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-----------------|----------------------|-----------------|---------|---------|---------|-------|
| $f_{IN}$ | Input Frequency | TEST_CLK; NOTE 1     |                 | 14      |         | 40      | MHz   |
|          |                 | XTAL1, XTAL2; NOTE 1 |                 | 14      |         | 40      | MHz   |
|          |                 | S_CLOCK              |                 |         |         | 50      | MHz   |

NOTE 1: For the input crystal and TEST\_CLK frequency range, the M value must be set for the VCO to operate within the 620MHz to 780MHz range. Using the minimum input frequency of 14MHz, valid values of M are  $45 \leq M \leq 55$ .

Using the maximum frequency of 40MHz, valid values of M are  $16 \leq M \leq 19$ .

**TABLE 6. CRYSTAL CHARACTERISTICS**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 | 14          |         | 40      | MHz      |
| Equivalent Series Resistance (ESR) |                 |             |         | 50      | $\Omega$ |
| Shunt Capacitance ( $C_0$ )        |                 |             |         | 7       | pF       |



**TABLE 7A. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol         | Parameter                  | Test Conditions   | Minimum | Typical | Maximum | Units |
|----------------|----------------------------|-------------------|---------|---------|---------|-------|
| $F_{OUT}$      | Output Frequency           |                   | 103.3   |         | 260     | MHz   |
| $f_{jit(per)}$ | Period Jitter, RMS; NOTE 1 | $N \div 3$        |         | 7.5     | 10      | ps    |
|                |                            | $N \div 4$        |         | 4.3     | 7       | ps    |
|                |                            | $N \div 5$        |         | 4.1     | 6       | ps    |
|                |                            | $N \div 6$        |         | 12.9    | 16      | ps    |
| $t_{sk(o)}$    | Output Skew; NOTE 2, 3     |                   |         |         | 100     | ps    |
| $t_R / t_F$    | Output Rise/Fall Time      | 20% to 80%        | 300     |         | 800     | ps    |
| $t_S$          | Setup Time                 | M, N to nP_LOAD   | 5       |         |         | ns    |
|                |                            | S_DATA to S_CLOCK | 5       |         |         | ns    |
|                |                            | S_CLOCK to S_LOAD | 5       |         |         | ns    |
| $t_H$          | Hold Time                  | M, N to nP_LOAD   | 5       |         |         | ns    |
|                |                            | S_DATA to S_CLOCK | 5       |         |         | ns    |
|                |                            | S_CLOCK to S_LOAD | 5       |         |         | ns    |
| odc            | Output Duty Cycle          |                   | 45      |         | 55      | %     |
| $t_{LOCK}$     | PLL Lock Time              |                   |         |         | 1       | ms    |

See Parameter Measurement Information section.

NOTE 1: Jitter performance using XTAL inputs.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 7B. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol         | Parameter                  | Test Conditions   | Minimum | Typical | Maximum | Units |
|----------------|----------------------------|-------------------|---------|---------|---------|-------|
| $F_{OUT}$      | Output Frequency           |                   | 103.3   |         | 260     | MHz   |
| $f_{jit(per)}$ | Period Jitter, RMS; NOTE 1 | $N \div 3$        |         | 6.4     | 8       | ps    |
|                |                            | $N \div 4$        |         | 4.3     | 8       | ps    |
|                |                            | $N \div 5$        |         | 4.2     | 7       | ps    |
|                |                            | $N \div 6$        |         | 9       | 12      | ps    |
| $t_{sk(o)}$    | Output Skew; NOTE 2, 3     |                   |         |         | 90      | ps    |
| $t_R / t_F$    | Output Rise/Fall Time      | 20% to 80%        | 300     |         | 800     | ps    |
| $t_S$          | Setup Time                 | M, N to nP_LOAD   | 5       |         |         | ns    |
|                |                            | S_DATA to S_CLOCK | 5       |         |         | ns    |
|                |                            | S_CLOCK to S_LOAD | 5       |         |         | ns    |
| $t_H$          | Hold Time                  | M, N to nP_LOAD   | 5       |         |         | ns    |
|                |                            | S_DATA to S_CLOCK | 5       |         |         | ns    |
|                |                            | S_CLOCK to S_LOAD | 5       |         |         | ns    |
| odc            | Output Duty Cycle          |                   | 45      |         | 55      | %     |
| $t_{LOCK}$     | PLL Lock Time              |                   |         |         | 1       | ms    |

See Parameter Measurement Information section.

NOTE 1: Jitter performance using XTAL inputs.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.



**TABLE 7C. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol         | Parameter                  | Test Conditions   | Minimum | Typical | Maximum | Units |
|----------------|----------------------------|-------------------|---------|---------|---------|-------|
| $F_{OUT}$      | Output Frequency           |                   | 103.3   |         | 260     | MHz   |
| $f_{jit(per)}$ | Period Jitter, RMS; NOTE 1 | $N \div 3$        |         | 6.8     | 8       | ps    |
|                |                            | $N \div 4$        |         | 4.5     | 8       | ps    |
|                |                            | $N \div 5$        |         | 4.2     | 6       | ps    |
|                |                            | $N \div 6$        |         | 8.5     | 10      | ps    |
| $t_{sk(o)}$    | Output Skew; NOTE 2, 3     |                   |         |         | 120     | ps    |
| $t_R / t_F$    | Output Rise/Fall Time      | 20% to 80%        | 300     |         | 800     | ps    |
| $t_S$          | Setup Time                 | M, N to nP_LOAD   | 5       |         |         | ns    |
|                |                            | S_DATA to S_CLOCK | 5       |         |         | ns    |
|                |                            | S_CLOCK to S_LOAD | 5       |         |         | ns    |
| $t_H$          | Hold Time                  | M, N to nP_LOAD   | 5       |         |         | ns    |
|                |                            | S_DATA to S_CLOCK | 5       |         |         | ns    |
|                |                            | S_CLOCK to S_LOAD | 5       |         |         | ns    |
| odc            | Output Duty Cycle          |                   | 42      |         | 58      | %     |
| $t_{LOCK}$     | PLL Lock Time              |                   |         |         | 1       | ms    |

See Parameter Measurement Information section.

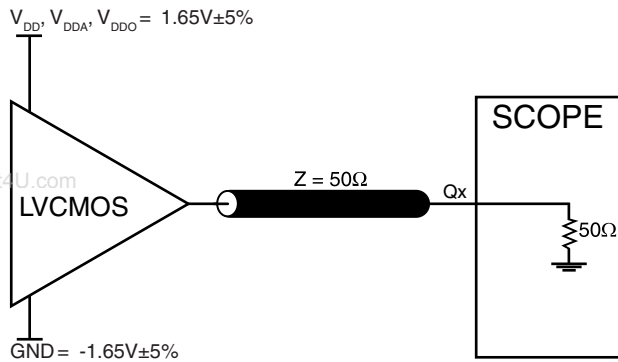
NOTE 1: Jitter performance using XTAL inputs.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

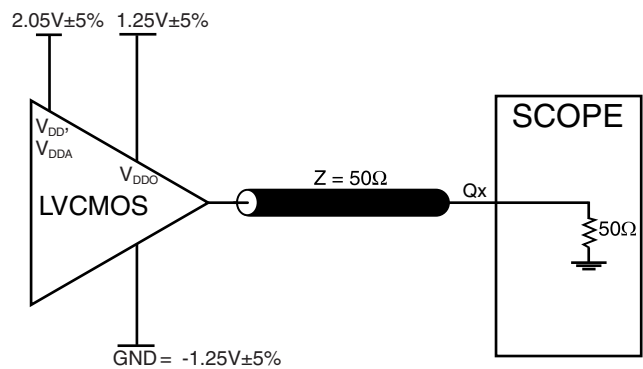
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.



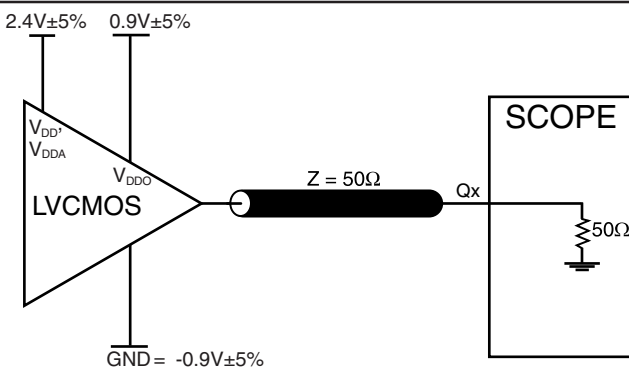
## PARAMETER MEASUREMENT INFORMATION



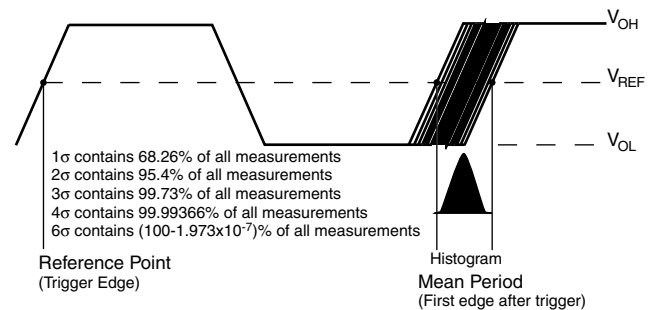
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



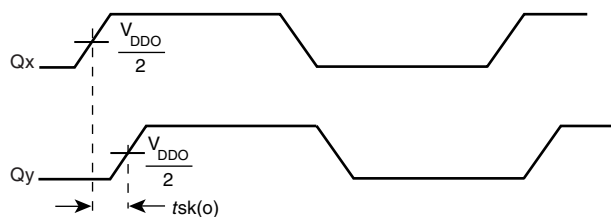
**3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT**



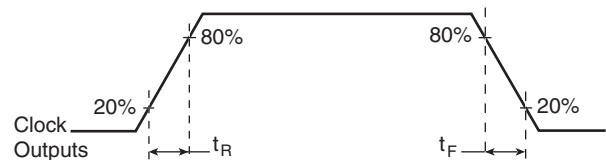
**3.3V/1.8V OUTPUT LOAD AC TEST CIRCUIT**



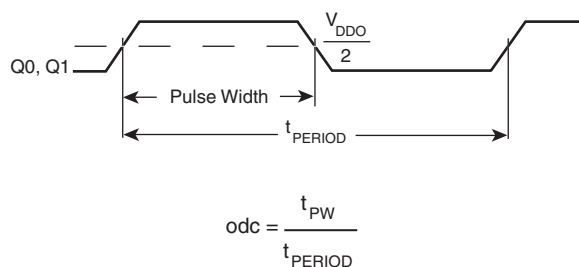
**PERIOD JITTER**



**OUTPUT SKEW**



**OUTPUT RISE/FALL TIME**



**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS84021 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$ , and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a  $24\Omega$  resistor along with a  $10\mu F$  and a  $.01\mu F$  bypass capacitor should be connected to each  $V_{DDA}$  pin.

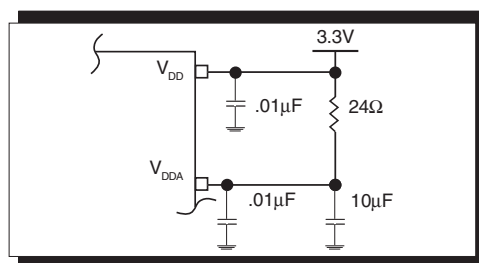


FIGURE 2. POWER SUPPLY FILTERING

### CRYSTAL INPUT INTERFACE

The ICS84021 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 3* below were determined using a 25MHz, 18pF

parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

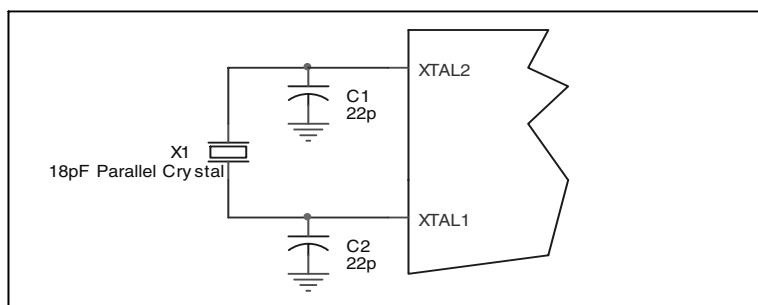


Figure 3. CRYSTAL INPUT INTERFACE



## RELIABILITY INFORMATION

TABLE 8.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 32 LEAD LQFP

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |          |          |          |
|----------------------------------------------------|----------|----------|----------|
|                                                    | 0        | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards       | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 47.9°C/W | 42.1°C/W | 39.4°C/W |

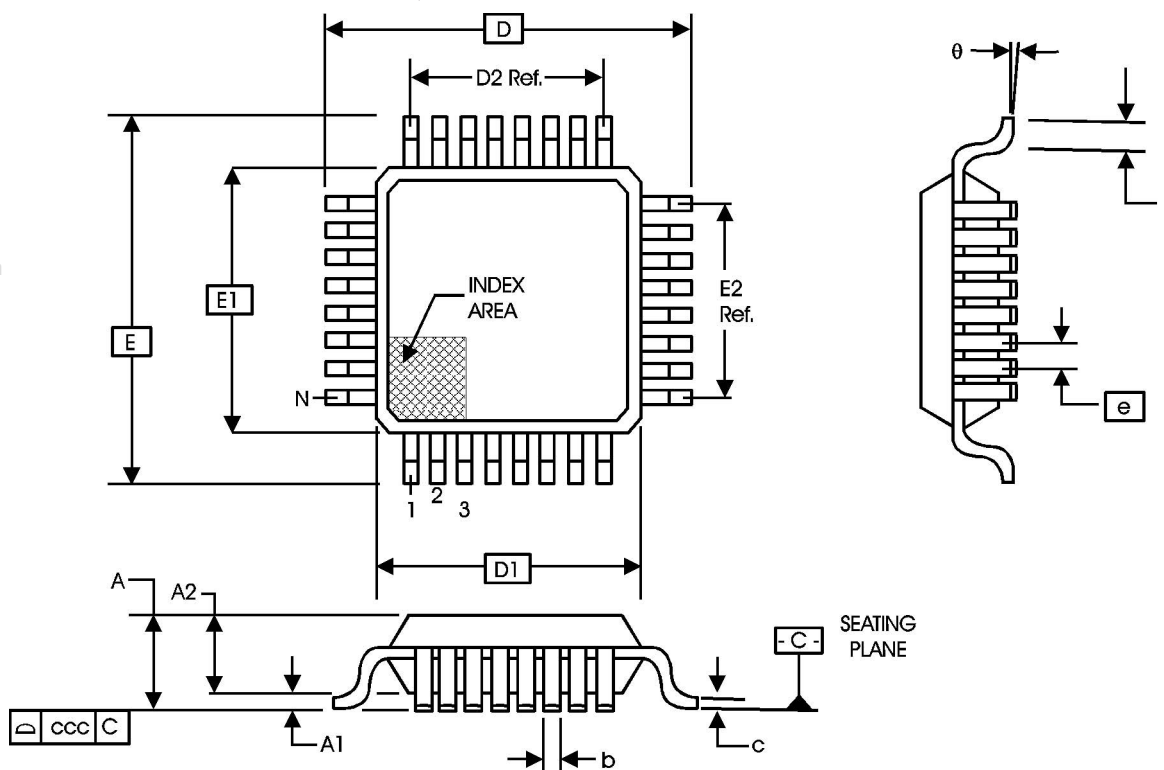
**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS84021 is: 4325



**PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP**



**TABLE 9. PACKAGE DIMENSIONS**

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS |            |         |         |
|--------------------------------------------------|------------|---------|---------|
| SYMBOL                                           | BBA        |         |         |
|                                                  | MINIMUM    | NOMINAL | MAXIMUM |
| N                                                | 32         |         |         |
| A                                                | --         | --      | 1.60    |
| A1                                               | 0.05       | --      | 0.15    |
| A2                                               | 1.35       | 1.40    | 1.45    |
| b                                                | 0.30       | 0.37    | 0.45    |
| c                                                | 0.09       | --      | 0.20    |
| D                                                | 9.00 BASIC |         |         |
| D1                                               | 7.00 BASIC |         |         |
| D2                                               | 5.60 Ref.  |         |         |
| E                                                | 9.00 BASIC |         |         |
| E1                                               | 7.00 BASIC |         |         |
| E2                                               | 5.60 Ref.  |         |         |
| e                                                | 0.80 BASIC |         |         |
| L                                                | 0.45       | 0.60    | 0.75    |
| $\theta$                                         | 0°         | --      | 7°      |
| ccc                                              | --         | --      | 0.10    |

Reference Document: JEDEC Publication 95, MS-026



Integrated  
Circuit  
Systems, Inc.

# ICS84021

260MHz, CRYSTAL-TO-LVCMOS / LVTTTL  
FREQUENCY SYNTHESIZER

TABLE 10. ORDERING INFORMATION

| Part/Order Number | Marking    | Package                       | Count        | Temperature |
|-------------------|------------|-------------------------------|--------------|-------------|
| ICS84021AY        | ICS84021AY | 32 Lead LQFP                  | 250 per tray | 0°C to 70°C |
| ICS84021AYT       | ICS84021AY | 32 Lead LQFP on Tape and Reel | 1000         | 0°C to 70°C |

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