Data Sheet

PowerPC 440SP Embedded Processor

Features

- PowerPC® 440 processor core operating at up to 667MHz with 32-KB I- and D-caches (with parity checking)
- On-chip 256-KB SRAM configurable as L2 Cache or Ethernet Packet/Code store memory
- Selectable Processor:Bus clock ratios (Refer to the Clocking chapter in the *PPC440SP Embedded Processor User's Manual* for details)
- Supports up to 4 GB (2 Chip Selects) of 64-bit/32-bit SDRAM with ECC
  - DDR1 266-333-400
  - DDR2 400-533-667
- Three DDR PCI-X interfaces (32-bit or 64-bit) up to 133 MHz (DDR 266) with support for conventional PCI
- XOR Accelerator with DMA controller
- Optional: High throughput RAID 6 hardware acceleration, performs XOR and Galois Field P & Q parity computations, supports up to 255 drives
- I2O Messaging Unit with two DMA controllers
- External Peripheral Bus (24-bit Address, 8-bit Data) for up to three devices
- One Ethernet 10/100/1000 Mbps half- or full-duplex interface. Operational modes supported are MII and GMII.
- Programmable Interrupt Controller supports interrupts from a variety of sources.
- Programmable General Purpose Timers (GPT)
- Three serial ports (16750 compatible UART)
- Two IIC interfaces
- General Purpose I/O (GPIO) interface available
- JTAG interface for board level testing
- Processor can boot from PCI memory

Description

Designed specifically to address high-end embedded applications for storage, the PowerPC 440SP Embedded Processor (PPC440SP) provides a high-performance, low power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and lower power dissipation.

This chip contains a high-performance RISC processor core, a DDR2 SDRAM controller, configurable 256KB SRAM to be used as L2 cache or software-controlled on-chip memory, three DDR PCI-X bus interfaces, an Ethernet interface, an I2O/DMA controller, control for external ROM and peripherals, optional RAID 6 acceleration, an XOR DMA unit, serial ports, IIC interfaces, and general purpose I/O.

Technology: CMOS Cu-11, 0.13mm

Package: 29mm, 783-ball, 1mm pitch, Flip Chip-Plastic Ball Grid Array (FC-PBGA)

Power (estimated): Less than 6W @533MHz

Supply voltages required: 3.3V, 2.5V, 1.8V, 1.5V

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Ordering and PVR Information

For information about the availability of the following parts, contact your local AMCC sales office.

Product Name	Order Part Number (see Notes:)	Package	Rev Level	PVR Value	JTAG ID
PPC440SP	PPC440SP-xpCfffC	29mm, 783 FC-PBGA	C	0x53221891	0x12056049

Notes:

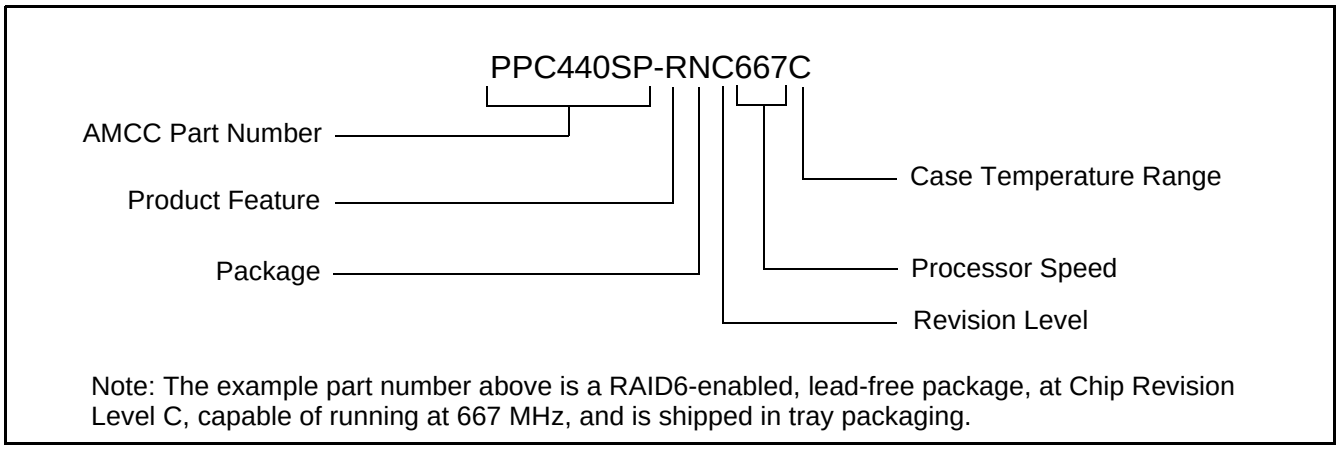
1. x = Product Feature
   A = RAID6 not enabled
   R = RAID6 enabled
2. p = Module Package Type
   F = leaded FC-PBGA
   N = lead free FC-PGBA (RoHS compliant)
3. C = Chip Revision Level C
4. fff = Processor Frequency
   533 = 533MHz
   667 = 667MHz
5. C = Case Temperature Range of -40°C to +100°C

Each part number contains a revision code. This is the die mask revision number and is included in the part number for identification purposes only.

The PVR (Processor Version Register) and the JTAG ID register are software accessible (read-only) and contain information that uniquely identifies the part. See the *PPC440SP Embedded Processor User's Manual* for details about accessing these registers.

Note: Raid-enabled versions (Product Feature = R) require a RAID key license.

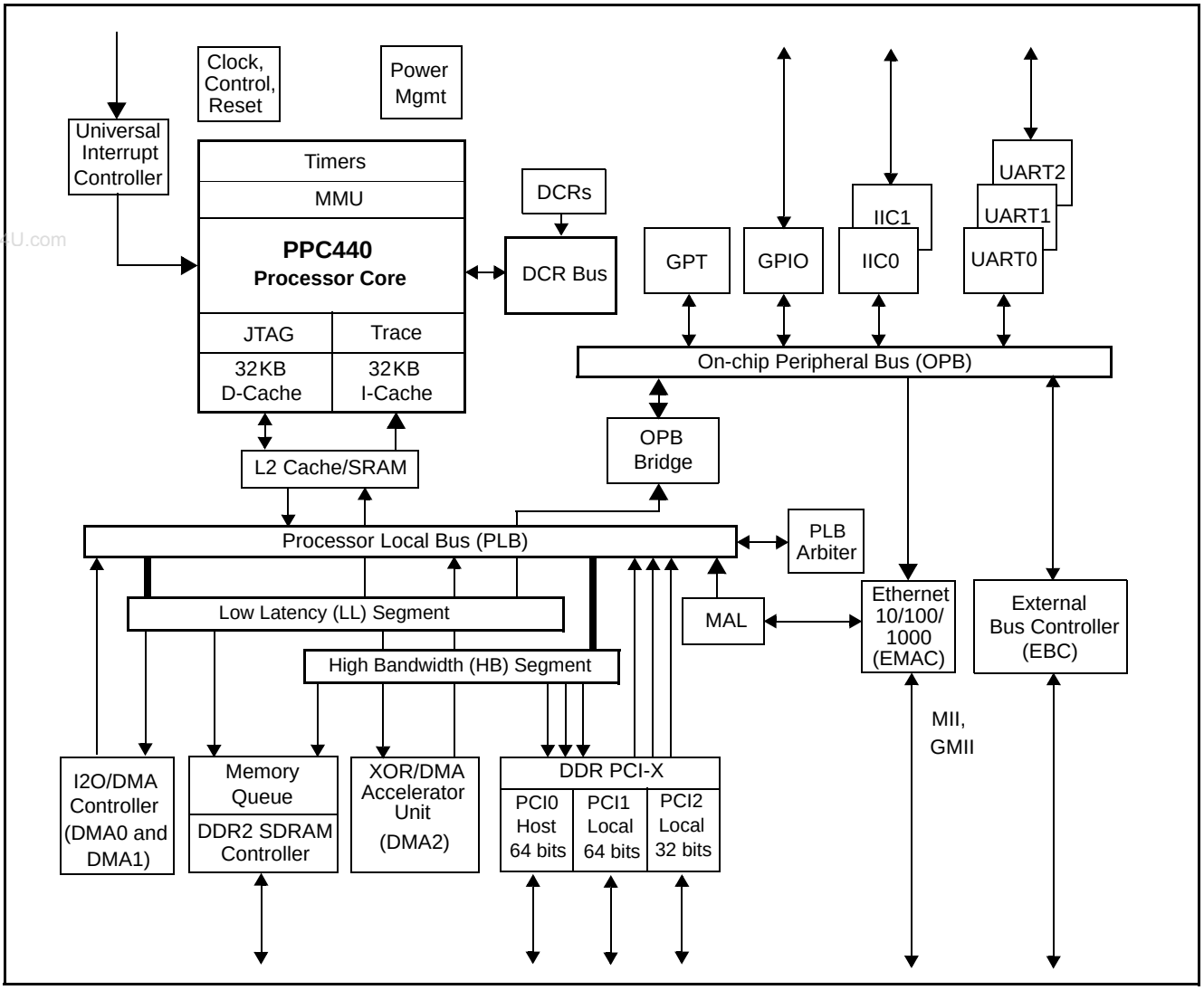
Figure 1. Order Part Number Key



Note: The example part number above is a RAID6-enabled, lead-free package, at Chip Revision Level C, capable of running at 667 MHz, and is shipped in tray packaging.

PPC440SP Functional Block Diagram

Figure 2. PPC440SP Functional Block Diagram



The PPC440SP is a System on a chip, which uses IBM® CoreConnect Bus™ Architecture.

Implemented with the Crossbar option, the IBM CoreConnect buses provide:

- 128-bit Data, 64-bit Address PLB interfaces up to 166.66MHz, 2.6GB/s on both the Read and Write data paths (10.6GB/sec total)
- 32-bit OPB interfaces up to 83.33MHz, 333MB/s

Address Maps

The PPC440SP incorporates two address maps. The first is a fixed processor system memory address map. This address map defines the possible contents of various processor accessible address regions. The second address map identifies the system Device Configuration Registers (DCRs). DCRs are accessed by software running on the PPC440SP processor through the use of **mtdcr** and **mfdcr** instructions.

Table 1. System Memory Address Map (Sheet 1 of 2)

Function	Sub Function	Start Address	End Address	Size
Local Memory (LL)[1]	DDR SDRAM	0000 0000 0000 0000	0000 0000 FFFF FFFF	4GB
	SRAM	0000 0001 0000 0000	0000 0001 0003 FFFF	256KB
	Reserved	0000 0001 0004 0000	0000 0001 000F FFFF	
Internal PLB Interfaces (LL)	I2O Registers	0000 0001 0010 0000	0000 0001 0010 00FF	256B
	DMA 0 Registers	0000 0001 0010 0100	0000 0001 0010 01FF	256B
	DMA 1 Registers	0000 0001 0010 0200	0000 0001 0010 02FF	256B
	I20/DMA Buffers	0000 0001 0010 0300	0000 0001 0010 0FFF	3.25KB
	Reserved	0000 0001 0010 1000	0000 0001 001F FFFF	
	XOR/DMA2	0000 0001 0020 0000	0000 0001 0020 3FFF	16KB
	Reserved	0000 0001 0020 4000	0000 0001 EFFF FFFF	
Internal OPB Peripherals (LL)	Reserved	0000 0001 F000 0000	0000 0001 F000 01FF	
	UART0	0000 0001 F000 0200	0000 0001 F000 0207	8B
	Reserved	0000 0001 F000 0208	0000 0001 F000 02FF	
	UART1	0000 0001 F000 0300	0000 0001 F000 0307	8B
	Reserved	0000 0001 F000 0308	0000 0001 F000 03FF	
	IIC0	0000 0001 F000 0400	0000 0001 F000 041F	32B
	Reserved	0000 0001 F000 0420	0000 0001 F000 04FF	
	IIC1	0000 0001 F000 0500	0000 0001 F000 051F	32B
	Reserved	0000 0001 F000 0520	0000 0001 F000 05FF	
	UART2	0000 0001 F000 0600	0000 0001 F000 0607	8B
	Reserved	0000 0001 F000 0608	0000 0001 F000 06FF	248B
	GPIO Controller Registers	0000 0001 F000 0700	0000 0001 F000 077F	128B
	Reserved	0000 0001 F000 0780	0000 0001 F000 07FF	
	Ethernet Controller Registers	0000 0001 F000 0800	0000 0001 F000 08FF	256B
	Reserved	0000 0001 F000 0900	0000 0001 F000 09FF	
	General Purpose Timers	0000 0001 F000 0A00	0000 0001 F000 0B3F	320B
	Reserved	0000 0001 F000 0B40	0000 0001 F7FF FFFF	
	EBC Memory	0000 0001 F800 0000	0000 0001 FFBF FFFF	124MB
	Additional Boot ROM[6]	0000 0001 FFC0 0000	0000 0001 FFDF FFFF	2MB
Boot ROM[2, 3]		0000 0001 FFE0 0000	0000 0001 FFFF FFFF	2MB
Reserved		0000 0002 0000 0000	0000 0007 FFFF FFFF	
Local Memory Alias (HB)	Aliased DDR SDRAM	0000 0008 0000 0000	0000 0008 FFFF FFFF	4GB

Table 1. System Memory Address Map (Sheet 2 of 2)

Function	Sub Function	Start Address	End Address	Size
DDR PCI-X Space (HB)	Reserved	0000 0009 0000 0000	0000 0009 07FF FFFF	
	PCIX0 I/O	0000 0009 0800 0000	0000 0009 0800 FFFF	64KB
	PCIX1 I/O	0000 0009 1800 0000	0000 0009 1800 FFFF	64KB
	PCIX2 I/O	0000 0009 2800 0000	0000 0009 2800 FFFF	64KB
	PCIX0 Addressing Config. Regs	0000 0009 0EC0 0000	0000 0009 0EC0 0007	8B
	PCIX1 Addressing Config. Regs	0000 0009 1EC0 0000	0000 0009 1EC0 0007	8B
	PCIX2 Addressing Config. Regs	0000 0009 2EC0 0000	0000 0009 2EC0 0007	8B
	PCIX0 Core Config. Regs	0000 0009 0EC8 0000	0000 0009 0EC8 0FFF	4KB
	PCIX1 Core Config. Regs	0000 0009 1EC8 0000	0000 0009 1EC8 0FFF	4KB
	PCIX2 Core Config. Regs	0000 0009 2EC8 0000	0000 0009 2EC8 0FFF	4KB
	PCIX0 Simple Message Passing	0000 0009 0EC8 1100	0000 0009 0EC8 11FF	256B
	PCIX1 Simple Message Passing	0000 0009 1EC8 1100	0000 0009 1EC8 11FF	256B
	PCIX2 Simple Message Passing	0000 0009 2EC8 1100	0000 0009 2EC8 11FF	256B
	PCIX0 Special Cycle	0000 0009 0ED0 0000	0000 0009 0EDF FFFF	1MB
	PCIX1 Special Cycle	0000 0009 1ED0 0000	0000 0009 1EDF FFFF	1MB
	PCIX2 Special Cycle	0000 0009 2ED0 0000	0000 0009 2EDF FFFF	1MB
	Reserved	0000 0009 2EE0 0000	0000 0009 2EFF FFFF	
	PCI Memory	0000 0009 2F00 0000	0000 0009 FFBF FFFF	3.3GB
	Reserved	0000 0009 FFC0 0000	0000 0009 FFDF FFFF	
	PCI Boot ROM (PCI Memory)	0000 0009 FFE0 0000	0000 0009 FFFF FFFF	2MB
	PCI Memory	0000 000A 0000 0000	0000 000F FFFF FFFF	24GB
Reserved[4]		0000 0010 0000 0000	03FF FFFF FFFF FFFF	
Reserved[5]		0400 0010 0000 0000	07FF FFFF FFFF FFFF	
DDR PCI-X Space (HB)	PCI Memory	0800 0000 0000 0000	FFFF FFFF FFFF FFFF	15.7EB

Notes:

1. DDR SDRAM and on-chip SRAM can be located anywhere in the Local Memory area of the memory map.
2. The Boot ROM and Expansion ROM areas of the memory map are intended for use by ROM or Flash-type devices. While locating volatile DDR SDRAM and SRAM in this region is supported, use of these regions for this purpose is not recommended.
3. When the optional boot from PCI-X memory is selected, the PCI-X Boot ROM address space begins at 9 FFE0 0000 (128 KB).
4. Never decoded.
5. Unpredictable results on Read and Write operations.
6. Accessed by means of EBC Peripheral Bank Configuration Registers

Table 2. DCR Address Map (4KB of Device Configuration Registers)

Function	Start Address	End Address	Size
Total DCR Address Space[1]	000	3FF	1KW (4KB)[1]
By function:			
Reserved	000	00B	12W
Clocking Power On Reset	00C	00D	2W
System DCRs	00E	00F	2W
Memory Controller	010	011	2W
External Bus Controller	012	013	2W
Reserved	014	01F	12W
SRAM	020	02F	16W
L2 Controller	030	03F	16W
Memory Queue	040	04F	16W
Reserved	050	05F	16W
I2O/DMA	060	07F	32W
PLB	080	08F	16W
PLB to OPB Bridge Out	090	09F	16W
Reserved	0A0	0AF	16W
Reserved	0B0	0B1	2W
Reserved	0B2	0BF	14W
Interrupt Controller 0	0C0	0CF	16W
Interrupt Controller 1	0D0	0DF	16W
Power Management	0E0	0E7	8W
Reserved	0E8	17F	152W
Ethernet MAL	180	1FF	128W
Reserved	200	3FF	512W

Notes:

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register. One KW (1024W) equals 4KB (4096 bytes).

PowerPC 440 Processor Core

The PowerPC 440 processor core is designed for high-end applications such as RAID controllers, SAN, iSCSI, routers, switches, printers, set-top boxes, and so on. It is the first processor core to implement the Book E PowerPC embedded architecture and the first to use the 128-bit version of IBM's on-chip CoreConnect Bus Architecture.

Features include:

- Up to 667 MHz operation
- PowerPC Book E architecture
- 32 KB I-cache, 32 KB D-cache
  - Parity on Data and Tag address - checking of parity with error injection
- Three logical regions in D-cache: Locked, Transient, and Normal
- D-cache full-line flush capability
- 41-bit virtual address, 36-bit (64 GB) physical address
- Superscalar, out-of-order execution
- Seven-stage pipeline
- Three execution pipelines
- Dynamic branch prediction
- Memory management unit
  - 64-entry, full associative, unified TLB with parity
  - Separate instruction and data micro-TLBs
  - Storage attributes for write-through, cache-inhibited, guarded, and big or little endian
- Debug facilities
  - Multiple instruction and data range breakpoints
  - Data value compare
  - Single step, branch, and trap events
  - Non-invasive real-time trace interface
- 24 DSP instructions
  - Single cycle multiply and multiply-accumulate
  - 32 x 32 integer multiply

Internal Buses

The PowerPC 440SP Embedded Processor features three standard on-chip buses: the Processor Local Bus (PLB), the On-Chip Peripheral Bus (OPB), and the Device Control Register Bus (DCR). The high performance, high bandwidth cores such as the PowerPC 440 processor core, the DDR SDRAM memory controller, and the DDR PCI-X bridge connect to the PLB. The OPB hosts lower data rate peripherals. The daisy-chained DCR provides a lower bandwidth path for passing status and control information between the processor core and the other on-chip cores.

The PLB has a Crossbar arbiter that supports data transfer between the PLB master and two slave segments identified as the Low Latency (LL) and High Bandwidth (HB) segments. The LL segment allows PLB masters CPU and I2O, that are adversely affected by latency, to communicate with slave devices with minimal latency. The HB segment allows PLB masters DMA, XOR, and PCI to exchange large blocks of data with SDRAM and PCI without interfering with the low latency PLB masters.

Bus features include:

- PLB
  - 128-bit Data implementation of the PLB architecture
  - Separate and simultaneous read and write data paths
  - 64-bit address
  - Simultaneous control, address, and data phases
  - Four levels of pipelining
  - Byte enable capability supporting unaligned transfers

  - 32- and 64-byte burst transfers
  - 166MHz, maximum 5.2GB/s (simultaneous read and write)
  - Processor:Bus clock ratios of N:1 and N:2
- OPB
  - Dynamic bus sizing: 32-, 16-, and 8-bit data path
  - 32-bit address
  - 83.33MHz, maximum 333MB/s
- DCR
  - 32-bit data path
  - 10-bit address

On-Chip SRAM/L2 Cache

Features include:
- Four banks of 64KB each for a total of 256KB
- Configurable as either L2 cache or SRAM
- Memory cycles supported:
  - Single beat read and write, 1 to 16 bytes
  - Quadword Read and Write burst for 12-bit master
  - Guarded memory accesses on 4KB boundaries
- Sustainable 2.6GB/s peak bandwidth at 166MHz
- Use as an L2 cache improves processor performance and reduces the PLB load
  - Cache coherency maintained by a hardware snoop mechanism on the Low Latency (LL) PLB or by software
  - Data Array and Tag Array parity
  - Unified data and instruction cache
  - Four-way set associative
  - 36-bit addressing
  - Full LRU replacement algorithm
  - Write through, look aside
- Use as Ethernet packet store allows Ethernet packets to be held for processing by the Ethernet core

DDR PCI-X Interface

The DDR PCI-X interface allows connection of PCI and PCI-X devices to the PowerPC processor and local memory. There are three separate interfaces supporting 32- and 64-bit PCI-X buses in DDR mode. All three interfaces can be configured for either host or adapter mode. PCI 32/64-bit legacy mode, compatible with PCI Version 2.3, is also supported.

Features include:
- PCI-X 2.0
  - Split transactions
  - Frequency to 266MHz
  - 32- and 64-bit address/data bus
  - ECC supported for 266MHz Mode 2 only
- PCI 2.3 backward compatibility
  - Frequency to 66MHz
  - 32- and 64-bit bus
- Can be the PCI Host Bus Bridge or an Adapter Device PCI interface
- Optional PCI arbitration function with PCI and PCI-X mode 1, supporting up to four external devices, that can be disabled for use with an external arbiter
- Support for Message Signaled Interrupts (MSI) on both in- and out-bound interrupts
- Simple message passing capability
- Asynchronous to the PLB

- PCI Power Management Version 1.1
- PCI arbitration function with PCI-X Mode 2 support (optional)
- PCI register set addressable both from on-chip processor and PCI device sides
- Ability to boot from PCI-X bus memory
- Error tracking/status
- Supports initiation of transfer to the following address spaces:
  - Single beat I/O reads and writes
  - Single beat and burst memory reads and writes
  - Single beat configuration reads and writes (Type 0 and Type 1)
  - Single beat special cycles
- PCI-X initialization sequence support (frequency & mode determination)
- Support for unexpected split completions
- Outbound transaction split discard timers
- Vital Product Data (VPD) support
- PCI-to-PCI opaque bridge

DDR1/DDR2 SDRAM Memory Controller

The DDR2 SDRAM memory controller supports industry standard 184-pin DIMMs, SO-DIMMs, and other discrete devices. Global memory timings, address and bank sizes, and memory addressing modes are programmable. The DDR2 SDRAM controller interfaces to the PLB through a Memory Queue (MQ) function that includes six high-speed 1KB FIFO buffers.

Features include:

- Registered and non-registered industry standard DIMMs
- DDR1 266-333-400
- DDR2 400-533-667
- 64-and 32-bit memory interfaces with optional 8-bit ECC (SEC/DED)
- 5.32GB/s peak bandwidth for the 64-bit interface
- 2.66GB/s peak bandwidth for the 32-bit interface
- Two chip (bank) select signals supporting two external banks
- CAS latencies of 2, 3, 4, 5, 6, and 7 supported
- Page mode accesses (up to 32 open pages) with configurable paging policy
- Look-ahead request queue with programmable depth of four commands.
- Optional optimized command scheduling (activate/precharge non-conflicting banks while accessing the current bank)
- Up to 4GB in two external banks
- Programmable address mapping and timing
- Hardware and software initiated self-refresh
- Sync DRAM configuration by means of mode register and extended mode register set commands
- Power management (self-refresh, suspend, sleep)
- Low Latency & High Bandwidth PLB ports
- Selectable PLB read response (immediate or deferred)
- Programmable Low Latency & High Bandwidth arbitration schemes
- High Bandwidth port has four 1KB read buffers and two1KB write buffers
- Low Latency port has four 128B read buffers and two 128B write buffers

External Peripheral Bus Controller (EBC)

Features include:

- Support 2MB Boot ROM
- Up to three ROM, EPROM, SRAM, Flash memory, and slave peripherals supported
- Burst and non-burst devices
- 8-bit data bus

- 24-bit address, 16MB address space
- Peripheral Device pacing with external “Ready”
- Latch data on Ready, synchronous or asynchronous
- Programmable access timing per device
  - 256 Wait States for non-burst
  - 32 Burst Wait States for first access and up to 8 Wait States for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (1 to 4 clock cycles) relative to CS
- Programmable address mapping

Ethernet Controller Interface

The Ethernet support interfaces to the physical layer, but the PHY is not included on the chip.

Features include:

- One 10/100/1000 interface running in full- and half-duplex modes
  - One full Media Independent Interface (MII) with 4-bit parallel data transfer
  - One Gigabit Media Independent Interface (GMII)

I2O/DMA Controller

The I20/DMA controller provides support for I20 messaging and two DMA controllers (DMA0 and DMA1). I2O manages message frame address (MFA) FIFOs or queues in memory in response to I2O register reads and writes and transfers message frames. The DMAs provide normal memory access support to ease the CPU burden.

I2O features include:

- I2O pull- and push-messaging methods
- Dynamic message frame size
- Programmable FIFO size (4096 64-bit MFAs maximum)
- 64-bit and 32-bit MFA sizes
- Three interrupt gathering methods
- Registered MFA prefetch and posting
- 32-bit inbound and outbound doorbell registers
- Four 32-bit scratch pad registers

DMA features include:

- Programmable Command Pointer FIFO and Completion FIFO size (up to 2048 DMA operations queued)
- 512-byte/1KB buffering for DMA0/DMA1
- Simultaneous fill and drain (PLB read/write pipelining)
- Any source PLB address to any destination address
- No memory alignment restrictions on source or destination
- 32-byte command descriptor block
- Maximum transfer size of 16MB
- 64-bit addressing
- Prefetch indicators for PCI-X buffer management (DMA1 only)

Optional RAID 5 and RAID 6 Acceleration Hardware

The 440SP provides integrated acceleration hardware that implements high throughput RAID 5 and RAID 6 algorithms to compute the single parity P for RAID 5, and dual parity P & Q for RAID 6. RAID 5 is used to recover data in the case of a single disk drive failure, and RAID 6 provides for data recovery if two disk drives fail.

The 440SP offers a choice of two XOR engines for computing the P parity. The first choice is available with the XOR/DMA2 acceleration unit and is used for RAID 5. The second choice for XOR parity computation, along with the RAID 6 Galois Field GF(2^8)-based polynomial computations, resides inside the Memory Queue functional block

of the Memory Controller unit.

The RAID 5 and RAID 6 parity computations performed in the Memory Queue are assisted by the two-channel DMA engine of the I2O/DMA controller unit, designated as DMA0 and DMA1. The RAID acceleration hardware also provides various alternatives for balancing load and performance, depending on customer-specific application firmware. The two-way crossbar bus architecture can perform data read and write operations simultaneously, resulting in extremely high throughput.

RAID 6 capability is available only with the RAID-enabled part numbers (PPC440SP-RpCfffC) as indicated in the ordering information section of this data sheet.

For more information about the RAID 6 implementation, description, and configuration of the acceleration hardware, refer to the following AMCC documents:

- PowerPC 440SP/440SPe RAID Support Application Note
- PowerPC 440SP RAID Addendum to the User's Manual

XOR/DMA2 Controller

The XOR/DMA2 controller performs the XOR functions needed to support RAID 5 applications including parity generation and check functions used across data stripes in a RAID 5 system.

Features include:

- Computes a bit-wise XOR on up to 16 data streams with result stored in designated target
- Performs XOR check on up to 16 data streams
- Driven by a linked list Command Block structure specifying control information, source operands, target operand, status information, and link
- Source and target streams may reside anywhere in PLB address space.
- Provides completion status per Command Block to be handled by software at a later time
- 96-byte and 160-byte Command Block formats are supported
- No memory alignment restrictions on operands or target
- Internal register arrays and data buffers are parity protected
- Can be used as a DMA controller (DMA2) with single source and target addresses

Serial Port

The serial port is compatible with the NS, 16570 UART interface.

Features include:

- One 8-pin, one 4-pin, and one 2-pin interfaces are provided
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with 16750 register set
- Complete status reporting capability
- Fully programmable serial-interface characteristics

IIC Bus Interface

Features include:

- Two IIC interfaces provided
- Support for Philips, Semiconductors I^2C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Full management of all IIC bus protocols
- Programmable error recovery
- Port 0 supports serial Bootstrap ROM with default parameters override at initialization

General Purpose Timers (GPT)

Provides a time base counter and system timers additional to those defined in the processor core.

- 32-bit time base counter driven by the OPB bus clock
- Seven 32-bit compare timers

General Purpose IO (GPIO) Controller

- Controller functions and GPIO registers are programmed and accessed by means of memory-mapped OPB bus master accesses.
- The 32 GPIOs are pin-shared with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose.
- Each GPIO output is a separately programmable tri-state driver (pull-up, pull-down, or open-drain).

Universal Interrupt Controller (UIC)

Two cascaded Universal Interrupt Controllers (UIC) process internal on-chip and external processor interrupts.

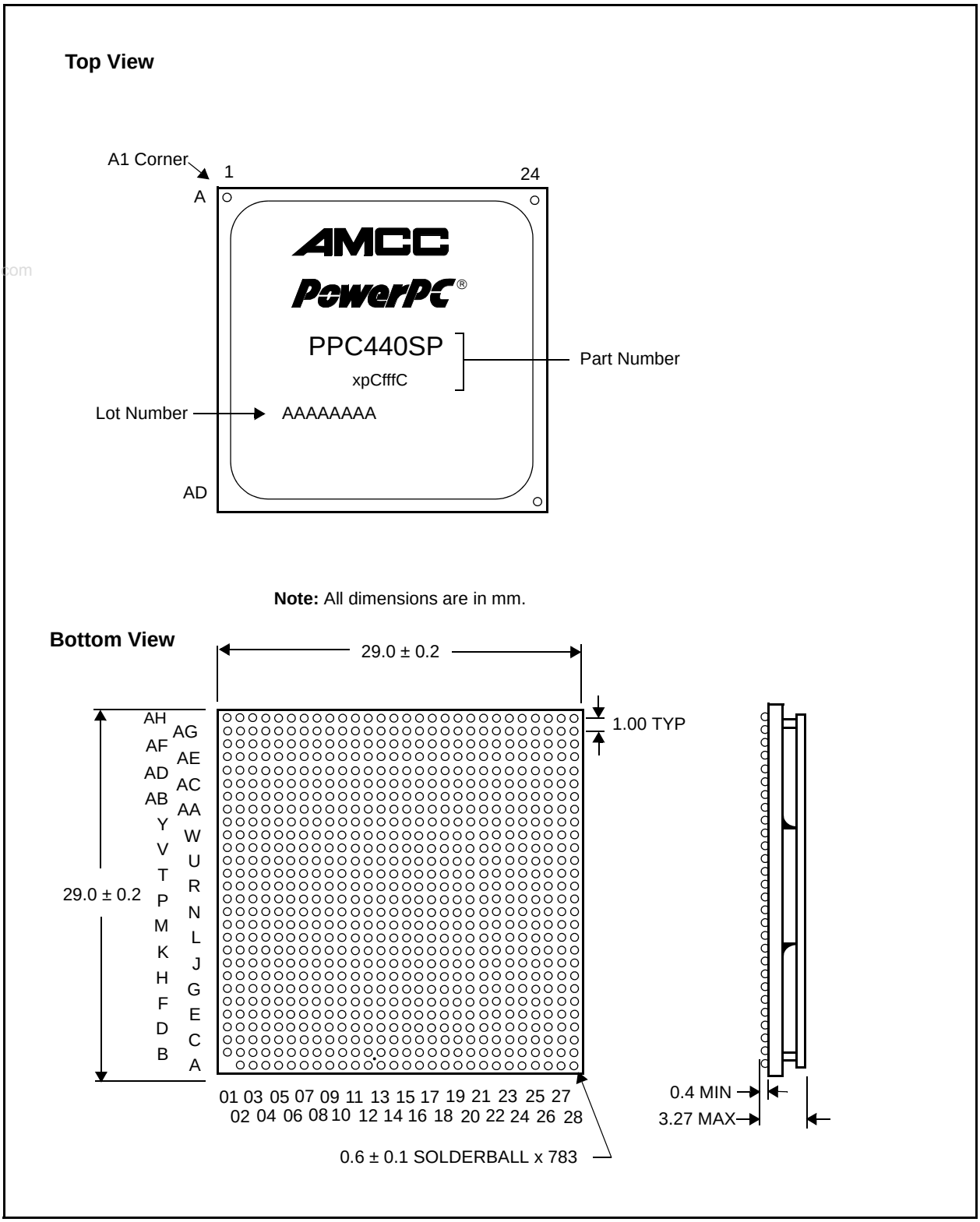
Note: Processor specific interrupts (for example, page faults) do not use UIC resources.

Features include:
- 6 external interrupts
- 56 internal interrupts
- Edge-triggered or level-sensitive
- Positive- or negative-active
- Non-critical or critical interrupt to the on-chip processor core
- Programmable interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

JTAG

Features include:
- IEEE 1149.1 Test Access Port
- IBM RISCWatch Debugger support
- JTAG Boundary Scan Description Language (BSDL)

Figure 3. 29mm, 783-Ball FC-PBGA Core Package



Signal Lists

This section contains two tables that list external signals.

Table 3 lists all the external signals in alphabetical order and shows the ball (pin) number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and the alternate signal or signals in brackets.

Multiplexed signals appear alphabetically multiple times in the list—once for each signal name on the ball. The page number listed gives the page in “Signal Functional Description” on page 56 where the signals in the indicated interface group begin.

Table 4 on page 47 lists all the external signals in order by ball (pin) number.

Signal List—Alphabetic Order

Table 3. Signals Listed Alphabetically (Sheet 1 of 30)

Signal Name	Ball	Interface Group	Page
A1GND	B01	Power	62
A2GND	AG28		
$A1V_{DD}$	C01		
$A2V_{DD}$	AF28		
AP0GND	AG01		
$AP0V_{DD}$	AF01		
AP1GND	B28		
$AP1V_{DD}$	C28		
AP2GND	T01		
$AP2V_{DD}$	R01		
BA0	AD21	DDR SDRAM	58
BA1	AE20		
BA2	AE25		
$\overline{\text{BankSel0}}$	T23		
$\overline{\text{BankSel1}}$	P22		
$\overline{\text{CAS}}$	AH25		
ClkEn0	AE23		
ClkEn1	AE24		

Table 3. Signals Listed Alphabetically (Sheet 2 of 30)

Signal Name	Ball	Interface Group	Page
DM0	AE26		
DM1	AA26		
DM2	V25		
DM3	P26		
DM4	K27		
DM5	M21		
DM6	R21		
DM7	U19		
DM8	AA24		
DQS0	AD26		
$\overline{\text{DQS0}}$	AD25		
DQS1	AA28		
$\overline{\text{DQS1}}$	AA27		
DQS2	U26	DDR SDRAM	58
$\overline{\text{DQS2}}$	U25		
DQS3	N27		
$\overline{\text{DQS3}}$	N28		
DQS4	K25		
$\overline{\text{DQS4}}$	K26		
DQS5	L25		
$\overline{\text{DQS5}}$	L26		
DQS6	R26		
$\overline{\text{DQS6}}$	R25		
DQS7	W27		
$\overline{\text{DQS7}}$	W26		
DQS8	AB26		
$\overline{\text{DQS8}}$	AB25		

Table 3. Signals Listed Alphabetically (Sheet 3 of 30)

Signal Name	Ball	Interface Group	Page
ECC0	AC24	DDR SDRAM	58
ECC1	Y23		
ECC2	Y21		
ECC3	AC23		
ECC4	AD23		
ECC5	AA23		
ECC6	W19		
ECC7	AF20		

Table 3. Signals Listed Alphabetically (Sheet 4 of 30)

Signal Name	Ball	Interface Group	Page
EMCCD	D02	Ethernet	59
EMCCrS	E03		
EMCMDClk	D01		
EMCMDIO	E04		
EMCRefClk	D12		
EMCRxClk	D03		
EMCRxD0	F04		
EMCRxD1	G04		
EMCRxD2	F03		
EMCRxD3	G01		
EMCRxD4	H03		
EMCRxD5	H02		
EMCRxD6	F05		
EMCRxD7	F06		
EMCRxDV	F07		
EMCRxErr	J01		
EMCTxClk	E01		
EMCGTxClk	B08		
EMCTxD0	F02		
EMCTxD1	F01		
EMCTxD2	H01		
EMCTxD3	G03		
EMCTxD4	H04		
EMCTxD5	K04		
EMCTxD6	K03		
EMCTxD7	A02		
EMCTxEn	C04		
EMCTxErr	A03		
$\overline{\text{ExtReset}}$	H11	External Slave Peripheral	59

Table 3. Signals Listed Alphabetically (Sheet 5 of 30)

Signal Name	Ball	Interface Group	Page
GND	B02	Power	62
GND	B05		
GND	B09		
GND	B20		
GND	B24		
GND	B27		
GND	C13		
GND	C16		
GND	E02		
GND	E07		
GND	E11		
GND	E18		
GND	E22		
GND	E27		
GND	F14		
GND	F15		
GND	G05		
GND	G09		
GND	G13		
GND	G16		
GND	G20		
GND	G24		
GND	J02		
GND	J07		
GND	J11		
GND	J18		
GND	J22		
GND	J27		
GND	L05		
GND	L09		
GND	L13		
GND	L16		

Table 3. Signals Listed Alphabetically (Sheet 6 of 30)

Signal Name	Ball	Interface Group	Page
GND	L20	Power	62
GND	L24		
GND	N03		
GND	N07		
GND	N11		
GND	N14		
GND	N15		
GND	N18		
GND	N22		
GND	N26		
GND	P06		
GND	P13		
GND	P16		
GND	P23		
GND	R06		
GND	R13		
GND	R16		
GND	R23		
GND	T03		
GND	T07		
GND	T11		
GND	T14		
GND	T15		
GND	T18		
GND	T22		
GND	T26		
GND	V05		
GND	V09		
GND	V13		
GND	V16		
GND	V20		
GND	V24		
GND	Y02		
GND	Y07		

Table 3. Signals Listed Alphabetically (Sheet 7 of 30)

Signal Name	Ball	Interface Group	Page
GND	Y11	Power	62
GND	Y18		
GND	Y22		
GND	Y27		
GND	AB05		
GND	AB09		
GND	AB13		
GND	AB16		
GND	AB20		
GND	AB24		
GND	AC14		
GND	AC15		
GND	AD02		
GND	AD07		
GND	AD11		
GND	AD18		
GND	AD22		
GND	AD27		
GND	AF13		
GND	AF16		
GND	AG02		
GND	AG05		
GND	AG09		
GND	AG20		
GND	AG24		
GND	AG27		

Table 3. Signals Listed Alphabetically (Sheet 8 of 30)

Signal Name	Ball	Interface Group	Page
[GPIO00] [TrcClk] PCIX0Req2	AA12	System	61
[GPIO01] [TrcBS0] PCIX0Req3	Y12		
[GPIO02] [TrcBS1] PCIX0Gnt2	AC13		
[GPIO03] [TrcBS2] PCIX0Gnt3	AF11		
[GPIO04] [TrcES0] PCIX1Req2	C23		
[GPIO05] [TrcES1] PCIX1Req3	E23		
[GPIO06] [TrcES2] PCIX1Gnt2	D21		
[GPIO07] [TrcES3] PCIX1Gnt3	D23		
[GPIO08] [TrcES4] PerReady	G12		
[GPIO09] PerCS1 [TrcTS0]	E12		
[GPIO10] PerCS2 [TrcTS1]	H10		
[GPIO11] IRQ0 [TrcTS2]	C07		
[GPIO12] IRQ1 [TrcTS3]	C06		
[GPIO13] IRQ2 [TrcTS4]	A05		
[GPIO14] IRQ3 [TrcTS5]	C05		
[GPIO15] IRQ4 [TrcTS6]	D06		
[GPIO16] IRQ5 [UART2_Rx]	D05		
[GPIO17] PerBE0 [UART2_Tx]	R09		
[GPIO18] PCIX0Gnt0	AF14		
[GPIO19] PCIX0Gnt1	AG13		
[GPIO20] PCIX0Req0	AH11		
[GPIO21] PCIX0Req1	AG12		
[GPIO22] PCIX1Gnt0	B19		
[GPIO23] PCIX1Gnt1	C19		
[GPIO24] PCIX1Req0	C20		
[GPIO25] PCIX1Req1	C22		
[GPIO26] PCIX2Gnt0	P01		
[GPIO27] PCIX2Gnt1	P03		
[GPIO28] PCIX2Req0	U05		
[GPIO29] PCIX2Req1	N04		
[GPIO30] UART1_Rx	A07		
[GPIO31] UART1_Tx	A06		
Halt	K18		
HISRRst	B06		

Table 3. Signals Listed Alphabetically (Sheet 9 of 30)

Signal Name	Ball	Interface Group	Page
IIC0SClk	D09	IIC Peripheral	60
IIC0SDA	E08		
IIC1SClk	F08		
IIC1SDA	E10		
IRQ0 [GPIO11] [TrcTS2]	C07	Interrupts	60
IRQ1 [GPIO12] [TrcTS3]	C06		
IRQ2 [GPIO13] [TrcTS4]	A05		
IRQ3 [GPIO14] [TrcTS5]	C05		
IRQ4 [GPIO15] [TrcTS6]	D06		
IRQ5 [GPIO16] [UART2_Rx]	D05		
MemAddr00	AF23	DDR SDRAM	58
MemAddr01	AE21		
MemAddr02	AD19		
MemAddr03	AE19		
MemAddr04	AH22		
MemAddr05	AH23		
MemAddr06	AE22		
MemAddr07	AF21		
MemAddr08	AF22		
MemAddr09	AG23		
MemAddr10	AG21		
MemAddr11	AF19		
MemAddr12	AH20		
MemAddr13	AH21		
MemAddr14	AF24		
MemClkOut0	AG26		
$\overline{\text{MemClkOut0}}$	AG25		
MemClkOut1	AH26		
$\overline{\text{MemClkOut1}}$	AH27		

Table 3. Signals Listed Alphabetically (Sheet 10 of 30)

Signal Name	Ball	Interface Group	Page
MemData00	AD28	DDR SDRAM	58
MemData01	AE27		
MemData02	AF27		
MemData03	AC26		
MemData04	AC27		
MemData05	AE28		
MemData06	AF25		
MemData07	AC25		
MemData08	Y26		
MemData09	AB28		
MemData10	AC28		
MemData11	Y28		
MemData12	Y25		
MemData13	AA25		
MemData14	AB23		
MemData15	W25		
MemData16	U27		
MemData17	V28		
MemData18	W28		
MemData19	T25		
MemData20	T27		
MemData21	V26		
MemData22	W23		
MemData23	T28		
MemData24	N25		
MemData25	P28		
MemData26	R28		
MemData27	M27		
MemData28	M26		
MemData29	P25		
MemData30	U24		
MemData31	M25		

Table 3. Signals Listed Alphabetically (Sheet 11 of 30)

Signal Name	Ball	Interface Group	Page
MemData32	J26	DDR SDRAM	58
MemData33	K28		
MemData34	L28		
MemData35	H28		
MemData36	H27		
MemData37	J28		
MemData38	P21		
MemData39	H26		
MemData40	P20		
MemData41	M23		
MemData42	M22		
MemData43	N23		
MemData44	N21		
MemData45	K24		
MemData46	M24		
MemData47	N19		
MemData48	U23		
MemData49	R22		
MemData50	R24		
MemData51	U22		
MemData52	T19		
MemData53	R20		
MemData54	P24		
MemData55	T21		
MemData56	W22		
MemData57	U20		
MemData58	U21		
MemData59	W24		
MemData60	W21		
MemData61	V23		
MemData62	V21		
MemData63	W20		
MemDCFdbkD	AB21		
MemDCFdbkR	AC21		

Table 3. Signals Listed Alphabetically (Sheet 12 of 30)

Signal Name	Ball	Interface Group	Page
MemODT0	AA22	DDR SDRAM	58
MemODT1	AC22		
MemVRef0	AA20		
MemVRef1	AA21		
No ball	A01	A physical ball does not exist at this coordinate	na
OV_{DD}	B07	Power	62
OV_{DD}	B11		
OV_{DD}	B14		
OV_{DD}	B15		
OV_{DD}	C03		
OV_{DD}	G02		
OV_{DD}	G07		
OV_{DD}	G11		
OV_{DD}	K14		
OV_{DD}	K15		
OV_{DD}	L02		
OV_{DD}	L07		
OV_{DD}	L11		
OV_{DD}	P10		
OV_{DD}	P14		

Table 3. Signals Listed Alphabetically (Sheet 13 of 30)

Signal Name	Ball	Interface Group	Page
$P0V_{DD}$	R14		
$P0V_{DD}$	W14		
$P0V_{DD}$	W15		
$P0V_{DD}$	AB07		
$P0V_{DD}$	AB11		
$P0V_{DD}$	AB18		
$P0V_{DD}$	AB22		
$P0V_{DD}$	AG07		
$P0V_{DD}$	AG11		
$P0V_{DD}$	AG14		
$P0V_{DD}$	AG15		
$P0V_{DD}$	AG18		
$P0V_{DD}$	AG22		
$P1V_{DD}$	B18		
$P1V_{DD}$	B22		
$P1V_{DD}$	C26	Power	62
$P1V_{DD}$	G18		
$P1V_{DD}$	G22		
$P1V_{DD}$	G27		
$P1V_{DD}$	L18		
$P1V_{DD}$	L22		
$P1V_{DD}$	L27		
$P1V_{DD}$	P15		
$P2V_{DD}$	P02		
$P2V_{DD}$	R02		
$P2V_{DD}$	R10		
$P2V_{DD}$	V02		
$P2V_{DD}$	V07		
$P2V_{DD}$	V11		
$P2V_{DD}$	AB02		
$P2V_{DD}$	AF03		

Table 3. Signals Listed Alphabetically (Sheet 14 of 30)

Signal Name	Ball	Interface Group	Page
PCIX0Ack64 [PCIX0ECC1]	AH06		
PCIX0AD00	AE12		
PCIX0AD01	AE11		
PCIX0AD02	AE10		
PCIX0AD03	AE09		
PCIX0AD04	AF10		
PCIX0AD05	AH08		
PCIX0AD06	AH09		
PCIX0AD07	AA11		
PCIX0AD08	AC09		
PCIX0AD09	AA09		
PCIX0AD10	AC08		
PCIX0AD11	AD08		
PCIX0AD12	AD10		
PCIX0AD13	AA10		
PCIX0AD14	AB10		
PCIX0AD15	AH07	PCI-X0	56
PCIX0AD16	AF06		
PCIX0AD17	AF07		
PCIX0AD18	AE08		
PCIX0AD19	AF05		
PCIX0AD20	AF04		
PCIX0AD21	AD06		
PCIX0AD22	AG04		
PCIX0AD23	AF08		
PCIX0AD24	AH02		
PCIX0AD25	AH03		
PCIX0AD26	AF02		
PCIX0AD27	AE03		
PCIX0AD28	AD04		
PCIX0AD29	AE05		
PCIX0AD30	AE01		
PCIX0AD31	AE02		

Table 3. Signals Listed Alphabetically (Sheet 15 of 30)

Signal Name	Ball	Interface Group	Page
PCIX0AD32	AE18	PCI-X0	56
PCIX0AD33	AF18		
PCIX0AD34	AH19		
PCIX0AD35	AG19		
PCIX0AD36	AD17		
PCIX0AD37	AA18		
PCIX0AD38	W18		
PCIX0AD39	AC20		
PCIX0AD40	AE17		
PCIX0AD41	Y17		
PCIX0AD42	W17		
PCIX0AD43	AA17		
PCIX0AD44	AC19		
PCIX0AD45	AB17		
PCIX0AD46	AC17		
PCIX0AD47	AB19		
PCIX0AD48	AC18		
PCIX0AD49	AH18		
PCIX0AD50	AG16		
PCIX0AD51	AF17		
PCIX0AD52	AF15		
PCIX0AD53	AH15		
PCIX0AD54	AE15		
PCIX0AD55	AD15		
PCIX0AD56	AB14		
PCIX0AD57	AB15		
PCIX0AD58	AA14		
PCIX0AD59	Y15		
PCIX0AD60	W16		
PCIX0AD61	AA16		
PCIX0AD62	AC16		
PCIX0AD63	AA15		

Table 3. Signals Listed Alphabetically (Sheet 16 of 30)

Signal Name	Ball	Interface Group	Page
PCIX0BE0	AF09		
PCIX0BE1	AG10		
PCIX0BE2	AE07		
PCIX0BE3	AE06		
PCIX0BE4	AH16		
PCIX0BE5	AG17		
PCIX0BE6	AE16		
PCIX0BE7	AE14		
PCIX0CalG0	AA08		
PCIX0CalG1	Y19		
PCIX0CalR0	AB08		
PCIX0CalR1	AA19		
PCIX0Cap	AA13		
PCIX0Clk	AF12		
PCIX0DevSel	Y10		
[PCIX0ECC0] PCIX0Par	AG06	PCI-X0	56
[PCIX0ECC1] PCIX0Ack64	AH06		
PCIX0ECC2	AG03		
PCIX0ECC3	AH04		
PCIX0ECC4	AH05		
PCIX0ECC5	AD03		
[PCIX0ECC6] PCIX0Req64	AG08		
[PCIX0ECC7] PCIX0Par64	AH14		
PCIX0Frame	AC12		
PCIX0Gnt0 [GPIO18]	AF14		
PCIX0Gnt1 [GPIO19]	AG13		
PCIX0Gnt2 [GPIO02] [TrcBS1]	AC13		
PCIX0Gnt3 [GPIO03] [TrcBS2]	AF11		
PCIX0IDSel	Y14		
PCIX0INTA	AB12		
PCIX0IRDY	W13		

Table 3. Signals Listed Alphabetically (Sheet 17 of 30)

Signal Name	Ball	Interface Group	Page
PCIX0M66En	AD14	PCI-X0	56
PCIX0Par [PCIX0ECC0]	AG06		
PCIX0Par64 [PCIX0ECC7]	AH14		
$\overline{\text{PCIX0PErr}}$	W11		
$\overline{\text{PCIX0Req0}}$ [GPIO20]	AH11		
$\overline{\text{PCIX0Req1}}$ [GPIO21]	AG12		
$\overline{\text{PCIX0Req2}}$ [GPIO00] [TrcClk]	AA12		
$\overline{\text{PCIX0Req3}}$ [GPIO01] [TrcBS0]	Y12		
$\overline{\text{PCIX0Req64}}$ [PCIX0ECC6]	AG08		
$\overline{\text{PCIX0Reset}}$	AH13		
$\overline{\text{PCIX0SErr}}$	AD12		
$\overline{\text{PCIX0Stop}}$	AE13		
$\overline{\text{PCIX0TRDY}}$	W12		
PCIX0VC	AH10		
PCIX0VRef0	AC11		
PCIX0VRef1	AC10		

Table 3. Signals Listed Alphabetically (Sheet 18 of 30)

Signal Name	Ball	Interface Group	Page
PCIX1Ack64 [PCIX1ECC1]	K23		
PCIX1AD00	D18		
PCIX1AD01	C18		
PCIX1AD02	F18		
PCIX1AD03	A19		
PCIX1AD04	F16		
PCIX1AD05	H20		
PCIX1AD06	F20		
PCIX1AD07	F21		
PCIX1AD08	C17		
PCIX1AD09	D16		
PCIX1AD10	B17		
PCIX1AD11	B16		
PCIX1AD12	E17		
PCIX1AD13	H19		
PCIX1AD14	F19		
PCIX1AD15	G19	PCI-X1	56
PCIX1AD16	A15		
PCIX1AD17	C14		
PCIX1AD18	C15		
PCIX1AD19	A16		
PCIX1AD20	D15		
PCIX1AD21	H17		
PCIX1AD22	G17		
PCIX1AD23	H18		
PCIX1AD24	D13		
PCIX1AD25	B13		
PCIX1AD26	B12		
PCIX1AD27	C12		
PCIX1AD28	E15		
PCIX1AD29	K16		
PCIX1AD30	H16		
PCIX1AD31	J15		

Table 3. Signals Listed Alphabetically (Sheet 19 of 30)

Signal Name	Ball	Interface Group	Page
PCIX1AD32	E28	PCI-X1	56
PCIX1AD33	F28		
PCIX1AD34	F27		
PCIX1AD35	D28		
PCIX1AD36	G28		
PCIX1AD37	M20		
PCIX1AD38	M19		
PCIX1AD39	L23		
PCIX1AD40	A27		
PCIX1AD41	G26		
PCIX1AD42	C27		
PCIX1AD43	D27		
PCIX1AD44	F26		
PCIX1AD45	K22		
PCIX1AD46	K21		
PCIX1AD47	K20		
PCIX1AD48	H25		
PCIX1AD49	J25		
PCIX1AD50	E25		
PCIX1AD51	B26		
PCIX1AD52	E26		
PCIX1AD53	J23		
PCIX1AD54	J21		
PCIX1AD55	H23		
PCIX1AD56	B25		
PCIX1AD57	C24		
PCIX1AD58	D24		
PCIX1AD59	C25		
PCIX1AD60	A26		
PCIX1AD61	A25		
PCIX1AD62	D25		
PCIX1AD63	F24		

Table 3. Signals Listed Alphabetically (Sheet 20 of 30)

Signal Name	Ball	Interface Group	Page
PCIX1BE0	F17	PCI-X1	56
PCIX1BE1	D17		
PCIX1BE2	D14		
PCIX1BE3	E14		
PCIX1BE4	D26		
PCIX1BE5	F25		
PCIX1BE6	G25		
PCIX1BE7	F22		
PCIX1CalG0	L19		
PCIX1CalG1	G14		
PCIX1CalR0	L21		
PCIX1CalR1	H14		
PCIX1Cap	G21		
PCIX1Clk	E21		
PCIX1DevSel	D19		
[PCIX1ECC0] PCIX1Par	K19		
[PCIX1ECC1] PCIX1Ack64	K23		
PCIX1ECC2	H21		
PCIX1ECC3	H22		
PCIX1ECC4	H15		
PCIX1ECC5	F23		
[PCIX1ECC6] PCIX1Req64	H24		
[PCIX1ECC7] PCIX1Par64	A24		
PCIX1Frame	B21		
PCIX1Gnt0 [GPIO22]	B19		
PCIX1Gnt1 [GPIO23]	C19		
PCIX1Gnt2 [GPIO06] [TrcES2]	D21		
PCIX1Gnt3 [GPIO07] [TrcES3]	D23		
PCIX1IDSel	B23		
PCIX1INTA	A22		
PCIX1IRDY	D22		
PCIX1M66En	G23		

Table 3. Signals Listed Alphabetically (Sheet 21 of 30)

Signal Name	Ball	Interface Group	Page
PCIX1Par [PCIX1ECC0]	K19	PCI-X1	56
PCIX1Par64 [PCIX1ECC7]	A24		
$\overline{\text{PCIX1PErr}}$	D20		
$\overline{\text{PCIX1Req0}}$ [GPIO24]	C20		
$\overline{\text{PCIX1Req1}}$ [GPIO25]	C22		
$\overline{\text{PCIX1Req2}}$ [GPIO04] [TrcES0]	C23		
$\overline{\text{PCIX1Req3}}$ [GPIO05] [TrcES1]	E23		
$\overline{\text{PCIX1Req64}}$ [PCIX1ECC6]	H24		
$\overline{\text{PCIX1Reset}}$	A20		
$\overline{\text{PCIX1SErr}}$	A23		
$\overline{\text{PCIX1Stop}}$	C21		
$\overline{\text{PCIX1TRDY}}$	E19		
PCIX1VC	A21		
PCIX1VRef0	J17		
PCIX1VRef1	K17		

Table 3. Signals Listed Alphabetically (Sheet 22 of 30)

Signal Name	Ball	Interface Group	Page
PCIX2AD00	AC03	PCI-X2	56
PCIX2AD01	AC04		
PCIX2AD02	AC05		
PCIX2AD03	AD01		
PCIX2AD04	AB01		
PCIX2AD05	AB04		
PCIX2AD06	AC01		
PCIX2AD07	AC02		
PCIX2AD08	Y04		
PCIX2AD09	AA01		
PCIX2AD10	Y03		
PCIX2AD11	Y01		
PCIX2AD12	AA03		
PCIX2AD13	AA04		
PCIX2AD14	AB06		
PCIX2AD15	AC06		
PCIX2AD16	W02		
PCIX2AD17	W01		
PCIX2AD18	W03		
PCIX2AD19	W04		
PCIX2AD20	V04		
PCIX2AD21	Y06		
PCIX2AD22	Y08		
PCIX2AD23	AA05		
PCIX2AD24	V01		
PCIX2AD25	U03		
PCIX2AD26	T04		
PCIX2AD27	T02		
PCIX2AD28	U04		
PCIX2AD29	W07		
PCIX2AD30	W06		
PCIX2AD31	W05		
$\overline{\text{PCIX2BE0}}$	AB03		
$\overline{\text{PCIX2BE1}}$	AA02		

Table 3. Signals Listed Alphabetically (Sheet 23 of 30)

Signal Name	Ball	Interface Group	Page
PCIX2BE2	V03	PCI-X2	56
PCIX2BE3	U02		
PCIX2CalG0	W08		
PCIX2CalR0	W09		
PCIX2Cap	T08		
PCIX2Clk	R03		
PCIX2DevSel	M03		
[PCIX2ECC0] PCIX2Par	AC07		
PCIX2ECC1	W10		
PCIX2ECC2	AA07		
PCIX2ECC3	U09		
PCIX2ECC4	N01		
PCIX2ECC5	AA06		
PCIX2ECC6	AE04		
PCIX2Frame	U08		
PCIX2Gnt0 [GPIO26]	P01		
PCIX2Gnt1 [GPIO27]	P03		
PCIX2IDSel	T10		
PCIX2INTA	U07		
PCIX2IRDY	P04		
PCIX2M66En	T06		
PCIX2Par [PCIX2ECC0]	AC07		
PCIX2PErr	U06		
PCIX2Req0 [GPIO28]	U05		
PCIX2Req1 [GPIO29]	N04		
PCIX2Reset	V06		
PCIX2SErr	V08		
PCIX2Stop	M02		
PCIX2TRDY	N02		
PCIX2VC	V10		
PCIX2VRef0	R04		
PCIX2VRef1	U10		

Table 3. Signals Listed Alphabetically (Sheet 24 of 30)

Signal Name	Ball	Interface Group	Page
PerAddr00	J04	External Slave Peripheral	59
PerAddr01	K06		
PerAddr02	K05		
PerAddr03	M08		
PerAddr04	L06		
PerAddr05	M07		
PerAddr06	L08		
PerAddr07	K07		
PerAddr08	K08		
PerAddr09	M05		
PerAddr10	N08		
PerAddr11	N06		
PerAddr12	P08		
PerAddr13	P05		
PerAddr14	P07		
PerAddr15	L03		
PerAddr16	L04		
PerAddr17	L01		
PerAddr18	M04		
PerAddr19	K01		
PerAddr20	K02		
PerAddr21	R07		
PerAddr22	R05		
PerAddr23	R08		
$\overline{\text{PerBE0}}$ [GPIO17] [UART2_Tx]	R09		
$\overline{\text{PerBLast}}$	B04		
PerClk	A04		
$\overline{\text{PerCS0}}$	M06		
$\overline{\text{PerCS1}}$ [GPIO09] [TrcTS0]	E12		
$\overline{\text{PerCS2}}$ [GPIO10] [TrcTS1]	H10		

Table 3. Signals Listed Alphabetically (Sheet 25 of 30)

Signal Name	Ball	Interface Group	Page
PerData0	H05	External Slave Peripheral	59
PerData1	J08		
PerData2	H07		
PerData3	D04		
PerData4	G08		
PerData5	E06		
PerData6	G06		
PerData7	J06		
PerErr	B03		
$\overline{\text{PerOE}}$	F12		
PerPar0	C02		
PerReady [GPIO08] [TrcES4]	G12		
PerR/$\overline{\text{W}}$	H06		
$\overline{\text{PerWE}}$	K10		
PSRO	M12	PSRO	62
PSRO	M17		
PSRO	U12		
PSRO	U17		
$\overline{\text{RAS}}$	AH24	DDR SDRAM	58

Table 3. Signals Listed Alphabetically (Sheet 26 of 30)

Signal Name	Ball	Interface Group	Page
Reserved	D07		
Reserved	F09		
Reserved	F13		
Reserved	H08		
Reserved	H09		
Reserved	H13		
Reserved	J10		
Reserved	J12		
Reserved	J14		
Reserved	K09		
Reserved	K11		
Reserved	K12		
Reserved	K13		
Reserved	L10		
Reserved	L12		
Reserved	L14		
Reserved	L15	Reserved	62
Reserved	L17		
Reserved	M09		
Reserved	M10		
Reserved	M11		
Reserved	M13		
Reserved	M14		
Reserved	M15		
Reserved	M16		
Reserved	M18		
Reserved	N10		
Reserved	N12		
Reserved	N17		
Reserved	P09		
Reserved	P11		
Reserved	P12		
Reserved	P17		

Table 3. Signals Listed Alphabetically (Sheet 27 of 30)

Signal Name	Ball	Interface Group	Page
Reserved	P18	Reserved	62
Reserved	R11		
Reserved	R12		
Reserved	R17		
Reserved	R18		
Reserved	T12		
Reserved	T17		
Reserved	U11		
Reserved	U13		
Reserved	U14		
Reserved	U15		
Reserved	U16		
Reserved	U18		
Reserved	V12		
Reserved	V14		
Reserved	V15		
Reserved	V17		
SV_{DD}	P19	Power	62
SV_{DD}	P27		
SV_{DD}	R15		
SV_{DD}	R19		
SV_{DD}	R27		
SV_{DD}	V18		
SV_{DD}	V22		
SV_{DD}	V27		
SV_{DD}	AB27		
SV_{DD}	AF26		
SysClk	J03	System	61
SysErr	J19		
SysPartSel	A14		
$\overline{\text{SysReset}}$	G15		

Table 3. Signals Listed Alphabetically (Sheet 28 of 30)

Signal Name	Ball	Interface Group	Page
TCK	D10	JTAG	61
TDI	A10		
TDO	D11		
TestEn	A18	System	61
TmrClk	D08		
TMS	C10	JTAG	61
[TrcClk] [GPIO00] PCIX0Req2	AA12	Trace	61
[TrcBS0] [GPIO01] PCIX0Req3	Y12		
[TrcBS1] [GPIO02] PCIX0Gnt2	AC13		
[TrcBS2] [GPIO03] PCIX0Gnt3	AF11		
[TrcES0] [GPIO04] PCIX1Req2	C23		
[TrcES1] [GPIO05] PCIX1Req3	E23		
[TrcES2] [GPIO06] PCIX1Gnt2	D21		
[TrcES3] [GPIO07] PCIX1Gnt3	D23		
[TrcES4] [GPIO08] PerReady	G12		
[TrcTS0] PerCS1 [GPIO09]	E12		
[TrcTS1] PerCS2 [GPIO10]	H10		
[TrcTS2] [GPIO11] IRQ0	C07		
[TrcTS3] [GPIO12] IRQ1	C06		
[TrcTS4] [GPIO13] IRQ2	A05		
[TrcTS5] [GPIO14] IRQ3	C05		
[TrcTS6] [GPIO15] IRQ4	D06		
TRST	B10	JTAG	61
UART0_CTS	C09	UART Peripheral	60
UART0_DCD	A08		
UART0_DSR	C11		
UART0_DTR	A11		
UART0_RI	A13		
UART0_RTS	F11		
UART0_Rx	H12		
UART0_Tx	C08		

Table 3. Signals Listed Alphabetically (Sheet 29 of 30)

Signal Name	Ball	Interface Group	Page
$\overline{\text{UART1\_DSR/CTS}}$	F10	UART Peripheral	60
$\overline{\text{UART1\_RTS/DTR}}$	G10		
UART1_Rx [GPIO30]	A07		
UART1_Tx [GPIO31]	A06		
[UART2_Rx] [GPIO16] IRQ5	D05		
[UART2_Tx] [GPIO17] $\overline{\text{PerBE0}}$	R09		
UARTSerClk	A09		
V_{DD}	A12	Power	62
V_{DD}	A17		
V_{DD}	A28		
V_{DD}	E05		
V_{DD}	E09		
V_{DD}	E13		
V_{DD}	E16		
V_{DD}	E20		
V_{DD}	E24		
V_{DD}	J05		
V_{DD}	J09		
V_{DD}	J13		
V_{DD}	J16		
V_{DD}	J20		
V_{DD}	J24		
V_{DD}	M01		
V_{DD}	M28		
V_{DD}	N05		
V_{DD}	N09		
V_{DD}	N13		
V_{DD}	N16		
V_{DD}	N20		
V_{DD}	N24		
V_{DD}	T05		
V_{DD}	T09		

Table 3. Signals Listed Alphabetically (Sheet 30 of 30)

Signal Name	Ball	Interface Group	Page
V_{DD}	T13	Power	62
V_{DD}	T16		
V_{DD}	T20		
V_{DD}	T24		
V_{DD}	U01		
V_{DD}	U28		
V_{DD}	Y05		
V_{DD}	Y09		
V_{DD}	Y13		
V_{DD}	Y16		
V_{DD}	Y20		
V_{DD}	Y24		
V_{DD}	AD05		
V_{DD}	AD09		
V_{DD}	AD13		
V_{DD}	AD16		
V_{DD}	AD20		
V_{DD}	AD24		
V_{DD}	AH01		
V_{DD}	AH12		
V_{DD}	AH17		
V_{DD}	AH28		
$\overline{WE}$	V19	DDR SDRAM	58

Signal List—Ball Assignment Order

In the following table, only the primary (default) signal name is shown for each pin. Multiplexed pins are marked with an asterisk (*). To determine the other signals that share a pin, look up the primary signal name in Table 3 on page 17.

Table 4. Signals Listed by Ball Assignment (Sheet 1 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	No ball	B01	A1GND	C01	$A1V_{DD}$	D01	EMCMDClk
A02	EMCTxD7	B02	GND	C02	PerPar0	D02	EMCCD
A03	EMCTxErr	B03	PerErr	C03	OV_{DD}	D03	EMCRxClk
A04	PerClk	B04	$\overline{\text{PerBLast}}$	C04	EMCTxEn	D04	PerData3
A05	IRQ2*	B05	GND	C05	IRQ3*	D05	IRQ5*
A06	UART1_Tx*	B06	$\overline{\text{HISRRst}}$	C06	IRQ1*	D06	IRQ4*
A07	UART1_Rx*	B07	OV_{DD}	C07	IRQ0*	D07	Reserved
A08	$\overline{\text{UART0\_DCD}}$	B08	EMCGTxClk	C08	UART0_Tx	D08	TmrClk
A09	UARTSerClk	B09	GND	C09	$\overline{\text{UART0\_CTS}}$	D09	IIC0SClk
A10	TDI	B10	$\overline{\text{TRST}}$	C10	TMS	D10	TCK
A11	$\overline{\text{UART0\_DTR}}$	B11	OV_{DD}	C11	$\overline{\text{UART0\_DSR}}$	D11	TDO
A12	V_{DD}	B12	PCIX1AD26	C12	PCIX1AD27	D12	EMCRefClk
A13	$\overline{\text{UART0\_RI}}$	B13	PCIX1AD25	C13	GND	D13	PCIX1AD24
A14	SysPartSel	B14	OV_{DD}	C14	PCIX1AD17	D14	$\overline{\text{PCIX1BE2}}$
A15	PCIX1AD16	B15	OV_{DD}	C15	PCIX1AD18	D15	PCIX1AD20
A16	PCIX1AD19	B16	PCIX1AD11	C16	GND	D16	PCIX1AD09
A17	V_{DD}	B17	PCIX1AD10	C17	PCIX1AD08	D17	$\overline{\text{PCIX1BE1}}$
A18	TestEn	B18	$P1V_{DD}$	C18	PCIX1AD01	D18	PCIX1AD00
A19	PCIX1AD03	B19	$\overline{\text{PCIX1Gnt0}}$*	C19	$\overline{\text{PCIX1Gnt1}}$*	D19	$\overline{\text{PCIX1DevSel}}$
A20	$\overline{\text{PCIX1Reset}}$	B20	GND	C20	$\overline{\text{PCIX1Req0}}$*	D20	$\overline{\text{PCIX1PErr}}$
A21	PCIX1VC	B21	$\overline{\text{PCIX1Frame}}$	C21	$\overline{\text{PCIX1Stop}}$	D21	$\overline{\text{PCIX1Gnt2}}$*
A22	$\overline{\text{PCIX1INTA}}$	B22	$P1V_{DD}$	C22	$\overline{\text{PCIX1Req1}}$*	D22	$\overline{\text{PCIX1IRDY}}$
A23	$\overline{\text{PCIX1SErr}}$	B23	PCIX1IDSel	C23	$\overline{\text{PCIX1Req2}}$*	D23	$\overline{\text{PCIX1Gnt3}}$*
A24	PCIX1Par64*	B24	GND	C24	PCIX1AD57	D24	PCIX1AD58
A25	PCIX1AD61	B25	PCIX1AD56	C25	PCIX1AD59	D25	PCIX1AD62
A26	PCIX1AD60	B26	PCIX1AD51	C26	$P1V_{DD}$	D26	$\overline{\text{PCIX1BE4}}$
A27	PCIX1AD40	B27	GND	C27	PCIX1AD42	D27	PCIX1AD43
A28	V_{DD}	B28	AP1GND	C28	$AP1V_{DD}$	D28	PCIX1AD35

Table 4. Signals Listed by Ball Assignment (Sheet 2 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01	EMCTxClk	F01	EMCTxD1	G01	EMCRxD3	H01	EMCTxD2
E02	GND	F02	EMCTxD0	G02	OV_{DD}	H02	EMCRxD5
E03	EMCCrS	F03	EMCRxD2	G03	EMCTxD3	H03	EMCRxD4
E04	EMCMDIO	F04	EMCRxD0	G04	EMCRxD1	H04	EMCTxD4
E05	V_{DD}	F05	EMCRxD6	G05	GND	H05	PerData0
E06	PerData5	F06	EMCRxD7	G06	PerData6	H06	PerR/$\overline{W}$
E07	GND	F07	EMCRxDV	G07	OV_{DD}	H07	PerData2
E08	IIC0SDA	F08	IIC1SClk	G08	PerData4	H08	Reserved
E09	V_{DD}	F09	Reserved	G09	GND	H09	Reserved
E10	IIC1SDA	F10	$\overline{\text{UART1\_DSR}}/\overline{\text{CTS}}$	G10	$\overline{\text{UART1\_RTS/DTR}}$	H10	$\overline{\text{PerCS2}}$*
E11	GND	F11	$\overline{\text{UART0\_RTS}}$	G11	OV_{DD}	H11	$\overline{\text{ExtReset}}$
E12	$\overline{\text{PerCS1}}$*	F12	$\overline{\text{PerOE}}$	G12	PerReady*	H12	UART0_Rx
E13	V_{DD}	F13	Reserved	G13	GND	H13	Reserved
E14	$\overline{\text{PCIX1BE3}}$	F14	GND	G14	PCIX1CalG1	H14	PCIX1CalR1
E15	PCIX1AD28	F15	GND	G15	$\overline{\text{SysReset}}$	H15	PCIX1ECC4
E16	V_{DD}	F16	PCIX1AD04	G16	GND	H16	PCIX1AD30
E17	PCIX1AD12	F17	$\overline{\text{PCIX1BE0}}$	G17	PCIX1AD22	H17	PCIX1AD21
E18	GND	F18	PCIX1AD02	G18	$P1V_{DD}$	H18	PCIX1AD23
E19	$\overline{\text{PCIX1TRDY}}$	F19	PCIX1AD14	G19	PCIX1AD15	H19	PCIX1AD13
E20	V_{DD}	F20	PCIX1AD06	G20	GND	H20	PCIX1AD05
E21	PCIX1Clk	F21	PCIX1AD07	G21	PCIX1Cap	H21	PCIX1ECC2
E22	GND	F22	$\overline{\text{PCIX1BE7}}$	G22	$P1V_{DD}$	H22	PCIX1ECC3
E23	$\overline{\text{PCIX1Req3}}$*	F23	PCIX1ECC5	G23	PCIX1M66En	H23	PCIX1AD55
E24	V_{DD}	F24	PCIX1AD63	G24	GND	H24	$\overline{\text{PCIX1Req64}}$*
E25	PCIX1AD50	F25	$\overline{\text{PCIX1BE5}}$	G25	$\overline{\text{PCIX1BE6}}$	H25	PCIX1AD48
E26	PCIX1AD52	F26	PCIX1AD44	G26	PCIX1AD41	H26	MemData39
E27	GND	F27	PCIX1AD34	G27	$P1V_{DD}$	H27	MemData36
E28	PCIX1AD32	F28	PCIX1AD33	G28	PCIX1AD36	H28	MemData35

Table 4. Signals Listed by Ball Assignment (Sheet 3 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01	EMCRxErr	K01	PerAddr19	L01	PerAddr17	M01	V_{DD}
J02	GND	K02	PerAddr20	L02	OV_{DD}	M02	$\overline{\text{PCIX2Stop}}$
J03	SysClk	K03	EMCTxD6	L03	PerAddr15	M03	$\overline{\text{PCIX2DevSel}}$
J04	PerAddr00	K04	EMCTxD5	L04	PerAddr16	M04	PerAddr18
J05	V_{DD}	K05	PerAddr02	L05	GND	M05	PerAddr09
J06	PerData7	K06	PerAddr01	L06	PerAddr04	M06	$\overline{\text{PerCS0}}$
J07	GND	K07	PerAddr07	L07	OV_{DD}	M07	PerAddr05
J08	PerData1	K08	PerAddr08	L08	PerAddr06	M08	PerAddr03
J09	V_{DD}	K09	Reserved	L09	GND	M09	Reserved
J10	Reserved	K10	$\overline{\text{PerWE}}$	L10	Reserved	M10	Reserved
J11	GND	K11	Reserved	L11	OV_{DD}	M11	Reserved
J12	Reserved	K12	Reserved	L12	Reserved	M12	PSRO
J13	V_{DD}	K13	Reserved	L13	GND	M13	Reserved
J14	Reserved	K14	OV_{DD}	L14	Reserved	M14	Reserved
J15	PCIX1AD31	K15	OV_{DD}	L15	Reserved	M15	Reserved
J16	V_{DD}	K16	PCIX1AD29	L16	GND	M16	Reserved
J17	PCIX1VRef0	K17	PCIX1VRef1	L17	Reserved	M17	PSRO
J18	GND	K18	$\overline{\text{Halt}}$	L18	$P1V_{DD}$	M18	Reserved
J19	SysErr	K19	PCIX1Par*	L19	PCIX1CalG0	M19	PCIX1AD38
J20	V_{DD}	K20	PCIX1AD47	L20	GND	M20	PCIX1AD37
J21	PCIX1AD54	K21	PCIX1AD46	L21	PCIX1CalR0	M21	DM5
J22	GND	K22	PCIX1AD45	L22	$P1V_{DD}$	M22	MemData42
J23	PCIX1AD53	K23	$\overline{\text{PCIX1Ack64}}$*	L23	PCIX1AD39	M23	MemData41
J24	V_{DD}	K24	MemData45	L24	GND	M24	MemData46
J25	PCIX1AD49	K25	DQS4	L25	DQS5	M25	MemData31
J26	MemData32	K26	$\overline{\text{DQS4}}$	L26	$\overline{\text{DQS5}}$	M26	MemData28
J27	GND	K27	DM4	L27	$P1V_{DD}$	M27	MemData27
J28	MemData37	K28	MemData33	L28	MemData34	M28	V_{DD}

Table 4. Signals Listed by Ball Assignment (Sheet 4 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01	PCIX2ECC4	P01	$\overline{\text{PCIX2Gnt0}}$*	R01	$AP2V_{DD}$	T01	AP2GND
N02	$\overline{\text{PCIX2TRDY}}$	P02	$P2V_{DD}$	R02	$P2V_{DD}$	T02	PCIX2AD27
N03	GND	P03	$\overline{\text{PCIX2Gnt1}}$*	R03	PCIX2Clk	T03	GND
N04	$\overline{\text{PCIX2Req1}}$*	P04	$\overline{\text{PCIX2IRDY}}$	R04	PCIX2VRef0	T04	PCIX2AD26
N05	V_{DD}	P05	PerAddr13	R05	PerAddr22	T05	V_{DD}
N06	PerAddr11	P06	GND	R06	GND	T06	PCIX2M66En
N07	GND	P07	PerAddr14	R07	PerAddr21	T07	GND
N08	PerAddr10	P08	PerAddr12	R08	PerAddr23	T08	PCIX2Cap
N09	V_{DD}	P09	Reserved	R09	$\overline{\text{PerBE0}}$*	T09	V_{DD}
N10	Reserved	P10	OV_{DD}	R10	$P2V_{DD}$	T10	PCIX2IDSel
N11	GND	P11	Reserved	R11	Reserved	T11	GND
N12	Reserved	P12	Reserved	R12	Reserved	T12	Reserved
N13	V_{DD}	P13	GND	R13	GND	T13	V_{DD}
N14	GND	P14	OV_{DD}	R14	$P0V_{DD}$	T14	GND
N15	GND	P15	$P1V_{DD}$	R15	SV_{DD}	T15	GND
N16	V_{DD}	P16	GND	R16	GND	T16	V_{DD}
N17	Reserved	P17	Reserved	R17	Reserved	T17	Reserved
N18	GND	P18	Reserved	R18	Reserved	T18	GND
N19	MemData47	P19	SV_{DD}	R19	SV_{DD}	T19	MemData52
N20	V_{DD}	P20	MemData40	R20	MemData53	T20	V_{DD}
N21	MemData44	P21	MemData38	R21	DM6	T21	MemData55
N22	GND	P22	$\overline{\text{BankSel1}}$	R22	MemData49	T22	GND
N23	MemData43	P23	GND	R23	GND	T23	$\overline{\text{BankSel0}}$
N24	V_{DD}	P24	MemData54	R24	MemData50	T24	V_{DD}
N25	MemData24	P25	MemData29	R25	$\overline{\text{DQS6}}$	T25	MemData19
N26	GND	P26	DM3	R26	DQS6	T26	GND
N27	DQS3	P27	SV_{DD}	R27	SV_{DD}	T27	MemData20
N28	$\overline{\text{DQS3}}$	P28	MemData25	R28	MemData26	T28	MemData23

Table 4. Signals Listed by Ball Assignment (Sheet 5 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01	V_{DD}	V01	PCIX2AD24	W01	PCIX2AD17	Y01	PCIX2AD11
U02	$\overline{\text{PCIX2BE3}}$	V02	$P2V_{DD}$	W02	PCIX2AD16	Y02	GND
U03	PCIX2AD25	V03	$\overline{\text{PCIX2BE2}}$	W03	PCIX2AD18	Y03	PCIX2AD10
U04	PCIX2AD28	V04	PCIX2AD20	W04	PCIX2AD19	Y04	PCIX2AD08
U05	$\overline{\text{PCIX2Req0}}$*	V05	GND	W05	PCIX2AD31	Y05	V_{DD}
U06	$\overline{\text{PCIX2PErr}}$	V06	$\overline{\text{PCIX2Reset}}$	W06	PCIX2AD30	Y06	PCIX2AD21
U07	$\overline{\text{PCIX2INTA}}$	V07	$P2V_{DD}$	W07	PCIX2AD29	Y07	GND
U08	$\overline{\text{PCIX2Frame}}$	V08	$\overline{\text{PCIX2SErr}}$	W08	PCIX2CalG0	Y08	PCIX2AD22
U09	PCIX2ECC3	V09	GND	W09	PCIX2CalR0	Y09	V_{DD}
U10	PCIX2VRef1	V10	PCIX2VC	W10	PCIX2ECC1	Y10	$\overline{\text{PCIX0DevSel}}$
U11	Reserved	V11	$P2V_{DD}$	W11	$\overline{\text{PCIX0PErr}}$	Y11	GND
U12	PSRO	V12	Reserved	W12	$\overline{\text{PCIX0TRDY}}$	Y12	$\overline{\text{PCIX0Req3}}$*
U13	Reserved	V13	GND	W13	$\overline{\text{PCIX0IRDY}}$	Y13	V_{DD}
U14	Reserved	V14	Reserved	W14	$P0V_{DD}$	Y14	PCIX0IDSel
U15	Reserved	V15	Reserved	W15	$P0V_{DD}$	Y15	PCIX0AD59
U16	Reserved	V16	GND	W16	PCIX0AD60	Y16	V_{DD}
U17	PSRO	V17	Reserved	W17	PCIX0AD42	Y17	PCIX0AD41
U18	Reserved	V18	SV_{DD}	W18	PCIX0AD38	Y18	GND
U19	DM7	V19	$\overline{\text{WE}}$	W19	ECC6	Y19	PCIX0CalG1
U20	MemData57	V20	GND	W20	MemData63	Y20	V_{DD}
U21	MemData58	V21	MemData62	W21	MemData60	Y21	ECC2
U22	MemData51	V22	SV_{DD}	W22	MemData56	Y22	GND
U23	MemData48	V23	MemData61	W23	MemData22	Y23	ECC1
U24	MemData30	V24	GND	W24	MemData59	Y24	V_{DD}
U25	$\overline{\text{DQS2}}$	V25	DM2	W25	MemData15	Y25	MemData12
U26	DQS2	V26	MemData21	W26	$\overline{\text{DQS7}}$	Y26	MemData08
U27	MemData16	V27	SV_{DD}	W27	DQS7	Y27	GND
U28	V_{DD}	V28	MemData17	W28	MemData18	Y28	MemData11

Table 4. Signals Listed by Ball Assignment (Sheet 6 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01	PCIX2AD09	AB01	PCIX2AD04	AC01	PCIX2AD06	AD01	PCIX2AD03
AA02	$\overline{\text{PCIX2BE1}}$	AB02	$P2V_{DD}$	AC02	PCIX2AD07	AD02	GND
AA03	PCIX2AD12	AB03	$\overline{\text{PCIX2BE0}}$	AC03	PCIX2AD00	AD03	PCIX0ECC5
AA04	PCIX2AD13	AB04	PCIX2AD05	AC04	PCIX2AD01	AD04	PCIX0AD28
AA05	PCIX2AD23	AB05	GND	AC05	PCIX2AD02	AD05	V_{DD}
AA06	PCIX2ECC5	AB06	PCIX2AD14	AC06	PCIX2AD15	AD06	PCIX0AD21
AA07	PCIX2ECC2	AB07	$P0V_{DD}$	AC07	PCIX2Par*	AD07	GND
AA08	PCIX0CalG0	AB08	PCIX0CalR0	AC08	PCIX0AD10	AD08	PCIX0AD11
AA09	PCIX0AD09	AB09	GND	AC09	PCIX0AD08	AD09	V_{DD}
AA10	PCIX0AD13	AB10	PCIX0AD14	AC10	PCIX0VRef1	AD10	PCIX0AD12
AA11	PCIX0AD07	AB11	$P0V_{DD}$	AC11	PCIX0VRef0	AD11	GND
AA12	$\overline{\text{PCIX0Req2}}$*	AB12	$\overline{\text{PCIX0INTA}}$	AC12	$\overline{\text{PCIX0Frame}}$	AD12	$\overline{\text{PCIX0SErr}}$
AA13	PCIX0Cap	AB13	GND	AC13	$\overline{\text{PCIX0Gnt2}}$*	AD13	V_{DD}
AA14	PCIX0AD58	AB14	PCIX0AD56	AC14	GND	AD14	PCIX0M66En
AA15	PCIX0AD63	AB15	PCIX0AD57	AC15	GND	AD15	PCIX0AD55
AA16	PCIX0AD61	AB16	GND	AC16	PCIX0AD62	AD16	V_{DD}
AA17	PCIX0AD43	AB17	PCIX0AD45	AC17	PCIX0AD46	AD17	PCIX0AD36
AA18	PCIX0AD37	AB18	$P0V_{DD}$	AC18	PCIX0AD48	AD18	GND
AA19	PCIX0CalR1	AB19	PCIX0AD47	AC19	PCIX0AD44	AD19	MemAddr02
AA20	MemVRef0	AB20	GND	AC20	PCIX0AD39	AD20	V_{DD}
AA21	MemVRef1	AB21	MemDCFdbkD	AC21	MemDCFdbkR	AD21	BA0
AA22	MemODT0	AB22	$P0V_{DD}$	AC22	MemODT1	AD22	GND
AA23	ECC5	AB23	MemData14	AC23	ECC3	AD23	ECC4
AA24	DM8	AB24	GND	AC24	ECC0	AD24	V_{DD}
AA25	MemData13	AB25	$\overline{\text{DQS8}}$	AC25	MemData07	AD25	$\overline{\text{DQS0}}$
AA26	DM1	AB26	DQS8	AC26	MemData03	AD26	DQS0
AA27	$\overline{\text{DQS1}}$	AB27	SV_{DD}	AC27	MemData04	AD27	GND
AA28	DQS1	AB28	MemData09	AC28	MemData10	AD28	MemData00

Table 4. Signals Listed by Ball Assignment (Sheet 7 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AE01	PCIX0AD30	AF01	AP0V_{DD}	AG01	AP0GND	AH01	V_{DD}
AE02	PCIX0AD31	AF02	PCIX0AD26	AG02	GND	AH02	PCIX0AD24
AE03	PCIX0AD27	AF03	P2V_{DD}	AG03	PCIX0ECC2	AH03	PCIX0AD25
AE04	PCIX2ECC6	AF04	PCIX0AD20	AG04	PCIX0AD22	AH04	PCIX0ECC3
AE05	PCIX0AD29	AF05	PCIX0AD19	AG05	GND	AH05	PCIX0ECC4
AE06	$\overline{\text{PCIX0BE3}}$	AF06	PCIX0AD16	AG06	PCIX0Par*	AH06	$\overline{\text{PCIX0Ack64}}$*
AE07	$\overline{\text{PCIX0BE2}}$	AF07	PCIX0AD17	AG07	P0V_{DD}	AH07	PCIX0AD15
AE08	PCIX0AD18	AF08	PCIX0AD23	AG08	$\overline{\text{PCIX0Req64}}$*	AH08	PCIX0AD05
AE09	PCIX0AD03	AF09	$\overline{\text{PCIX0BE0}}$	AG09	GND	AH09	PCIX0AD06
AE10	PCIX0AD02	AF10	PCIX0AD04	AG10	$\overline{\text{PCIX0BE1}}$	AH10	PCIX0VC
AE11	PCIX0AD01	AF11	$\overline{\text{PCIX0Gnt3}}$*	AG11	P0V_{DD}	AH11	$\overline{\text{PCIX0Req0}}$*
AE12	PCIX0AD00	AF12	PCIX0Clk	AG12	$\overline{\text{PCIX0Req1}}$*	AH12	V_{DD}
AE13	$\overline{\text{PCIX0Stop}}$	AF13	GND	AG13	$\overline{\text{PCIX0Gnt1}}$*	AH13	$\overline{\text{PCIX0Reset}}$
AE14	$\overline{\text{PCIX0BE7}}$	AF14	$\overline{\text{PCIX0Gnt0}}$*	AG14	P0V_{DD}	AH14	PCIX0Par64*
AE15	PCIX0AD54	AF15	PCIX0AD52	AG15	P0V_{DD}	AH15	PCIX0AD53
AE16	$\overline{\text{PCIX0BE6}}$	AF16	GND	AG16	PCIX0AD50	AH16	$\overline{\text{PCIX0BE4}}$
AE17	PCIX0AD40	AF17	PCIX0AD51	AG17	$\overline{\text{PCIX0BE5}}$	AH17	V_{DD}
AE18	PCIX0AD32	AF18	PCIX0AD33	AG18	P0V_{DD}	AH18	PCIX0AD49
AE19	MemAddr03	AF19	MemAddr11	AG19	PCIX0AD35	AH19	PCIX0AD34
AE20	BA1	AF20	ECC7	AG20	GND	AH20	MemAddr12
AE21	MemAddr01	AF21	MemAddr07	AG21	MemAddr10	AH21	MemAddr13
AE22	MemAddr06	AF22	MemAddr08	AG22	P0V_{DD}	AH22	MemAddr04
AE23	ClkEn0	AF23	MemAddr00	AG23	MemAddr09	AH23	MemAddr05
AE24	ClkEn1	AF24	MemAddr14	AG24	GND	AH24	$\overline{\text{RAS}}$
AE25	BA2	AF25	MemData06	AG25	$\overline{\text{MemClkOut0}}$	AH25	$\overline{\text{CAS}}$
AE26	DM0	AF26	SV_{DD}	AG26	MemClkOut0	AH26	MemClkOut1
AE27	MemData01	AF27	MemData02	AG27	GND	AH27	$\overline{\text{MemClkOut1}}$
AE28	MemData05	AF28	A2V_{DD}	AG28	A2GND	AH28	V_{DD}

Signal Description

The PPC440SP embedded controller is packaged in a 783-ball flip-chip plastic ball grid array (FC-PBGA). The following table describes the package level pinout.

Table 5. Pin Summary

Group	No. of Pins
Signal pins, non-multiplexed	496
Signal pins, multiplexed	32
Total Signal Pins	**528**
AxV_{DD}	2
$APxV_{DD}$	3
AxGND	5
OV_{DD} (3.3V I/Os)	15
PxV_{DD} (3.3V-1.5V PCI)	31
SV_{DD} G(2.5-1.8V SDRAM)	10
V_{DD} (1.5V Logic)	47
GND	92
Total Power Pins	**205**
Reserved	50
Total Pins	**783**

In the table “Signal Functional Description” on page 56, each I/O signal is listed along with a short description of its function. Active-low signals (for example, $\overline{RAS}$) are marked with an overline. Please see “Signals Listed Alphabetically” on page 17 for the pin (ball) number to which each signal is assigned.

Multiplexed Signals

Some signals are multiplexed on the same pin so that the pin can be used for different functions. The signal names shown in Signal Functional Description are not accompanied by signal names that might be multiplexed on the same pin. If you need to know what, if any, signals are multiplexed with a particular signal, look up the name in “Signals Listed Alphabetically” on page 17. It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

Strapping Pins

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Strapping” on page 83). Note that these are *not multiplexed* pins since the function of the pins is not programmable.

Multipurpose Signals

In addition to multiplexing, some pins are also multi-purpose. For example, the PCIX0Ack can function instead as PCIX0ECC1 depending on the PCI interface mode of operation.

Table 6. Signal Functional Description (Sheet 1 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCI-X0:2 Interfaces				
$\overline{\text{PCIX0:1Ack64}}$/PCIX0:1ECC1	Ack64 or ECC1. Normally used as Ack64 indicating that the target can transfer data using 64 bits. or Used as ECC1 for PCI-X mode 2.	I/O	3.3V PCI or 1.5V PCI for mode 2	4
PCIX0:1AD63:00 PCIX2AD31:00	Address/Data bus (bidirectional) for PCI-X0 and PCI-X1. Address/Data bus (bidirectional) for PCI-X 2.	I/O	3.3V PCI or 1.5V PCI for mode 2	
$\overline{\text{PCIX0:1BE7:0}}$ $\overline{\text{PCIX2BE3:0}}$	PCI-X Byte Enables for PCI-X0 and PCI-X1. PCI-X Byte Enables for PCI-X2.	I/O	3.3V PCI or 1.5V PCI for mode 2	
PCIX0:1CalG0:1 PCIX2CalG0	External calibration resistor pads (G) for PCI-X0:2 (one pad for each 32-bit bus group).	I	na	
PCIX0:1CalR0:1 PCIX2CalR0	External calibration resistor pads (R) for PCIX0:2 (one pad for each 32-bit bus group).	I	na	
PCIX0:2Cap	Capable of PCI-X operation. This analog input is sampled to configure PCI and determine the state of the PCIX0:2VC output signal: $0.00V_{DD}$ (0.0V) = Conventional PCI & PCIX0:2VC = 0 $0.49V_{DD}$ (1.6V) = PCI-X DDR 266 Mode 2 & PCIX0:2VC = 1 $0.75V_{DD}$ (2.5V) = PCI-X 66 & PCIX0:2VC = 0 $1.00V_{DD}$ (3.3V) = PCI-X 133 & PCIX0:2VC = 0	I	na	
PCIX0:2Clk	Provides timing to the PCI interface for PCI transactions. **Note:** If the PCI-X interface is not being used, drive this pin with a 3.3V clock signal at a frequency between 1 and 66MHz	I	3.3V PCI	
$\overline{\text{PCIX0:2DevSel}}$	Indicates the driving device has decoded its address as the target of the current access.	I/O	3.3V PCI	4
PCIX0:2ECC5:2 PCIX2ECC1 PCIX2ECC6	ECC check bits 5–2. All ECC bits are valid only for PCIX DDR mode 2. **Note:** See PCIX0:2Par for ECC0. See PCIX0:1Ack64 for ECC1. See PCIX0:1Req64 for ECC6. See PCIX0:1Par64 for ECC7.	I/O	3.3V PCI or 1.5V PCI for mode 2	
$\overline{\text{PCIX0:2Frame}}$	Driven by the current master to indicate beginning and duration of an access.	I/O	3.3V PCI	4
$\overline{\text{PCIX0:2Gnt0:1}}$ $\overline{\text{PCIX0:1Gnt2:3}}$	Indicates that the specified agent is granted access to the bus. When using an external PCI/PCI-X arbiter, connect the external arbiter's Grant line to this signal.	I/O	3.3V PCI	4
PCIX0:2IDSel	Used as a chip select during configuration read and write transactions.	I	3.3V PCI	5
$\overline{\text{PCIX0:2INTA}}$	Level sensitive PCI interrupt.	O	3.3V PCI	
$\overline{\text{PCIX0:2IRDY}}$	Indicates initiating agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	4

Table 6. Signal Functional Description (Sheet 2 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCIX0M66En	Capable of 66MHz operation.	I	3.3V PCI or 1.5V PCI for mode 2	
PCIX1:2M66En	Capable of 66MHz operation.	I	3.3V PCI or 1.5V PCI for mode 2	5
PCIX0:2Par/PCIX0:2ECC0	Even parity indicator or ECC0. Normally used to indicate even parity across PCIAD31:00 and BE3:0. Used as ECC0 for PCIX0:2 mode 2.	I/O	3.3V PCI or 1.5V PCI for mode 2	
PCIX0:1Par64/PCIX0:1ECC7	Even parity indicator or ECC7. Normally used to indicate even parity across PCIAD63:32 and BE7:4 for PCI0 and PCI1. or Used as ECC7 for PCIX0:1 mode 2.	I/O	3.3V PCI or 1.5V PCI for mode 2	
$\overline{\text{PCIX0:2PErr}}$	Reports data parity errors during all PCI transactions except a Special Cycle.	I/O	3.3V PCI	4
$\overline{\text{PCIX0:2Req0:1}}$ $\overline{\text{PCIX0:1Req2:3}}$	An indication to the PCI-X arbiter that the specified agent wishes to use the bus. When using an external PCI/PCI-X arbiter, connect the external arbiter's Request line to this signal.	I/O	3.3V PCI	4
$\overline{\text{PCIX0:1Req64}}$/PCIX0:1ECC6	Request 64-bit transfer or ECC6. Normally used by the current bus master to indicate a 64-bit transfer. or Used as ECC6 for PCIX2 mode 2.	I/O	3.3V PCI or 1.5V PCI for mode 2	4
$\overline{\text{PCIX0:2Reset}}$	Sets PCI device registers and logic to a consistent state.	O	3.3V PCI	
$\overline{\text{PCIX0:2SErr}}$	Reports address parity errors, data parity errors on the Special Cycle command, or other catastrophic system errors.	I/O	3.3V PCI	4
$\overline{\text{PCIX0:2Stop}}$	Indicates the current target is requesting the master to stop the current transaction.	I/O	3.3V PCI	4
$\overline{\text{PCIX0:2TRDY}}$	Indicates the target agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	4
PCIX0:2VC	Voltage control output. Used to control the voltage regulator supplying the PCI I/O voltage. See PCI-XCap signal. 0 = 3.3V (PCI I/O) 1 =1.5V (PCI-X DDR)	O	3.3(1.5)V PCI	
PCIX0:2VRef0:1	Voltage reference input for PCI-X mode 2/DDR (1.5V) I/O. Not used for PCI or PCI-X mode 1.	I	VPCIXDDR	5

Table 6. Signal Functional Description (Sheet 3 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
DDR SDRAM Interface				
BA0:2	Bank Address supporting up to eight internal banks.	O	2.5(1.8)V DDR SDRAM	
$\overline{\text{BankSel0:1}}$	Selects up to two external DDR SDRAM banks.	O	2.5(1.8)V DDR SDRAM	
$\overline{\text{CAS}}$	Column Address Strobe.	O	2.5(1.8)V DDR SDRAM	
ClkEn0:1	Clock Enable. One for each external bank.	O	2.5(1.8)V DDR SDRAM	
DM0:8	Memory write data byte lane masks. MEMDM8 is the byte lane mask for the ECC byte lane.	O	2.5(1.8)V DDR SDRAM	
DQS0:8 $\overline{\text{DQS0:8}}$	Byte lane data strobe. DQS8 is the data strobe for the ECC byte lane. These signals are differential pairs.	I/O	2.5(1.8)V DDR SDRAM DIFF	
ECC0:7	ECC check bits 0:7.	I/O	2.5(1.8)V DDR SDRAM	
MemAddr14:00	Memory address bus. **Note:** MemAddr14 is the most significant bit (msb).	O	2.5(1.8)V DDR SDRAM	
MemClkOut0:1 $\overline{\text{MemClkOut0:1}}$	Subsystem clocks. These signals are differential pairs.	O	2.5(1.8)V DDR SDRAM DIFF	
MemData63:00	Memory data bus. **Note:** MemData63 is the most significant bit (msb).	I/O	2.5(1.8)V DDR SDRAM	
MemDCFdbkD	Feedback driver, for I/O timing measurements.	O	2.5(1.8)V DDR SDRAM	
MemDCFdbkR	Feedback receiver. Connect externally to MemDCFdbkD.	I	2.5(1.8)V DDR SDRAM	
MemODT0:1	Memory on-die termination control.	O	2.5(1.8)V DDR SDRAM	
MemVRef0	Memory reference voltage (SV_{REF}) input.	I	2.5(1.8)V DDR SDRAM Volt Ref Rcv	
MemVRef1	Memory reference voltage (SV_{REF}) supplemental input.	I	2.5(1.8)V DDR SDRAM Volt Ref Sup	
$\overline{\text{RAS}}$	Row Address Strobe.	O	2.5(1.8)V DDR SDRAM	
$\overline{\text{WE}}$	Write Enable.	O	2.5(1.8)V DDR SDRAM	

Table 6. Signal Functional Description (Sheet 4 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Ethernet Interface				
EMCCD	Collision detection.	I	3.3V LVTTL	
EMCCrS	Carrier sense.	I	3.3V LVTTL	
EMCMDClk	Management data clock.	O	3.3V LVTTL	
EMCMDIO	Transfer command and status information between MII and PHY.	I/O	3.3V LVTTL	
EMCRxD0:7	Receive data.	I	3.3V LVTTL	
EMCRxDV	Receive data valid.	I	3.3V LVTTL	
EMCRxErr	Receive error.	I	3.3V LVTTL	
EMCRxClk	Receive clock.	I	3.3V LVTTL	
EMCRefClk	Reference clock.	I	3.3V LVTTL	
EMCTxClk	Transmit clock.	I	3.3V LVTTL	
EMCGTxClk	Ethernet gigabit transmit clock.	O	3.3V LVTTL	
EMCTxD0:7	Transmit data.	O	3.3V LVTTL	
EMCTxEn	Transmit data enabled.	O	3.3V LVTTL	
EMCTxErr,	Transmit error.	O	3.3V LVTTL	
External Slave Peripheral Interface				
PerAddr00:23	Peripheral address bus. **Note:** PerAddr00 is the most significant bit (msb).	O	3.3V LVTTL	1
$\overline{\text{PerBE0}}$	External peripheral data bus byte enable.	O	3.3V LVTTL	1
$\overline{\text{PerBLast}}$	Used by the peripheral controller to indicates the last transfer of a memory access.	O	3.3V LVTTL	
$\overline{\text{PerCS0:2}}$	External peripheral device select.	O	3.3V LVTTL	
PerData0:7	Peripheral data bus. **Note:** PerData0 is the most significant bit (msb).	I/O	3.3V LVTTL	1
$\overline{\text{PerOE}}$	Used by peripheral controller or DMA controller depending upon the type of transfer involved. When the PPC440SP is the bus master, it enables the selected device to drive the bus.	O	3.3V LVTTL	
PerPar0	External peripheral data bus byte parity.	I/O	3.3V LVTTL	1
PerReady	Used by a peripheral slave to indicate it is ready to transfer data.	I	3.3V LVTTL	
PerR/$\overline{\text{W}}$	Used as output by the peripheral controller. High indicates a read from memory, low indicates a write to memory.	O	3.3V LVTTL	1
$\overline{\text{PerWE}}$	Write Enable.	O	3.3V LVTTL	
PerClk	Peripheral clock used by synchronous peripheral slaves.	O	3.3V LVTTL	
PerErr	External error used as an input to record external slave peripheral errors.	I	3.3V LVTTL	1, 5

Table 6. Signal Functional Description (Sheet 5 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
UART Peripheral Interface				
UARTSerClk	Serial clock input that provides an alternative to the internally generated serial clock. Used in cases where the allowable internally generated clock rates are not satisfactory.	I	3.3V LVTTL	1, 4
UART0_Rx	UART0 Receive data.	I	3.3V LVTTL	1, 4
UART0_Tx	UART0 Transmit data.	O	3.3V LVTTL	4
$\overline{\text{UART0\_DCD}}$	UART0 Data Carrier Detect.	I	3.3V LVTTL	6
$\overline{\text{UART0\_DSR}}$	UART0 Data Set Ready.	I	3.3V LVTTL	6
$\overline{\text{UART0\_CTS}}$	UART0 Clear To Send.	I	3.3V LVTTL	1, 4
$\overline{\text{UART0\_DTR}}$	UART0 Data Terminal Ready.	O	3.3V LVTTL	4
$\overline{\text{UART0\_RTS}}$	UART0 Request To Send.	O	3.3V LVTTL	4
$\overline{\text{UART0\_RI}}$	UART0 Ring Indicator.	I	3.3V LVTTL w/pull-up	1, 4
UART1_Rx	UART1 Receive data.	I	3.3V LVTTL	1, 4
UART1_Tx	UART1 Transmit data.	O	3.3V LVTTL	1, 4
$\overline{\text{UART1\_DSR}}$/$\overline{\text{CTS}}$	UART1 Data Set Ready or Clear To Send. The choice is determined by a DCR register bit setting.	I	3.3V LVTTL	1, 4
$\overline{\text{UART1\_DTR/RTS}}$	UART1 Request To Send or Data Terminal Ready. The choice is determined by a DCR register bit setting.	O	3.3V LVTTL	1, 4
UART2_Rx	UART2 Receive data.	I	3.3V LVTTL	1, 4
UART2_Tx	UART2 Transmit data.	O	3.3V LVTTL	1, 4
IIC Peripheral Interface				
IIC0SClk	IIC0 Serial Clock.	I/O	3.3V IIC	1, 2
IIC0SDA	IIC0 Serial Data.	I/O	3.3V IIC	1, 2
IIC1SClk	IIC1 Serial Clock.	I/O	3.3V IIC	1, 2
IIC1SDA	IIC1 Serial Data.	I/O	3.3V IIC	1, 2
Interrupts Interface				
IRQ0:5	External interrupt Requests 0 through 5.	I	3.3V LVTTL	1, 5

Table 6. Signal Functional Description (Sheet 6 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
System Interface				
$\overline{\text{Halt}}$	Halt from external debugger.	I	3.3V LVTTL	1, 4
GPIO00:17	General purpose I/O 0 through 17. To access these functions, software must set DCR register bits.	I/O	3.3V LVTTL	
GPIO18:29	General purpose I/O 18 through 29. To access these functions, software must set DCR register bits.	I/O	3.3V PCI	
GPIO30:31	General purpose I/O 30 through 31. To access these functions, software must set DCR register bits.	I/O	3.3V LVTTL	
SysClk	Main system clock input.	I	3.3V LVTTL	
SysErr	Set to 1 when a machine check is generated.	O	3.3V LVTTL	
SysPartSel	Not used.	I	na	3
$\overline{\text{SysReset}}$	Main system reset. External logic can drive this bidirectional pin low (minimum of 16 cycles) to initiate a system reset. A system reset can also be initiated by software.	I	3.3V LVTTL	1, 2
$\overline{\text{HISRRst}}$	Hardware initiated self-refresh and system reset.	I	3.3V LVTTL	1, 2
$\overline{\text{ExtReset}}$	External Reset. During the PPC440SP's reset phase, this signal is at down level.	O	3.3V LVTTL	
TestEn	Test Enable.	I	3.3V LVTTL	3
TmrClk	Processor timer external input clock.	I	3.3V LVTTL	
JTAG Interface				
TCK	Test Clock.	I	3.3V LVTTL	1
TDI	Test Data In.	I	3.3V LVTTL w/pull-down	4
TDO	Test Data Out.	O	3.3V LVTTL	
TMS	Test Mode Select.	I	3.3V LVTTL with pull-up	1
$\overline{\text{TRST}}$	Test Reset. During chip power-up, this signal must be low from the start of VDD ramp-up until at least 16 SysClk cycles after VDD is stable in order to initialize the JTAG controller.	I	3.3V LVTTL with pull-up	5
Trace Interface				
TrcClk	Trace data capture clock, runs at 1/4 the frequency of the processor.	O	3.3V LVTTL	
TrcBS0:2	Trace branch execution status.	O	3.3V LVTTL	
TrcES0:4	Trace Execution Status is presented every fourth processor clock cycle.	O	3.3V LVTTL	
TrcTS0:6	Additional information on trace execution and branch status.	O	3.3V LVTTL	

Table 6. Signal Functional Description (Sheet 7 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Power				
AxGND	Analog ground.	na	na	
$APxV_{DD}$	Analog voltage—1.5V. Filtered voltages input for PCI PLLs (analog circuits). **Note:** A separate filter for all analog voltages is recommended.	na	na	
AxV_{DD}	Analog voltage—1.5V. Filtered voltages input for system PLLs (analog circuits). **Note:** A separate filter for all analog voltages is recommended.	na	na	
GND	Logic and I/O ground.	na	na	
OV_{DD}	I/O supply (except DDR SDRAM and PCI-X)— 3.3V.	na	na	
PxV_{DD}	PCI-X I/O voltage supply. **Note:** PCI-X operates at 3.3V. PCI-X 266 DDR operates at 1.5V	na	na	
SV_{DD}	DDR SDRAM I/O voltage supply. **Note:** DDR SDRAM operates at 2.5V DDR2 SDRAM operates as 1.8V	na	na	
V_{DD}	Logic voltage supply—1.5V.	na	na	
PSRO				
PSRO	Performance Screen Ring Oscillator. **Note:** All PSRO signals should be connected to logic ground (GND).	na	na	
Reserved				
Reserved	Do not connect voltage, ground, or any signals to these pins.	na	na	

Device Characteristics

Table 7. Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. *Operation at or beyond these maximum ratings can cause permanent damage to the device. None of the performance specifications contained in this document are guaranteed when operating at these maximum ratings.*

Characteristic	Symbol	Value	Unit	Notes
1.5V Supply Voltage (Internal logic)	V_{DD}	0 to +1.6	V	
3.3V Supply Voltage (I/O interface, except DDR SDRAM)	OV_{DD}	0 to +3.6	V	
3.3V Supply Voltage (PCI-X I/O)	PxV_{DD}	0 to +3.6	V	
1.5V Supply Voltage (PCI-X DDR I/O)	PxV_{DD}	0 to +1.6	V	
1.5V Supply Voltages (System PLLs)	AxV_{DD}	0 to +1.6	V	1
1.5V Supply Voltages (PCI-X PLLs)	$APxV_{DD}$	0 to +1.6	V	1
2.5V Supply Voltage (DDR SDRAM logic)	SV_{DD}	0 to +2.7	V	
1.8V Supply Voltage (DDR2 SDRAM logic)	SV_{DD}	0 to +1.95	V	
3.3V LVTTL receivers Input Voltage	V_{IN}	0 to +3.6	V	
Storage temperature range	T_{STG}	-55 to +150	°C	
Case temperature under bias	T_C	-40 to +120	°C	2

Notes:

1. The analog voltages used for the on-chip PLLs can be derived from the logic voltage, but must be filtered before entering the PPC440SP. A separate filter, as shown below, is recommended for each voltage:

2. This value is not a specification of the operational temperature range, it is a stress rating only.

Table 8. Package Thermal Specifications

Thermal resistance values for the PPC440SP package in a convection environment are as follows:

Parameter	Symbol	Airflow ft/min (m/sec)			Unit	Notes
		0 (0)	100 (0.51)	200 (1.02)		
Junction-to-case thermal resistance	θ_{JC}	0.6	0.6	0.6	°C/W	1
Case-to-ambient thermal resistance (w/o heat sink)	θ_{CA}	15.5	13.1	11.9	°C/W	2
		Range				
		Minimum		Maximum		
Junction-to-ball (typical)	θ_{JB}	6.5		6.5	°C/W	3

Notes:

1. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board. For this part the junction temperature and the case temperature are essentially identical.
2. The case-to-ambient thermal resistance is measured in a JEDEC JESD51-6 standard environment; and may not accurately predict thermal performance in production equipment environments. The operational case temperature must be maintained.
3. 6.5 °C/W is the theoretical θ_{JB} using an infinite heat sink. The larger number applies to the module mounted on a 1.8mm thick, 2P card using 1oz. copper power planes, with an effective heat transfer area of 75mm^2.

Table 9. Recommended DC Operating Conditions (Sheet 1 of 3)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage 533 MHz	V_{DD}	+1.4	+1.5	+1.6	V	4
Logic Supply Voltage 667 MHz	V_{DD}	+1.425	+1.5	+1.575	V	4
I/O Supply Voltage	OV_{DD}	+3.0	+3.3	+3.6	V	4
PCI-X I/O Supply Voltage PCI-X DDR	PxV_{DD}	+3.0 1.425	+3.3 1.5	+3.6 1.575	V	4
Voltage Reference Input for PCI-X DDR mode 2	PCIX0VRef0:1	+1.425	+1.5	+1.575	V	4
DDR1 SDRAM Supply Voltage DDR2 SDRAM	SV_{DD}	+2.3 1.7	+2.5 (2.6) 1.8	+2.7 1.9	V	4
System PLL Supply Voltages	AxV_{DD}	+1.4	+1.5	+1.6	V	3
PCI-X PLL Supply Voltages	$APxV_{DD}$	+1.4	+1.5	+1.6	V	3
DDR1 SDRAM Reference Voltage	SV_{REF}	+1.15	+1.25	+1.35	V	3
DDR2 SDRAM Reference Voltage	SV_{REF}	0.49 x SV_{DD}	0.50 x SV_{DD}	0.51 x SV_{DD}	V	

Table 9. Recommended DC Operating Conditions (Sheet 2 of 3)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Input Logic High (2.5V DDR SDRAM)	V_{IH}	SV_{REF}+0.18		SV_{DD}+0.3	V	2
Input Logic High (1.8V DDR2 SDRAM)		SV_{REF}+0.125		SV_{DD}+0.3	V	
Input Logic High (2.5V CMOS, 3.3V tolerant receiver)		1.7			V	
Input Logic High (3.3V PCI-X)		$0.5OV_{DD}$		OV_{DD}+0.5	V	1
Input Logic High (1.5V PCI-X DDR)		V_{REF}+0.10		$V_{I/O}$+0.50	V	1
Input Logic High (3.3V LVTTL)		+2.0		+3.6	V	
Input Logic Low (2.5V DDR SDRAM)	V_{IL}	-0.3		SV_{REF}-0.18	V	
Input Logic Low (1.8V DDR2 SDRAM)		-0.3		SV_{REF}-0.125	V	
Input Logic Low (2.5V CMOS, 3.3V tolerant receiver)				0.7	V	
Input Logic Low (3.3V PCI-X)		-0.5		$0.35OV_{DD}$	V	1
Input Logic Low (1.5V PCI-X DDR)		-0.5		V_{REF}-0.10V	V	1
Input Logic Low (3.3V LVTTL)		0		+0.8	V	
Output Logic High (2.5V DDR SDRAM)	V_{OH}	+1.95		SV_{DD}	V	
Output Logic High (1.8V DDR2 SDRAM)		SV_{DD}-0.45		SV_{DD}	V	
Output Logic High (2.5V CMOS, 3.3V tolerant receiver)		2.0			V	
Output Logic High (3.3V PCI-X)		$0.9OV_{DD}$		OV_{DD}	V	1
Output Logic High (1.5V PCI-X DDR)					V	1
Output Logic High (3.3V LVTTL)		+2.4		OV_{DD}	V	
Output Logic Low (2.5V DDR SDRAM)	V_{OL}	0		0.45	V	
Output Logic Low (1.8V DDR2 SDRAM)		0		0.45	V	
Output Logic Low (2.5V CMOS, 3.3V tolerant receiver)				0.4	V	
Output Logic Low (3.3V PCI-X)				$0.1OV_{DD}$	V	1
Output Logic Low (1.5V PCI-X DDR)					V	1
Output Logic Low (3.3V LVTTL)		0		+0.4	V	
Input Leakage Current (with no internal pull-up or pull-down)	I_{IL1}	0		1	µA	
Input Leakage Current (with internal pull-down)	I_{IL2}	0 (LPDL)		200 (MPUL)	µA	5
Input Leakage Current (with internal pull-up)	I_{IL3}	-150 (LPDL)		0 (MPUL)	µA	5

Table 9. Recommended DC Operating Conditions (Sheet 3 of 3)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Input Max Allowable Overshoot (3.3V LVTTL)	V_{IMAO}			+3.9	V	
Input Max Allowable Undershoot (3.3V LVTTL)	V_{IMAU}	-0.6			V	
Output Max Allowable Overshoot (3.3V LVTTL)	V_{OMAO}			+3.9	V	
Output Max Allowable Undershoot (3.3V LVTTL)	V_{OMAU3}	-0.6			V	
Case Temperature	T_C	-40		+100	°C	6

Notes:

1. PCI-X drivers meet PCI-X specifications.
2. $SV_{REF} = SV_{DD}/2$
3. The analog voltages used for the on-chip PLLs can be derived from the logic voltage, but must be filtered before entering the PPC440SP. See “Absolute Maximum Ratings” on page 63.
4. Power supply sequencing: It is recommended that the 1.5V Vdd of the core reach its nominal value before applying power to the I/Os. Voltage applied to I/Os from an external source must not be allowed to exceed the 0Vdd ramp. A power down cycle must complete (0Vdd and Vdd are below 0.4V) before a new power up cycle is started.
5. LPDL is least positive down level; MPUL is most positive up level.
6. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.

Table 10. Input Capacitance

Parameter	Symbol	Maximum	Unit	Notes
Group 1 (2.5V SSTL I/O)	C_{IN1}	5.2	pF	
Group 2 (3.3V LVTTL I/O)	C_{IN2}	7.1	pF	
Group 3 (PCI-X I/O)	C_{IN3}	5.7	pF	
Group 4 (Receivers)	C_{IN4}	6.9	pF	
Group 5 (3.3V tolerant CMOS I/O)	C_{IN5}	3.4	pF	

Table 11. DC Power Supply Loads

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
V_{DD} (1.5V) active operating current	I_{DD}			3000	mA	2
OV_{DD} (3.3V) active operating current	I_{ODD}			40	mA	2
PxV_{DD} (3.3V) active operating current	I_{PDD}			730	mA	2
PxV_{DD} (1.5V) active operating current	I_{PDD}			1600	mA	
SV_{DD} (2.5V) active operating current	I_{SDD}			1100	mA	2
SV_{DD} (1.8V) active operating current	I_{SDD}			750	mA	2
AxV_{DD} (1.5V) input current	I_{ADD}		33		mA	1, 2
$APxV_{DD}$ (1.5V) input current	I_{APDD}		33		mA	1, 2

Notes:
1. See “Absolute Maximum Ratings” on page 63 for filter recommendations.
2. Valid only for CPU/PLB/OPB = 533.33/133.33/66.66 MHz.

Clock Test Conditions

Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” AC specifications are characterized with V_{DD} = 1.5V, T_C = +85 °C and a 10pF test load as shown in the figure to the right.

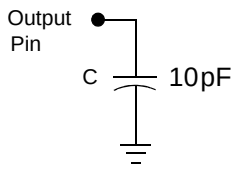
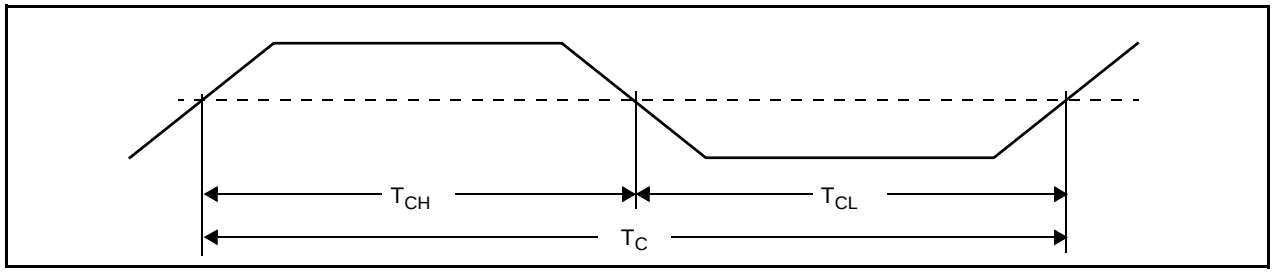


Table 12. Clocking Specifications

Symbol	Parameter	Min	Max	Units
SysClk Input				
F_C	Frequency	33.33	83.33	MHz
T_C	Period	12	30	ns
T_{CS}	Edge stability (cycle-to-cycle jitter)	–	±0.15	ns
T_{CH}	High time	40% of nominal period	60% of nominal period	ns
T_{CL}	Low time	40% of nominal period	60% of nominal period	ns
Note: Input slew rate ≥ 1 V/ns				
PLL VCO				
F_C	Frequency	600	1333.33	MHz
T_C	Period	0.75	1.66	ns
Processor Clock (CPU Clock)				
F_C	Frequency	400	666.66	MHz
T_C	Period	1.5	2.5	ns
MemClkOut				
F_C	Frequency	200	333.33	MHz
T_C	Period	3	5	ns
T_{CH}	High time	45% of nominal period	55% of nominal period	ns
OPB Clock and PerClk				
F_C	Frequency	–	83.33	MHz
T_C	Period	12	–	ns
MAL Clock				
F_C	Frequency	45	83.33	MHz
T_C	Period	12	22.2	ns

Figure 4. Clock Timing Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the PPC440SP. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the PPC440SP the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC440SP with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed -1%, and the modulation frequency cannot exceed 40 kHz. In some cases, on-board PPC440SP peripherals impose more stringent requirements.
- Use the Peripheral Bus Clock for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the DDR SDRAM MemClkOut since it also tracks the modulation.
- For PCI-X and PCI 66 the maximum spread spectrum is -1% modulated between 30 kHz and 33kHz.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates.
2. Ethernet operation is unaffected.
3. IIC operation is unaffected.

Important: It is up to the system designer to ensure that any SSCG used with the PPC440SP meets the above requirements and does not adversely affect other aspects of the system.

I/O Specifications

Table 13. Peripheral Interface Clock Timings

Parameter	Min	Max	Units	Notes
PCIXxClk input frequency (asynchronous mode)	–	133.33	MHz	2
PCIXxClk period (asynchronous mode)	7.5	–	ns	
PCIXxClk input high time	40% of nominal period	60% of nominal period	ns	
PCIXxClk input low time	40% of nominal period	60% of nominal period	ns	
EMCMDClk output frequency	–	2.5	MHz	
EMCMDClk period	400	–	ns	
EMCMDClk output high time	160	–	ns	
EMCMDClk output low time	160	–	ns	
EMCTxClk input frequency	2.5	25	MHz	
EMCTxClk period	40	400	ns	
EMCTxClk input high time	35% of nominal period	–	ns	
EMCTxClk input low time	35% of nominal period	–	ns	
EMCRxClk input frequency	2.5	25	MHz	
EMCRxClk period	40	400	ns	
EMCRxClk input high time	35% of nominal period	–	ns	
EMCRxClk input low time	35% of nominal period	–	ns	
PerClk output frequency (for sync. slaves)	–	83.33	MHz	
PerClk period	12	–	ns	
PerClk output high time	50% of nominal period	66% of nominal period	ns	
PerClk output low time	33% of nominal period	50% of nominal period	ns	
UARTSerClk input frequency	–	$1000/(2T_{OPB}+2ns)$	MHz	1
UARTSerClk period	$2T_{OPB}+2$	–	ns	1
UARTSerClk input high time	$T_{OPB}+1$	–	ns	1
UARTSerClk input low time	$T_{OPB}+1$	–	ns	1
TmrClk input frequency	–	100	MHz	
TmrClk period	10	–	ns	
TmrClk input high time	40% of nominal period	60% of nominal period	ns	
TmrClk input low time	40% of nominal period	60% of nominal period	ns	

Notes:

1. T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at an integral divisor ratio of the frequency of the PLB clock. The maximum OPB clock frequency is 83.33 MHz. Refer to the Clocking chapter of the *PPC440SP Embedded Processor User's Manual* for details.
2. When the PCI-X interface is used to support a legacy PCI interface, the maximum PCIXClk frequency is 66.66 MHz.

Input/Output Timing

These timing diagrams illustrate the relationship of the timing parameters defined in the I/O Specification tables that follow.

Figure 5. Input Setup and Hold Timing Waveform

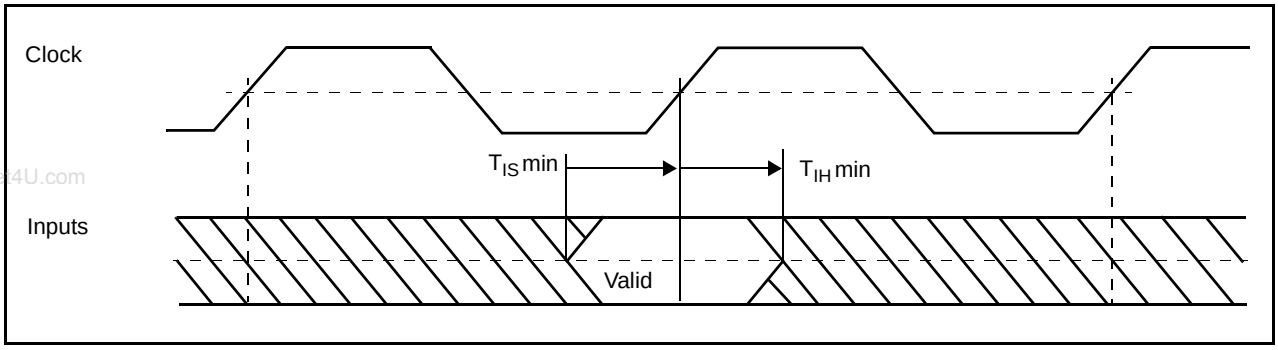


Figure 6. Output Delay and Hold Timing Waveform

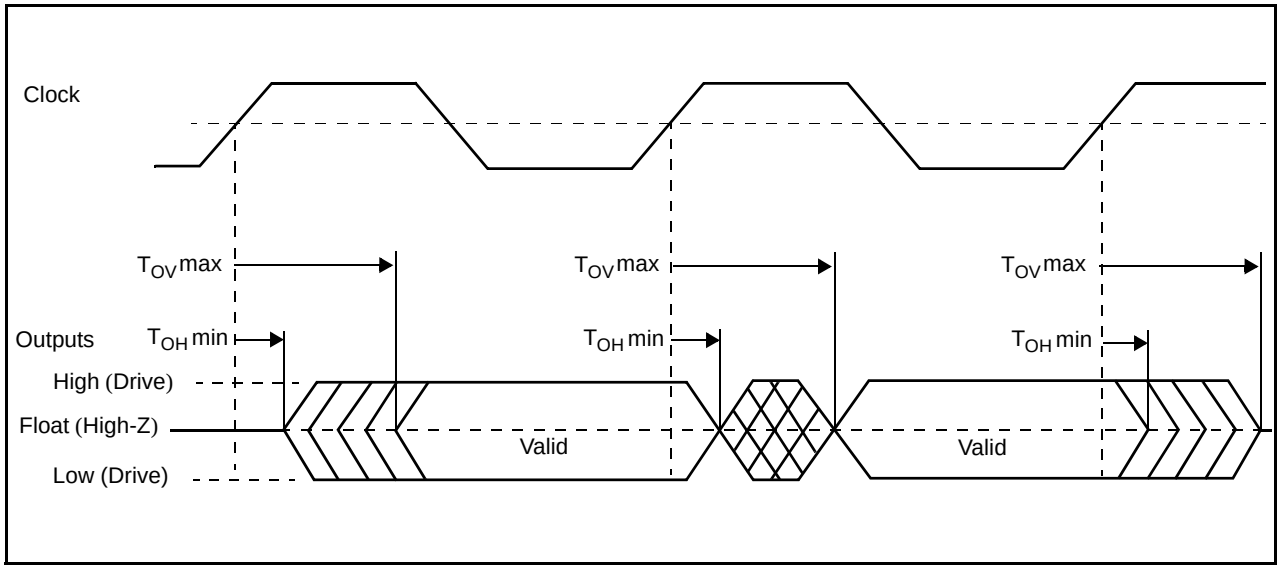


Table 14. I/O Specifications—All Speeds

(Sheet 1 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133.33MHz. PCI-X input setup time requirement is 1.2ns for 133.33MHz and 1.7ns for 66.66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66.66MHz. PCI output hold time requirement is 1ns for 66.66MHz and 2ns for 33.33MHz.
3. These are DDR signals that can change on both the positive and negative clock transitions.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
PCI-X Interfaces								
PCIX0:2Ack64	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:1AD63:00 PCIX2AD31:00	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:1BE7:0 PCIX2BE3:0	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2CalG0:1	Note 2 (2)	0.5(0)	na	na	na	na	PCIX0:2Clk	2
PCIX0:1CalR0:1	dc	dc	na	na	na	na		async
PCIX0:2Cap	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2Clk	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2DevSel	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2ECC5:2	na	na	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2Frame	na	na	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2Gnt0	na	na	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2Gnt1	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:1Gnt2:3	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2IDSel	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2INTA	Note 2 (2)	0.5(0)	na	na	na	na	PCIX0:2Clk	2
PCIX0:2IRDY	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:1M66En	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2Par	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:1Par64	Note 2 (2)	0.5(0)	na	na	na	na	PCIX0:2Clk	2
PCIX0:2PErr	Note 2 (2)	0.5(0)	na	na	na	na	PCIX0:2Clk	2
PCIX0:1Req0	Note 2 (2)	0.5(0)	na	na	na	na	PCIX0:2Clk	2
PCIX0:1Req1:3 PCIX2Req1	na	na	na	na	na	na	PCIX0:2Clk	2
PCIX0:2Req64	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2Reset	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2SErr	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2Stop	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2TRDY	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2
PCIX0:2VC	Note 2 (2)	0.5(0)	3.5(6)	0.7 (Note 2)	0.5	1.5	PCIX0:2Clk	2

Table 14. I/O Specifications—All Speeds

(Sheet 2 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133.33MHz. PCI-X input setup time requirement is 1.2ns for 133.33MHz and 1.7ns for 66.66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66.66MHz. PCI output hold time requirement is 1ns for 66.66MHz and 2ns for 33.33MHz.
3. These are DDR signals that can change on both the positive and negative clock transitions.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
Ethernet Interface								
EMCCD			na	na	19.1	8.7		1, async
EMCCrS			na	na	19.1	8.7		1, async
EMCMDClk	na	na	na	na	19.1	8.7		1, async
EMCMDIO					19.1	8.7	EMCMDClk	
EMCRxD0:7	4	1	na	na	19.1	8.7	EMCRxClk	
EMCRxDV	4	1	na	na	19.1	8.7	EMCRxClk	
EMCRxErr			na	na	19.1	8.7	EMCRxClk	
EMCRxClk			na	na	19.1	8.7		1, async
EMCRefClk			na	na	19.1	8.7		
EMCTxClk	na	na	na	na	19.1	8.7		1, async
EMCGTxClk	na	na	na	na	19.1	8.7		1, async
EMCTxD0:7	na	na	15	2	19.1	8.7	EMCTxClk	
EMCTxEn	na	na	15	2	19.1	8.7	EMCTxClk	
EMCTxErr,	na	na	15	2	19.1	8.7	EMCTxClk	
Internal Peripheral Interface								
IIC0SClk	na	na	na	na	15.3	10.2		
IIC0SDA					15.3	10.2	IIC0SClk	
IIC1SClk	na	na	na	na	15.3	10.2		
IIC1SDA					15.3	10.2	IIC0SClk	
UARTSerClk	na	na	na	na	19.1	8.7		
UART0_Rx			na	na			UARTSerClk	
UART0_Tx	na	na			19.1	8.7	UARTSerClk	
UART0_DCD			na	na	19.1	8.7	async	
UART0_DSR			na	na	19.1	8.7	async	
UART0_CTS			na	na	19.1	8.7	async	
UART0_DTR	na	na			19.1	8.7	async	
UART0_RI			na	na			async	
UART0_RTS	na	na			19.1	8.7	async	
UART1_Rx			na	na	19.1	8.7	UARTSerClk	
UART1_Tx	na	na			19.1	8.7	UARTSerClk	
UART1_DSR/CTS			na	na	19.1	8.7	async	
UART1_RTS/DTR	na	na			19.1	8.7	async	
UART2_Rx			na	na	19.1	8.7	UARTSerClk	
UART2_Tx	na	na			19.1	8.7	UARTSerClk	
Interrupts Interface								
IRQ0:5					na	na	async	
JTAG Interface								
TDI			n/a	n/a	n/a	n/a	async	
TMS			n/a	n/a	n/a	n/a	async	
TDO	n/a	n/a			19.1	8.7	async	
TCK			n/a	n/a	n/a	n/a	async	
TRST			n/a	n/a	n/a	n/a	async	

Table 14. I/O Specifications—All Speeds

(Sheet 3 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PCI-X timings are for asynchronous operation up to 133.33MHz. PCI-X input setup time requirement is 1.2ns for 133.33MHz and 1.7ns for 66.66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66.66MHz. PCI output hold time requirement is 1ns for 66.66MHz and 2ns for 33.33MHz.
3. These are DDR signals that can change on both the positive and negative clock transitions.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
System Interface								
Halt			n/a	n/a	n/a	n/a	async	
GPIO00:31					19.1	8.7	async	
SysClk			n/a	n/a	n/a	n/a	n/a	
SysErr	n/a	n/a			19.1	8.7	async	
SysPartSel			n/a	n/a	n/a	n/a	async	
SysReset					n/a	n/a	async	
HISRRst					19.1	8.7	async	
TestEn			n/a	n/a	n/a	n/a	async	
TmrClk			n/a	n/a	n/a	n/a	n/a	
Trace Interface								
TrcClk	n/a	n/a			19.1	8.7		
TrcBS0:2					19.1	8.7		
TrcES0:4					19.1	8.7		
TrcTS0:6					19.1	8.7		

Table 15. I/O Specifications—533MHz

Notes:
1. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 1.3ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
External Slave Peripheral Interface								
PerAddr00:23	n/a	1	6.2	0	19.1	8.7	PerClk	
PerBE0					27.7	12.8	PerClk	
PerBLast	n/a	1	5.7	n/a	19.1	8.7	PerClk	
PerCS0:2	n/a	n/a	5.9	0	19.1	8.7	PerClk	
PerData0:7	1.2	1	6	0	19.1	8.7	PerClk	
PerOE	n/a	n/a	5.8	0	19.1	8.7	PerClk	
PerPar0	1.7	1	5.7	n/a	19.1	8.7	PerClk	
PerReady	3.6	1	n/a	n/a	19.1	8.7	PerClk	
PerR/W	n/a	1	5.7	n/a	19.1	8.7	PerClk	
PerWE	n/a	n/a	5.7	0	19.1	8.7	n/a	
ExtReset	n/a	n/a	n/a	n/a	19.1	8.7	PerClk	
PerClk	n/a	n/a	n/a	n/a	19.1	8.7	PLB clk	
PerErr	1.2		n/a	n/a	19.1	8.7	PerClk	

DDR SDRAM I/O Specifications

The DDR SDRAM controller times its operation with internal PLB clock signals and generates MemClkOut0 from the PLB clock. The PLB clock is an internal signal that cannot be directly observed. However MemClkOut0 is the same frequency as the PLB clock signal and is in phase with the PLB clock signal.

Note: MemClkOut0 can be advanced with respect to the PLB clock by means of the SDRAM0_CLKTR programming register. In a typical system, users advance MemClkOut by 90×. This depends on the specific application and requires a thorough understanding of the memory system in general (refer to the DDR SDRAM controller chapter in the *PPC440SP Embedded Processor User's Manual*).

In the following sections, the label MemClkOut0(0) refers to MemClkOut0 when it has not been phase-shifted, and MemClkOut0(90) refers to MemClkOut0 when it has been phase-advanced 90°. Advancing MemClkOut0 by 90° creates a 3/4 cycle setup time and 1/4 cycle hold time for the address and control signals in relation to MemClkOut0(90). The rising edge of MemClkOut0(90) aligns with the first rising edge of the DQS signal.

The following DDR data is generated by means of *simulation* and includes logic, driver, package RLC, and lengths. It is *not* to be used as a circuit design recommendation. Values are calculated over best case and worst case processes with speed, temperature, and voltage as follows:

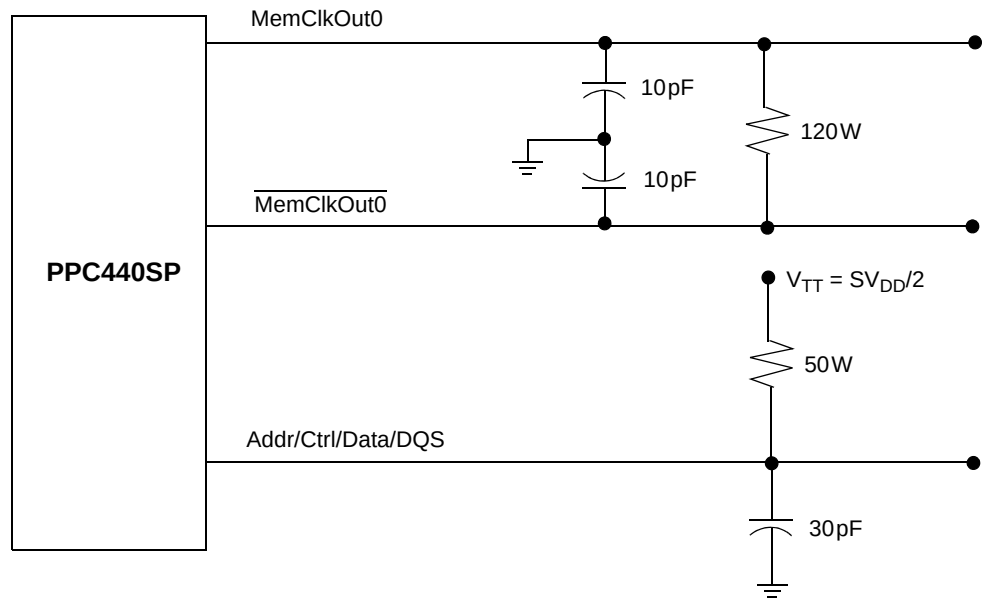
Best Case = Fast process, -40×C, +1.6V

Worst Case = Slow process, +85×C, +1.4V

Note: In all the following DDR tables and timing diagrams, *minimum* values are measured under *best* case conditions and *maximum* values are measured under *worst* case conditions.

The signals are terminated as indicated in the figure below for the DDR timing data in the following sections.

Figure 7. DDR SDRAM Simulation Signal Termination Model



Note: This diagram illustrates the model of the DDR SDRAM interface used when generating simulation timing data. It is *not* a recommended physical circuit design for this interface. An actual interface design will depend on many factors, including the type of memory used and the board layout.

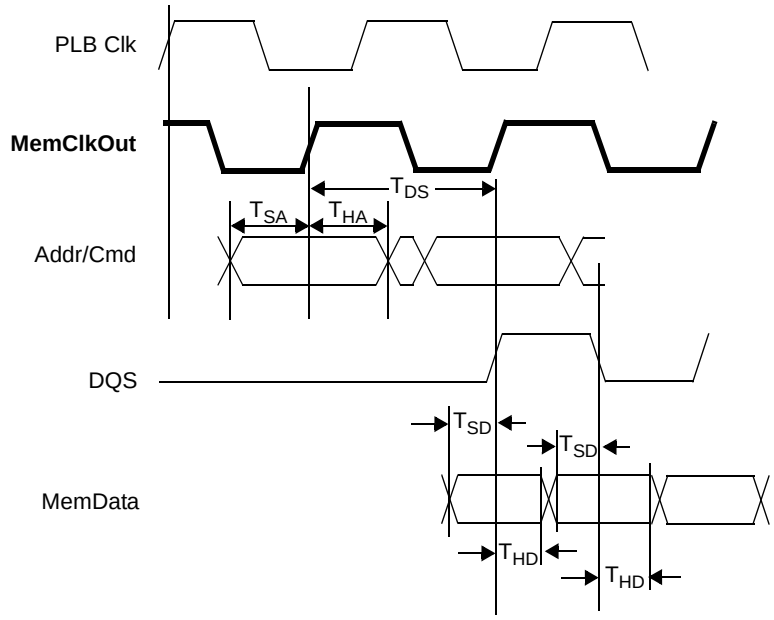
Table 16. DDR SDRAM Output Driver Specifications

Signal Path	Output Current (mA)	
	I/O H (maximum)	I/O L (minimum)
Write Data		
MemData00:07	15.2	15.2
MemData08:15	15.2	15.2
MemData16:23	15.2	15.2
MemData24:31	15.2	15.2
MemData32:39	15.2	15.2
MemData40:47	15.2	15.2
MemData48:55	15.2	15.2
MemData56:63	15.2	15.2
ECC0:7	15.2	15.2
DM0:8	15.2	15.2
MemClkOut0	15.2	15.2
MemAddr00:12	15.2	15.2
BA0:1	15.2	15.2
$\overline{\text{RAS}}$	15.2	15.2
$\overline{\text{CAS}}$	15.2	15.2
$\overline{\text{WE}}$	15.2	15.2
$\overline{\text{BankSel0:3}}$	15.2	15.2
ClkEn0:3	15.2	15.2
DQS0:8	15.2	15.2

DDR SDRAM Write Operation

The following timing chart shows the relationship between the signals involved in a DDR write operation.

Figure 8. DDR SDRAM Write Cycle Timing



T_{SA} = Setup time for address and command signals to MemClkOut
T_{HA} = Hold time for address and command signals from MemClkOut
T_{SD} = Setup time for data signals (minimum time data is valid *before* rising/falling edge of DSQ)
T_{HD} = Hold time for data signals (minimum time data is valid *after* rising/falling edge of DSQ)
T_{DS} = Delay from rising/falling edge of clock to the rising/falling edge of DQS

DDR SDRAM Read and Write I/O Timing—T_{SA} and T_{HA}

Note 1: Clock speed is 333 MHz. T_{SA} and T_{HA} are referenced to MemClkOut.

Note 2: Memory clock signal is shifted by 90° from the internal clock.

Table 17. DDR SDRAM Read and Write I/O Timing—T_{SA} and T_{HA}

Signal Name	T_{SA} (ns)	T_{HA} (ns)
	Minimum	Minimum
MemAddr00:12	1.32	1.2
BA0:1	1.15	1.49
BankSel0:3	1.12	1.52
ClkEn0:3	1.29	1.45
$\overline{CAS}$	1.24	1.14
$\overline{RAS}$	1.29	1.48
$\overline{WE}$	1.35	1.43

DDR SDRAM Clock to Write DQS Timing—T_{DS}

Note 1: All of the DQS signals are referenced to MemClkOut.

Note 2: Clock speed is 333 MHz.

Note 3: The TDS values in the table include 1.5 × 3ns cycle at 333 MHz (3 ns × 1.5 = 4.5 ns).

Note 4: To obtain adjusted values for lower clock frequencies, subtract 4 ns from the values in the following table and add × 1.5 of the cycle time for the lower clock frequency (T_{DS} - 4.5 + 1.5 T_{CYC}).

Table 18. DDR SDRAM Clock to Write DQS Timing—T_{DS}

Signal Name	T_{DS} (ns)	
	Minimum	Maximum
DQS0	4.76	5.07
DQS1	4.78	5.09
DQS2	4.78	5.10
DQS3	4.76	5.07
DQS4	4.79	5.11
DQS5	4.80	5.13
DQS6	4.81	5.11
DQS7	4.79	5.11
DQS8	4.77	5.07

DDR SDRAM Write Data to DQS Timing—T_{SD} and T_{HD}

Note 1: T_{SD} and T_{HD} are measured under worst-case conditions.

Note 2: Clock speed for the values in the following table is 333 MHz.

Table 19. DDR SDRAM Write Data to DQS Timing—T_{SD} and T_{HD}

Signal Name	Reference Signal	T_{SD} (ns)	T_{HD} (ns)
MemData00:07, DM0	DQS0	0.58	0.64
MemData08:15, DM1	DQS1	0.62	0.55
MemData16:23, DM2	DQS2	0.62	0.60
MemData24:31, DM3	DQS3	0.63	0.57
MemData32:39, DM4	DQS4	0.68	0.54
MemData40:47, DM5	DQS5	0.67	0.52
MemData48:55, DM6	DQS6	0.62	0.61
MemData56:63, DM7	DQS7	0.65	0.55
ECC0:7, DM8	DQS8	0.63	0.61

DDR SDRAM Read Operation

The read of the incoming data from the SDRAM is done on the rising and falling edges of the differential DQS signal. The data must be centered on these edges for correct operation.

The PPC440SP can delay in very small increments the DQS by means of the programming of the MCIF0_RODC[RQFD] register field.

DDR SDRAM MemClkOut0 and Read Clock Delay

To accommodate timing variations introduced by the system designs using this chip, the three-stage data path shown in Figure 9, below, is used to eliminate metastability and allow data sampling to be adjusted for minimum latency. The data is stored in the eight Flip Flops of Stage 1, so that it can be transferred later, within an 8X period.

Figure 9. DDR SDRAM Read Data Path.

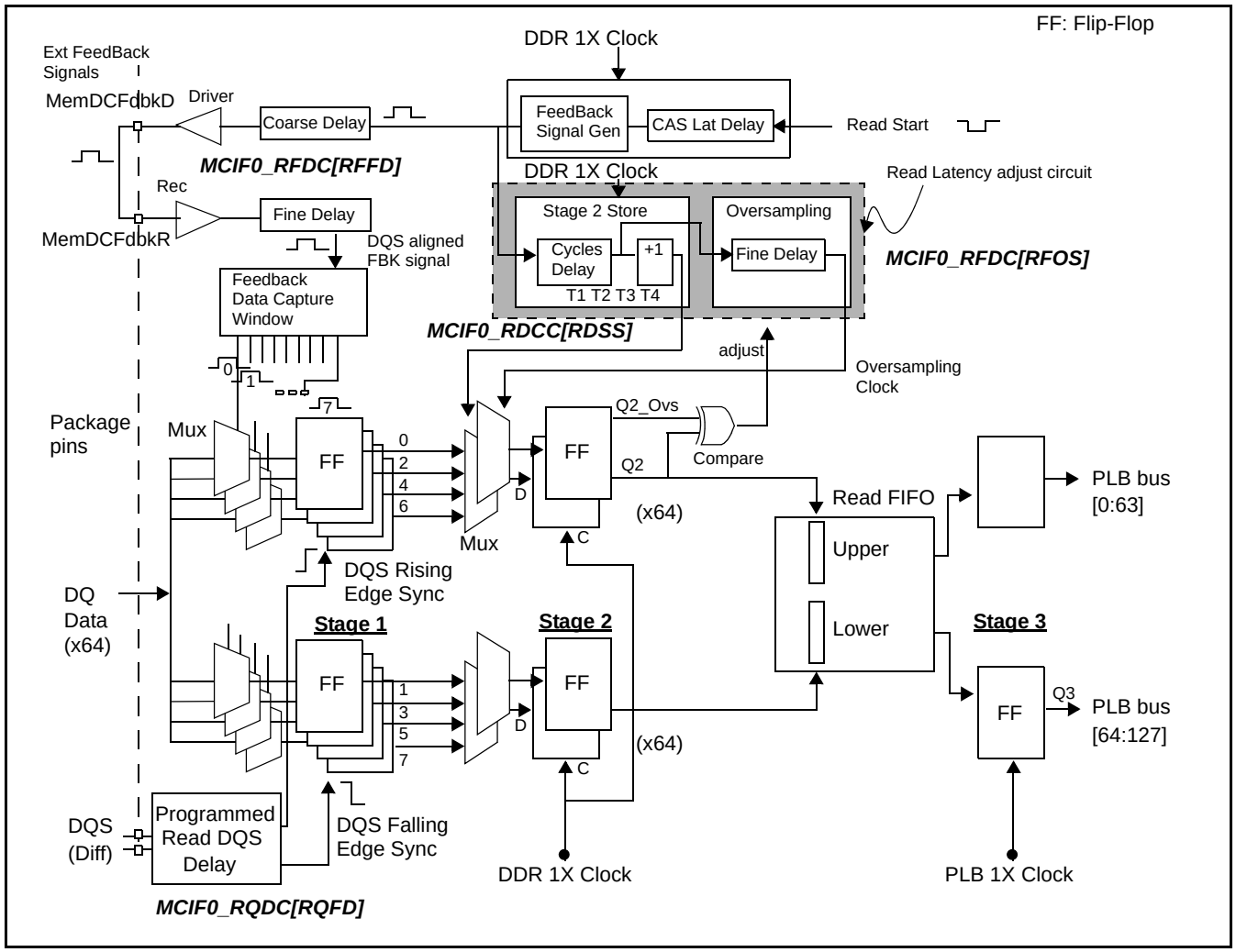


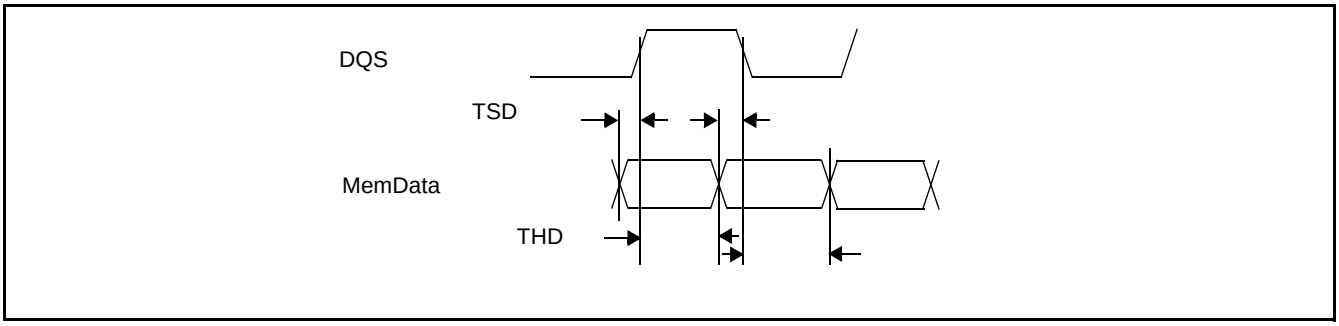
Table 20. DDR SDRAM I/O Read Timing—T_{SD} and T_{HD}

Notes:
1. T_{SD} and T_{HD} are measured under worst case conditions.
2. Clock speed for the values in the table is 333.33 MHz.
3. The time values in the table include 1/4 of a cycle at 166 MHz (3 ns x 0.25 = 0.75 ns).
4. To obtain adjusted T_{SD} and T_{HD} values for lower clock frequencies, subtract 0.75 ns from the values in the table and add 1/4 of the cycle time for the lower clock frequency (e.g., T_{SD} - 0.75 + 0.25T_{CYC}).

Signal Names	Reference Signal	Read Data vs DQS Setup T_{SD} (ns)	Read Data vs DQS Hold T_{HD} (ns)
MemData00:07	DQS0	0.00	1.00
MemData08:15	DQS1	0.00	1.00
MemData16:23	DQS2	0.00	1.00
MemData24:31	DQS3	0.00	1.00
MemData32:39	DQS4	0.00	1.00
MemData40:47	DQS5	0.00	1.00
MemData48:55	DQS6	0.00	1.00
MemData56:63	DQS7	0.00	1.00
ECC0:7	DQS8	0.00	1.00

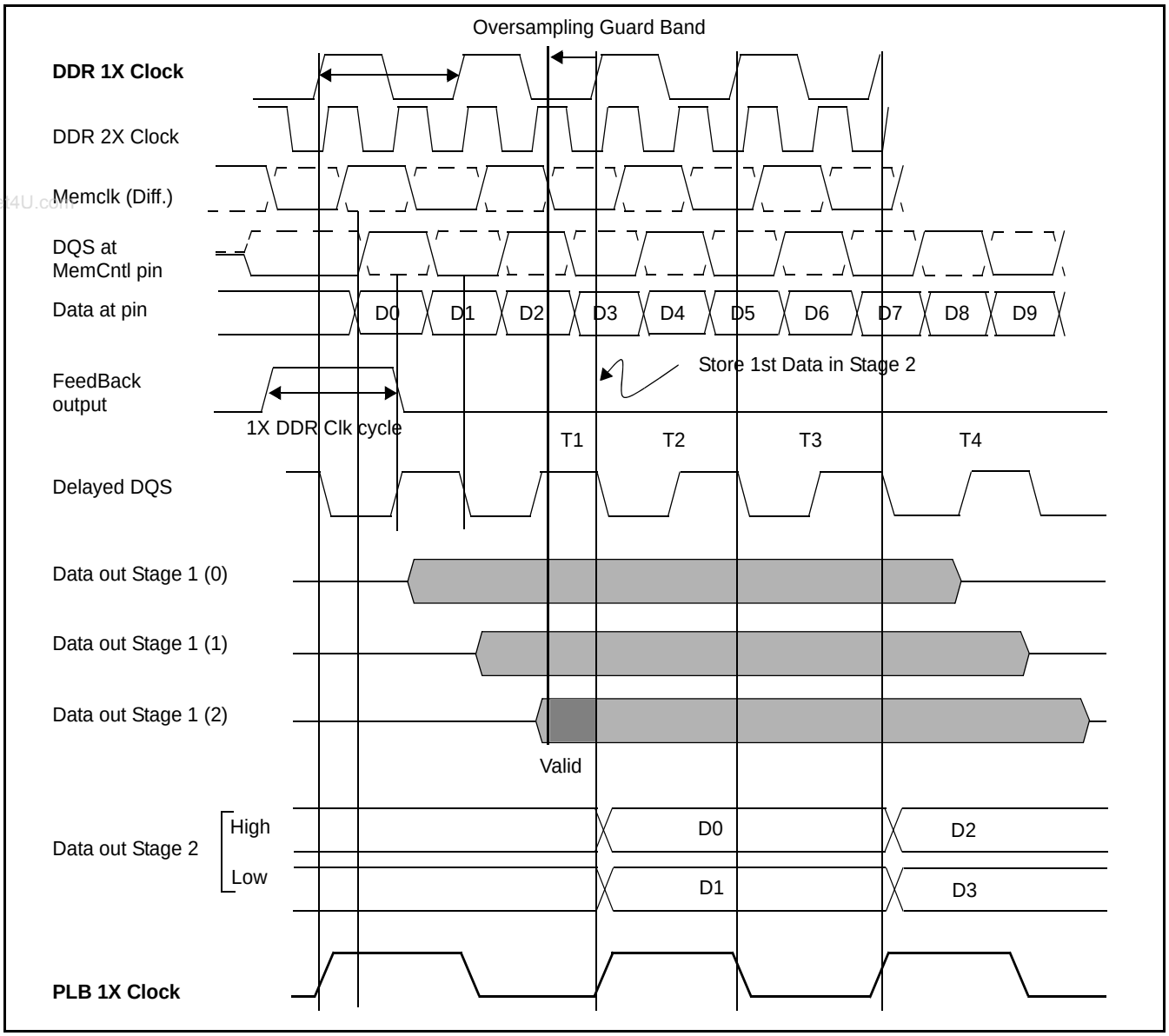
Figure 10 shows the data strobe (DQS) and the data to be coincident. There is actually a slight skew as specified by the SDRAM specifications, and there can be additional skew due to loading and signal routing. It is recommended that the signal length for all of the eight DQS signals be matched.

Figure 10. DDR SDRAM Memory Data and DQS



The following figure shows the timing relationship between SDRAM DDR Data at the input pin and the store of the data in stage 1.

Figure 11. DDR SDRAM Read Cycle Timing Example



Initialization

The PPC440SP provides an option for setting initial parameters based on default values or by reading them from a serial “bootstrap” ROM attached to the IIC0 bus. These options are defined by strapping on three external pins (see “Strapping” below).

Strapping

While the SysReset input pin is low (system reset), the state of certain I/O pins is read to enable certain default initial conditions prior to PPC440SP start-up. The actual capture instant is the nearest SysClk edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. They are used for strap functions only during reset. Following reset they are used for normal functions.

Figure 21 lists the strapping pins along with their functions and strapping options:

Table 21. Strapping Pin Assignments

Function	Option	Pin Strapping		
		Bit 0 A08 (UART0_DCD)	**Bit 1 C11** (UART0_DSR)	**Bit2 C09** (UART0_CTS)
Serial Bootstrap ROM is disabled (Bit 0 off). Refer to the IIC Bootstrap Controller chapter in the *PPC440SP Embedded Processor User’s Manual* for details.	Boot from EBC	0	0	
	Boot from PCI	0	1	
Serial Bootstrap ROM is enabled (Bit 0 on). The options being selected are the IIC0 slave address that responds with strapping data and reading *128 bits* from the Bootstrap ROM.	0x54	1	0	0
	0x50	1	1	0
Serial Bootstrap ROM is enabled (Bit 0 on). The options being selected are the IIC0 slave address that responds with strapping data and reading *256 bits* from the Bootstrap ROM.	0x54	1	0	1
	0x50	1	1	1

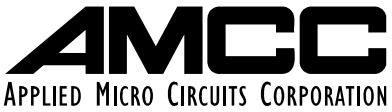
Serial Bootstrap ROM

During reset, if the serial device is enabled, initial conditions can be read from a ROM connected to the IIC0 port. In this case, at the de-assertion of SysReset, the PPC440SP sequentially reads up to 32 bytes from the ROM device on the IIC0 port and sets the SDR0_SDSTP0 - SDR0_SDSTP7 registers accordingly.

The initialization settings and their default values are described in detail in the *PPC440SP Embedded Processor User’s Manual*.

Document Revision History

Revision	Date	Description
1.23	Sept 26, 2006	Corrected Package Thermal Specifications table where the letter q appeared instead of the symbol for theta.
1.22	Sept 22, 2006	Updated Recommended DC Operating Conditions table.
1.21	Sept 12, 2006	Updated Processor Clock values in Clocking Specifications table.
1.20	June 27, 2006	Updated Recommended DC Op Conditions and Signal Functional Description tables for PCI-X DDR mode 2.
1.19	June 14, 2006	Updated signal lists.
1.18	May 23, 2006	Fixed doc issue for PEROE signal in Signal Functional Description table. Updated Clocking Specifications table and Serial Bootstrap ROM paragraph.
1.17	May 1, 2006	Updated core package graphic in Figure 3. Added RAID acceleration section to Features, Description, and functional details sections.
1.16	March 8, 2006	Updated ordering and PVR information, part number list, and package diagram. GJG
1.15	March 7, 2006	Removed DMA statement from Serial Port feature statement. Removed reference to notes from PERBLAST entry in signal functional description table. GJG
1.14	March 6, 2006	Updated description of On-Chip SRAM/L2 Cache in Introduction. GJG
1.13	February 9, 2006	Updated Signal Function Description table per JB, updated mailing address and copyright date in disclaimer. GJG
1.12	Nov 15, 2005	Clarified information about DDR SDRAM I/O specifications, updated note in system memory address map table per GB, updated ordering and PVR information, part number list, and package diagram, deleted Preliminary from running head. GJG
1.11	July 12, 2005	Updated leakage current info, case temp range, DDR SDRAM Signal Termination graphic. GJG
1.10	May 23, 2005	Changed PVR numbers for pass 2. Corrected functional block diagram. Updated Write timing diagrams. GJG
1.09	Mar 8, 2005	Changed part numbers in Ordering and PVR Information section to reflect pass 2. Removed text for unsupported COLA component. GJG
1.08	Feb 16, 2005	Added table to document muxed usage of GPIO signals. Removed additional references to unsupported COLA serial interface. Reformatted LOF and LOT to comply with AMCC style. Updated Description information on first page, sections on DC power supply loads and recommended DC operating conditions. GJG
1.07	Jan 19, 2005	Remove references to unsupported COLA serial interface. GJG
1.06	Dec 21, 2004	Update max case temp in Recommended DC Op Conditions table to match Ordering and PVR Information table. GJG
1.05	Dec 14, 2004	Update Order Part Number Key information, DDR SDRAM Read data Path block diagram, and DDR SDRAM Read Cycle Timing example diagram per GB. GJG
1.04	Dec 01, 2004	Update Ordering and PVR information. GJG
1.03	Oct 19, 2004	Update table in Recommended DC Operating Conditions section per Docs Issue Database ID #12. GJG
1.02	Oct 12, 2004	Update functional block diagram and text, signal functional description table, and recommended DC operating conditions section with GB's comments. GJG
1.01	Sept 08, 2004	First official draft. GJG
1.00	Dec 31, 2003	Create initial data sheet.



Applied Micro Circuits Corporation

215 Moffett Park Dr., Sunnyvale, CA 94089
Phone: (858) 450-9333 — (800) 755-2622 — Fax: (858) 450-9885
http://www.amcc.com