Actions

炬力集成

ACU7503 Datasheet

Latest Version: 1.3

Declaration

Circuit diagrams and other information relating to products of Actions Semiconductor Company, Ltd. ("Actions") are included as a means of illustrating typical applications. Consequently, complete information sufficient for construction is not necessarily given. Although the information has been examined and is believed to be accurate, Actions makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and disclaims any responsibility for inaccuracies. Information in this document is provided solely to enable use of Actions' products. The information presented in this document does not form part of any quotation or contract of sale. Actions assumes no liability whatsoever, including infringement of any patent or copyright, for sale and use of Actions' products, except as expressed in Actions' Terms and Conditions of Sale for. All sales of any Actions products are conditional on your agreement of the terms and conditions of recently dated version of Actions' Terms and Conditions of Sale agreement Dated before the date of your order.

This information does not convey to the purchaser of the described semiconductor devices any licenses under any patent rights, copyright, trademark rights, rights in trade secrets and/or know how, or any other intellectual property rights of Actions or others, however denominated, whether by express or implied representation, by estoppel, or otherwise.

Information Documented here relates solely to Actions products described herein supersedes, as of the release date of this publication, all previously published data and specifications relating to such products provided by Actions or by any other person purporting to distribute such information. Actions reserves the right to make changes to specifications and product descriptions at any time without notice. Contact your Actions sales representative to obtain the latest specifications before placing your product order. Actions product may contain design defects or errors known as anomalies or errata which may cause the products functions to deviate from published specifications. Anomaly or "errata" sheets relating to currently characterized anomalies or errata are available upon request. Designers must not rely on the absence or characteristics of any features or instructions of Actions' products marked "reserved" or "undefined." Actions reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

Actions' products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal

injury or severe property damage. Any and all such uses without prior written approval of an Officer of Actions and further testing and/or modification will be fully at the risk of the customer.

Copies of this document and/or other Actions product literature, as well as the Terms and Conditions of Sale Agreement, may be obtained by visiting Actions' website at http://www.actions-semi.com/ or from an authorized Actions representative. The word "ACTIONS", the Actions' LOGO, whether used separately and/or in combination, and the phase "ACU7503", are trademarks of Actions Semiconductor Company, Ltd., Names and brands of other companies and their products that may from time to time descriptively appear in this product data sheet are the trademarks of their respective holders; no affiliation, authorization, or endorsement by such persons is claimed or implied except as may be expressly stated therein.

ACTIONS DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES, INCLUDING WITHOUT LIMITATION ANY AND ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND AGAINST INFRINGEMENT AND THE LIKE, AND ANY AND ALL WARRANTIES ARISING FROM ANY COURSE OF DEALING OR USAGE OF TRADE.

IN NO EVENT SHALL ACTIONS BE RELIABLE FOR ANY DIRECT, INCIDENTAL, INDIRECT, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES; OR FOR LOST DATA, PROFITS, SAVINGS OR REVENUES OF ANY KIND; REGARDLESS OF THE FORM OF ACTION, WHETHER BASED ON CONTRACT; TORT; NEGLIGENCE OF ACTIONS OR OTHERS; STRICT LIABILITY; BREACH OF WARRANTY; OR OTHERWISE; WHETHER OR NOT ANY REMEDY OF BUYER IS HELD TO HAVE FAILED OF ITS ESSENTIAL PURPOSE, AND WHETHER ACTIONS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES OR NOT.

Additional Support

Additional product and company information can be obtained by visiting the Actions website at: http://www.actions-semi.com

Contents

Declaration **2**

Contents **4**

1 Introduction **6**

2 Pin Description **7**

2.1 Pin Assignment 7

2.2 Pin Definition 8

3 Function Description **11**

3.1 Functional Block Diagram 11

3.2 MCU Core 11

3.2.1 Internal RAM 12

3.2.2 Internal ROM 12

3.2.3 External RAM/ROM Access 12

3.3 DSP Core 12

3.4 Clock Management Unit (CMU) 13

3.4.1 HOSC 13

3.5 Power Management Unit (PMU) 13

3.5.1 Voltage Generator 13

3.5.2 Voltage monitor 13

3.5.3 External Power Supply Controller 14

3.6 DMA Controller 14

3.7 GPIO and Multifunction Configuration 14

3.8 USB 2.0 SIE 14

3.8.1 Features 15

3.8.2 USB Using Memory 15

3.9 Nand Flash and SMC Controller 15

3.10 Key Scan Interface 16

3.11 DAC 16
3.12 ADC 16
4 Electrical Characteristics 17
4.1 Absolute Maximum Ratings 17
4.2 Capacitance 17
4.3 DC Characteristics 17
4.4 AC Characteristics 18
4.4.1 AC Test Input Waveform 18
4.4.2 AC Test Output Measuring Points 18
4.4.3 Reset Parameter 19
4.4.4 Initialization Parameter 19
4.4.5 GPIO Interface Parameter 19
4.4.6 Ordinary ROM Parameter 20
4.4.7 External System Bus Parameter 21
4.4.8 Bus Operation 21
4.4.9 A/D Converter Characteristics 22
4.4.10 Headphone Driver Characteristics Table 23
4.4.11 LCM Driver Parameter 24
5 Soldering Conditions and Package Description 25
5.1 Recommended Soldering Conditions (Lead Free) 25
5.2 Precaution against ESD for Semiconductors 25
5.3 Handling of Unused Input Pins for CMOS 26
5.4 Status before Initialization of MOS Devices 26
5.5 ACU7503 Package Drawing 26

1 Introduction

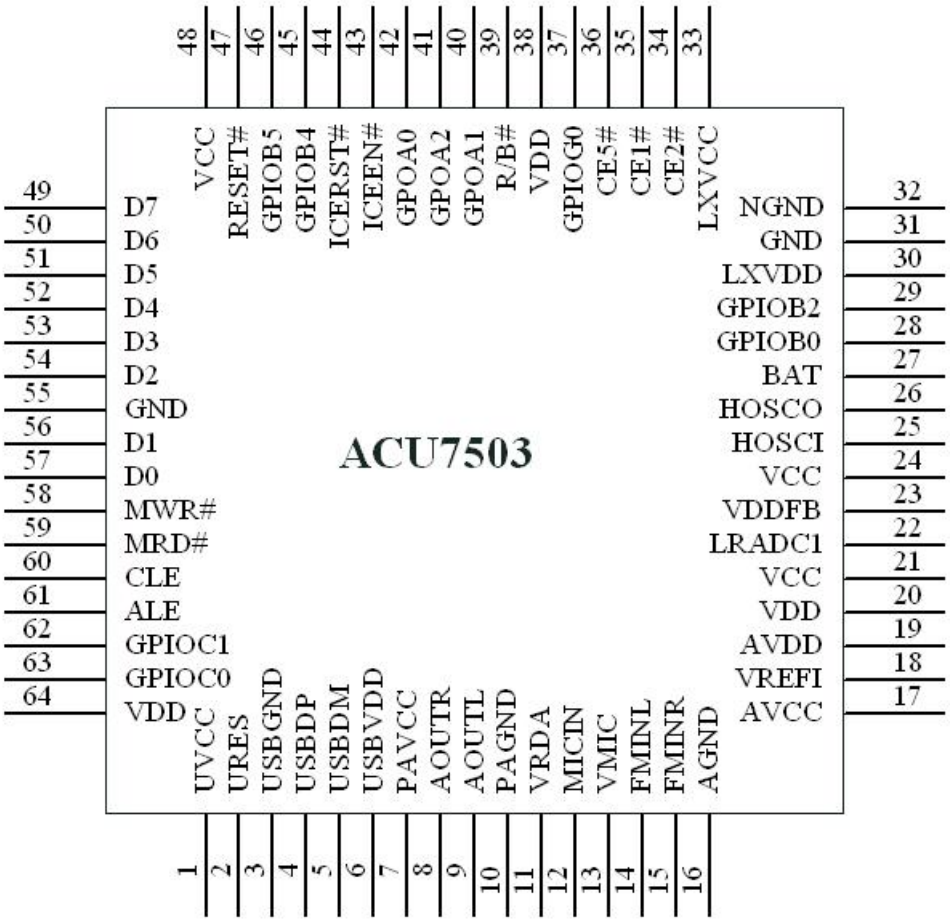
The ACU7503 is one of the ACU750x Single-cell Series SOC which is the second generation highly-integrated digital music system solutions for devices such as audio players and photo viewers. Besides an audio decoder with a high performance DSP that has built-in RAM and ROM, the ACU7503 includes ADPCM record capabilities and USB interface for downloading and uploading. It also provides interface for flash memory, LED/ OLED/color LCD, buttons and switch inputs, headphone, microphone, and FM radio input and control. The ACU7503 has programmable architecture supporting the WMA and other digital audio standards. For storage device, it can act as a USB mass storage slave device to personal computer system. ACU7503 has low power consumption to ensure longer battery life. It has two flexible on-chip DC-DC converters using 1xAA or 1xAAA battery as power supply. And a Low Drop Regulator is also embedded to replace one of the DC-DC generating VDD when Battery is not present. The built-in Sigma-Delta (Σ-Δ) DAC includes a headphone driver to directly drive low impedance headphone(s). The ADC includes inputs for both Microphone and Analog Audio In to support voice and FM radio recording. Thus, it provides a true 'ALL-IN-ONE' solution that is ideally suitable for highly optimized digital multimedia players.

Features

- Instruction set of MCU compatible with Z80
- Internal SRAM access time<7ns, MROM access time<16ns
- Accurate Clock Management Unit, supplies 24MHz OSC
- Energy saving Power Management Unit, supports 1xAA, 1xAAA
- 2-channel DMA, 1-channel Counter/Timer Controller and Interrupt Controller
- Support USB 2.0 high speed, acting as mass storage device
- Support up to 4(pcs)*64M-4G bytes Nand type SLC/MLC Flash
- Built-in Key Scan Circuit and GPIOs
- Built-in Stereo Sigma-Delta DAC and ADC
  Digital voice recording at ultra low 4.4 or 8Kbps with Actions Speech Algorithm
- Headphone driver output 2x11mW @16ohm
- Support FM Radio input and 32 levels volume control
- Support extended low frequency crystal to generalize RTC
- 0.18um 1P5M CMOS process and packaged at LQFP-80(10*10mm)

2 Pin Description

2.1 Pin Assignment



2.2 Pin Definition

Pin No.	Pin Name	I/O Type	Driver Capacity	Reset Default	Short Description
1	UVCC	PWR	/	/	Power supply for USB
2	URES	AO	/	/	USB precision Resistor
3	USBGND	PWR	/	/	USB ground
4	USBDP	A	/	H	USB data plus
5	USBDM	A	/	H	USB data minus
6	USBVDD	PWR	/	/	USB power
7	PAVCC	PWR	/	/	Power supply for Power Amplifier
8	AOUTR	AO	/	/	Int. PA right channel analog output
9	AOUTL	AO	/	/	Int. PA left channel analog output
10	PAGND	PWR	/	/	Power Amplifier ground
11	VRDA	AO	/	/	Bypass capacitor connect pin for int. DAC Reference voltage
12	MICIN	AI	/	/	Microphone pre-amplifier input
13	VMIC	PWR	/	/	Power supply for Microphone
14	FMINL	AI	/	/	Left channel of FM line input
15	FMINR	AI	/	/	Right channel of FM line input
16	AGND	PWR	/	/	Analog ground
17	AVCC	PWR	/	/	Power supply of analog
18	VREFI	AI	/	/	Voltage reference input
19	AVDD	PWR	/	/	Analog core power pin
20	VDD	PWR	/	Z	Core power
21	VCC	PWR	/	/	IO power
22	LRADC1	AI	/	/	Low resolution A/D input 1
23	VDDFB	AI	/	/	VDD feedback
24	VCC	PWR	/	/	IO power
25	HOSCI	AI	/	/	High frequency crystal OSC input
26	HOSCO	AO	/	/	High frequency crystal OSC output
27	BAT	I	/	/	Battery voltage input.
28	GPIO_B0	BI	2mA	Z	Bit0 of General Purpose I/O port B
	KEYI0	I		H	Bit0 of key scan circuit input
	CE3-	O		H	Chip enable 3

29	GPIO_B2	BI	2mA	Z	Bit2 of General Purpose I/O port B
	KEYI2	I		H	Bit2 of key scan circuit input
	CE4-	O		H	Chip enable 4.
30	LXVDD	PWR	/	/	VDD DC-DC pin
31	GND	PWR	/	/	Ground
32	NGND	PWR	/	/	NMOS ground
33	LXVCC	PWR	/	/	VCC DC-DC pin
34	CE2-	O	NF_PAD	H	Ext. memory chip enable 2
35	CE1-	O	NF_PAD	H	Ext. memory chip enable 1
36	CE5-	O	4mA	H	Ext. memory chip enable 5
	GPO_A3	BI		/	Bit3 of General Purpose Output port A
37	GPIO_G0	BI	2mA	Z	Bit0 of General Purpose I/O port G
	MMC_CMD	O		/	Command/Respond of SD/MMC
38	VDD	PWR	/	/	Digital core power
39	RB-	I	4mA	H	Nand Flash Ready/Busy status input
40	GPO_A1	O	4mA	L	Bit1 of General Purpose Output port A
	ICECK	I		/	Clock input of DSU
41	GPO_A2	O	4mA	L	Bit2 of General Purpose Output port A
	ICEDO	O		/	Data output of DSU
42	GPO_A0	O	4mA	0	Bit0 of General Purpose Output port A
	ICEDI	I		/	Data input of DSU
43	ICEEN-	I	4mA	/	DSU enable (active low)
44	ICERST-	I	4mA	/	DSU reset (active low)
45	GPIO_B4	BI	2mA	Z	Bit4 of General Purpose I/O port B
	KEYO0	O		/	Bit0 of key scan circuit output
46	GPIO_B5	BI	2mA	Z	Bit5 of General Purpose I/O port B
	KEYO1	O		/	Bit1 of key scan circuit output
47	RESET-	I	USCU	H	System reset input (active low)
48	VCC	PWR	/	/	Digital power pad
49	D7	BI	NF_PAD	L	Bit7 of ext. memory data bus
50	D6	BI	NF_PAD	L	Bit6 of ext. memory data bus
51	D5	BI	NF_PAD	L	Bit5 of ext. memory data bus
52	D4	BI	NF_PAD	L	Bit4 of ext. memory data bus
53	D3	BI	NF_PAD	L	Bit3 of ext. memory data bus
54	D2	BI	NF_PAD	L	Bit2 of ext. memory data bus

55	GND	PWR	/	/	Ground
56	D1	BI	NF_PAD	L	Bit1 of ext. memory data bus
57	D0	BI	NF_PAD	L	Bit0 of ext. memory data bus
58	MWR-	O	NF_PAD	H	Ext. memory write strobe
59	MRD-	O	NF_PAD	H	Ext. memory read strobe
60	CLE	O	NF_PAD	L	Command Latch Enable fo NandFlash
61	ALE	O	NF_PAD	L	Address latch enable for NAND flash
62	GPIO_C1	BI	2mA	OD	Bit1 of General Purpose I/O port C
	I²C_SDA	O		/	I²C Serial data (Open drain)
	SIRQ-	I		/	Ext. interrupt request input
63	GPIO_C0	BI	2mA	OD	Bit0 of General Purpose I/O port C
	I²C_SCL	O		/	I²C serial clock (Open drain)
64	VDD	PWR	/	/	Digital core power

NOTE:

1 PWR—Power Supply

2 AI—Analog Input

3 AO—Analog Output

4 O—Output

5 I—Input

6 BI—Bi-direction

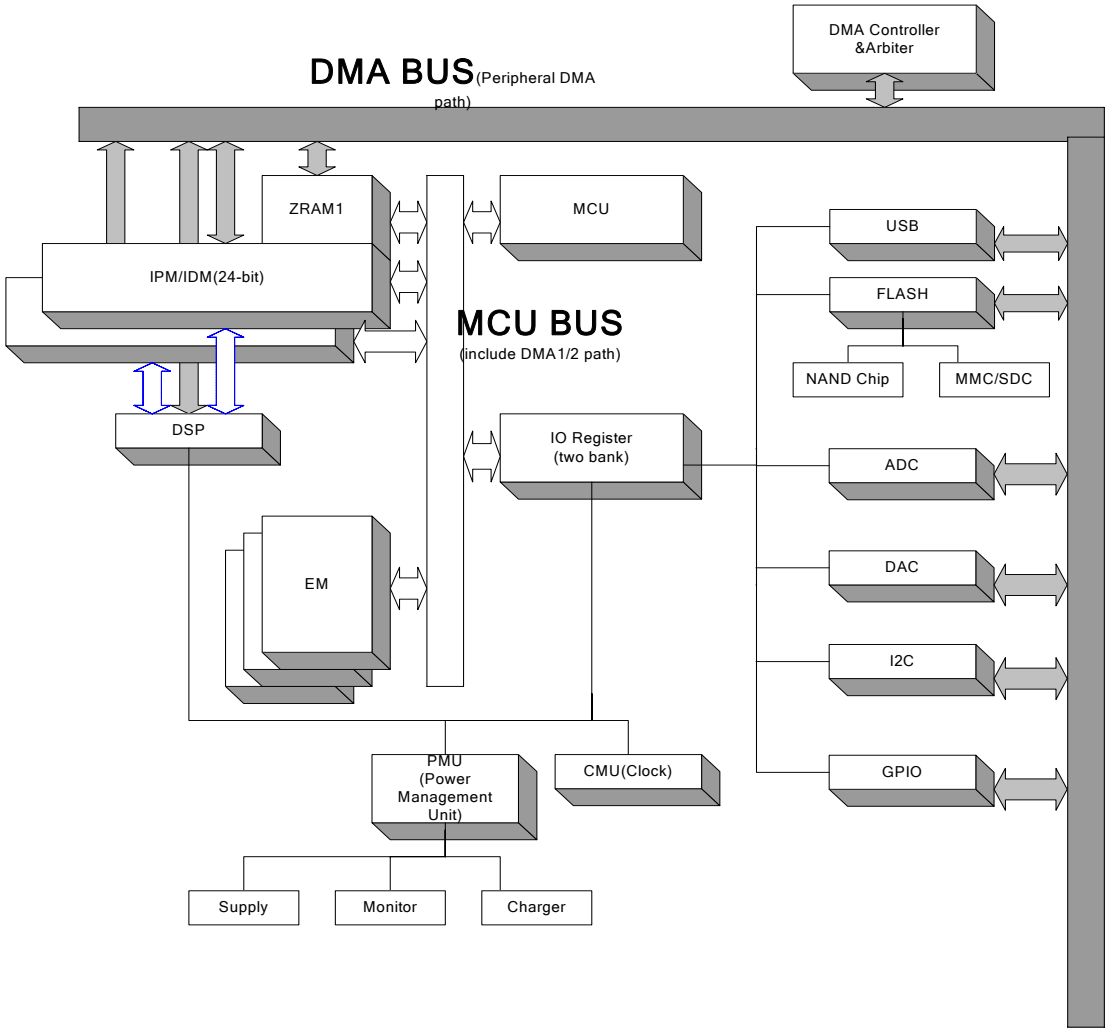
7 NF_PAD—Pad of Nand Flash

8 USCU, USCL—USB SCHIMIT CU, USB SCHIMIT CL

9 Driver capacity here refers to a pin's driving capacity in GPIO mode.

3 Function Description

3.1 Functional Block Diagram

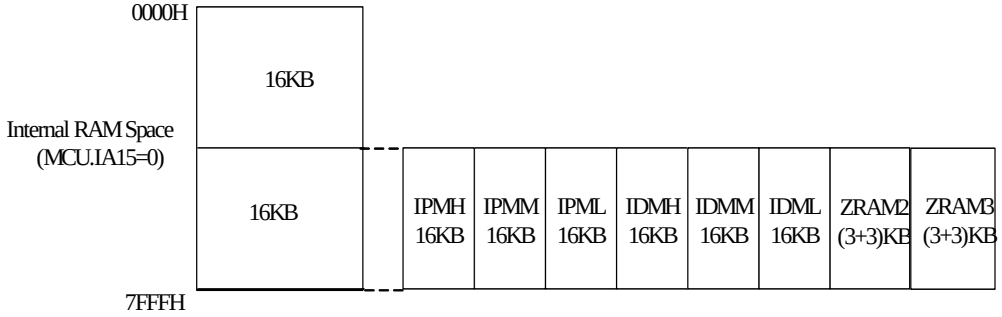


3.2 MCU Core

ACU7503 has 126K+192 bytes on-chip SRAM and 50K bytes on-chip ROM.

3.2.1 Internal RAM

There are three independent banks of SRAM called ZRAM1 (16KB-64B), ZRAM2 (3KB+3KB) and ZRAM3 (3KB+3KB) that can be accessed by MCU and DMA only. The internal SRAM memory mapping is as follows.



3.2.2 Internal ROM

Of the 50KB on-chip ROM, 12KB is boot up BROM that has USB upgrade firmware built in.

3.2.3 External RAM/ROM Access

The External RAM/ROM Controller is able to support up to 6 pieces of 32M*8bit SRAM/ROM. There are up to 6 chip select signals (CE1- to CE6-) for selecting 6 pieces of SRAM/ROM. At any time only one chip select signal can be controlled by the bit [5:3] of EMHIGHP register. There are three extended memory control registers, EMLOWP, EMHIGHP and EMPIORD.

Note: There is no CE6- pin at all. One of the GPIOs would be used as CE6-. When accessing the memory space of CE6-, The GPIO should be pulled down before reading or writing to this memory space.

3.3 DSP Core

24-bit Harvard architecture DSP with DSU built in. Works with a memory word length of 24 bits. ACU7503 has 16K*3 bytes program memory (PM) and 16K*3 bytes data memory (DM). Memory-Mapped register includes DAC interface. Both DSP and MCU can access the Host Interface Port (HIP) registers with reading or writing operations and information can be communicated between the DSP and MCU through it.

3.4 Clock Management Unit (CMU)

The CMU uses 24MHz Oscillator to generate clocks for DSP/USB/CTC/ADC/DAC/MCU/ DMA, etc.

3.4.1 HOSC

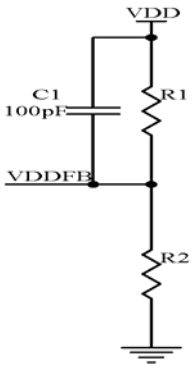
HOSC is a high frequency clock source which:

- Generates clock for DSP and for serial communication interfaces such as USB
- Generates 22.5792MHz for sample rate 44.1K/22.05KHz/11.025KHz and 24.576MHz for audio sequence of 48 KHz.
- Generates high frequency clock up to 72MHz for MCU and DMA.
- Generates Counter/Timer Controller(CTC)

3.5 Power Management Unit (PMU)

The PMU is made up of a Voltage Monitor and Voltage Generator.

3.5.1 Voltage Generator



ACU7503 embeds two DC-DC converters and an LDO on chip. The output of DC-DC1 depends on the external feedback circuit, while the DC-DC2 can generate VCC which is a fixed 3.1V voltage. The power source of DC-DC1 is the AA/AAA battery while the power source of this LDO is USB host, so when the Battery is removed and being plugged on an USB host, the LDO built-in will take the place of DC-DC1 supplying VDD. VDDFB as the Voltage-feedback is fixed once the ratio of R1/R2 fixed by the external feedback circuit as show.

3.5.2 Voltage monitor

Voltage monitor is used to detect the battery voltage and has it displayed on LCD.

3.5.3 External Power Supply Controller

The Battery Charger uses the external power supply from either USB VBUS or adapter.

3.6 DMA Controller

The ACU7503 series SOC has four DMA Controllers. DMA1/2 can transfer data between memory and memory, memory and I/O, I/O and I/O. DMA5 is for flash controller, DMA6 is USB DMA. Both DMA1 and DMA2 can be configured to have higher priority over the other. The DMA Controller Arbiter is embedded to prevent any conflict of transferring from happening, and let the DMA Controller with higher priority to start first and end first.

3.7 GPIO and Multifunction Configuration

There are two Multi Function Modes that can be configured, including GPIO mode, KEY mode. In different mode, GPIO pins can be configured to have alternated functions.

PIN No	PIN NAME	F1(GPIO)	F2(Key)
42	GPO_A0	GPO_A0/ICEDI	GPO_A0/ICEDI
40	GPO_A1	GPO_A1/ICECK	GPO_A1/ICECK
41	GPO_A2	GPO_A2/ICEDO	GPO_A2/ICEDO
28	GPIO_B0	KEYI0/GPIO_B0/CE3-	KEYI0/GPIO_B0/CE3-
29	GPIO_B2	KEYI2/GPIO_B2/CE4-	KEYI2/GPIO_B2/
45	GPIO_B4	KEYO0/GPIO_B4	KEYO0/GPIO_B4
46	GPIO_B5	KEYO1/GPIO_B5	KEYO1/GPIO_B5/
63	GPIO_C0	GPIO_C0	GPIO_C0
62	GPIO_C1	GPIO_C1	GPIO_C1/SIRQ-
37	GPIO_G0	GPIO_G0	GPIO_G0

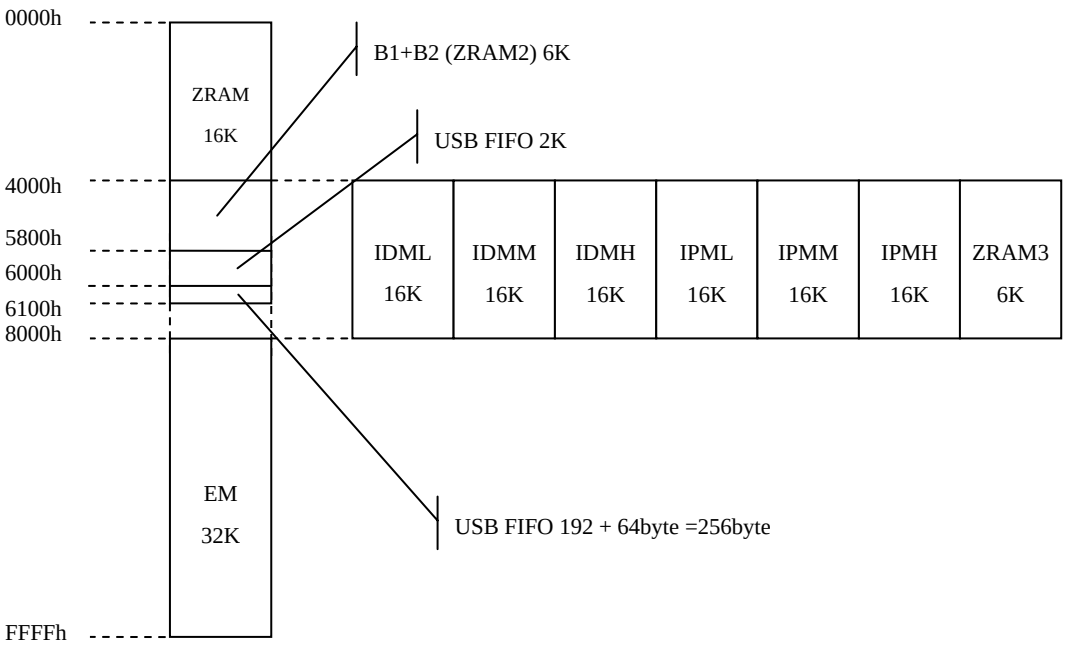
3.8 USB 2.0 SIE

The Actions USB2.0 device controller is fully compliant with the Universal Serial Bus 2.0 specification. This high performance USB2.0 device controller integrates USB transceiver, SIE, and provides multifarious interfaces for generic MCU, RAM, ROM and DMA controller. So it is suitable for a variety of peripherals, such as: scanners, printers, mass storage devices, and digital cameras. It is designed to be a cost-effective USB total solution.

3.8.1 Features

- Fully compliant with USB Specification 2.0
- Supports USB High Speed (480Mb/s) and Full Speed (12Mb/s)
- Supports Control, Bulk, Isochronous and Interrupt Transfers
- Embedded USB high-speed Transceiver which complies with Inter UTMI
- Supports DMA interface (16-bit)
- 2KB configurable FIFO for endpoints and provides double buffer to increase throughput.
- Supports USB remote wake-up feature
- Software controlled connection to USB bus for re-enumeration

3.8.2 USB Using Memory



3.9 Nand Flash and SMC Controller

The Nand Flash and Smart Media Card controller uses DMA5 for transferring data between Nand Flash and Internal SRAM.

Features

- Support up to 4 pieces of SMC/Nand Flash with 4 Chip Select pins

- Support Reed Solomon ECC & Hamming ECC
- Command and address control state machine
- Reading and writing timing generator
- ECC accelerator (Reed-Solomon & Hamming)
- Sense R/B# status
- Comply with "Smart Media Software Algorithm Guidelines"
- Bad block detection and replacement
- Both SLC and MLC flash are supported

3.10 Key Scan Interface

The key scan circuit's pins are composed of KEYI[0,2,] and KEYO[0,1,]. The maximum key matrix is 2*2.

When the key scan circuit is enabled, KEYI[x]'s logical level is high, while KEYO[x]'s logical level is low. If any key is pressed which pulls the corresponding KEYI[x]'s logical level to low, KEYO[x] will output a series of scanning waves. In case that key interrupt is enabled, an interrupt will occur after the 12 key data have been stored in KEYSCANDAT (Reg: 0C0H).

3.11 DAC

The internal DAC is an on-chip Sigma-Delta Modulator and the DAC interface support 4-level play back FIFO (8 X 20-bit PCM data) for L/R channel and variable sample rates. Internal DAC can drive earphone application.

Note: the pin PAVCC needs a bypass capacitor of about 100uF to eliminate the "PENG" sound when DAC is powered on or off.

3.12 ADC

The audio A/D is an 18 bits sigma delta Analog-to-Digital Converter; it can work in a 16 bit or 18 bit mode. Its input source can be selected from MIC amplifier or line-in sources.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Typical	Rating	Unit
Supply voltage	VDD	1.8	+10%	V
	VCC	3.1	+10%	V
Input voltage	VIH	2.4	+10%	V
	VIL	1.0	+10%	V
Storage temperature	Tstg		-65~150	℃

Note:

1. TO = 25℃（Operating Temperature）
2. Do not short-circuit two or more output pins simultaneously.
3. Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify at which point the product may be physically damaged. Use the product well within these ratings.
4. The specifications and conditions shown in the DC and AC characteristics are the ranges for normal operation and quality assurance of the product.

4.2 Capacitance

Parameter	Symbol	Condition	MIN	MAX	Unit
Input capacitance	CI	fC = 1 MHz		15	pF
I/O capacitance	CIO	Unmeasured pins returned to 0V		15	pF

Note: TO = 25℃, VCC = 0 V.

4.3 DC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	VOH	IOH = -2 mA	2.4			V

Low-level output voltage	VOL	IOL = 2 mA			0.4	V
High-level input voltage	VIH		0.6VCC		VCC+0.6	V
Low-level input voltage	VIL		-0.3		0.4VCC	V
Input leakage current	ILI	VCC = 3.1V, VI = VCC, 0 V			+10	uA
Output leakage current	ILO	VCC = 3.1 V, VI = VCC, 0 V			+5	uA
GPIO Drive	Idrive1	GPOA0,GPOA1,GPOA2		4		mA
	Idrive2	GPIO_B2, GPIO_B4, GPIO_B5		10		mA
	Idrive3	Other GPIO		2		mA
Supply Current （One battery mode）	IVDD	In Full speed mode		12	15	mA
		In Standby mode		50	60	uA
	IVCC	In Full speed mode		0.2	0.5	mA
		In Standby mode		73	76	uA

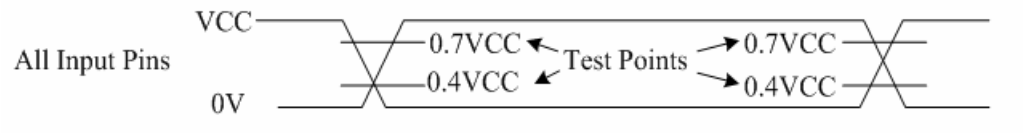
NOTES:

1. To = -10 to +70℃, VDD = 1.8, VCC = 3.1 V
2. IVDD is a total power supply current for the 1.8V power supply. IVDD is applied to the LOGIC and PLL and OSC block.
3. IVCC is a total power supply current for the 3.1 V power supply. IVCC is applied to the USB, IO, TP, and AD block.

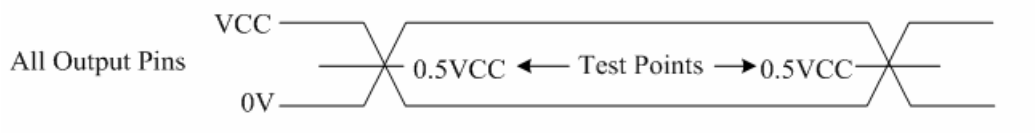
4.4 AC Characteristics

To = -10 to +70℃

4.4.1 AC Test Input Waveform



4.4.2 AC Test Output Measuring Points

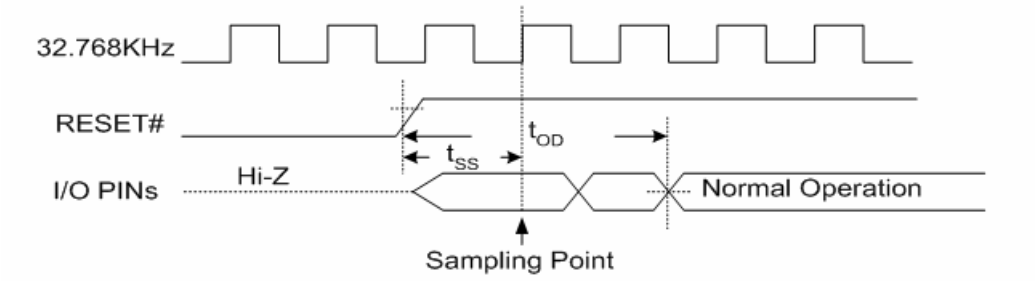


4.4.3 Reset Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	RESET# pin	160		us

4.4.4 Initialization Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time(from RESET#)	t_{SS}			61.04	us
Output delay time (from RESET#)	t_{OD}		61.04		us

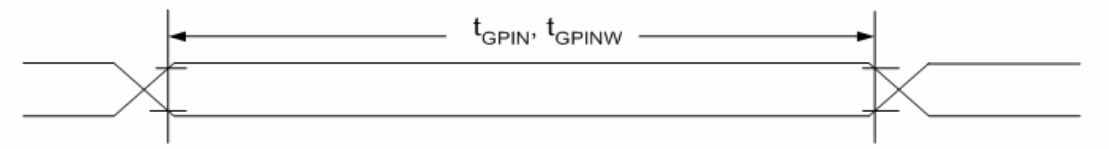


4.4.5 GPIO Interface Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{GPIN}	Normal operation	11/f_{MCUCLK}		s
GPIO input rise time	t_{GPRISE}			200	ns
GPIO input fall time	t_{GPFALL}			200	ns
Output level width	t_{GPOUT}		11/ f_{MCUCLK}		s

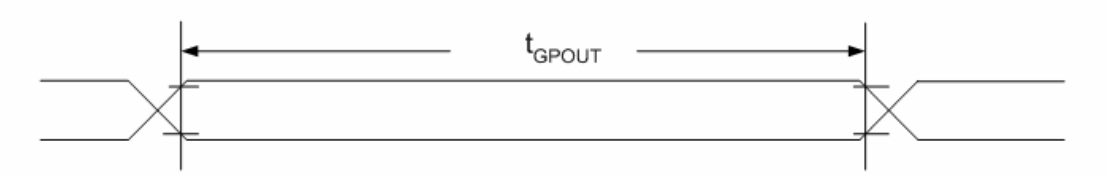
Note: f_{MCUCLK} is the frequency that MCU is running upon.

Input level width



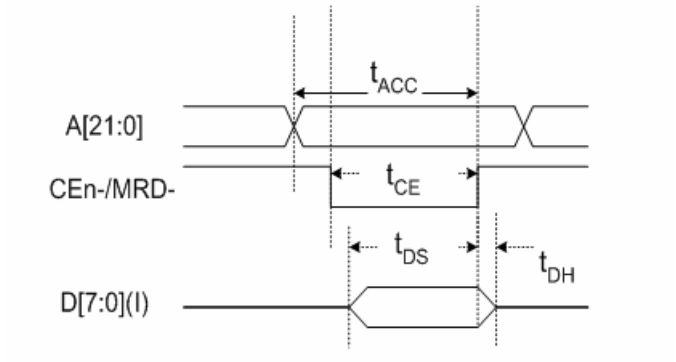
Input rise/fall time

Output level width

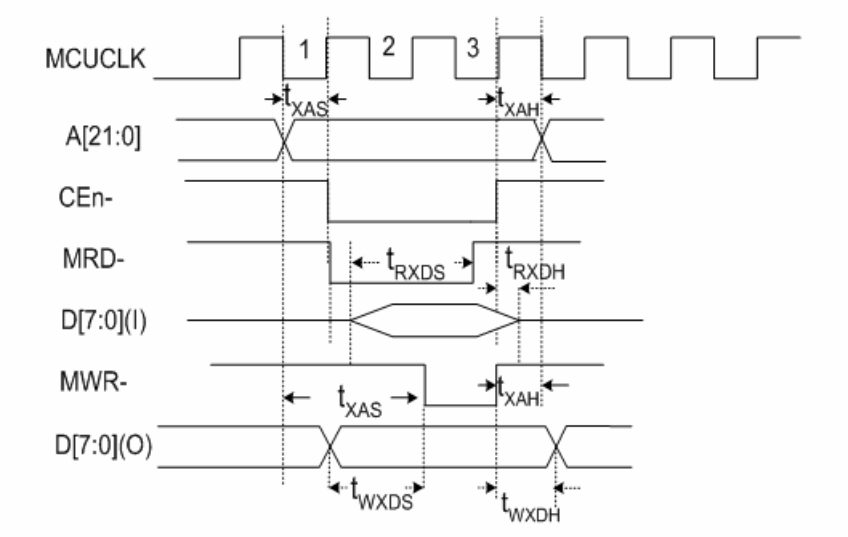


4.4.6 Ordinary ROM Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)Note	t_{ACC}	HOSC=24MHz	102		ns
Data access time (from CEx#)Note	t_{CE}	HOSC=24MHz	82		ns
Data input setup time	t_{DS}	HOSC=24MHz	0		ns
Data input hold time	t_{DH}	HOSC=24MHz	0		ns



4.4.7 External System Bus Parameter



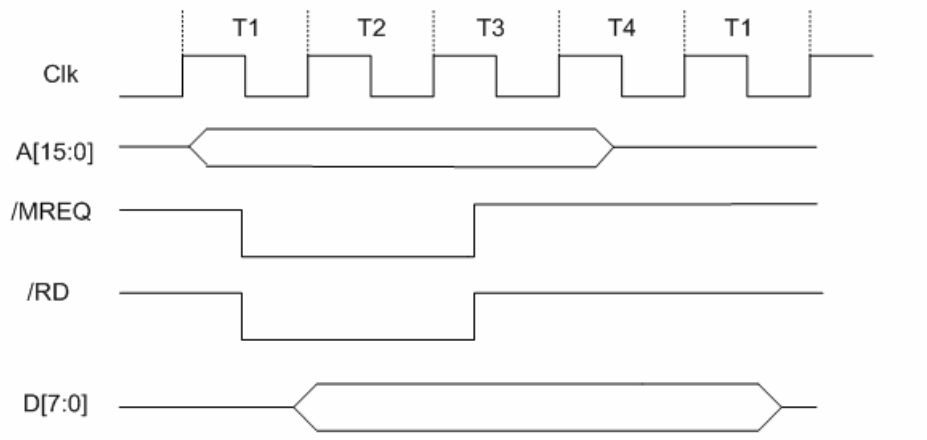
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal)Note 1, 2	t_{XAS}	Memory Read	25		ns
	t_{XAS}	Memory Write	10		ns
Address hold time (from command signal)Note 1, 2	t_{XAH}		5		ns
Data output setup time (to command signal)Note 1	t_{WXDS}		20		ns
Data output hold time(from command signal)Note 1	t_{WXDH}		10		ns
Data input setup time (to command signal)Note 1	t_{RXDS}		20		ns
Data input hold time (from command signal)Note 1	t_{RXDH}		10		ns

Notes:

1. MRD# and MWR# are called the command signals for the External System Bus Interface.
2. T (ns) = 1/ f_{MCUCLK}

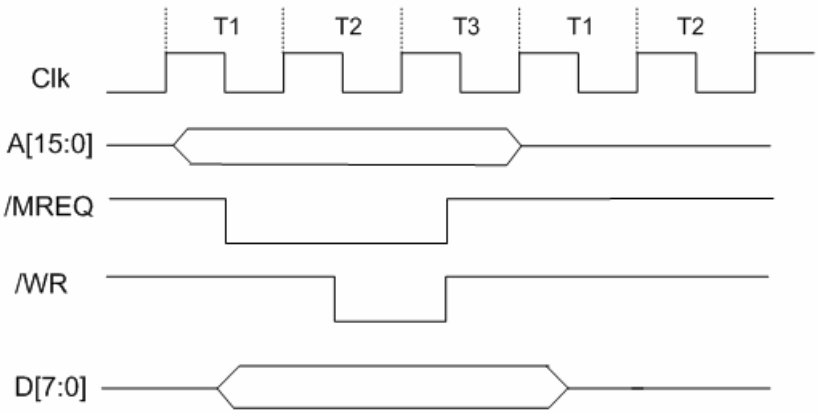
4.4.8 Bus Operation

Memory Read Timing



Memory Read Timing

Memory Write Timing



Memory Write Timing

4.4.9 A/D Converter Characteristics

(TA = -10 - +70℃, VDD = 1.8V, VCC = 3.1V, Sample Rate=32KHz)

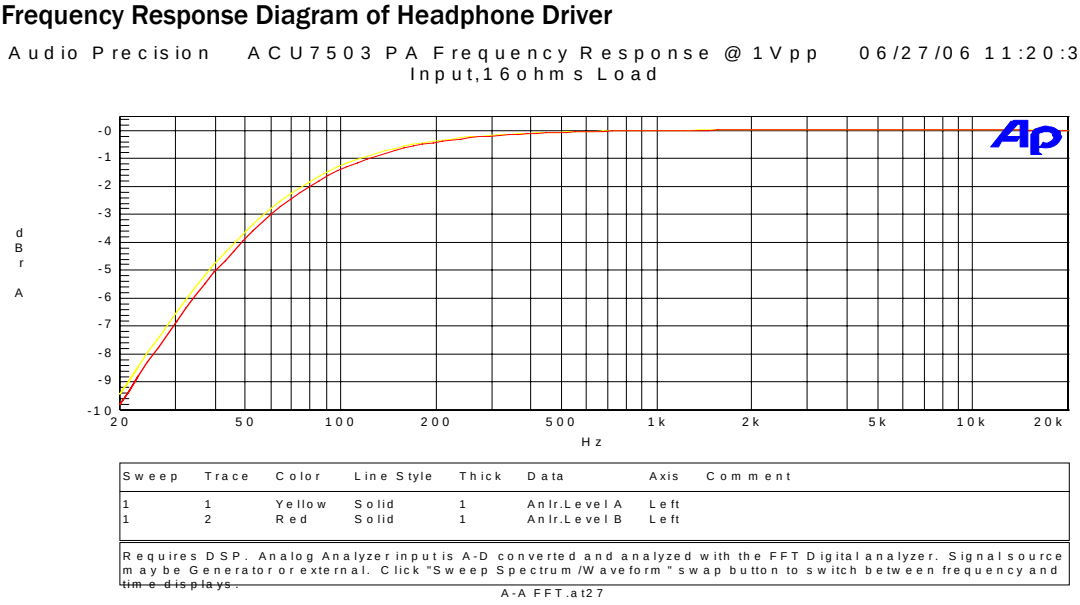
Characteristics	Min	Typ.	Max	Unit
Dynamic range		80		dB
Total Harmonic Distortion + Noise	76			dB
Frequency Response Fluctuation (20-13KHz)			±0.3	dB
Full Scale Input Voltage(Gain=0dB)		2		V_{PP}

4.4.10 Headphone Driver Characteristics Table

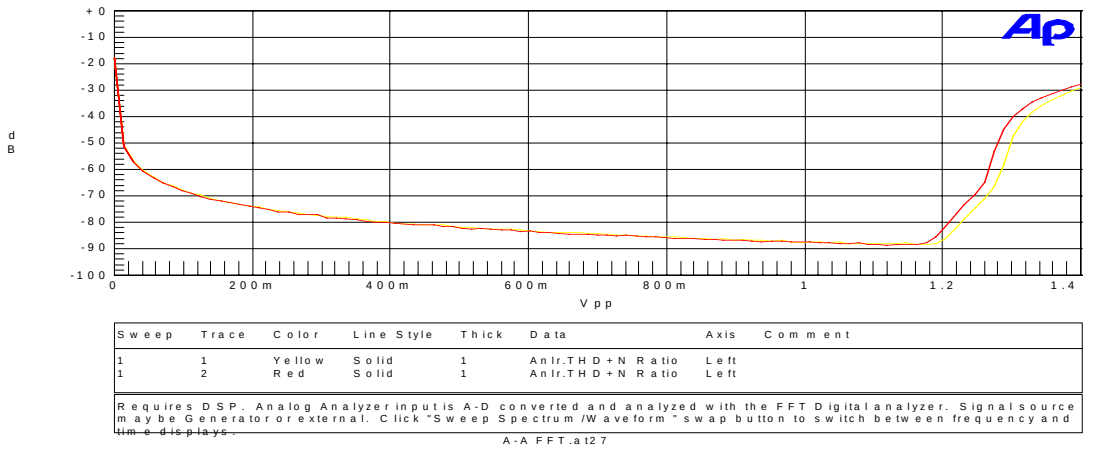
(To =-10 - +70℃, VDD = 1.8V, VCC = 3.1 V, Sample Rate=32KHz, Volume Level=0x1F)

Characteristics	Min	Typ	Max	Unit
Dynamic Range –60 dBFS Input		90		dB
Total Harmonic Distortion + Noise	81			dB
Frequency Response Fluctuation 20-20KHz			±0.1	dB
Output Common Mode Voltage		1.5		V
Full Scale Output Voltage		1.1		V_{PP}
Inter-channel Isolation (1KHz)	94			dB

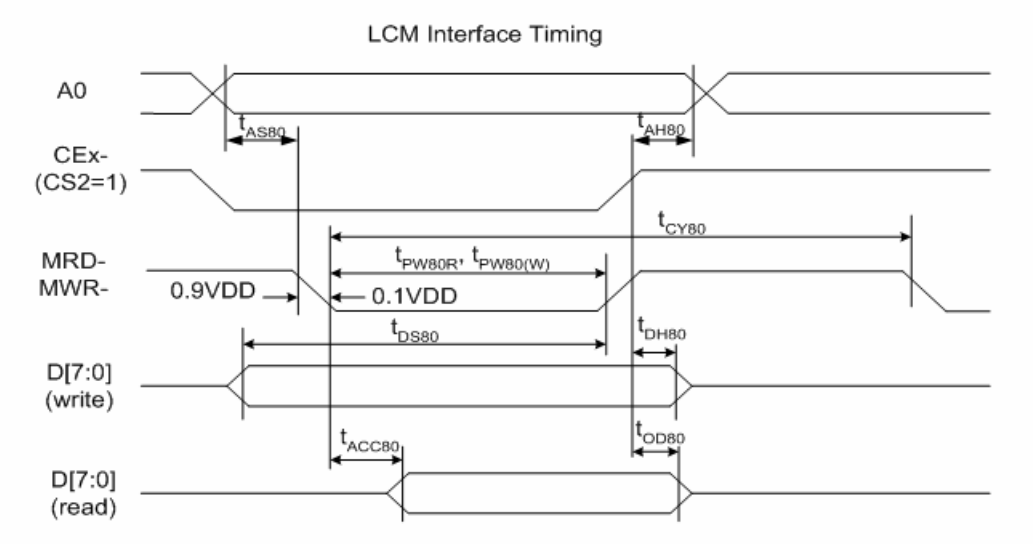
Frequency Response Diagram of Headphone Driver



THD + N Amplitude Diagram of Headphone Driver:



4.4.11 LCM Driver Parameter



Parameter	Symbol	Condition	Typ	Unit
Data access time(write)	tPW80(W)	HOSC=24MHZ	29	ns
Data access time (Read)	tPW80(R)	HOSC=24MHZ	67	ns
Write cycle time	tCY80(W)	HOSC=24MHZ	407	ns
Read cycle time	tCY80(R)	HOSC=24MHZ	284	ns
Data setup time	tDS80	HOSC=24MHZ	79	ns
Data hold time	tDH80	HOSC=24MHZ	8	ns
Address setup time	tAS80	HOSC=24MHZ	11	ns
Address hold time	tAH80	HOSC=24MHZ	11	ns
Read access time	tACC80	HOSC=24MHZ	13	ns
Data input hold time	tOD80	HOSC=24MHZ	8	ns

5 Soldering Conditions and Package Description

5.1 Recommended Soldering Conditions (Lead Free)

Soldering Conditions for Surface-Mount Devices

Soldering Process	Soldering Conditions
Infrared ray reflow	Peak package's surface temperature: 260℃
	Reflow time: 60 seconds or less (217℃ or more)
	Maximum allowable number of reflow processes: 2
	Exposure limit: 1 days at Rh=60%, Tem=30℃ (12 hours of pre-baking is required at 125℃ afterward).
Partial heating method	Terminal temperature: 300℃ or less
	Heat time: 3 seconds or less (for one side of a device)

Note: Maximum number of days during which the product can be stored at a temperature of 25℃ and a relative humidity of 65% or less after dry-pack package is opened.

Caution: Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

5.2 Precaution against ESD for Semiconductors

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once that has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

5.3 Handling of Unused Input Pins for CMOS

No connection for CMOS device inputs can be the cause of a malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to a VDD or GND with a resistor if it is considered to have the possibility of being an output pin. All handling related to the unused pins must be judged device by device using the related specifications governing the devices.

5.4 Status before Initialization of MOS Devices

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operations must be executed immediately after power-on.

5.5 ACU7503 Package Drawing

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.60	---	---	0.063
A_1	0.05	---	0.15	0.002	---	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.012	0.015	0.018
b_1	0.17	0.20	0.23	0.012	0.014	0.016
c	0.09	---	0.20	0.004	---	0.008
c_1	0.09	---	0.16	0.004	---	0.006
D	12.00 BSC			0.472 BSC		
D_1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E_1	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	---	---	0.003	---	---
R_2	0.08	---	0.20	0.003	---	0.008
S	0.20	---	---	0.008	---	---
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	---	---	0°	---	---
θ_2	12°TYP			12°TYP		
θ_3	12°TYP			12°TYP		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 , BCD.

COPY CONTROLLED

REV NO	DESCRIPTION	DATE

TITLE: 64LD LQFP(10x10x1.4mm)PACKAGE OUTLINE -Cu L/F,FOOTPRINT 2.0mm

MATERIAL: C7025 1/2H

APPR	MCHLIN	DWG NO	S-S-D064-SW1
R&D	FB.CAO	REV NO	A
Q.M	YingChang	SCALE	FULL
CHK	CSJ.CHEN	DATE	6-21-04
DEN	LIANG.ZHAO	SHT NO	1/1

SILICONWARE TECHNOLOGY (SUZHOU) LIMITED

Actions Semiconductor Co., Ltd.

Address: Bldg.15-1, NO.1, HIT Rd., Tangjia, Zhuhai, Guangdong, China
Tel: +86-756-3392353
Fax: +86-756-3392251
Post code: 519085
http://www.actions-semi.com
Business Email: mp-sales@actions-semi.com
Technical Service Email: mp-cs@actions-semi.com