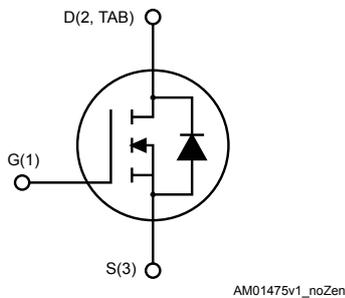
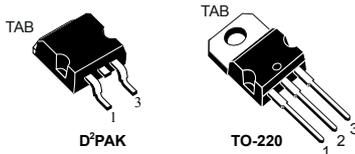


N-channel 600 V, 0.4 Ω typ., 11 A, MDmesh™ II Power MOSFETs in D²PAK and TO-220 packages



Features

Order codes	V _{DSS} (@ T _{Jmax})	R _{DS(on)} max.	I _D	Package
STB11NM60T4	650 V	0.45 Ω	11 A	D ² PAK
STP11NM60				TO-220

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high-efficiency converters.

Product status link

[STB11NM60T4](#)

[STP11NM60](#)

Product summary

Order code	STB11NM60T4
Marking	B11NM60
Package	D ² PAK
Packing	Tape and reel
Order code	STP11NM60
Marking	P11NM60
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Gate-source voltage	600	V
V_{GS}	Gate- source voltage	±30	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	11	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	7	
$I_{DM}^{(1)}$	Drain current (pulsed)	44	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	160	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-65 to 150	°C
T_j	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 11\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	TO-220	
$R_{thj-case}$	Thermal resistance junction-case	0.78		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35		

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_{jmax})	5.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	350	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}^{(1)}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 30\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}$		0.4	0.45	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance		-	1000	-	pF
C_{oss}	Output capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	230	-	pF
C_{riss}	Reverse transfer capacitance		-	25	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	100	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	1.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 11\text{ A},$ $V_{GS} = 0\text{ to } 10\text{ V}$ (see Figure 12. Test circuit for gate charge behavior)	-	30	-	nC
Q_{gs}	Gate-source charge		-	10	-	nC
Q_{gd}	Gate-drain charge		-	15	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 5.5\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 11. Test circuit for resistive load switching times and Figure 16. Switching time waveform)	-	20	-	ns
t_r	Rise time		-	20	-	ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD} = 480\text{ V}, I_D = 11\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for inductive load switching and diode recovery times and Figure 16. Switching time waveform)	-	6	-	ns
t_f	Fall time		-	11	-	ns
t_c	Cross-over time		-	19	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 11\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$	-	390		ns
Q_{rr}	Reverse recovery charge		-	3.8		μC
I_{RRM}	Reverse recovery current	(see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	19.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$	-	570		ns
Q_{rr}	Reverse recovery charge		-	5.7		μC
I_{RRM}	Reverse recovery current		(see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	20	

1. Pulse width is limited by safe operating area

2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

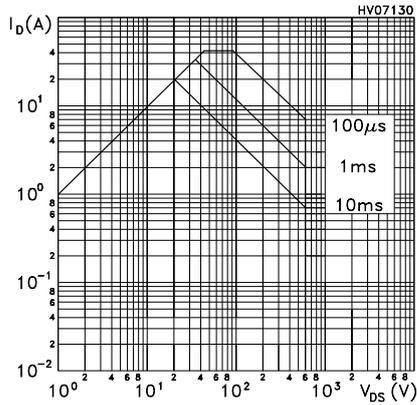
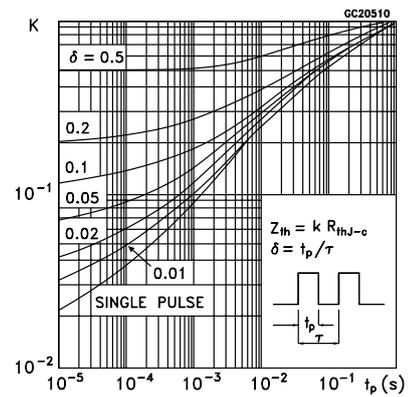
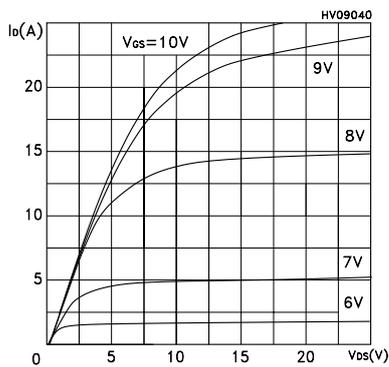
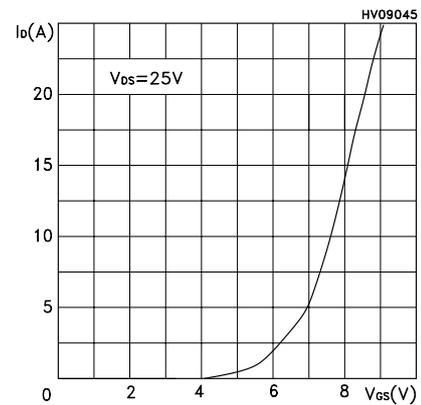
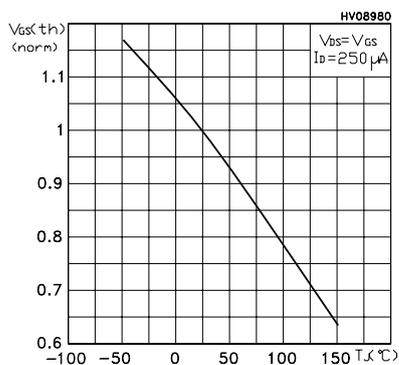
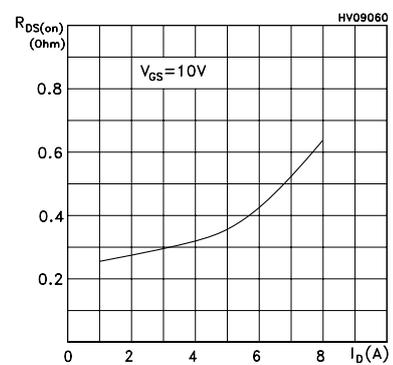
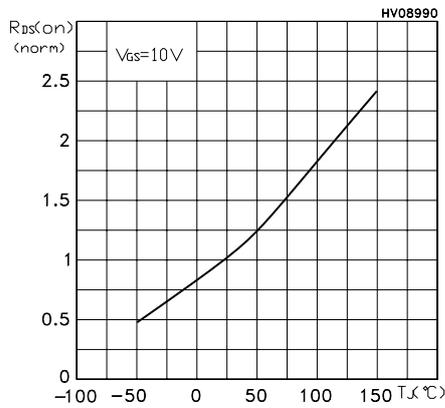
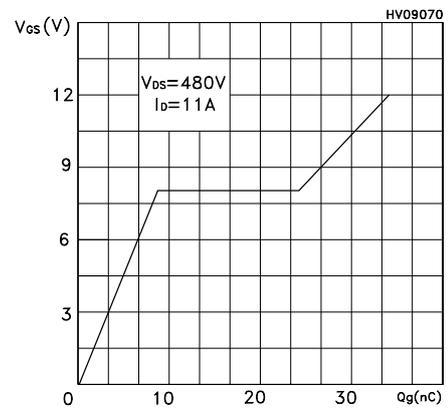
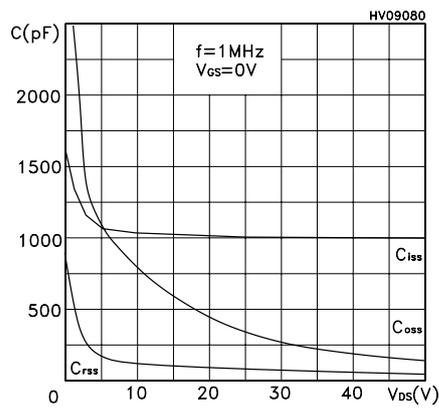
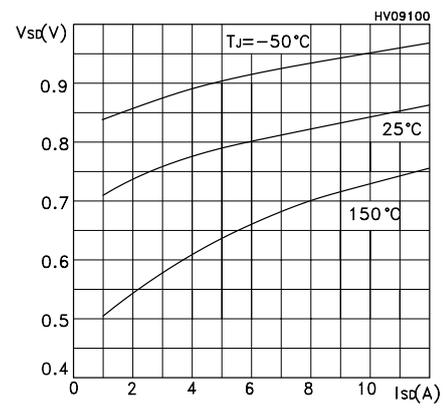
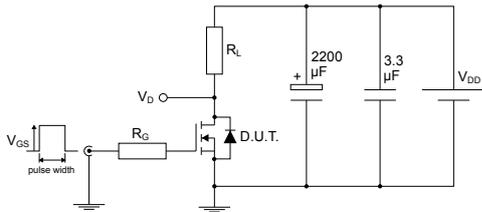
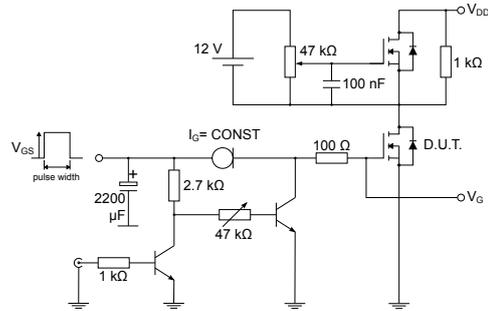
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Normalized gate threshold voltage vs temperature

Figure 6. Static drain-source on-resistance


Figure 7. Normalized on-resistance vs temperature

Figure 8. Gate charge vs gate-source voltage

Figure 9. Capacitance variations

Figure 10. Source-drain diode forward characteristics


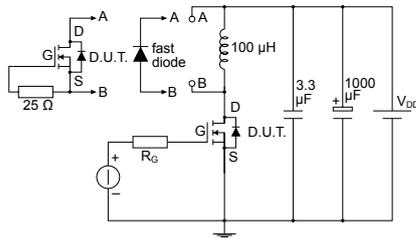
3 Test circuits

Figure 11. Test circuit for resistive load switching times


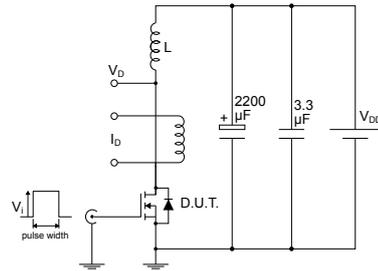
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Figure 12. Test circuit for gate charge behavior


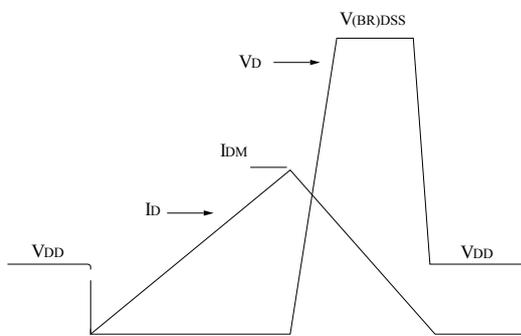
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Figure 13. Test circuit for inductive load switching and diode recovery times


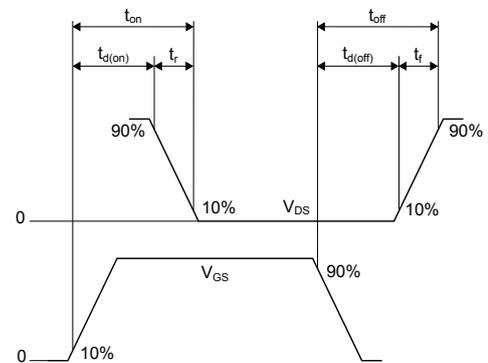
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Figure 14. Unclamped inductive load test circuit


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Figure 15. Unclamped inductive waveform


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Figure 16. Switching time waveform


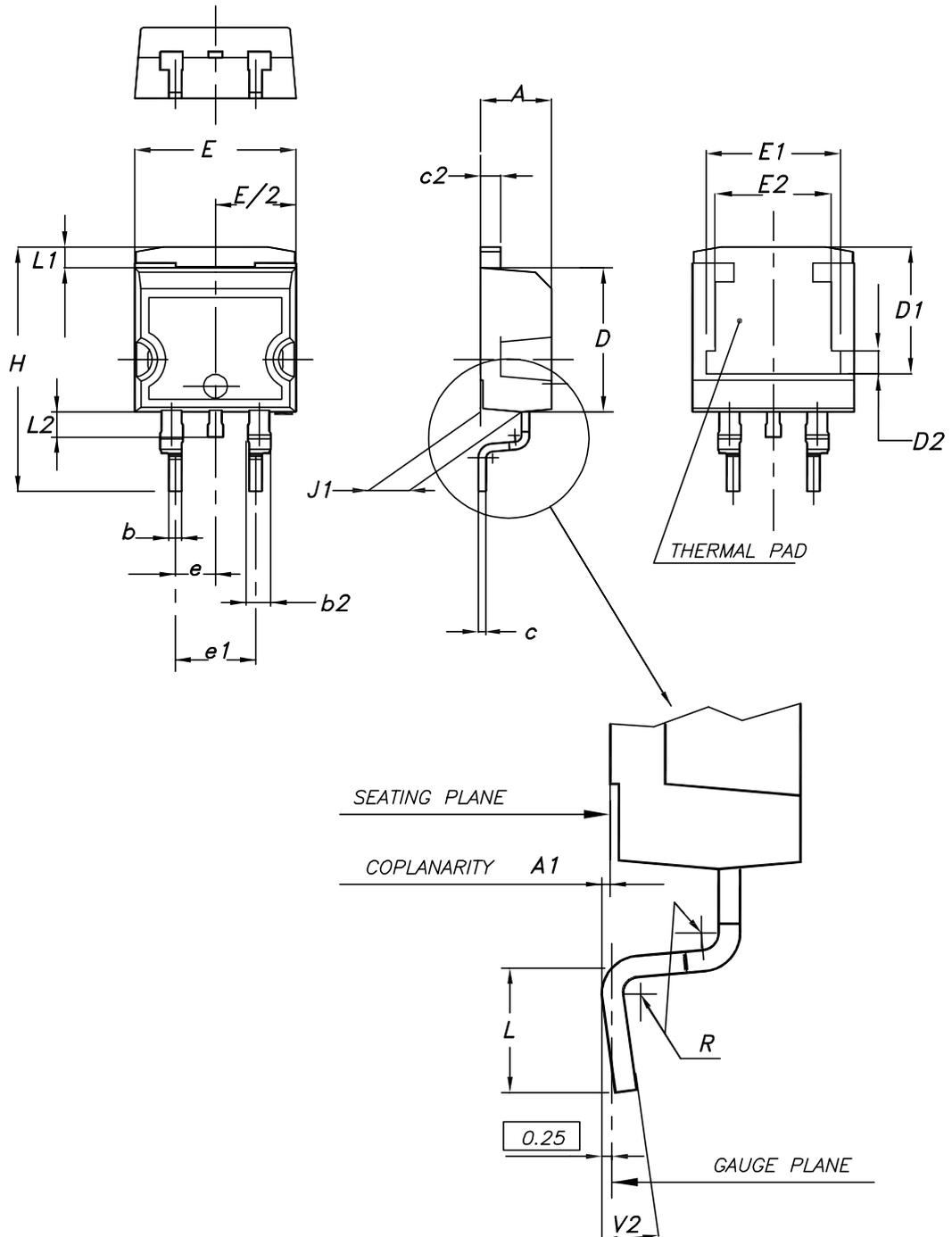
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 17. D²PAK (TO-263) type A package outline



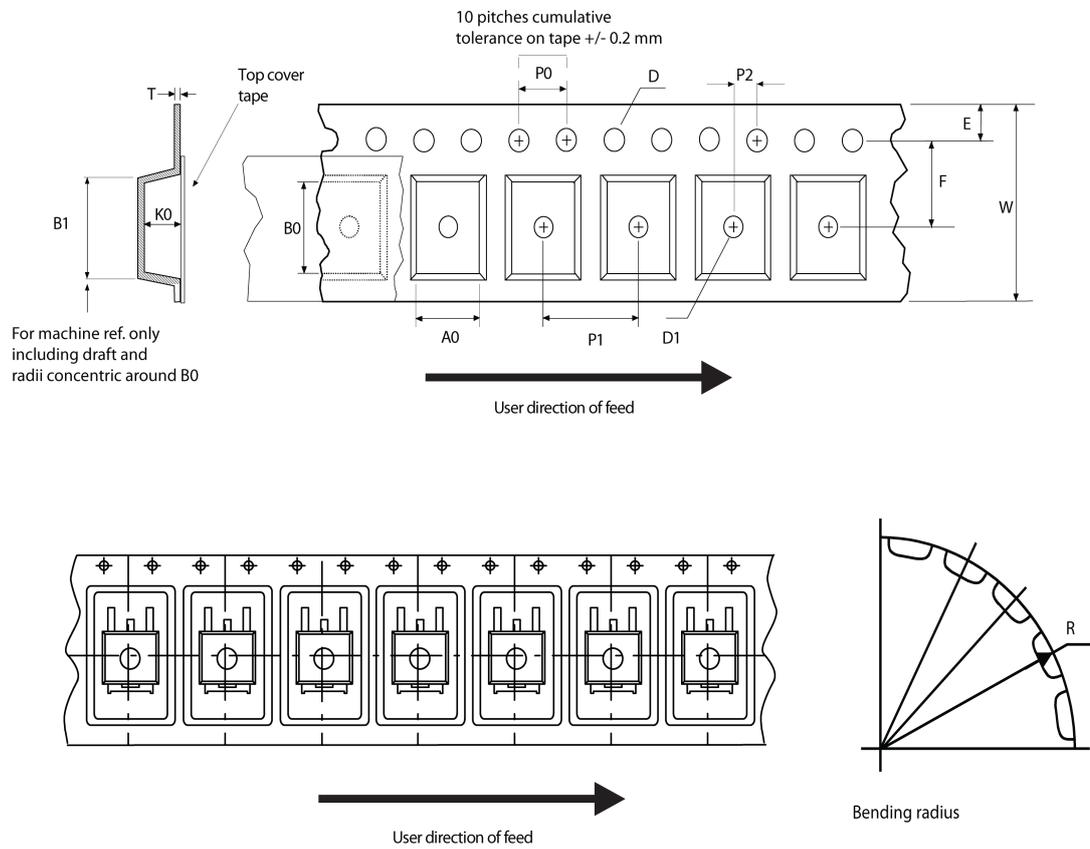
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Table 8. D²PAK (TO-263) type A package mechanical data

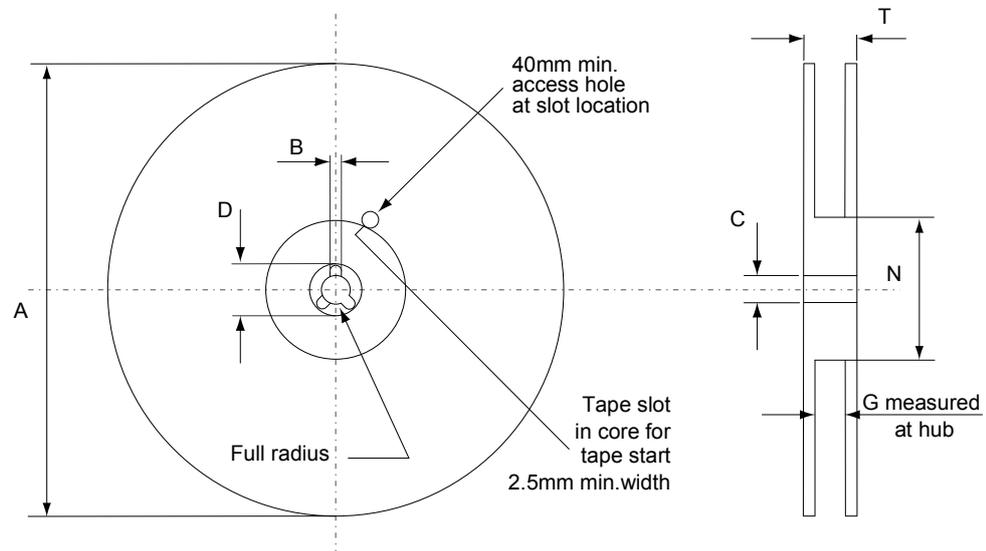
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

4.2 D²PAK packing information

Figure 18. D²PAK tape outline



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Figure 19. D²PAK reel outline


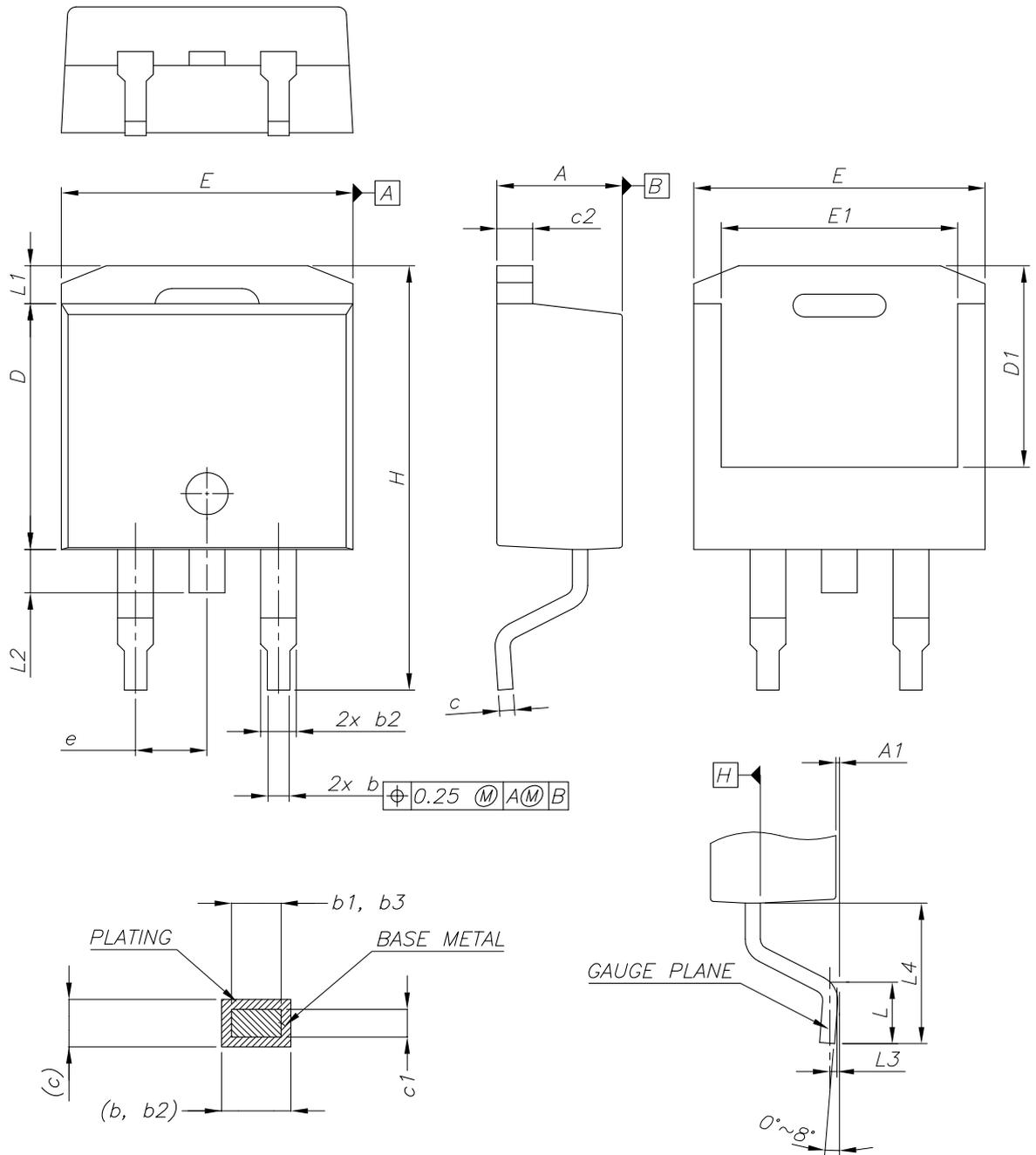
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Table 9. D²PAK tape and reel mechanical data

Tape			Reel			
Dim.	mm		Dim.	mm		
	Min.	Max.		Min.	Max.	
A0	10.5	10.7	A		330	
B0	15.7	15.9	B	1.5		
D	1.5	1.6	C	12.8	13.2	
D1	1.59	1.61	D	20.2		
E	1.65	1.85	G	24.4	26.4	
F	11.4	11.6	N	100		
K0	4.8	5.0	T		30.4	
P0	3.9	4.1	Base quantity Bulk quantity			
P1	11.9	12.1				1000
P2	1.9	2.1				1000
R	50					
T	0.25	0.35				
W	23.7	24.3				

4.3 D²PAK (TO-263) type B package information

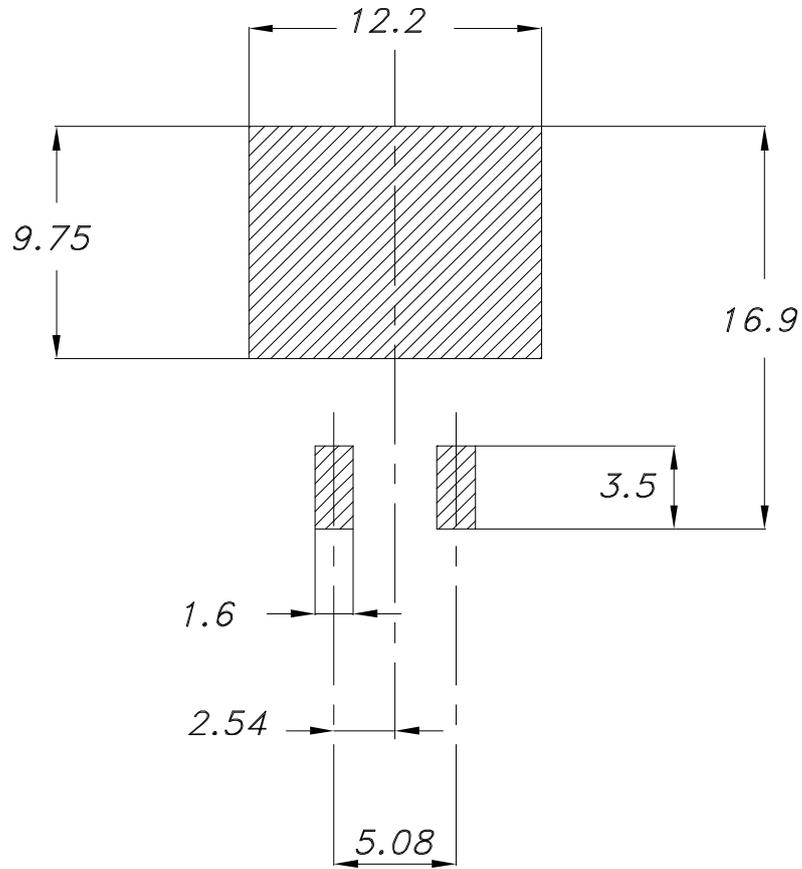
Figure 20. D²PAK (TO-263) type B package outline



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Table 10. D²PAK (TO-263) type B mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
b3	1.36		1.46
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

Figure 21. D²PAK (TO-263) recommended footprint (dimensions are in mm)


Footprint

4.4 D²PAK type B packing information

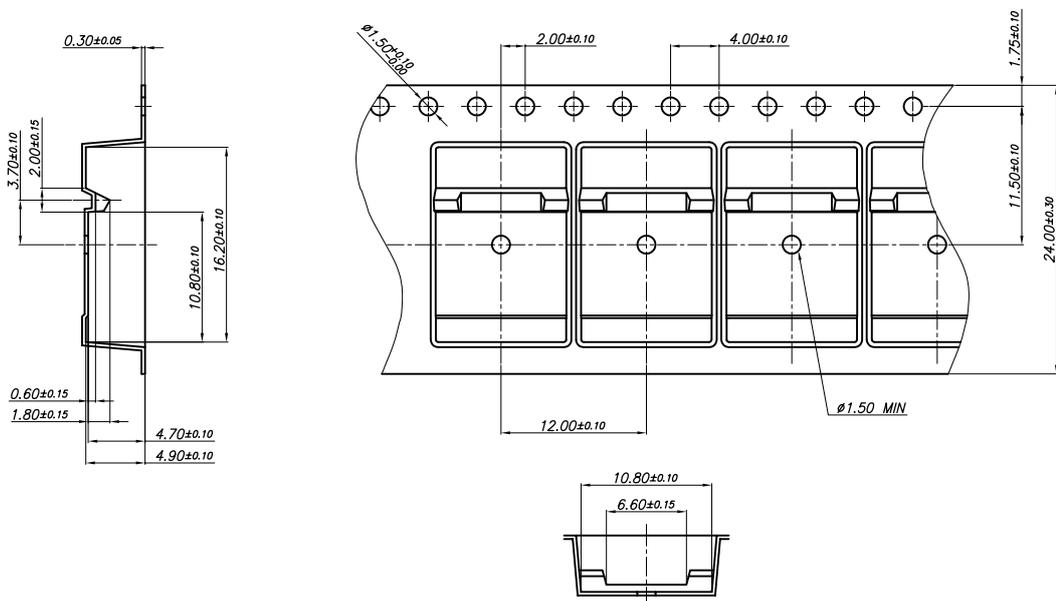
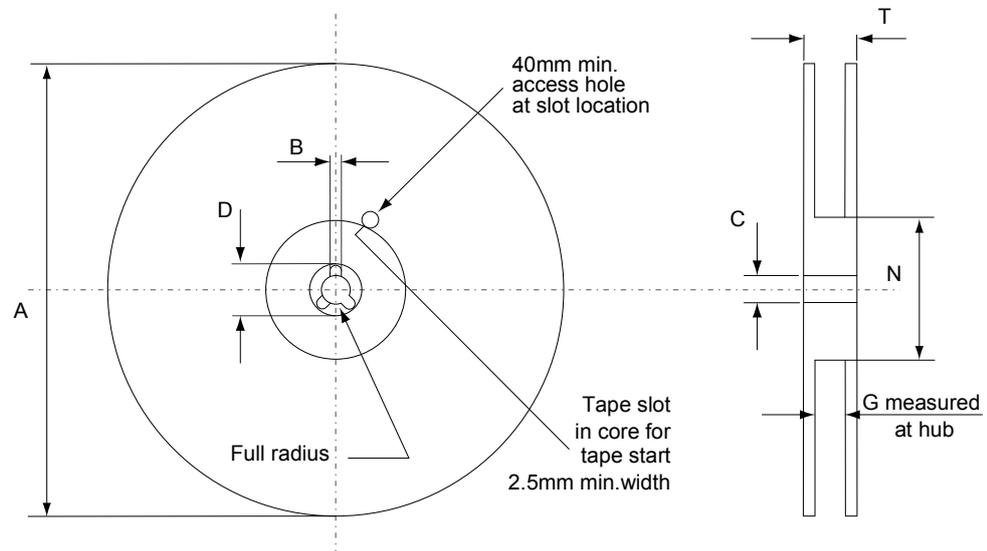
Figure 22. D²PAK type B tape outline


Figure 23. D²PAK type B reel outline


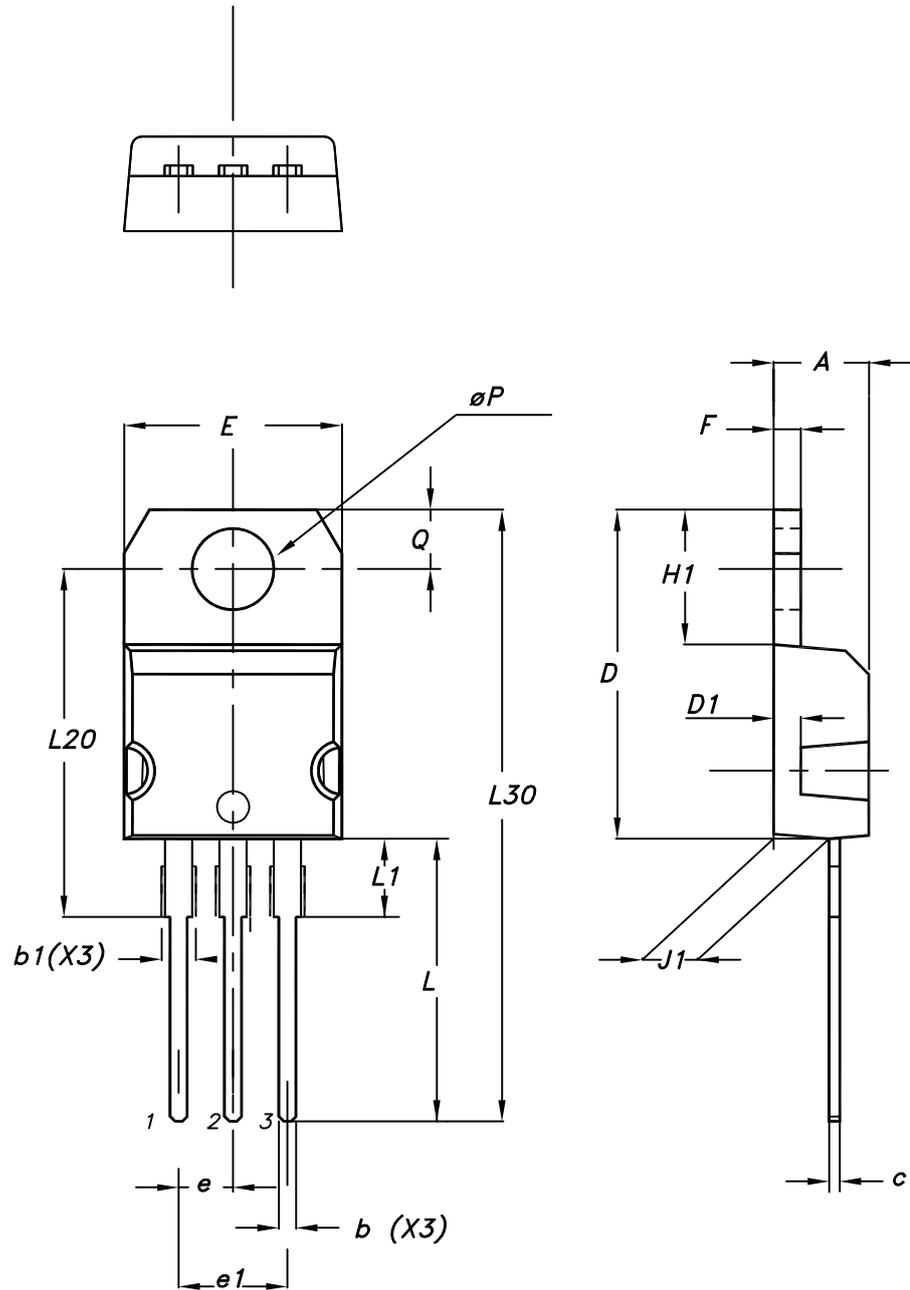
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Table 11. D²PAK type B reel mechanical data

Dim.	mm	
	Min.	Max.
A		330
B	1.5	
C	12.8	13.2
D	20.2	
G	24.4	26.4
N	100	
T		30.4

4.5 TO-220 type A package information

Figure 24. TO-220 type A package outline



0015988_typeA_Rev_21

Table 12. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

Revision history

Table 13. Document revision history

Date	Version	Changes
09-Sep-2004	1	First release
10-Jun-2005	2	Typing error, wrong description
26-Jul-2006	3	The document has been reformatted, no content change
31-Aug-2006	4	Typo mistake on order code
21-Dec-2006	5	Various changes on "Test conditions" for Table 5. and Table 6.
12-Jan-2007	6	Order code has been corrected
01-Oct-2018	7	<p>The part numbers STB11NM60-1 and STP11NM60FP have been moved to a separate datasheet and the document has been updated accordingly.</p> <p>Modified Table 1. Absolute maximum ratings, Table 2. Thermal data and Table 5. Dynamic.</p> <p>Modified Section 2.1 Electrical characteristics (curves).</p> <p>Updated Section 4 Package information.</p> <p>Minor text changes.</p>

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