OKI Semiconductor

MSM54V24616

131,072-Word × 16-Bit × 2-bank SYNCHRONOUS DYNAMIC RAM

DESCRIPTION

The MSM54V24616 is a 131,072-word × 16-bit × 2-bank synchronous dynamic RAM, fabricated in OKI's CMOS silicon gate process technology. The device operates at 3.3 V. The inputs and outputs are LVTTL compatible. This device can operate up to 125MHz by using synchronous interface.

FEATURES

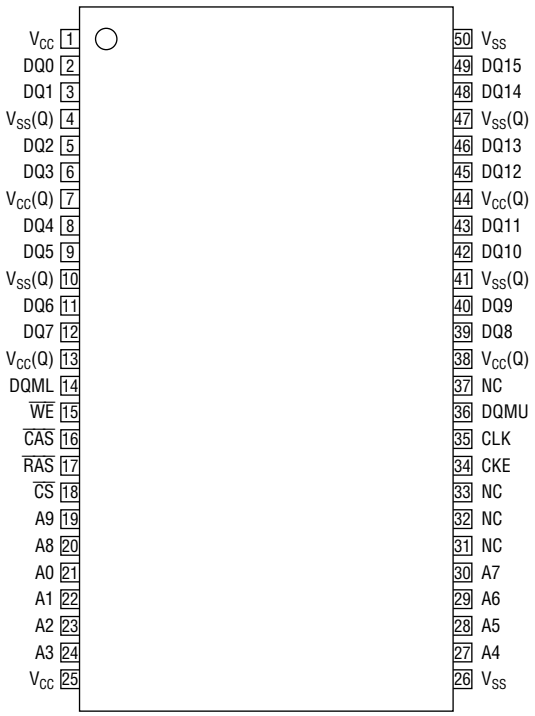
- 131,072-words × 16-bit × 2 banks configuration
- Single 3.3 V±10% power supply
- LVTTL compatible inputs and outputs

- All input signals are latched at rising edge of system clock
- Auto precharge and controlled precharge
- Internal pipelined operation: column address can be changed every clock cycle
- Dual internal banks controlled by A9 (Bank Address: BA)
- Independent byte operation via DQML and DQMU
- Programmable burst sequence (Sequential / Interleave)
- Programmable burst length (1, 2, 4, 8 and full page)
- Programmable $\overline{CAS}$ latency (1, 2 and 3)
- Programmable Write burst (Burst write / Single write)
- Burst stop function (full-page burst)
- Power Down operation and Active Power Down (Clock Suspend) operation
- Auto refresh and Self refresh capability
- Refresh period: 1,024 cycles / 16 ms
- Package options:
  50-pin plastic TSOP (type II) (TSOPII50-P-400-0.80-K) (Product : MSM54V24616-xxTS-K)
  xx indicates speed rank.

PRODUCT FAMILY

Family	Max. Frequency	Access Time (Max.)			Power Dissipation	
		t_{AC1}	t_{AC2}	t_{AC3}	Operating (Max.)	Standby (Max.)
MSM54V24616-8	125 MHz	22 ns	10 ns	7 ns	648 mW	7.2 mW
MSM54V24616-10	100 MHz	27 ns	12 ns	9 ns	540 mW	
MSM54V24616-12	83MHz	32 ns	15 ns	10 ns	468 mW	

PIN CONFIGURATION (TOP VIEW)



50-Pin Plastic TSOP (II)
(K Type)

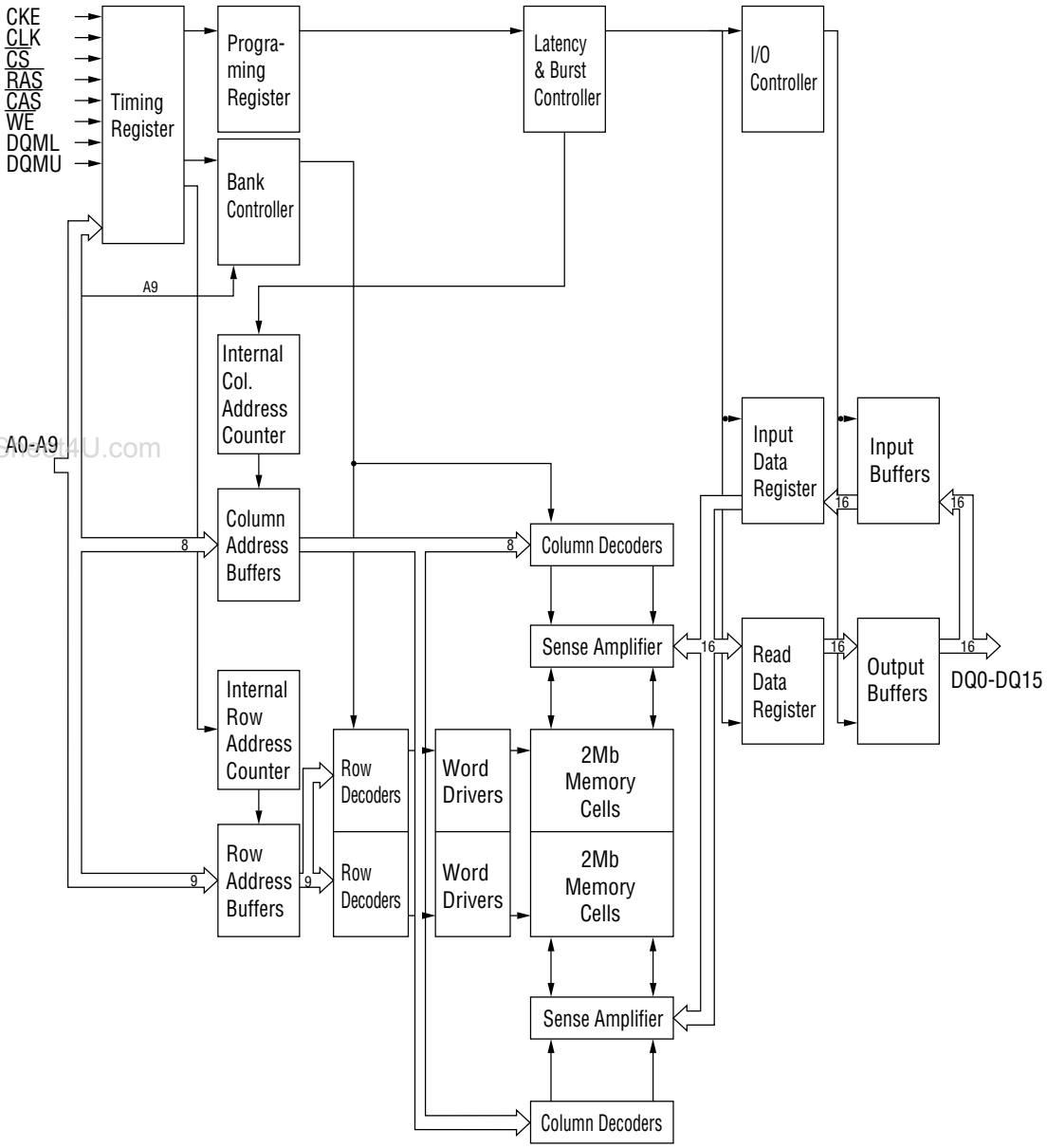
Pin Name	Function	Pin Name	Function
CLK	System Clock	DQML / DQMU	Data Input/Output Mask
$\overline{CS}$	Chip Select	DQ0 - DQ15	Data Input/Output
CKE	Clock Enable	V_{CC}	Power Supply (3.3 V)
A0 - A8	Address	V_{SS}	Ground (0 V)
A9	Bank Select Address	$V_{CC}(Q)$	Data Output Power Supply (3.3 V)
$\overline{RAS}$	Row Address Strobe	$V_{SS}(Q)$	Data Output Ground (0 V)
$\overline{CAS}$	Column Address Strobe	NC	No Connection
$\overline{WE}$	Write Enable		

Note: The same power supply voltage must be provided to every V_{CC} pin and $V_{CC}(Q)$pin. The same GND voltage level must be provided to every V_{SS} pin and $V_{SS}(Q)$ pin.

PIN DESCRIPTION

CLK	Fetches all inputs at the "H" edge.
$\overline{CS}$	Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE, DQMU and DQML.
CKE	Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command.
Address	Row & column multiplexed. Row address: RA0 - RA8 Column address: CA0 - CA7
A9	Selects bank to be activated during row address latch time and selects bank for precharge and read/write during column address latch time. A9= "L" : Bank A, A9= "H" : Bank B
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Functionality depends on the combination. For details, see the function truth table.
DQML DQMU	Masks the read data of two clocks later when DQMU / DQML is set "H" at the "H" edge of the clock signal. Masks the write data of the same clock when DQMU / DQML is set "H" at the "H" edge of the clock signal.
DQ0 - DQ15	Data inputs/outputs are multiplexed on the same pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(Voltages referenced to V_{SS})

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to 4.6	V
V_{CC} Supply Voltage	V_{CC}, $V_{CC}Q$	–0.5 to 4.6	V
Storage Temperature	T_{stg}	–55 to 150	°C
Power Dissipation	P_D*	1	W
Short Circuit Current	I_{OS}	50	mA
Operating Temperature	T_{opr}	0 to 70	°C

*: Ta = 25°C

Recommended Operating Conditions

(Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}, $V_{CC}Q$	2.97	3.3	3.63	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V

Capacitance

(V_{CC} = 3.3 V ±0.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	C_{IN1}	—	5	pF
Input Capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQML, DQMU)	C_{IN2}	—	5	pF
Input/Output Capacitance (DQ0 - DQ15)	C_{OUT}	—	7	pF

DC Characteristics

Parameter	Symbol	Condition			Version						Unit	Note
		Bank	CKE	Others	–8		–10		–12			
					Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	—	—	I_{OH} = –2 mA	2.4	—	2.4	—	2.4	—	V	
Output Low Voltage	V_{OL}	—	—	I_{OL} = 2 mA	—	0.4	—	0.4	—	0.4	V	
Input Leakage Current	I_{LI}	—	—	—	–10	10	–10	10	–10	10	µA	
Output Leakage Current	I_{LO}	—	—	—	–10	10	–10	10	–10	10	µA	
Average Power Supply Current (Operating)	$I_{CC}1$	One Bank Active	CKE ≥ V_{IH}	t_{CC} = min t_{RC} = min No Burst	—	130	—	110	—	90	mA	1, 2
	$I_{CC}1D$	Both Banks Active	CKE ≥ V_{IH}	t_{CC} = min t_{RC} = min t_{RRD} = min No Burst	—	180	—	150	—	130	mA	1, 2
Power Supply Current (Stand by)	$I_{CC}2$	Both Banks Precharge	CKE ≥ V_{IH}	t_{CC} = min	—	55	—	45	—	40	mA	3
Average Power Supply Current (Active Stand by Power Down Mode)	$I_{CC}3P$	One Bank Active	CKE ≤ V_{IL}	t_{CC} = min	—	5	—	5	—	5	mA	3
Average Power Supply Current (Active Stand by Non Power Down Mode)	$I_{CC}3N$	One Bank Active	CKE ≥ V_{IH}	t_{CC} = min	—	75	—	65	—	55	mA	3
Power Supply Current (Burst)	$I_{CC}4$	Both Banks Active	CKE ≥ V_{IH}	t_{CC} = min	—	150	—	130	—	110	mA	1, 2
Power Supply Current (Auto-Refresh)	$I_{CC}5$	One Bank Active	CKE ≥ V_{IH}	t_{CC} = min t_{RC} = min	—	120	—	100	—	80	mA	2
Average Power Supply Current (Self-Refresh)	$I_{CC}6$	Both Banks Precharge	CKE ≤ V_{IL}	t_{CC} = min	—	2	—	2	—	2	mA	
Average Power Supply Current (Power down)	$I_{CC}7$	Both Banks Precharge	CKE ≤ V_{IL}	t_{CC} = min	—	2	—	2	—	2	mA	

Notes: 1. Measured with outputs open.
2. Address and data can be changed once or not be changed during one cycle.
3. Address and data can be changed once or not be changed during two cycles.

Mode Set Address Keys

Operation Code			$\overline{CAS}$ Latency				Burst Type		Burst Length				
A9	A8	TM	A6	A5	A4	CL	A3	BT	A2	A1	A0	BT = 0	BT = 1
0	0	Burst Read and Burst Write	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	1	1	Interleave	0	0	1	2	2
1	0	Burst Read and Single Write	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
			1	0	0	Reserved			1	0	0	Reserved	Reserved
			1	0	1	Reserved			1	0	1	Reserved	Reserved
			1	1	0	Reserved			1	1	0	Reserved	Reserved
			1	1	1	Reserved			1	1	1	Full Page	Reserved

Note: A7 should stay "L" during mode set cycle.

MSM54V24616 series has two types of power on sequence.

POWER ON SEQUENCE 1

1. With inputs in NOP state, turn on the power supply and start the system clock.
2. After the V_{CC} voltage has reached the specified level, pause for 200 µs or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Apply an Auto-refresh eight or more times.
5. Enter the mode register setting command.

POWER ON SEQUENCE 2

1. With inputs in NOP state, turn on the power supply and start the system clock.
2. After the V_{CC} voltage has reached the specified level, pause for 100 µs or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Enter the mode register setting command.
5. Apply an Auto-refresh two or more times.

AC Characteristics 1

Note 1, 2

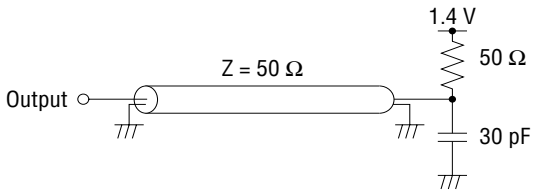
Parameter		Symbol	MSM54V24616-8		MSM54V24616-10		MSM54V24616-12		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Clock Cycles Time	CL = 3	t_{CC}	8	—	10	—	12	—	ns	
	CL = 2		12	—	15	—	18	—	ns	
	CL = 1		24	—	30	—	36	—	ns	
Access Time from Clock	CL = 3	t_{AC}	—	7	—	9	—	10	ns	3, 4
	CL = 2		—	10	—	12	—	15	ns	3, 4
	CL = 1		—	22	—	27	—	32	ns	3, 4
Clock "H" Pulse Time		t_{CH}	2.5	—	3	—	4	—	ns	
Clock "L" Pulse Time		t_{CL}	2.5	—	3	—	4	—	ns	
Input Setup Time		t_{SI}	2.5	—	3	—	3	—	ns	
Input Hold Time		t_{HI}	1	—	1	—	1.5	—	ns	
Output Low Impedance Time form Clock		t_{OLZ}	3	—	3	—	3	—	ns	
Output High Impedance Time form Clock		t_{OHZ}	—	6	—	8	—	10	ns	
Output Hold from Clock		t_{OH}	3	—	3	—	3	—	ns	3
$\overline{RAS}$ Cycle Time		t_{RC}	72	—	90	—	108	—	ns	
$\overline{RAS}$ Precharge Time		t_{RP}	24	—	30	—	36	—	ns	
$\overline{RAS}$ Active Time		t_{RAS}	48	10^5	60	10^5	72	10^5	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	24	—	30	—	36	—	ns	
Write Recovery Time		t_{WR}	16	—	20	—	24	—	ns	
Write Command Input Time form Output		t_{OWD}	16	—	20	—	24	—	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay Time		t_{RRD}	16	—	20	—	24	—	ns	
Refresh Time		t_{REF}	—	16	—	16	—	16	ms	
Power-down Exit Set-up Time		t_{PDE}	8	—	10	—	12	—	ns	
Input Level Transition Time		t_T	1	5	1	5	1	5	ns	

AC Characteristics 2

Note 1, 2

Parameter	Symbol	MSM54V24616-8			MSM54V24616-10			MSM54V24616-12			Unit	Note
CL		3	2	1	3	2	1	3	2	1		
t_{CK}		8	12	24	10	15	30	12	18	36	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay Time (Min.)	l_{CCD}	1	1	1	1	1	1	1	1	1	Cycle	
Clock Disable Time from CKE	l_{CKE}	1	1	1	1	1	1	1	1	1	Cycle	
Data Output High Impedance Time from DQM	l_{DOZ}	2	2	2	2	2	2	2	2	2	Cycle	
Data Input Mask Time from DQM	l_{DOD}	0	0	0	0	0	0	0	0	0	Cycle	
Data Input Time from Write Command	l_{DWD}	0	0	0	0	0	0	0	0	0	Cycle	
Data Output High Impedance Time from Precharge Command	l_{ROH}	3	2	1	3	2	1	3	2	1	Cycle	
Burst stop to output valid data hold	l_{BSR}	2	1	0	2	1	0	2	1	0	Cycle	
Burst stop to write data ignore	l_{BSW}	1	1	1	1	1	1	1	1	1	Cycle	
Active Command Input Time from Mode Register Set Command Input (Min.)	l_{MRD}	3	3	3	3	3	3	3	3	3	Cycle	

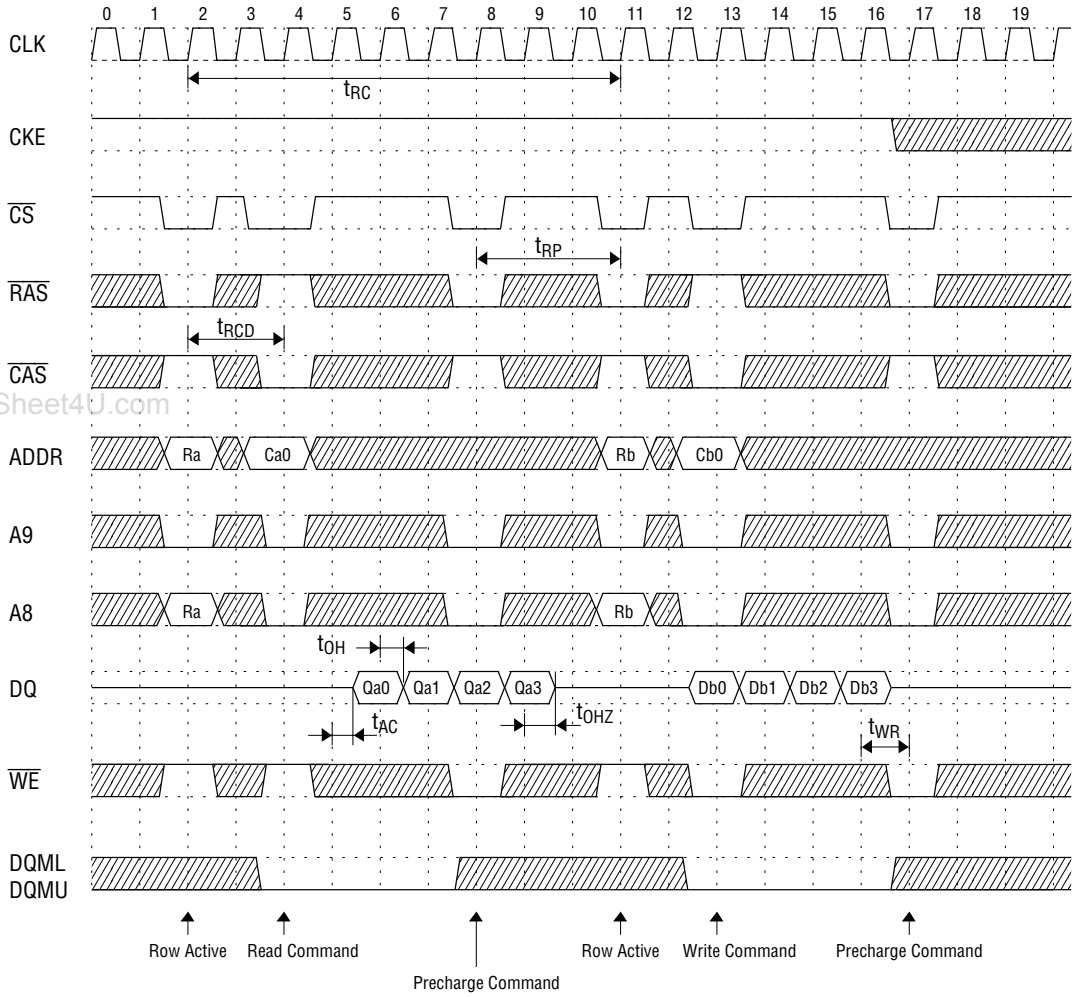
Notes : 1. AC measurements assume t_T = 1 ns.
2. The reference level for timing of input signals is 1.4 V.
3. Output load.



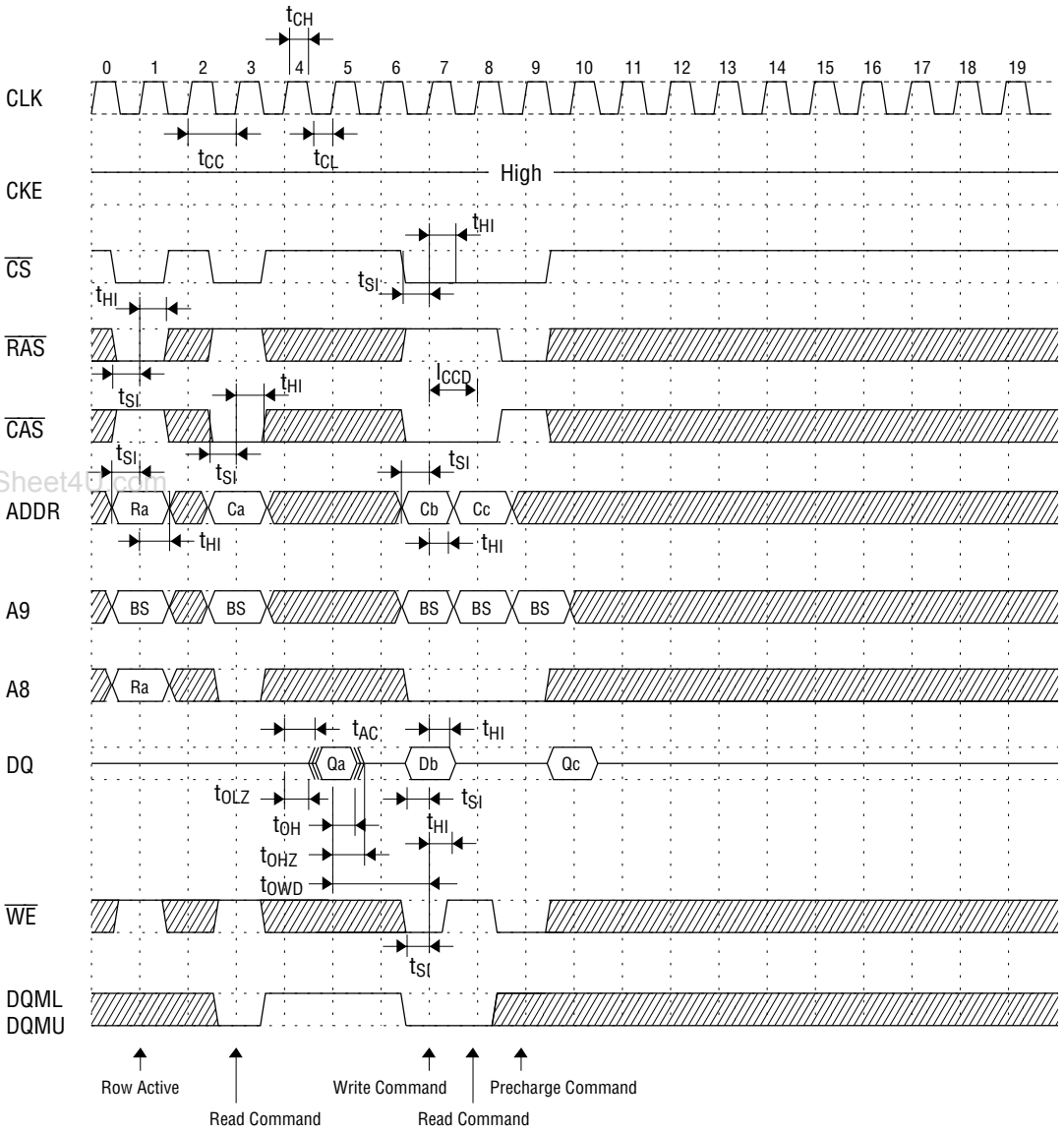
4. An access time is measured at 1.4 V.
5. If t_T is longer than 1ns, the reference level for timing of input signals is V_{IH} and V_{IL}.

TIMING WAVEFORM

Read & Write Cycle (Same Bank) @ $\overline{CAS}$ Latency = 2, Burst Length = 4



Single Bit Read-Write-Read Cycle (Same Page) @ $\overline{CAS}$ Latency = 2, Burst Length = 4



***Notes:** 1. When $\overline{CS}$ is set "High" at a clock transition from "Low" to "High", all inputs except CKE and DQML, DQMU are invalid.

2. When issuing an active, read or write command, the bank is selected by A9.

A9	Active, read or write
0	Bank A
1	Bank B

3. The auto precharge function is enabled or disabled by the A8 input when the read or write command is issued.

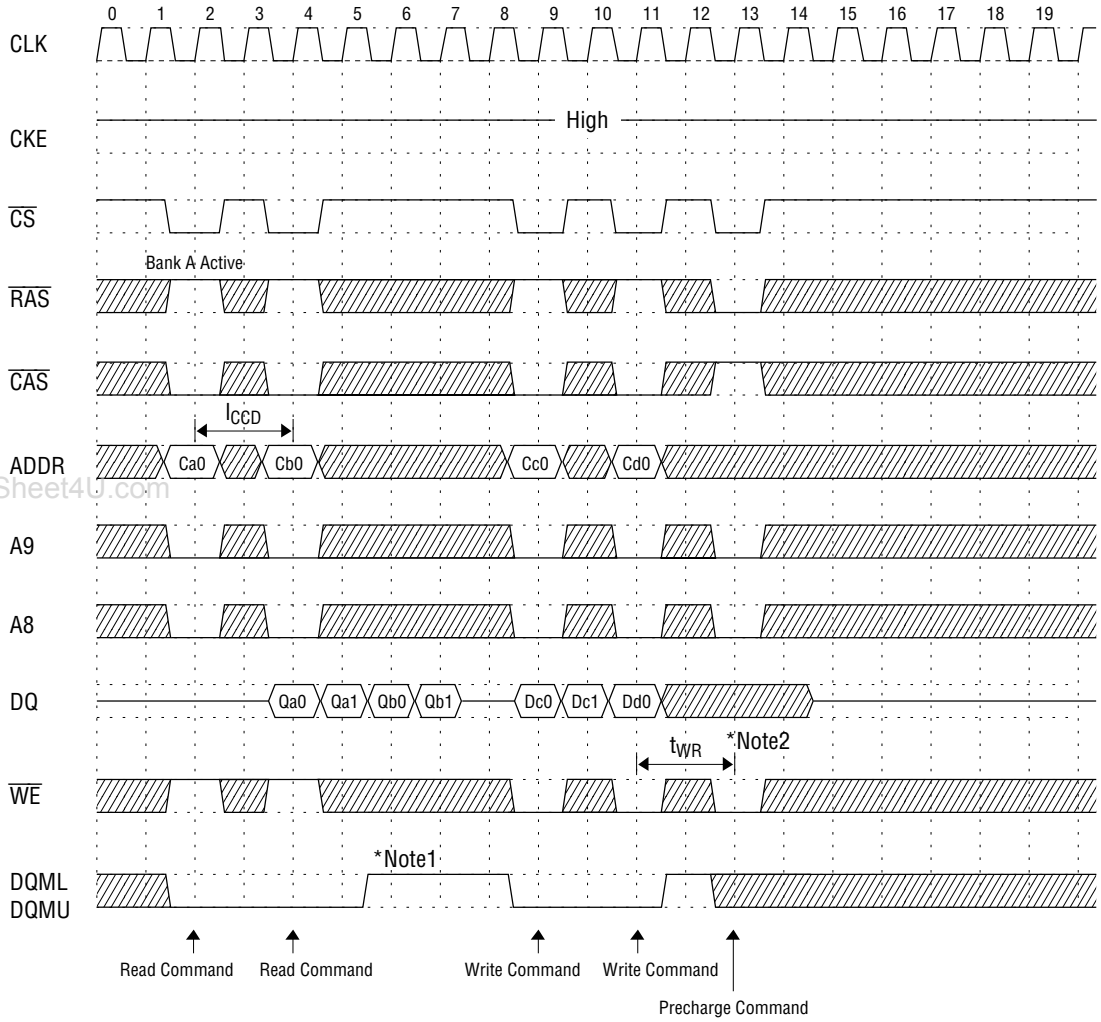
A8	A9	Operation
0	0	After the end of burst, bank A holds the active status.
1	0	After the end of burst, bank A is precharged automatically.
0	1	After the end of burst, bank B holds the active status.
1	1	After the end of burst, bank B is precharged automatically.

4. When issuing a precharge command, the bank to be precharged is selected by the A8 and A9 inputs.

A8	A9	Operation
0	0	Bank A is precharged.
0	1	Bank B is precharged.
1	X	Both bank A and B are precharged.

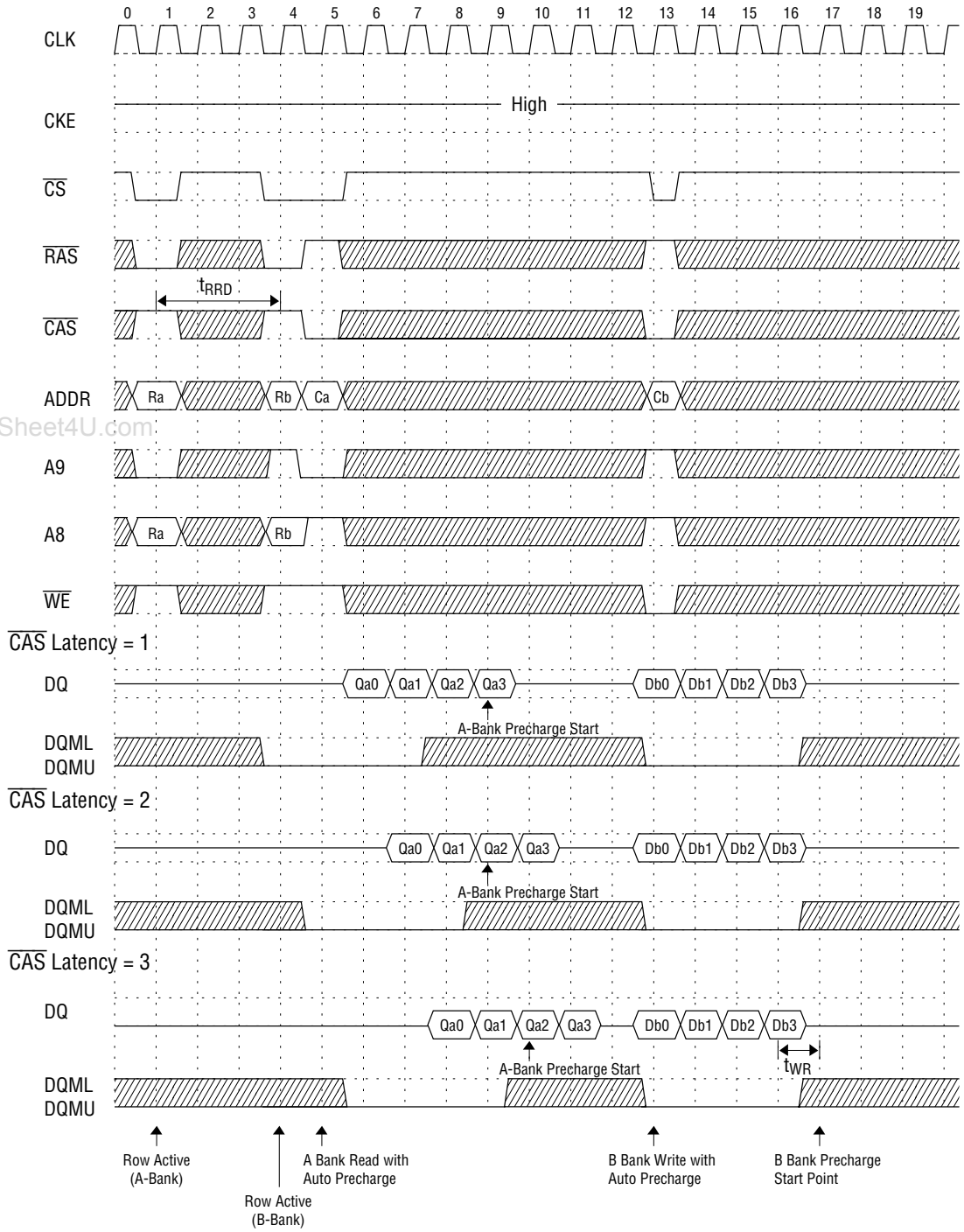
5. The input data and the write command are latched by the same clock (Write latency = 0).
6. The output is forced to high impedance by (1 CLK + t_{OHZ}) after DQML or DQMU entry.

Page Read & Write Cycle (Same Bank) @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4

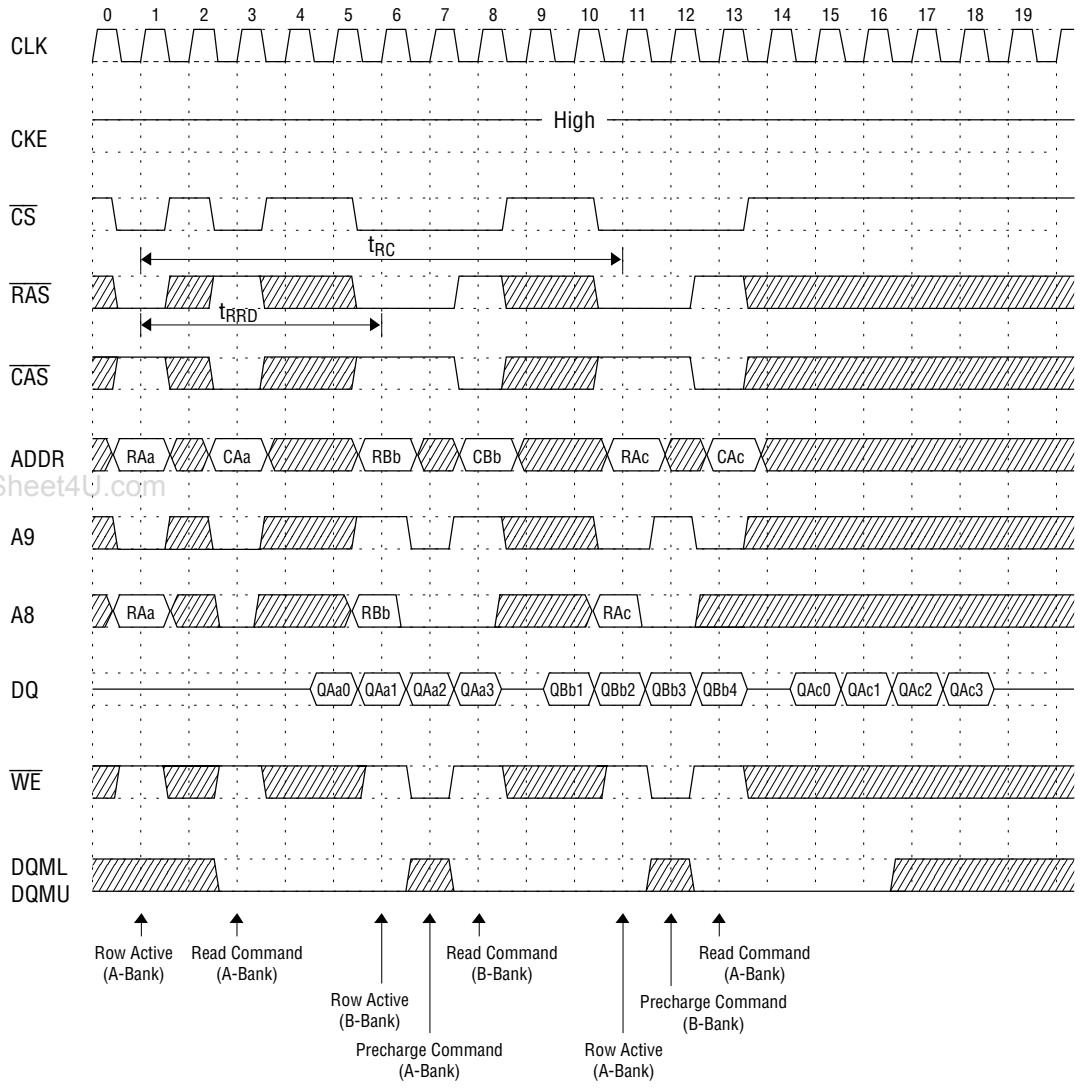


***Notes:**
1. To write data before a burst read ends, DQMi should be asserted three cycles prior to the write command, to avoid bus contention.
2. To assert row precharge before a burst write ends, wait t_{WR} after the last write data input. Input data during the precharge input cycle will be masked internally.

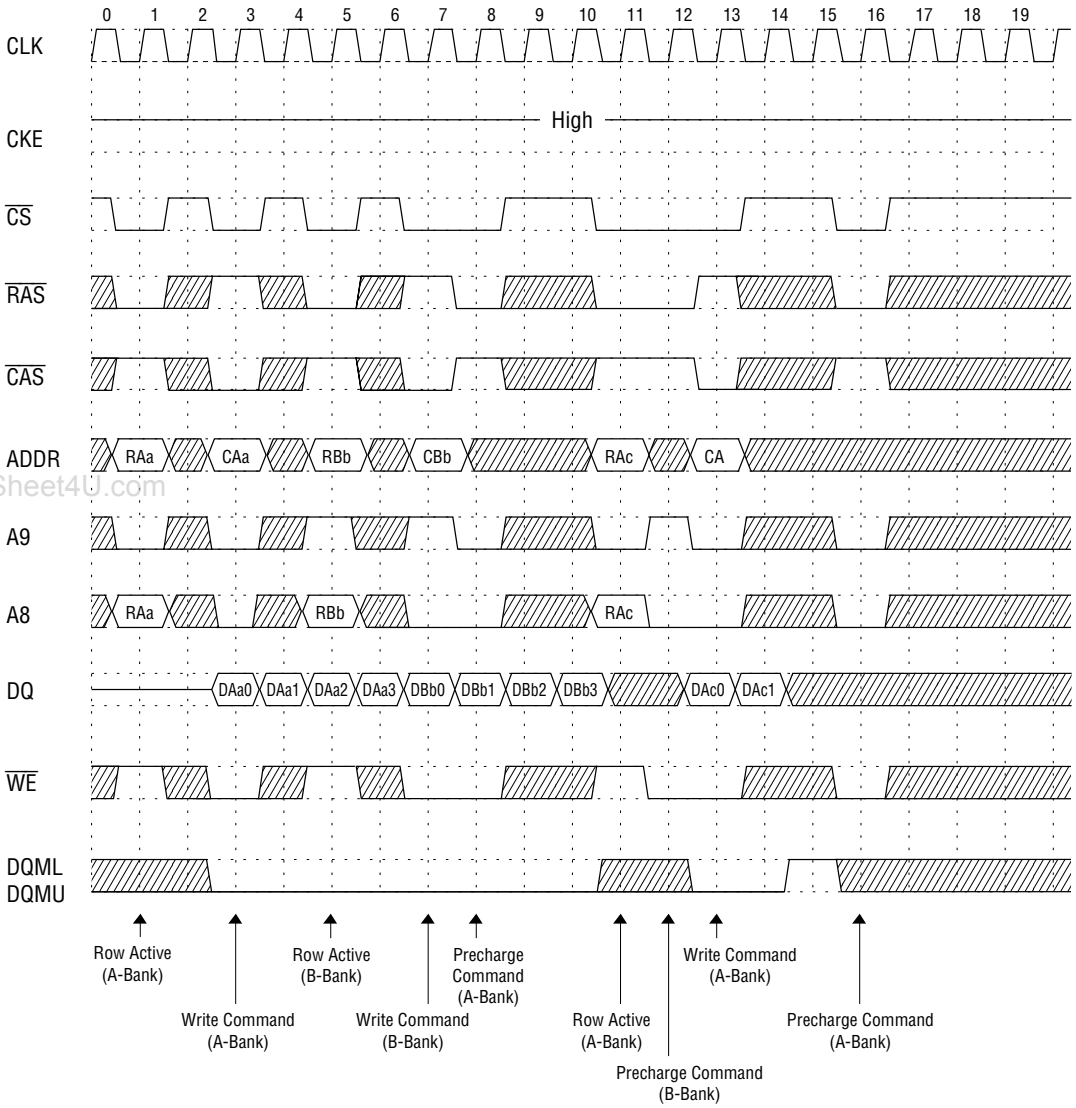
Read & Write Cycle with Auto Precharge @ Burst Length = 4



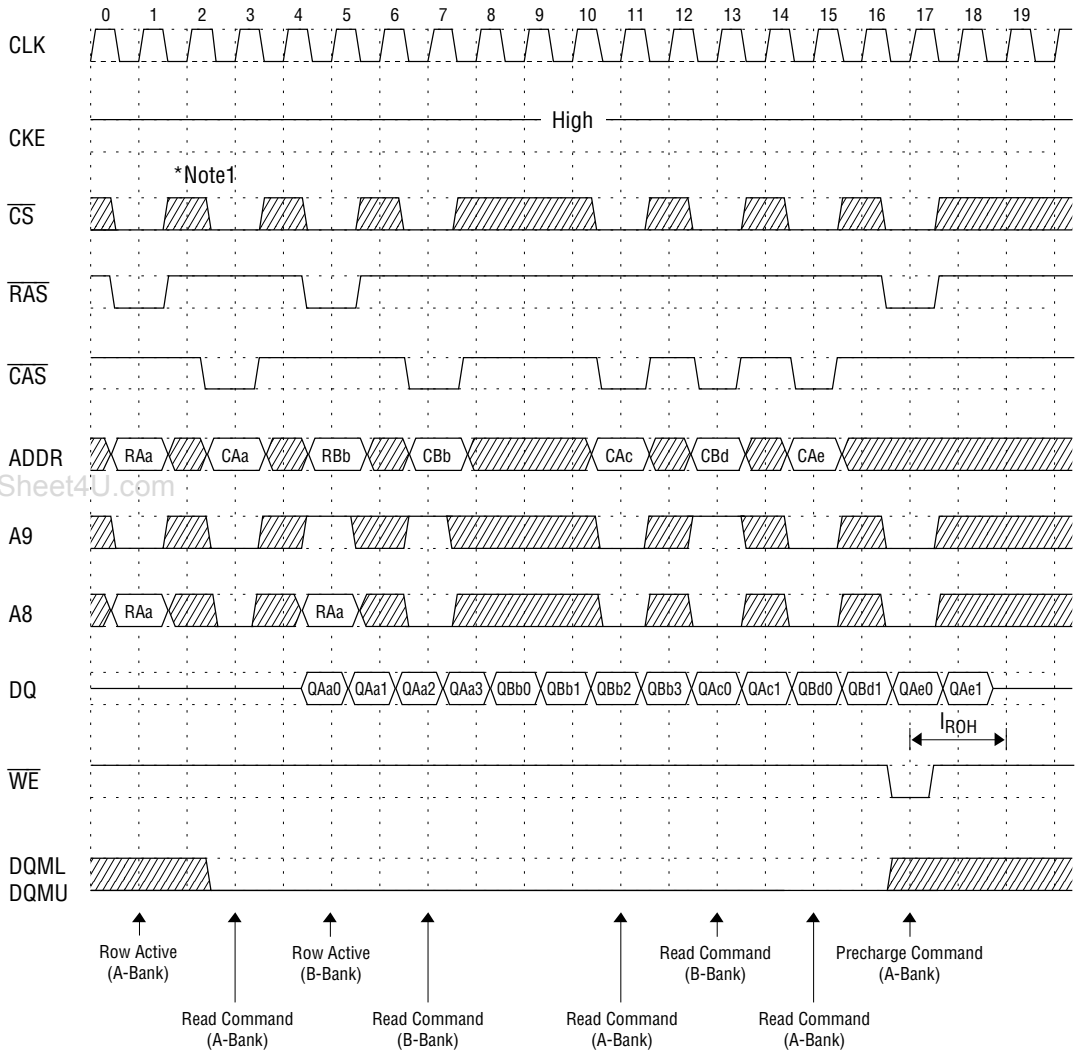
Bank Interleave Random Row Read Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



Bank Interleave Random Row Write Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4

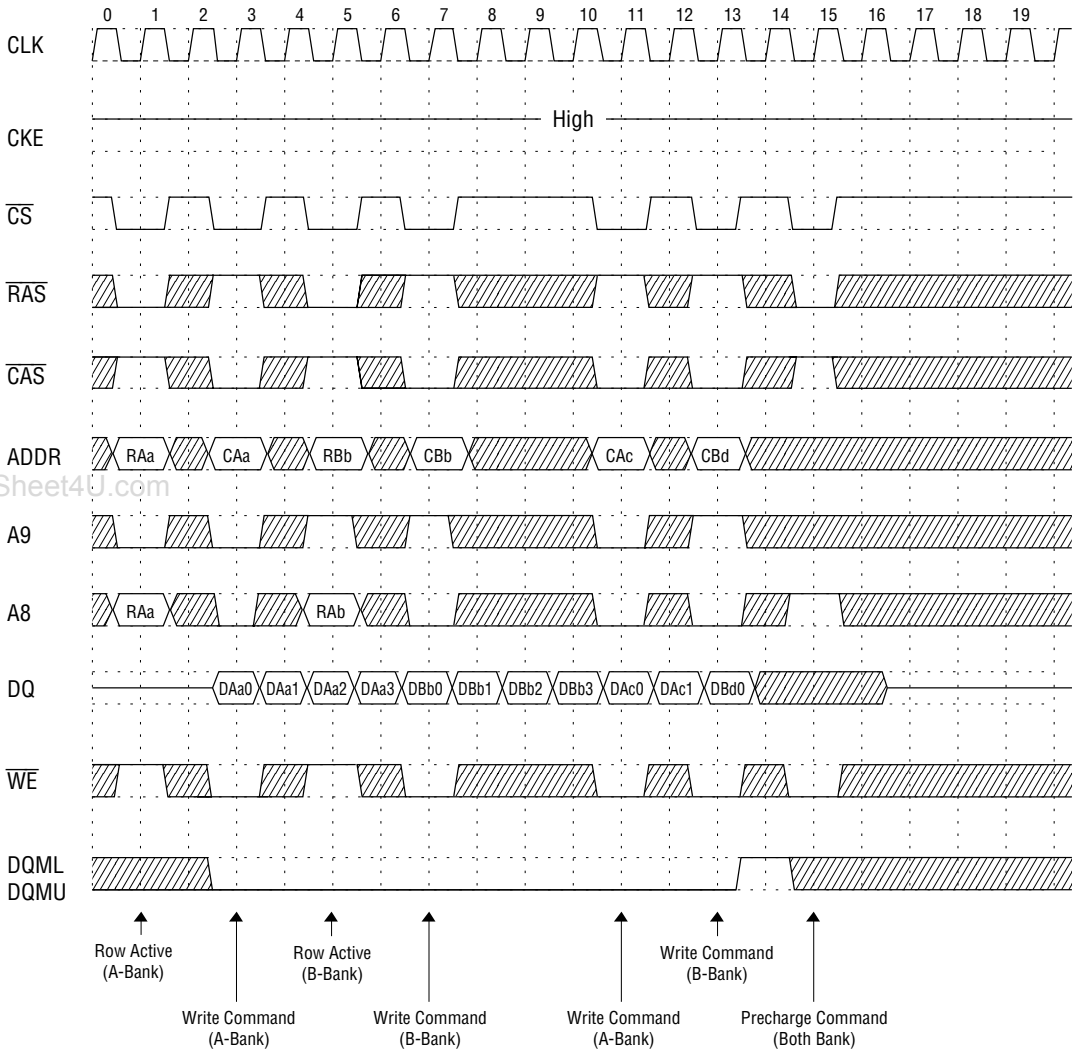


Bank Interleave Page Read Cycle @ $\overline{CAS}$ Latency = 2, Burst Length = 4

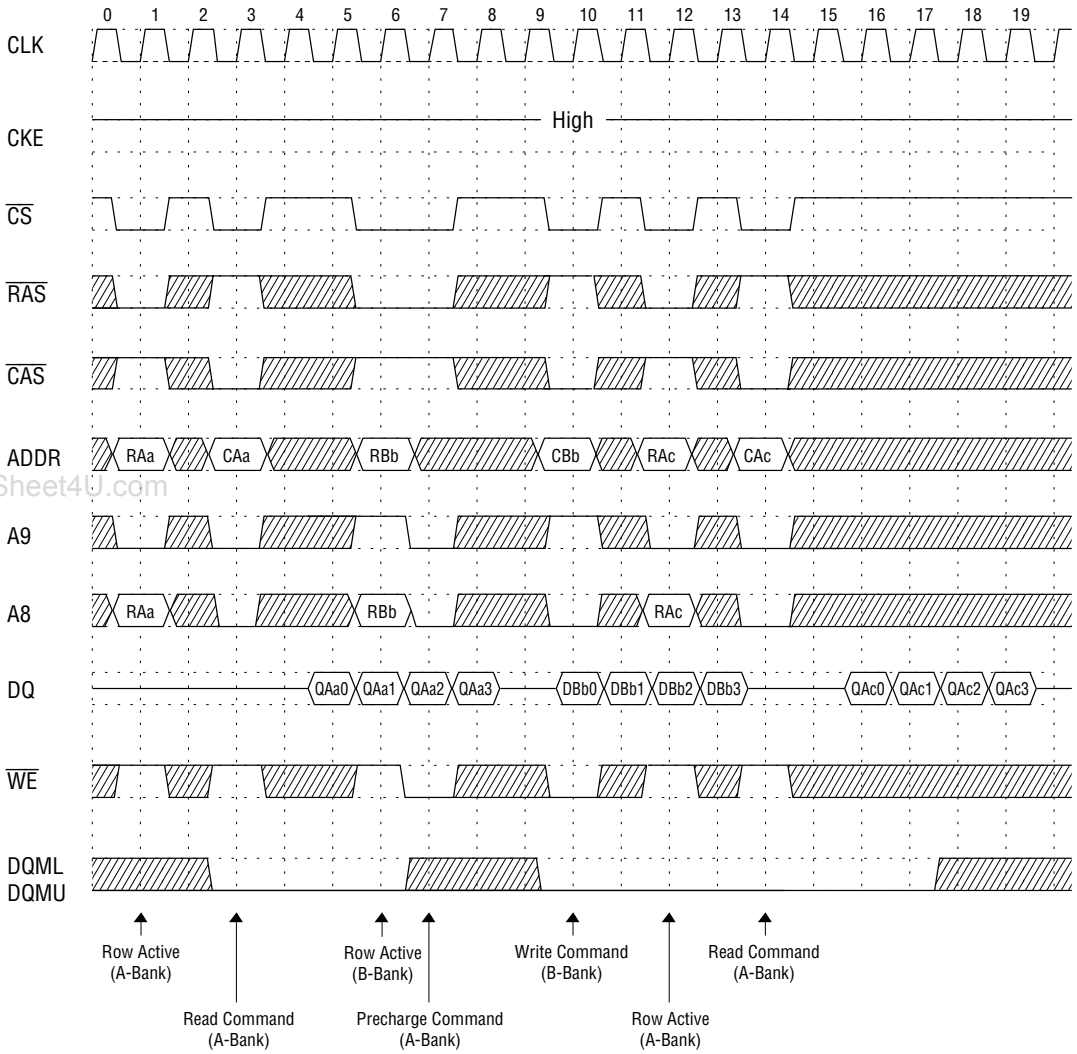


***Note:** 1. $\overline{CS}$ is ignored when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the same cycle.

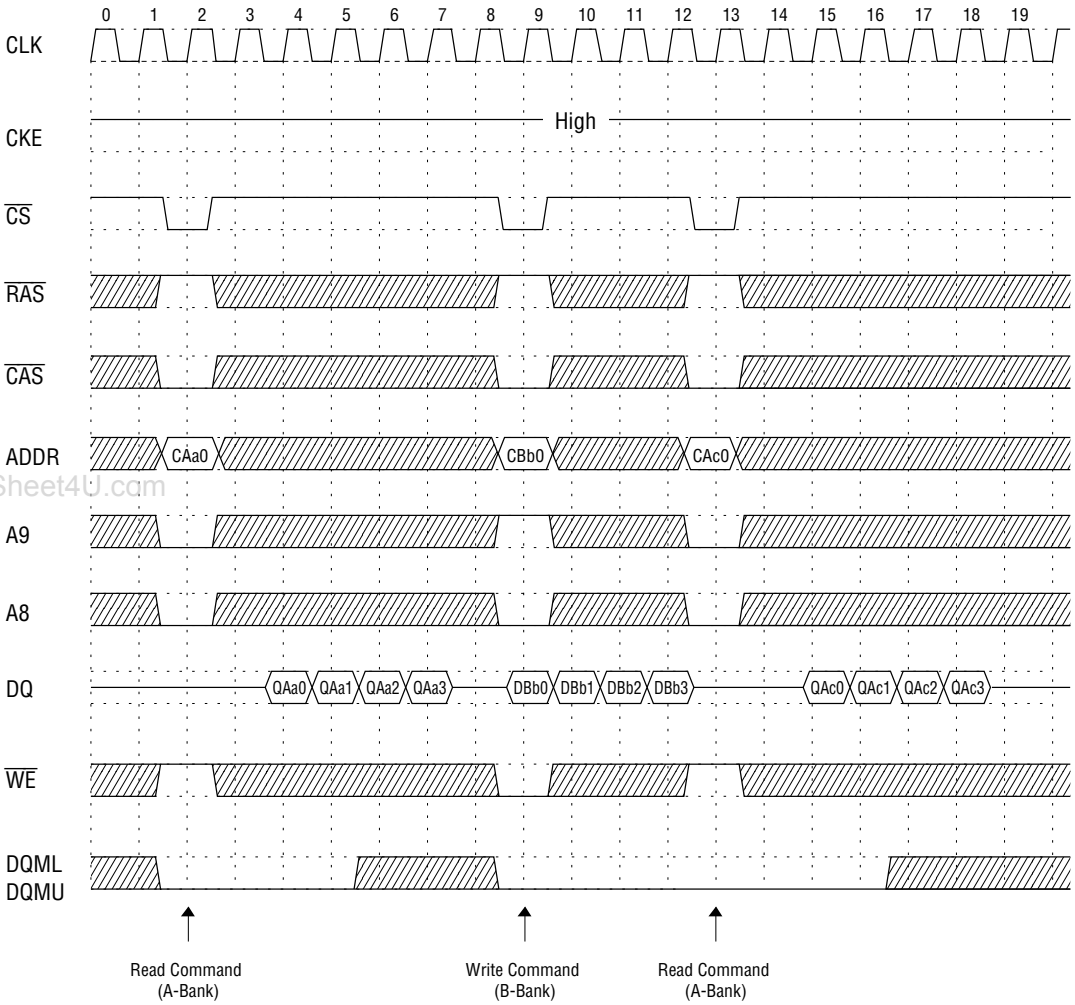
Bank Interleave Page Write Cycle @ $\overline{CAS}$ Latency = 2, Burst Length = 4



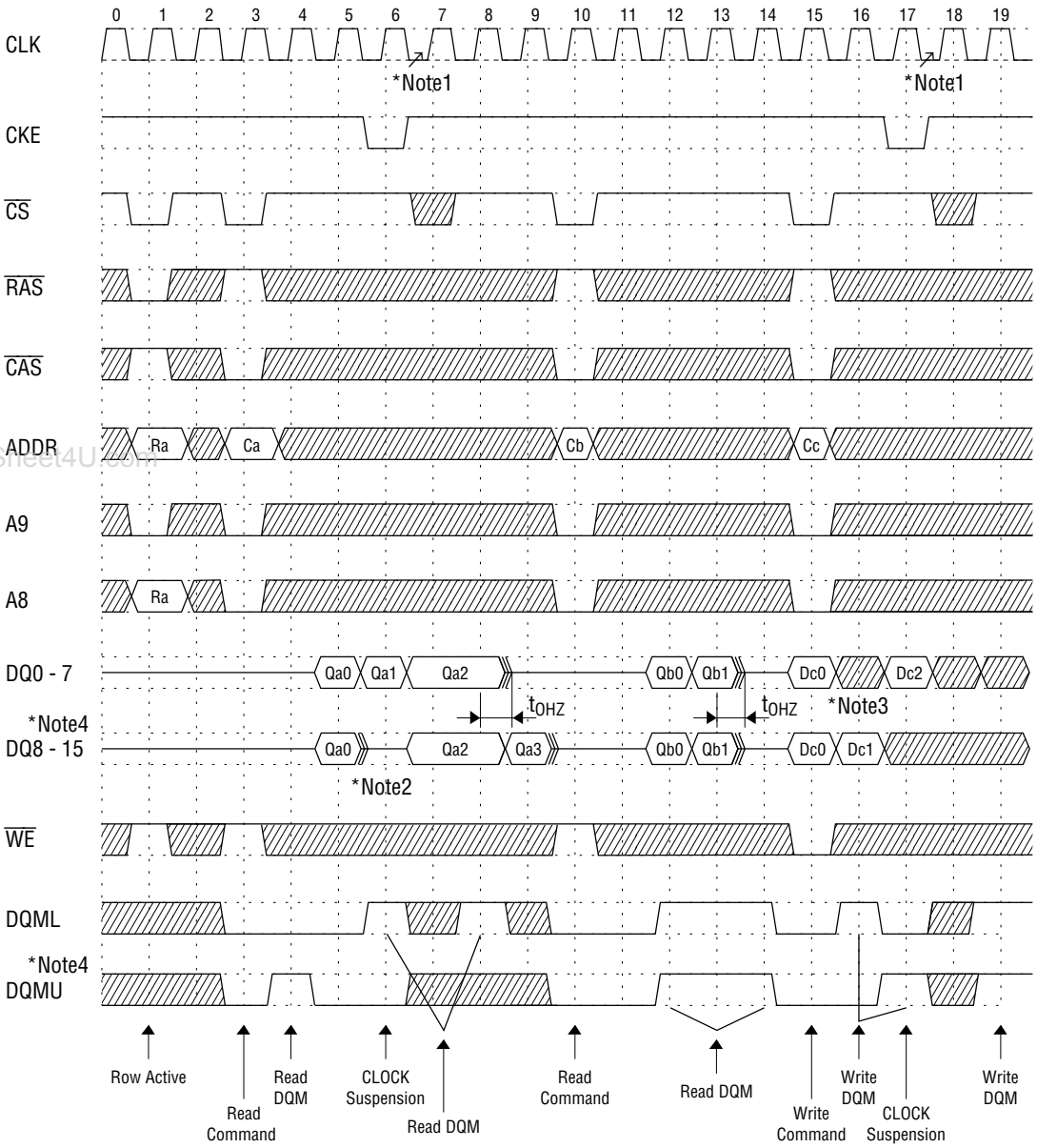
Bank Interleave Random Row Read/Write Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



Bank Interleave Page Read/Write Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4

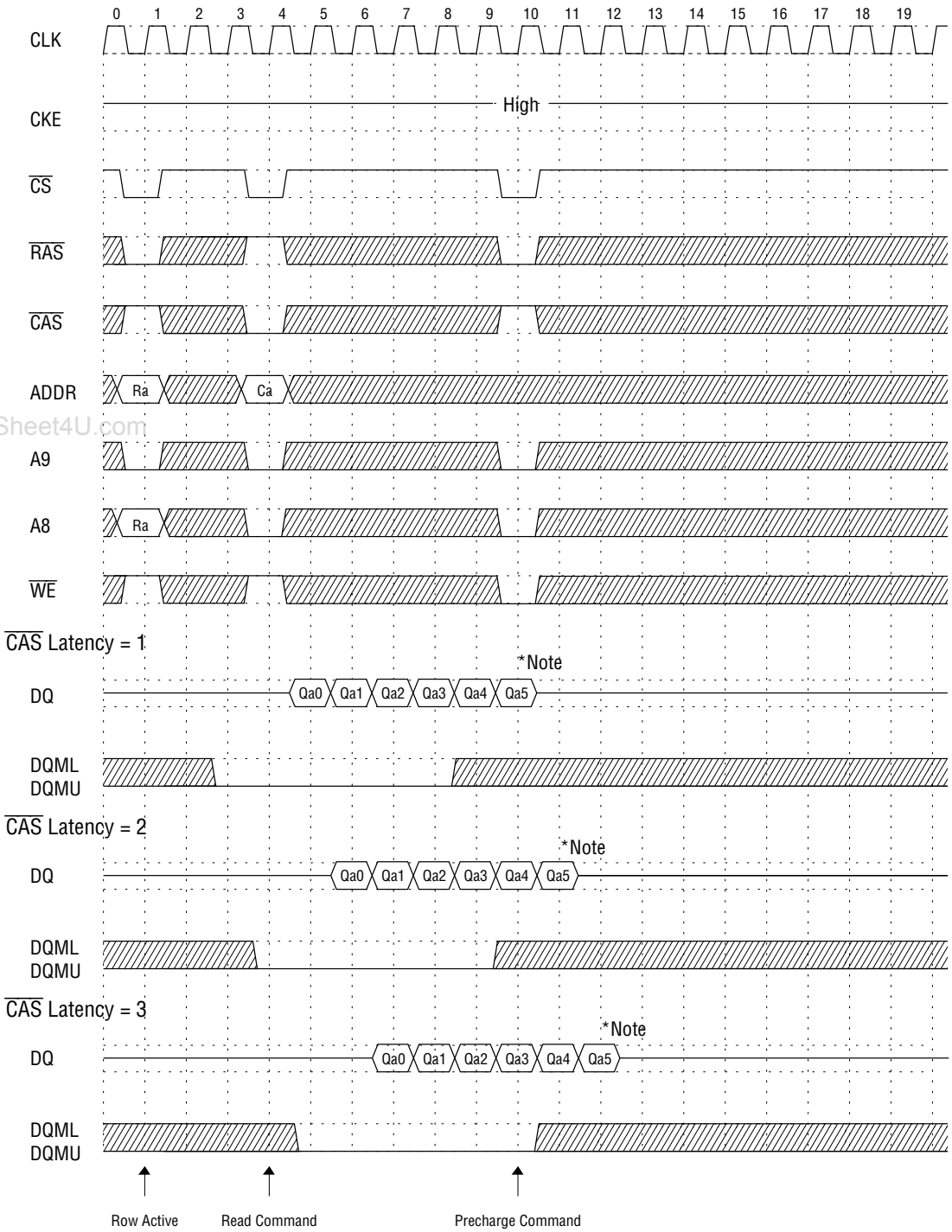


Clock Suspension & DQM Operation Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



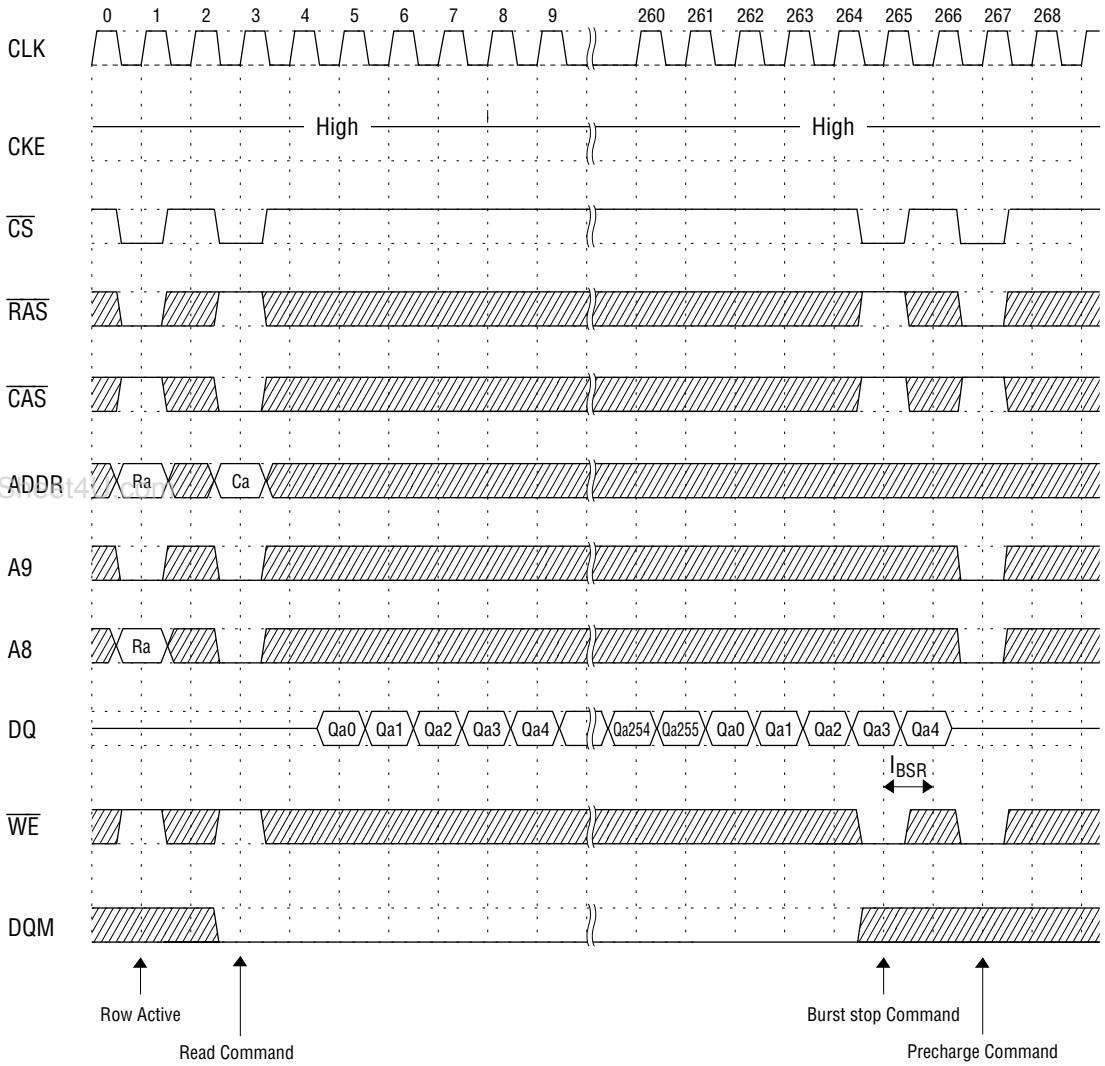
***Notes:**
1. When CKE is deactivated, the next clock cycle will be ignored.
2. When DQMs are asserted, the read data after two clock cycles will be masked.
3. When DQMs are asserted, the write data in the same clock cycle will be masked.
4. When DQML is set High, the input/output data of DQ0 - DQ7 will be masked.
   When DQMU is set High, the input/output data of DQ8 - DQ15 will be masked.

Read Interruption by Precharge Command @ Burst Length = 8

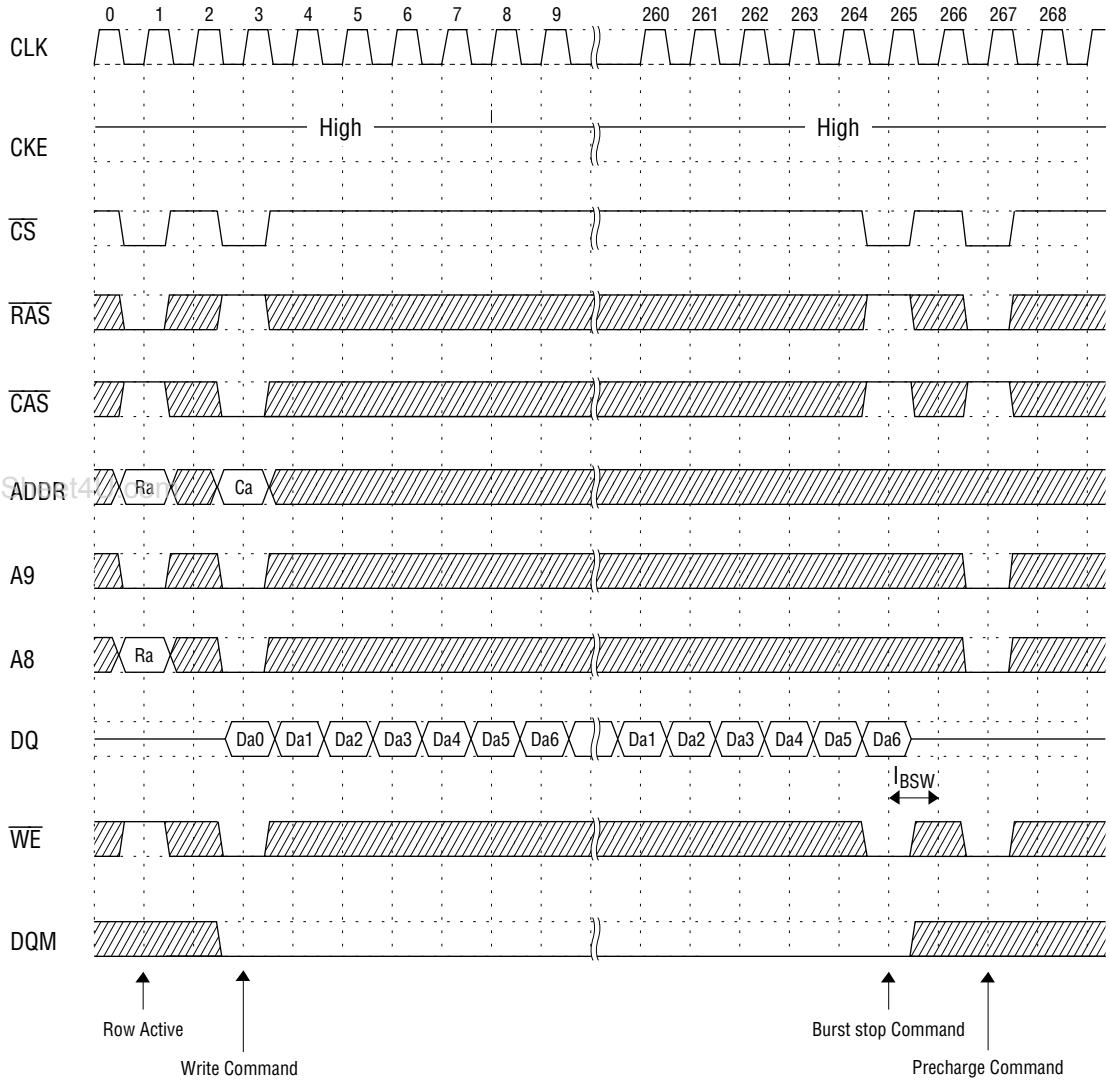


***Note:** When $\overline{CAS}$ latency = n, and if row precharge is asserted before a burst read ends, then the read data will not output after the n clock cycle of precharge command.

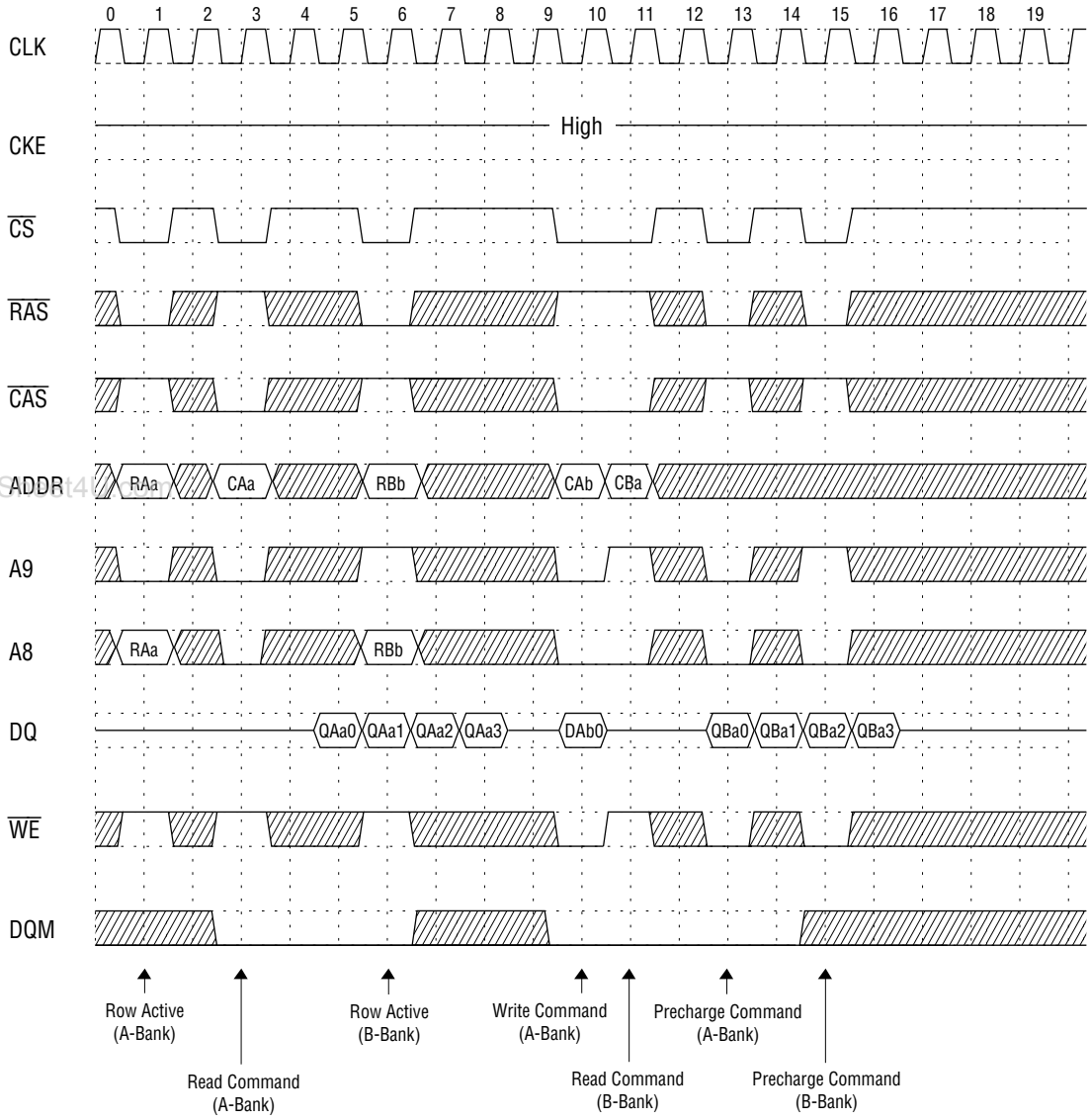
Full Page Burst Read Cycle @ $\overline{\text{CAS}}$ Latency = 2, Burst Length = Full page



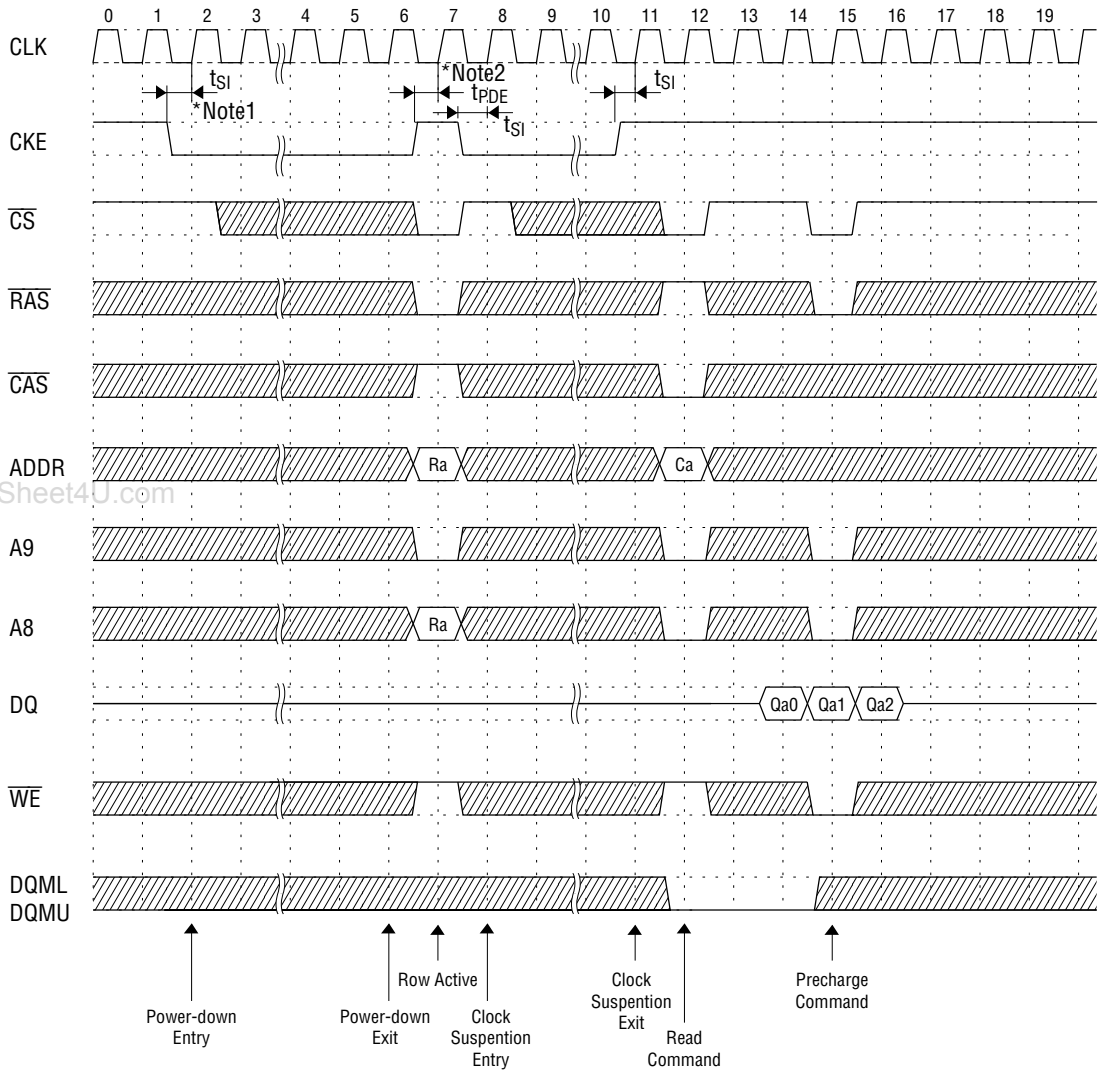
Full Page Burst Write Cycle @ $\overline{CAS}$ Latency = 2, Burst Length = Full page



Burst Read Single Write Cycle @ $\overline{CAS}$ Latency = 2, Burst Length = 4

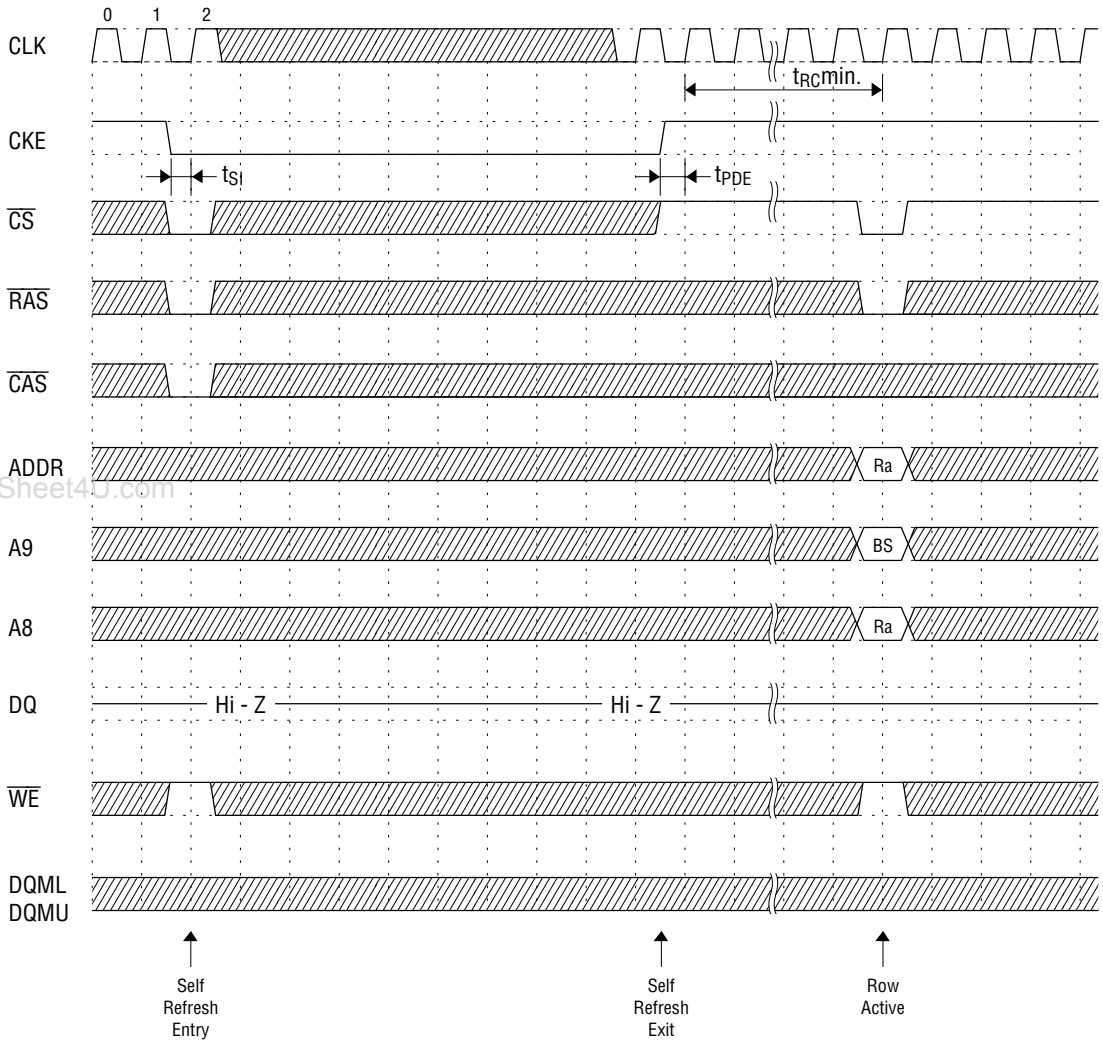


Power Down Mode @ $\overline{CAS}$ Latency = 2, Burst Length = 4

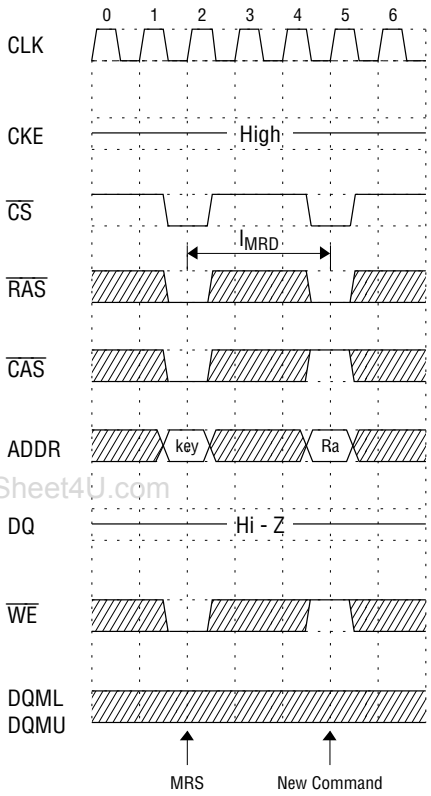


***Notes:**
1. When both banks are in precharge state, and if CKE is set low, then the MSM54V24616 enters power-down mode and maintains the mode while CKE is low.
2. To release the circuit from power-down mode, set CKE high for longer than t_{PDE}, and the inputs will be set within the same cycle.

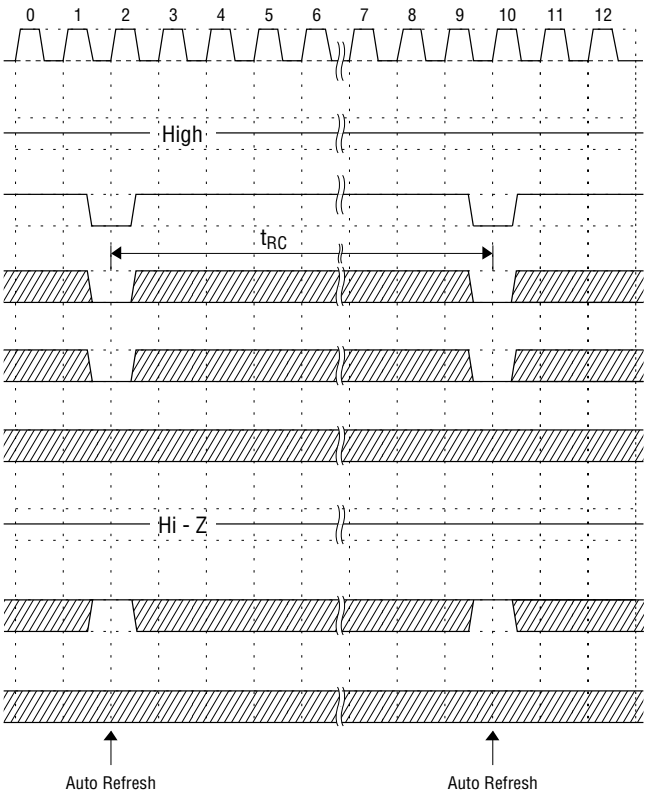
Self Refresh Cycle



Mode Register Set Cycle



Auto Refresh Cycle



FUNCTION TRUTH TABLE (Table 1) (1/2)

Current State[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	Action
Idle	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	Row Active
	L	L	H	L	BA	A8	NOP [4]
	L	L	L	H	X	X	Auto-Refresh or Self-Refresh [5]
	L	L	L	L		OP Code	Mode Register write
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BA	CA, A8	Read
	L	H	L	L	BA	CA, A8	Write
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A8	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	Burst stop (Full page), NOP (BL=1, 2, 4 and 8)
	L	H	L	H	BA	CA, A8	Term Burst, start new Burst Read
	L	H	L	L	BA	CA, A8	Term Burst, start new Burst Write
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A8	Term Burst, execute Row Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	Burst stop (Full page), NOP (BL=1, 2, 4 and 8)
	L	H	L	H	BA	CA, A8	Term Burst, Start new Burst Read
	L	H	L	L	BA	CA, A8	Term Burst, start new Burst write
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A8	Term Burst, executo Row Precharge
	L	L	L	X	X	X	ILLEGAL
Read with	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
Auto Precharge	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	H	BA	CA, A8	ILLEGAL [2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A8	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Write with	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
Auto Precharge	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	H	BA	CA, A8	ILLEGAL [2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A8	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL

FUNCTION TRUTH TABLE (Table 1) (2/2)

Current State[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	Action
Precharge	H	X	X	X	X	X	NOP --> Idle after t_{RP}
	L	H	H	H	X	X	NOP --> Idle after t_{RP}
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A8	NOP [4]
	L	L	L	X	X	X	ILLEGAL
Write Recovery	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A8	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Row Active	H	X	X	X	X	X	NOP --> Row Active after t_{RCD}
	L	H	H	H	X	X	NOP --> Row Active after t_{RCD}
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A8	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Refresh	H	X	X	X	X	X	NOP --> Idle after t_{RC}
	L	H	H	X	X	X	NOP --> Idle after t_{RC}
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Mode Register	H	X	X	X	X	X	NOP
Access	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

ABBREVIATIONS
RA = Row Address BA = Bank Address NOP = No OPeration command
CA = Column Address AP = Auto Precharge

Notes:
1. All inputs will be enabled when CKE is set high for at least 1 cycle prior to the inputs.
2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
3. Satisfy the timing of t_{CCD} and t_{WR} to prevent bus contention.
4. NOP to bank precharging or in idle state. Precharges activated bank by BA or A8.
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE for CKE (Table 2)

Current State (n)	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	Action
Self Refresh [6]	H	x	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh --> ABI
	L	H	L	H	H	H	X	Exit Self Refresh --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)
Power Down [6]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Power Down --> ABI
	L	H	L	H	H	H	X	Exit Power Down --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL [7]
	L	L	X	X	X	X	X	NOP (Continue power down mode)
All Banks Idle [7]	H	H	X	X	X	X	X	Refer to Table 1
(ABI)	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	L	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State Other	H	H	X	X	X	X	X	Refer to Operations in Table 1
than Listed Above	H	L	X	X	X	X	X	Begin Clock Suspend Next Cycle
	L	H	X	X	X	X	X	Enaole Clock of Next Cycle
	L	L	X	X	X	X	X	Continue Clock Suspension

Notes: 6. If a minimam set-up time t_{PDE} is satisfied when CKE transitions from "L" to "H", CKE operates asynchronously so that a command can be input in the same internal clock cycle.
7. Power-down and self refresh can be entered only when all the banks are in an idle state.