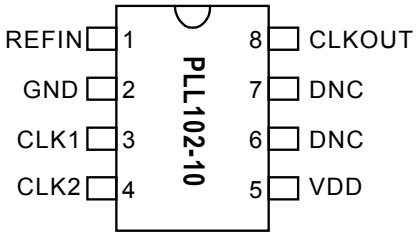
PLL102-10

Low Skew Output Buffer

FEATURES

- Frequency range 50 ~ 120MHz.
- Internal phase locked loop will allow spread spectrum modulation on reference clock to pass to outputs.
- Zero input - output delay.
- Less than 700 ps device - device skew.
- Less than 250 ps skew between outputs.
- Less than 100 ps cycle - cycle jitter.
- 2.5V or 3.3V power supply operation.
- Available in 8-Pin SOIC or MSOP package.

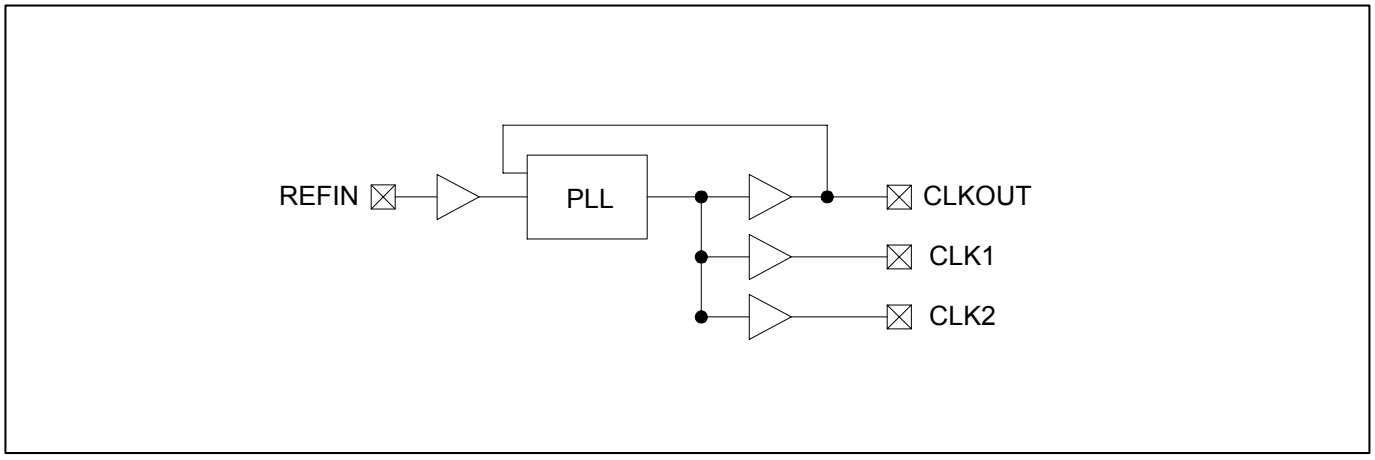
PIN CONFIGURATION



DESCRIPTION

The PLL102-10 is a high performance, low skew, low jitter zero delay buffer designed to distribute high speed clocks and is available in 8-pin SOIC or MSOP package. It has two outputs that are synchronized with the input. The synchronization is established via CLKOUT feed back to the input of the PLL. Since the skew between the input and output is less than ±350 ps, the device acts as a zero delay buffer.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Number	Type	Description
REFIN	1	I	Input reference frequency. Spread spectrum modulation on this signal will be passed to the output (up to 100kHz SST modulation).
GND	2	P	Ground Connection.
CLK1	3	O	Buffered clock output.
CLK2	4	O	Buffered clock output.
VDD	5	P	2.5V or 3.3V Power Supply connection.
DNC	6 & 7	-	Do Not Connect
CLKOUT2	8	O	Buffered clock output. Internal feed back on this pin.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Electrical Characteristics

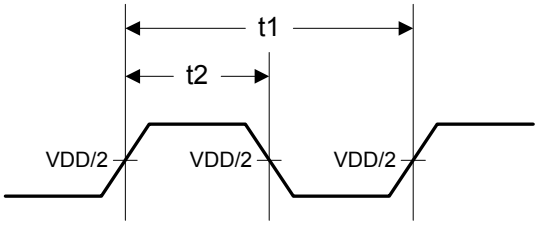
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}		2.25		3.63	V
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Output Low Voltage	V_{OL}	I_{OL} = 24mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 24mA	2.4			V
Supply Current	I_{DD}	Unloaded outputs at 100MHz, VDD=3.3V.		22	30	mA

3. Switching Characteristics

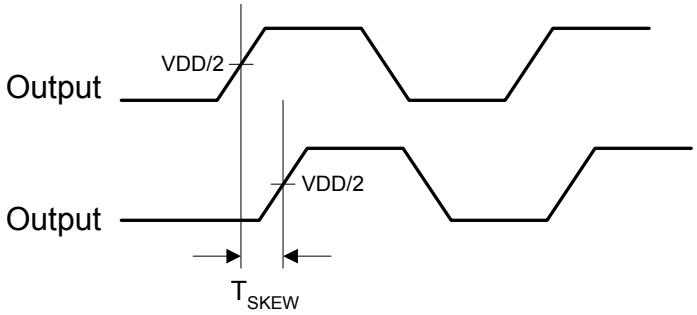
PARAMETERS	SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Output Frequency	t1		50		120	MHz
Duty Cycle	DC	Measured at VDD/2, C_L=15pF, F_{out} = 100MHz	45	50	55	%
Rise Time	T_r	Measured between 10% and 90%VDD, C_L=15pF		1.2	1.5	ns
Fall Time	T_f	Measured between 90% and 10%, C_L=15pF		1.2	1.5	ns
Output to Output Skew	T_{skew}	All outputs equally loaded, C_L=15pF			250	ps
Delay, REF Rising Edge to CLKOUT Rising Edge	T_{delay}	Measured at VDD/2		0	±350	ps
Device to Device Skew	$T_{dsk-dsk}$	Measured at V_{DD}/2 on the CLKOUT pins of devices		0	700	ps
Cycle to Cycle Jitter	$T_{cyc-cyc}$	Measured at 100MHz			60	ps peak
PLL Lock Time	T_{lock}	Stable power supply, valid clock presented on REF pin			1.0	ms
Jitter; Absolute Jitter	T_{jabs}	At 10,000 cycles, low jitter input signal		20	50	ps
Jitter; 1-sigma	T_{j1-s}	At 10,000 cycles, low jitter input signal		9	15	ps

SWITCHING WAVEFORMS

Duty Cycle Timing

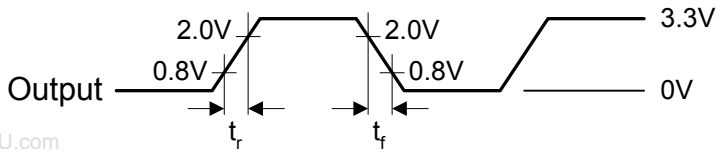


Output - Output Skew

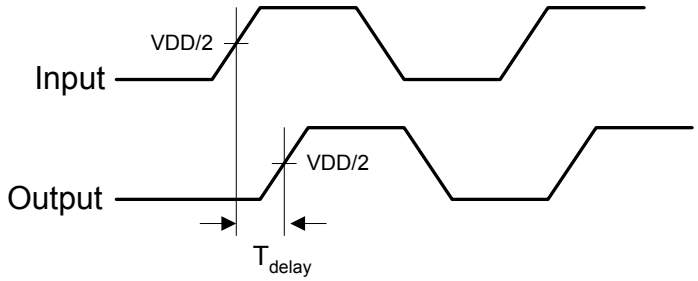


SWITCHING WAVE FORMS

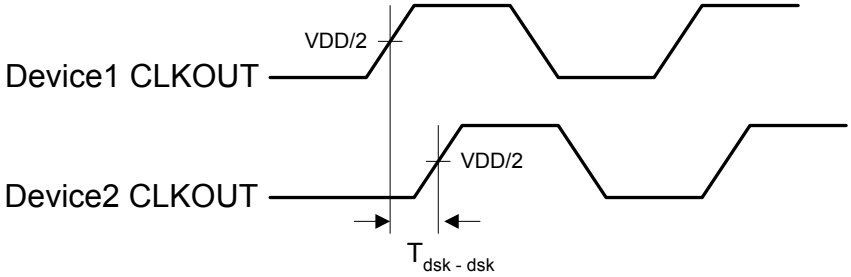
All Outputs Rise/Fall Time



Input to Output Propagation Delay



Device to Device Skew



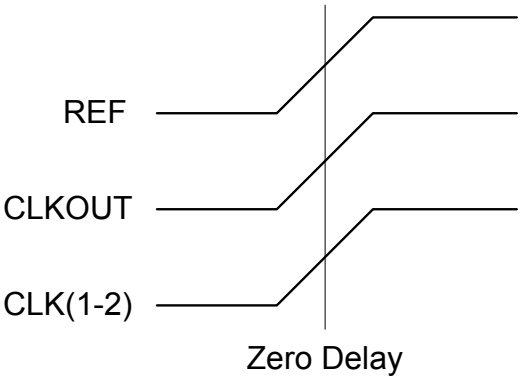
Output-Output Skew

The skew between CLKOUT and the CLK(1-2) outputs is not dynamically adjusted by the PLL. Since CLKOUT is one of the inputs to the PLL, zero phase difference is maintained from REF to CLKOUT. If all outputs are equally loaded, zero phase difference will be maintained from REF to all outputs.

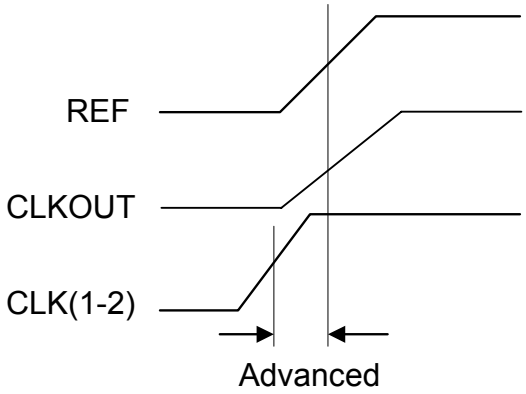
If applications requiring zero output-output skew, all the outputs must be equally loaded.

If the CLK(1-2) outputs are less loaded than CLKOUT, CLK(1-2) outputs will lead it; if the CLK(1-2) is more loaded than CLKOUT, CLK(1-2) will lag the CLKOUT.

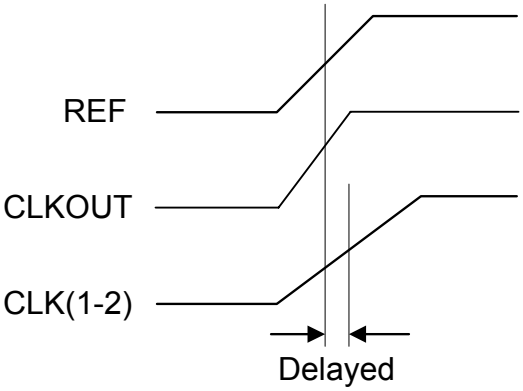
Since the CLKOUT and the CLK(1-2) outputs are identical, they all start at the same time, but difference loads cause them to have different rise times and different times crossing the measurement thresholds.



REF input and all outputs are equally loaded



REF input and CLK(1-2) outputs are equally loaded, with CLK(1-2) less loaded than CLKOUT.

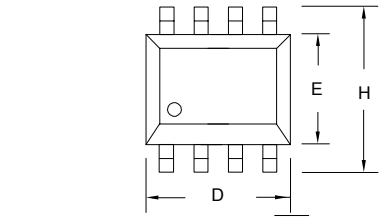


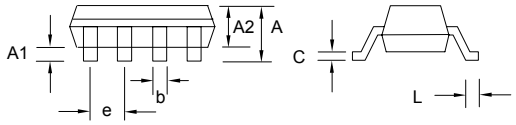
REF input and CLK(1-2) outputs loaded equally, withCLK(1-2) more loaded then CLKOUT.

PACKAGE INFORMATION

SOIC 8L

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	





ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL102-10 S C

PART NUMBER

TEMPERATURE
C=COMMERCIAL
I=INDUSTRIAL

PACKAGE TYPE
S=SOIC

Order Number	Marking	Package Option
PLL102-10SC-R	P102-10SC	SOIC - Tape and Reel
PLL102-10SC	P102-10SC	SOIC - Tube