

## MSM65344A

### 8-Bit Microcontroller with A/D Converter (with LCD Driver)

#### GENERAL DESCRIPTION

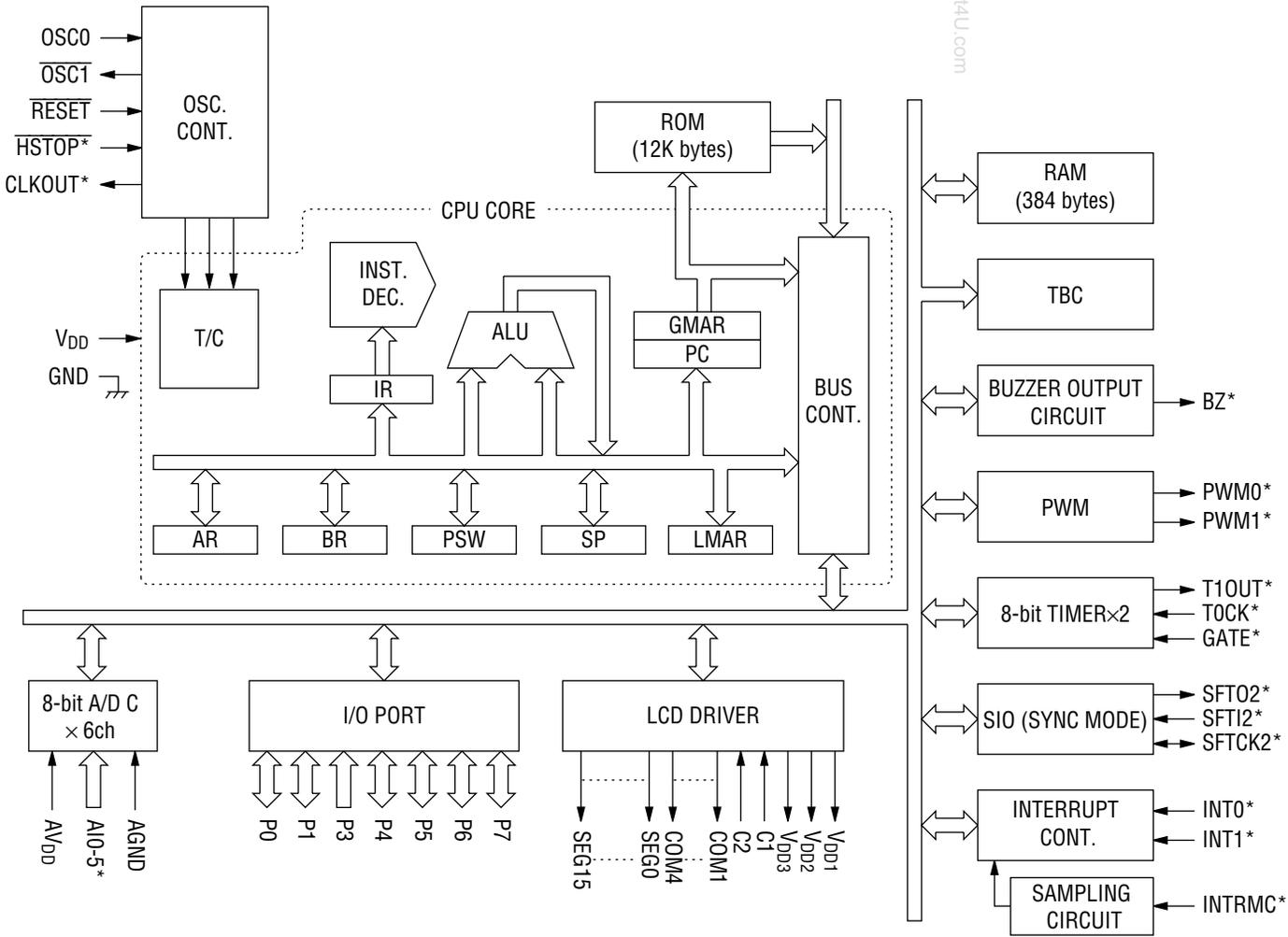
The MSM65344A is a high performance 8-bit microcontroller that employs OKI original CPU core nX-8/50. The MSM65344A includes 12K-byte program memory, 384-byte data memory, LCD driver, timer, PWM, serial I/O, and 8-bit A/D converter. Also available is the MSM65P344, which replace the on-chip program memory with one-time PROM.

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#### FEATURES

- Operating range
  - Operating voltage : 2.7V to 5.5V
  - Operating temperature : -20°C to +70°C
  - Operating frequency : 0 to 10MHz (@V<sub>DD</sub>=5V±10%)  
0 to 5MHz (@V<sub>DD</sub>=2.7V to 5.5V)
  - Current consumption (TYP.) : 5mA (@5MHz, V<sub>DD</sub>=3V)  
20mA (@10MHz, V<sub>DD</sub>=5V)  
1.5mA (@5MHz, V<sub>DD</sub>=3V, HALT MODE)  
4μA (V<sub>DD</sub>=3V, STOP MODE)
- Minimum instruction execution time : 400ns (@10MHz), 800ns (5MHz)
- CPU core : 8-bit CPU core nX-8/50
- General memory space : Internal 12K-byte program memory
- Local memory space : Internal 384-byte data memory + SFR
- LCD driver : 16 × 4 (selectable duty cycle from 1/4, 1/3 or 1/2 with software)
- I/O port : 7 ports, 48 bits
  - Input-output port : 3 ports × 8 bits, 1 port × 7 bits, 1 port × 6 bits, 1 port × 3 bits
  - Input port : 1 port × 6 bits, 1 port × 1 bit
  - Output-port : 1 port × 1 bit
- Timer : 8-bit auto-reload timer × 2
- Counter : Time base counter × 1 (14 bits)
- Serial I/O : 1ch, clock sync × 1
- PWM : 2ch, 8-bit duty, cycle from 1Hz to 80kHz (@10MHz)
- Buzzer output circuit : 1 circuit, selectable from 1kHz to 16kHz
- A/D converter : 8-bit × 6-ch
- External interrupt : 2 lines, selectable from rising edge/falling edge/both edges
- External interrupt for remote control : With sampling circuit for noise prevention
- Interrupt source : 11 sources
- Package:
  - 80-pin plastic QFP (QFP80-P-1420-0.80-BK) (Product name: MSM65344A-xxxGS-BK)  
xxx indicates the code number.
- Others : CPU clock can be an OSC or half-OSC clock.  
Time base counter can be selected with 1/4n of a CPU clock (n=1 to 8).

**BLOCK DIAGRAM**



\* Secondary function of each port



## PIN DESCRIPTION

## Basic Function

Function	Pin	Symbol	Type	Description
Power Supply	52	$V_{DD}$	—	Digital supply voltage (5V)
	63	GND	—	Digital ground (0V)
	25	$AV_{DD}$	—	Analog supply voltage (5V)
	18	AGND	—	Analog ground (0V)
	73	$V_{DD1}$	—	Bias output for LCD driver
	74	$V_{DD2}$	—	Bias output for LCD driver
	75	$V_{DD3}$	—	Bias output for LCD driver
	76	C1	—	Pins for connecting capacitors that generate bias for the LCD driver.
	77	C2	—	
Oscillation	62	OSC0	Input	Oscillation input pin on the OSC side: Connect to a quartz oscillator (ceramic resonator), or input external clock.
	61	$\overline{OSC1}$	Output	Oscillation output pin on the OSC side: Connect to a quartz oscillator (ceramic resonator). When external clock is input to the OSC0 pin, the $\overline{OSC1}$ pin should be kept open.
Control	64	$\overline{RESET}$	Input	System reset input: When this pin is set to the "L" level, the internal status is initialized to start execution of instructions from address 0040H. The input is pulled up to $V_{DD}$ with an internal pull-up resistor.

**Basic Function (Continued)**

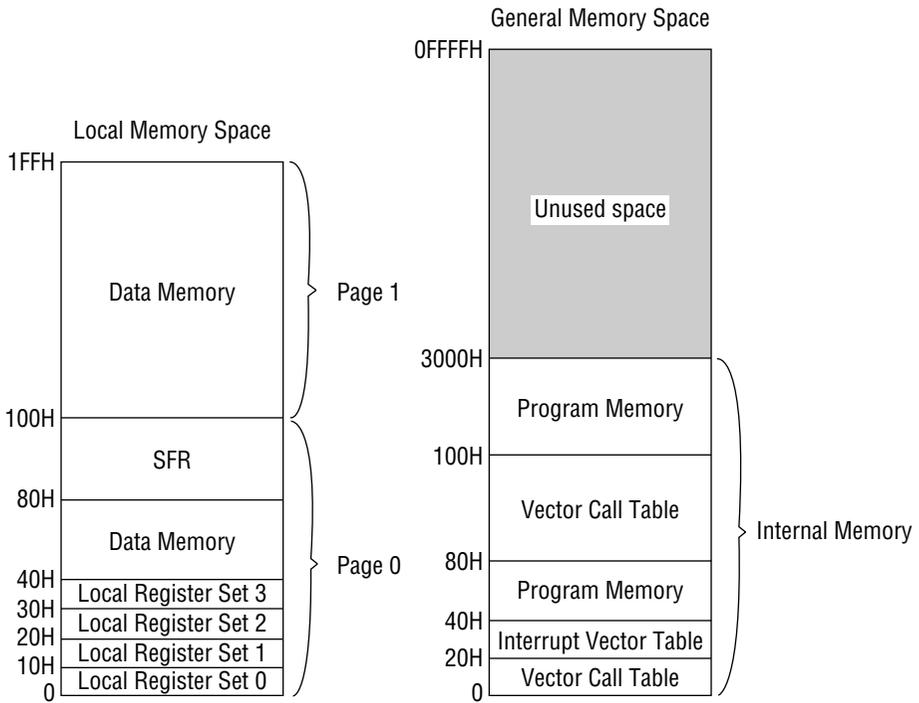
Function	Pin	Symbol	Type	Description
Port	60 to 53	P0.0 to P0.7	I/O	8-bit input-output port (port 0): Each of bits 0 to 7 can be configured to be an input or an output by the direction register of port 0 (PODIR). In addition to the basic function as an input-output port, a secondary function is allocated to each of P0.0 through P0.7. Refer to the next table.
	51 to 49	P1.2 to P1.4	I/O	3-bit input-output port (port 1): Each of bits 1.2 to 1.4 is configured to be input or output by the direction register of port 1 (P1DIR). In addition to the basic function as an input-output port, a secondary function is allocated to each of P1.2 through P1.4. Refer to "PIN DESCRIPTION (Secondary Function)".
	19 to 24	P3.0 to P3.5	I	6-bit input port (port 3): Each of P3.0 to P3.5 functions as analog input channel of A/D converter.
	40 to 33	P4.0 to P4.7	I/O	8-bit input-output port (port 4): 8-bit input-output port.
	32 to 26	P5.0 to P5.6	I/O	7-bit input-output port (port 5): Each of bits 5.0 to 5.6 can be configured to be an input or an output by the direction register of port 5 (P5DI).
	65	P6.0 (IN)	I	1-bit input port (port 6.0): 1-bit input port.
	66	P6.1 (OUT)	O	1-bit output port (port 6.1): Pulled high when reset is done. If this pin is set to the "0" level during reset, this IC goes into a test mode, disabling execution of the user program.
	67 to 72	P6.2 to P6.7	I/O	6-bit input-output port (port 6): 6-bit input-output port.
	41 to 48	P7.0 to P7.7	I/O	8-bit input-output port (port 7): Each of bits 7.0 to 7.7 can be configured to be an input or an output by the direction register of port 7 (P7DIR). In addition to the basic function as the input-output port, a secondary function is allocated to each of P7.4 through P7.7. Refer to the next table.
LCD Driver	78 to 1	COM1 to COM4	O	LCD common signal output pins
	2 to 17	SEG0 to SEG15	O	LCD segment signal output pins

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## Secondary Functions

Function	Pin	Symbol	Type	Description
External Interrupt	60	INT0	I	Secondary function of P0.0: Input pin for external interrupt 0. This pin can receive an input at rising edge, falling edge, or both the rising/falling edges.
	56	INT1/GATE	I	Secondary function of P0.4: Input pin for external interrupt 1. This pin can receive input at an rising edge, falling edge, or both the rising/falling edges. Also used as a gate signal input pin to enable or disable the count of timer 0.
Timer 0	70	T0CK	I	Secondary function of P0.3: External clock input pin for timer 0.
Timer 1	71	T1OUT	O	Secondary function of P0.2: Output pin that provides waveform with twice the cycle of the overflow of timer 1.
A/D Converter	19 to 24	A0 to A5	I	Secondary function of P3.0 to 3.5: These are used for analog channels during A/D conversion.
PWM	61	PWM0	O	Secondary function of P1.3: Output pin of PWM channel 0.
	62	PWM1	O	Secondary function of P1.2: Output pin of PWM channel 1.
Clock Output	55	CLKOUT	O	Secondary function of P0.5: Output pin that provides clocks equal to OSCCLK divided by 2 or 4.
Buzzer Output	53	BZ	O	Secondary function of P0.7: Output pin for buzzer.
Remote Control Input	49	INTRMC	I	Secondary function of P1.4: Input pin for remote control.
Shift Register	48	SFTO2	O	Secondary function of P7.7: Data output pin for shift register 2.
	47	SFTI2	I	Secondary function of P7.6: Data input pin for shift register 2.
	46	SFTCK2	I/O	Secondary function of P7.5: Sync clock input-output pin for shift register 2. This provides a clock output when used as the master, while it functions as a clock input when used as a slave.
Control	59	$\overline{\text{HSTOP}}$	I	Secondary function of P0.1

MEMORY MAPS



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**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	$V_{DD}$	$T_a = 25^\circ\text{C}$	-0.3 to +7.0	V
Input Voltage	$V_I$		-0.3 to $V_{DD}+0.3$	
Output Voltage	$V_O$		-0.3 to $V_{DD}+0.3$	
Power Dissipation	$P_D$	$T_a = 25^\circ\text{C}$ , per package	400	mW
		$T_a = 25^\circ\text{C}$ , per output	50	
Storage Temperature	$T_{STG}$	—	-55 to +150	$^\circ\text{C}$

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	$V_{DD}$	—	2.7 to 5.5	V
Memory Hold Voltage	$V_{DDMH}$	$f_{OSC} = 0\text{Hz}$	2.0 to 5.5	
Oscillation Frequency *1	$f_{OSC}$	—	1 to 10	MHz
External Clock Operating Frequency	$f_{EXTCLK}$	—	0 to 10	MHz
Operating Temperature	$T_{op}$	—	-20 to +70	$^\circ\text{C}$

\*1 Determined by the crystal or ceramic resonator to be used.

## ELECTRICAL CHARACTERISTICS

DC Characteristics 1 ( $V_{DD}=4.5$  to  $5.5V$ )(GND = 0V,  $T_a = -20$  to  $+70^\circ C$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 *1	$V_{IH1}$	CPUCLK=1MHz	2.4	—	—	V
"H" Input Voltage 2 *2	$V_{IH2}$	CPUCLK=1MHz	$0.75V_{DD}$	—	—	
"L" Input Voltage	$V_{IL}$	CPUCLK=1MHz	—	—	0.8	
"H" Output Voltage 1 *3	$V_{OH1}$	$I_{OH} = -200\mu A$	$0.75V_{DD}$	—	—	
"H" Output Voltage 2 *4	$V_{OH2}$	$I_{OH} = -400\mu A$	$0.75V_{DD}$	—	—	
"L" Output Voltage 1 *3	$V_{OL1}$	$I_{OL} = 1.6mA$	—	—	0.4	
"L" Output Voltage 2 *4	$V_{OL2}$	$I_{OL} = 3.2mA$	—	—	0.4	
Bias Output Voltage for LCD driver	$V_{DD1}$	$V_{DD} = 5V$ $C_1, C_2, C_3 = 0.1\mu F$ $VSEL = 0$ (5V mode)	1.2	1.4	—	
	$V_{DD2}$		2.6	2.8	—	
	$V_{DD3}$		4.0	4.2	—	
Segment and Common Driver Output Voltage	$V_0$	$I = +10\mu A$	—	—	0.4	
	$V_1$	$V_{DD1} = 1.4V, I = \pm 10\mu A$	$V_{DD1}-0.4$	—	$V_{DD1}+0.4$	
	$V_2$	$V_{DD2} = 2.8V, I = \pm 10\mu A$	$V_{DD2}-0.4$	—	$V_{DD2}+0.4$	
	$V_3$	$V_{DD3} = 4.2V, I = -10\mu A$	$V_{DD3}-0.4$	—	—	
Input Leakage Current *5	$I_{LI2}$	$V_I = V_{DD}/OV$	—	—	$\pm 10$	$\mu A$
"L" Input Current *6	$I_{IL}$	$V_I = 0V, V_{DD} = 5V$	-40	-200	-400	
Input Capacitance	$C_1$	$f = 1MHz, T_a = 25^\circ C$	—	5	—	pF
Operating Current Consumption $V_{DD} = 5V$ $OSC = 10MHz$	$I_{DD1}$	Stop mode, LCD stop, No load *7	—	7	14	$\mu A$
	$I_{DD4}$	CPUCLK = 10MHz, HALT mode	—	8	16	mA
	$I_{DD5}$	CPUCLK = 10MHz, no load	—	20	50	mA

\*1 Excluding OSC0 and  $\overline{RESET}$ \*2 Only for OSC0 and  $\overline{RESET}$ 

\*3 Excluding P4

\*4 Only for P4

\*5 Excluding  $\overline{RESET}$ \*6 Only for  $\overline{RESET}$ 

\*7 Including Hardware Stop Mode

DC Characteristics 2 (2.7V ≤ V<sub>DD</sub> < 4.5V)

(GND = 0V, Ta = -20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 <sup>*1</sup>	V <sub>IH1</sub>	CPUCLK=1MHz	0.3V <sub>DD</sub> +0.9	—	—	V
"H" Input Voltage 2 <sup>*2</sup>	V <sub>IH2</sub>	CPUCLK=1MHz	0.6V <sub>DD</sub> +0.6 <sup>*8</sup>	—	—	
"L" Input Voltage	V <sub>IL</sub>	CPUCLK=1MHz	—	—	0.25V <sub>DD</sub> -0.1 <sup>*9</sup>	
"H" Output Voltage 1 <sup>*3</sup>	V <sub>OH1</sub>	I <sub>OH</sub> = -10μA	0.75V <sub>DD</sub>	—	—	
"H" Output Voltage 2 <sup>*4</sup>	V <sub>OH2</sub>	I <sub>OH</sub> = -20μA	0.75V <sub>DD</sub>	—	—	
"L" Output Voltage 1 <sup>*3</sup>	V <sub>OL1</sub>	I <sub>OL</sub> = 10μA	—	—	0.1	
"L" Output Voltage 2 <sup>*4</sup>	V <sub>OL2</sub>	I <sub>OL</sub> = 20μA	—	—	0.1	
Bias Output Voltage for LCD driver	V <sub>DD1</sub>	V <sub>DD</sub> = 3V C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> = 0.1μF VSEL = 1 (3V mode)	1.2	1.4	—	
	V <sub>DD2</sub>		2.6	2.8	—	
	V <sub>DD3</sub>		4.0	4.2	—	
Segment and Common Driver Output Voltage	V <sub>0</sub>	I = +10μA	—	—	0.4	
	V <sub>1</sub>	V <sub>DD1</sub> = 1.4V, I = ±10μA	V <sub>DD1</sub> -0.4	—	V <sub>DD1</sub> +0.4	
	V <sub>2</sub>	V <sub>DD2</sub> = 2.8V, I = ±10μA	V <sub>DD2</sub> -0.4	—	V <sub>DD2</sub> +0.4	
	V <sub>3</sub>	V <sub>DD3</sub> = 4.2V, I = -10μA	V <sub>DD3</sub> -0.4	—	—	
Input Leakage Current <sup>*5</sup>	I <sub>LI2</sub>	V <sub>I</sub> = V <sub>DD</sub> /0V	—	—	±10	μA
"L" Input Current <sup>*6</sup>	I <sub>IL</sub>	V <sub>I</sub> = 0V, V <sub>DD</sub> = 3V	-40	-125	-250	
Input Capacitance	C <sub>I</sub>	f = 1MHz, Ta = 25°C	—	5	—	pF
Operating Current Consumption V <sub>DD</sub> = 3V OSC = 5MHz	I <sub>DD1</sub>	Stop mode, LCD stop, No load <sup>*7</sup>	—	4	8	μA
	I <sub>DD4</sub>	CPUCLK = 5MHz, HALT mode	—	1.5	3	mA
	I <sub>DD5</sub>	CPUCLK = 5MHz, no load	—	5	10	mA

- \*1 Excluding OSC0 and  $\overline{\text{RESET}}$
- \*2 Only for OSC0 and  $\overline{\text{RESET}}$
- \*3 Excluding P4
- \*4 Only for P4
- \*5 Excluding  $\overline{\text{RESET}}$
- \*6 Only for  $\overline{\text{RESET}}$
- \*7 Including Hardware Stop Mode
- \*8 More than 3.375V
- \*9 Less than 0.8V

**AC Characteristics**

• **CPU control**

(V<sub>DD</sub> = 2.7 to 5.5V, GND = 0V, Ta = -20 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
RESET Pulse Width	t <sub>RESW</sub>	—	20	—	ns

• **Peripheral control 1**

(V<sub>DD</sub> = 2.7 to 5.5V, GND = 0V, Ta = -20 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
OSC	Clock Cycle	V <sub>DD</sub> = 4.5 to 5.5V	100	—	ns
		2.7V ≤ V <sub>DD</sub> < 4.5V	200	—	
	Clock "L" Pulse Width	t <sub>CLW</sub>	—	0.45t <sub>C</sub>	
EXI	External Interrupt Pulse Width	t <sub>EXIW</sub>	4CPUCLK *1	—	
T0	External Clock Pulse Width	t <sub>TOCW</sub>	4CPUCLK *1	—	
	GATE Pulse Width	t <sub>TOGW</sub>	1 t <sub>TOCLK</sub> *2	—	

\*1 CPUCLK : Supply clock to the CPU selected by SBYCON.

\*2 t<sub>TOCLK</sub> : Cycle time of timer 0 count clock selected by T0CON.

• **Peripheral control 2**

(V<sub>DD</sub> = 2.7 to 5.5V, GND = 0V, Ta = -20 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit	
OSC	Clock Cycle	V <sub>DD</sub> = 4.5 to 5.5V	100	—	ns	
		2.7V ≤ V <sub>DD</sub> < 4.5V	200	—		
SFT2	SFTCK Cycle	t <sub>SFC2</sub>	8CPUCLK *	—		
	SFTCK "L" Pulse Width	t <sub>SFCLW2</sub>	4CPUCLK -20 *	—		
	SFTCK "H" Pulse Width	t <sub>SFCHW2</sub>	4CPUCLK -20 *	—		
	SFTO Setting Time	t <sub>SFOS2</sub>	C <sub>L</sub> = 100 pF	t <sub>SFCLW2</sub> -100		—
	SFTO Hold Time	t <sub>SFOH2</sub>	t <sub>SFCHW2</sub> -100	—		
	SFTI Setting Time	t <sub>SFIS2</sub>	100	—		
	SFTI Hold Time	t <sub>SFIH2</sub>	100	—		

\* CPUCLK : Supply clock to the CPU selected by SBYCON.

## A/D Converter Characteristics 1

(V<sub>DD</sub> = AV<sub>DD</sub> = 4.5 to 5.5V, GND = AGND = 0V, T<sub>a</sub> = -20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to recommended circuit. Analog input source impedance R <sub>I</sub> ≤ 5kΩ	—	8	—	bit
Linearity Error	E <sub>L</sub>		—	—	+1.5 -1.5	LSB
Differential Linearity Error	E <sub>D</sub>		—	—	±0.5	LSB
Zero Scale Error	E <sub>ZS</sub>		—	—	+1.5	LSB
Full Scale Error	E <sub>FS</sub>		—	—	-1.5	LSB
Crosstalk	E <sub>CT</sub>	Refer to measuring circuit.	—	—	±0.5	LSB
Conversion Time*	t <sub>CONV</sub>	f <sub>OSC</sub> = 10MHz	—	16	—	μs/CH

\* The conversion time immediately after GO bit is set to "1" is 14.8μs/CH.

## A/D Converter Characteristics 2

(V<sub>DD</sub> = AV<sub>DD</sub>, 2.7V ≤ V<sub>DD</sub> < 4.5V, GND = AGND = 0V, T<sub>a</sub> = -20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to recommended circuit. Analog input source impedance R <sub>I</sub> ≤ 5kΩ	—	8	—	bit
Linearity Error	E <sub>L</sub>		—	—	+2 -2	LSB
Differential Linearity Error	E <sub>D</sub>		—	—	±1	LSB
Zero Scale Error	E <sub>ZS</sub>		—	—	+2	LSB
Full Scale Error	E <sub>FS</sub>		—	—	-2	LSB
Crosstalk	E <sub>CT</sub>	Refer to measuring circuit.	—	—	±1	LSB
Conversion Time*	t <sub>CONV</sub>	f <sub>OSC</sub> = 5MHz	—	32	—	μs/CH

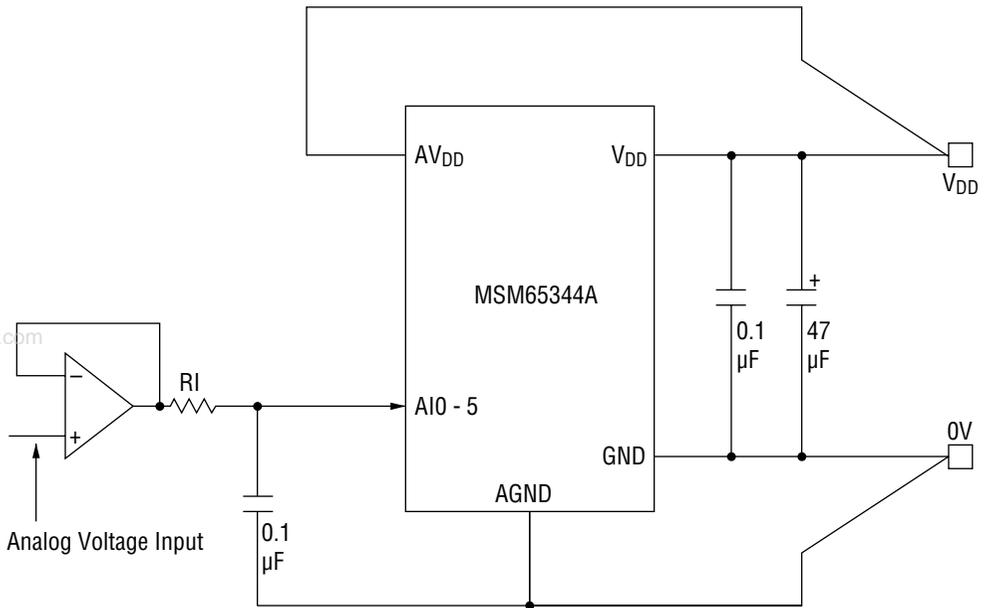
\* The conversion time immediately after GO bit is set to "1" is 29.6μs/CH.

**Definition of Terms**

Resolution	Recognizable minimum input analog value. This can be resolved into $2^8 = 256$ , that is $AV_{DD} \div 256$ in 8 bits.
Linearity Error	Deviation between ideal conversion characteristics as an 8-bit A/D converter and actual conversion characteristics. (Not including quantization error.) Ideal conversion characteristics means a step which divides voltage between $V_{RH}$ and $L_{RL}$ into 256.
Differential Linearity Error	Smoothness of conversion characteristics. $1\text{LSB} = AV_{DD} \div 256$ is ideal for analog input voltage width corresponding to change per 1 bit of digital output. Deviation between the ideal bit size and bit size at arbitrary point in conversion range.
Zero Scale Error	Deviation between ideal conversion characteristics of transfer point for digital outputs "000H" to "001H" and actual conversion characteristics.
Full Scale Error	Deviation between ideal conversion characteristics of transfer point for digital outputs "0FEH" to "0FFH" and actual conversion characteristics.

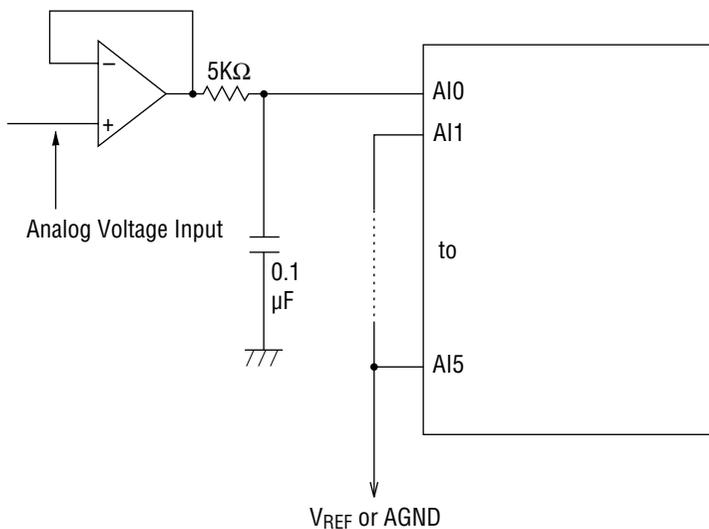
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**Recommended Circuit**



$R_I$  (Analog Input Source Impedance)  $\leq 5k\Omega$

**Crosstalk Measuring Circuit**

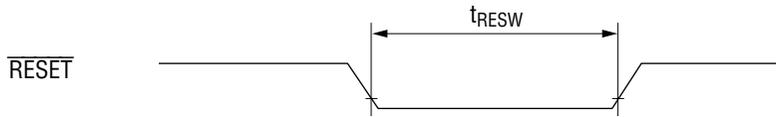


Crosstalk is defined as the difference of A/D conversion result between supplying the same voltage to AI0 to AI5 and supplying voltage shown in this left diagram.

**Timing Diagram**

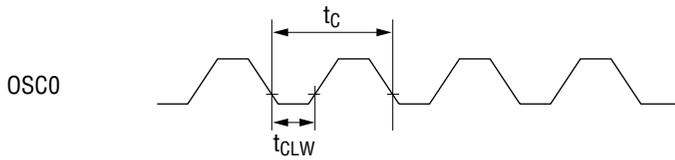
**CPU control**

1)  $\overline{\text{RESET}}$  Pulse width

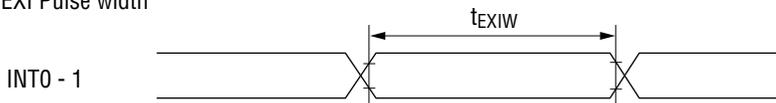


**Peripheral control 1**

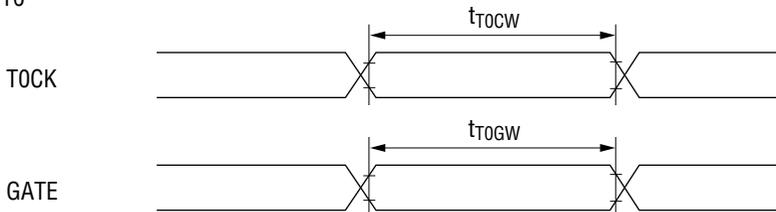
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1) EXI Pulse width

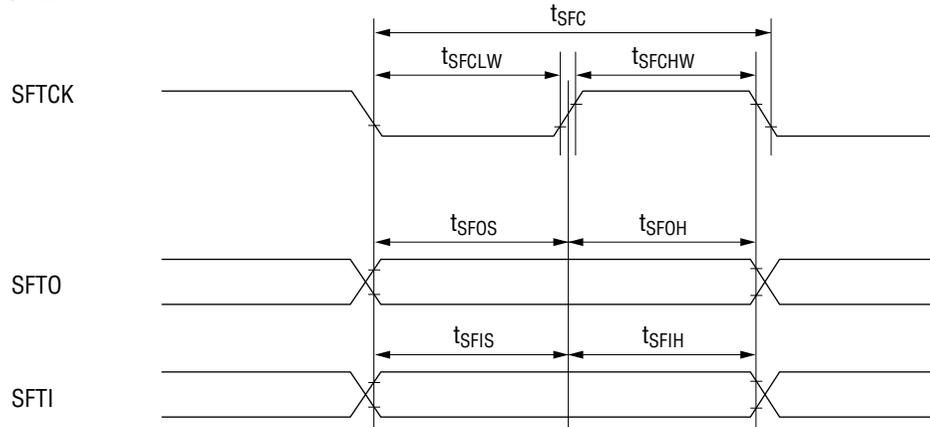


2) T0



**Peripheral control 2**

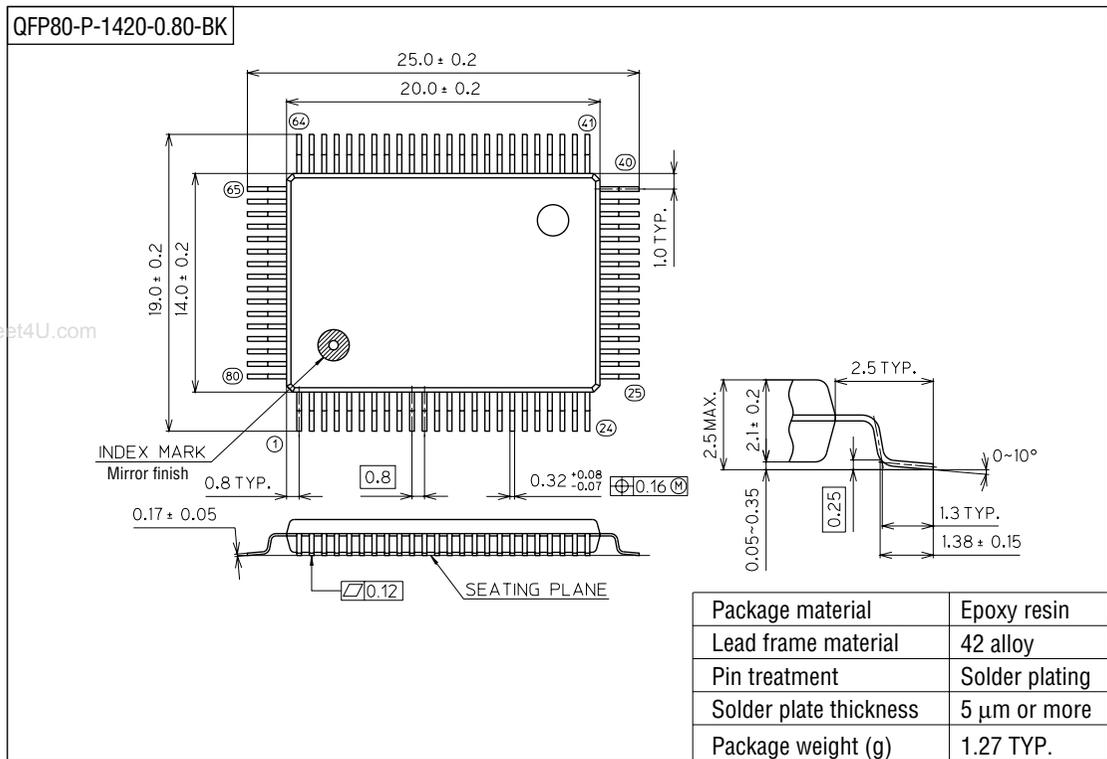
1) SFT2



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PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).