OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM65352/65352B

8-Bit Microcontroller with 4-Bit A/D Converter (with LCD Driver)

GENERAL DESCRIPTION

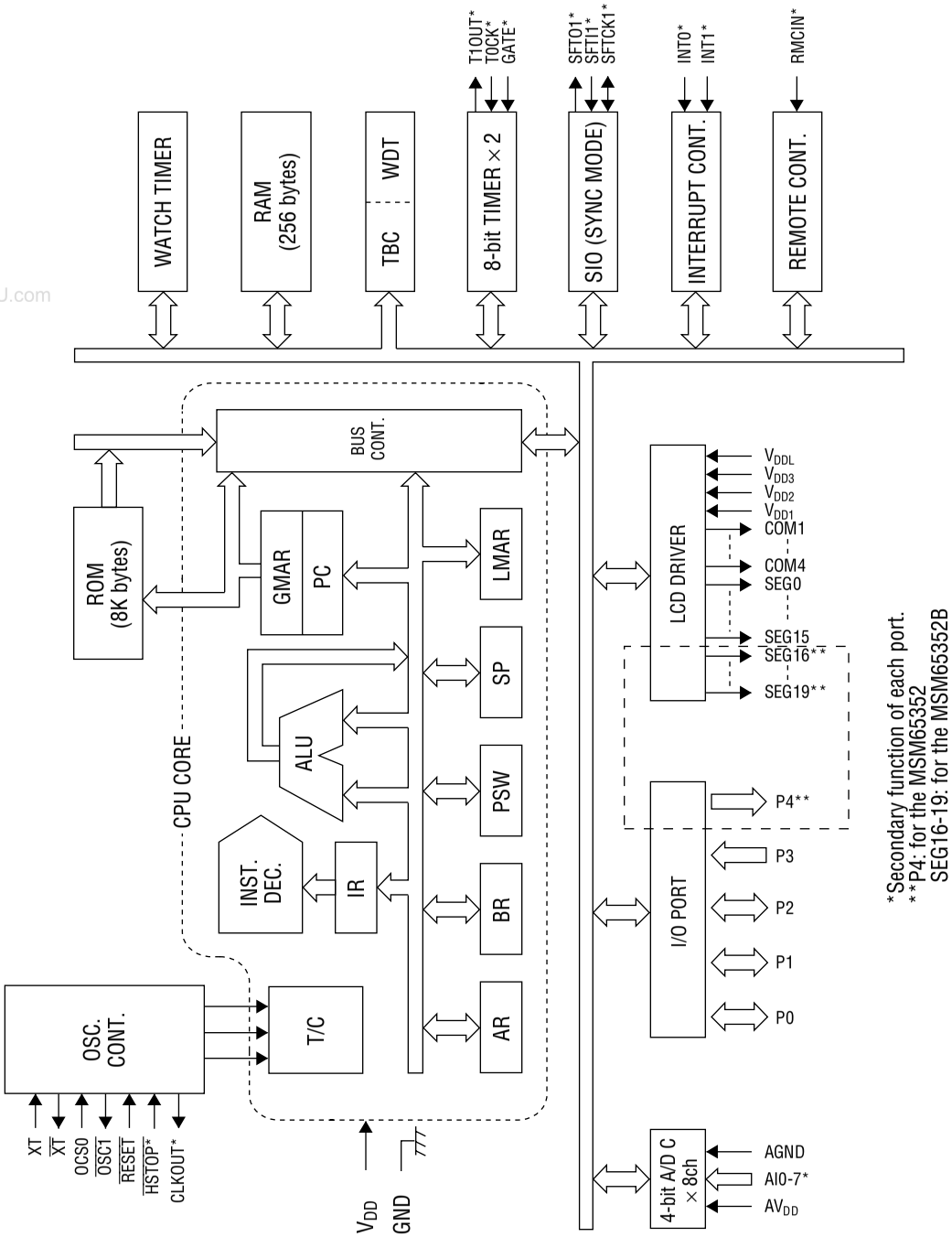
The MSM65352 is a high performance 8-bit microcontroller that employs OKI original CPU core, the nX-8/50. The MSM65352 includes 8K-byte program memory, 256-byte data memory, LCD driver, timer, serial I/O and 4-bit A/D converter. Also available is the MSM65352B, which has four LCD outputs in place of four output ports. Also available are the MSM65P352 and MSM65P352B, which replace the on-chip program memory with one-time PROM.

FEATURES

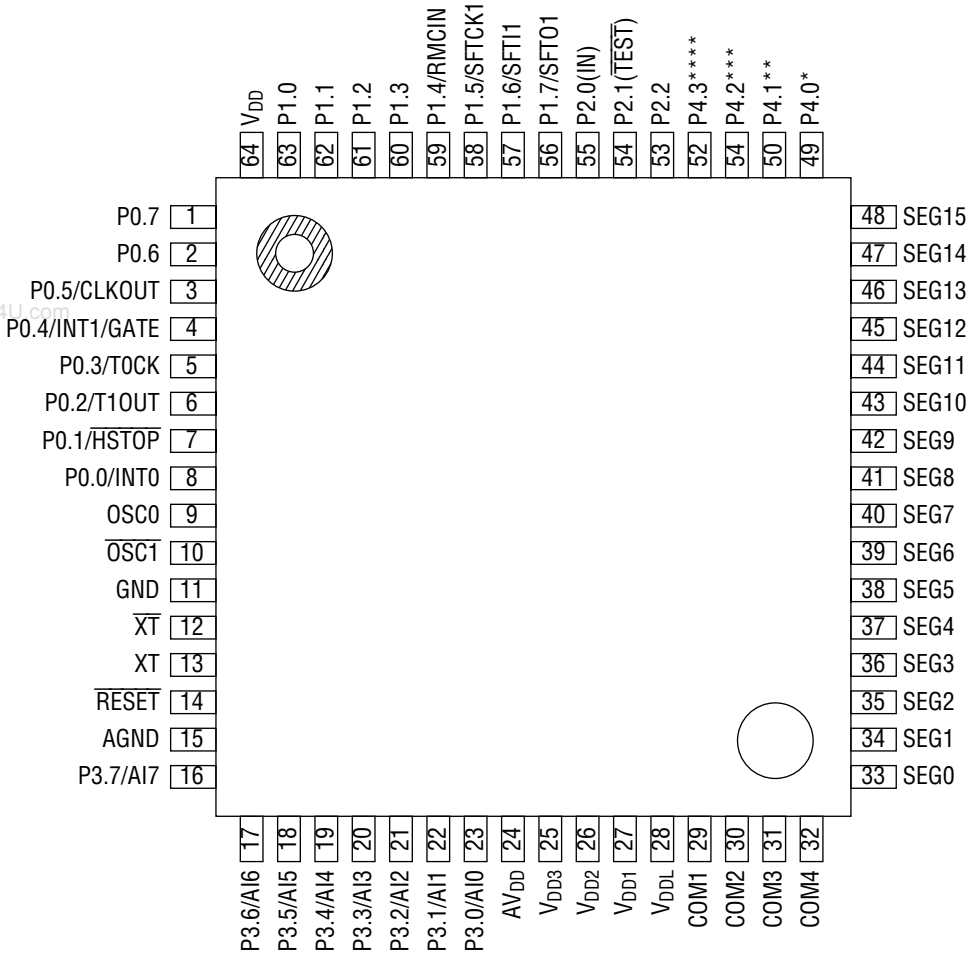
- Operating range
  - Operating voltage : 2.7V to 5.5V
  - Operating temperature : –20°C to +70°C
  - Operating frequency: High speed side : 0 to 10MHz (@V_{DD}=5V±10%)
  - (dual clock) : 0 to 5MHz (@V_{DD}=2.7V to 5.5V)
  - Low speed side : 32.768kHz (@V_{DD}=2.7V to 5.5V)
- Current consumption (Typ.): High speed side : 5mA (@5MHz, V_{DD}=3V)
  - 20mA (@10MHz, V_{DD}=5V)
  - 1.5mA (@5MHz, V_{DD}=3V, halt mode)
  - Low speed side : 45µA (@32.768kHz, V_{DD}=3V)
  - 4µA (@V_{DD}=3V, stop mode)
- Minimum instruction execution time : 400ns (@10MHz), 800ns (@5MHz)
- CPU core : 8-bit CPU core nX-8/50
- General memory space : 8K-byte program memory
- Local memory space : 256-byte data memory + SFR
- LCD driver : 16 × 4 (MSM65352), 20 × 4 (MSM65352B)
- I/O port : 5 ports, 31 bits (MSM65352)
  - 4 ports, 27 bits (MSM65352B)
  - Input-output port : 2 ports × 8 bits, 1 port × 1 bit
  - Input port : 1 port × 1 bit
  - 1 port × 4 bits (Only for MSM65352)
  - Output port : 1 port × 8 bits, 1 port × 1 bit
- Timer : 8-bit auto-reload timer × 2
  - Watchdog timer × 1
  - Watch timer
  - (counter clock is fixed at XT=32.768kHz)
- Counter : Time base counter × 1 (14 bits)
- Serial I/O : 1ch, clock sync × 1
- A/D converter : 4-bit × 8-ch, with reference current cutoff function
- Remote control input circuit : Receives signal in 32kHz/5MHz/10MHz operations
- Interrupt source : 9 sources
- Package:
  - 64-pin plastic QFP (QFP64-P-1414-0.80-BK)(Product name: MSM65352-×××GS-BK,
  - MSM65352B-×××GS-BK)
  - ××× indicates the Date Number.

- Others : CPU clock can be an OSC, half-OSC, or XT clock. Time base counter can be selected with 1/4n of a CPU clock (n=1 to 8).

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



* SEG16 for MSM65352B
** SEG17 for MSM65352B
*** SEG18 for MSM65352B
**** SEG19 for MSM65352B

64-Pin Plastic QFP

PIN DESCRIPTION

Basic Function

Function	Pin	Symbol	Type	Description
Power Supply	64	V_{DD}	—	Digital supply voltage (5V)
	11	GND	—	Digital ground
	24	AV_{DD}	—	Analog supply voltage (5V)
	15	AGND	—	Analog ground
	27	V_{DD1}	—	Bias input for LCD driver
	26	V_{DD2}	—	Bias input for LCD driver
	25	V_{DD3}	—	Bias input for LCD driver
	28	V_{DDL}	—	Ground for LCD driver bias
Oscillation	9	OSC0	I	Oscillation input pin on the OSC side: Connect to a quartz oscillator (ceramic resonator), or input external clock.
	10	$\overline{OSC1}$	O	Oscillation output pin on the OSC side: Connect to a quartz oscillator (ceramic resonator). When external clock is input to the OSC0 pin, the $\overline{OSC1}$ pin should be kept open.
	13	XT	I	Oscillation input pin on the XT side: Connect to a quartz oscillator of 32.768kHz.
	12	$\overline{XT}$	O	Oscillation output pin on the XT side: Connect to a quartz oscillator of 32.768kHz.
Control	14	$\overline{RESET}$	I	System reset input: When this pin is set to the "L" level, the internal status is initialized to start execution of instructions from address 0040H. The input is pulled up to V_{DD} with an internal pull-up resistor.

Basic Function (Continued)

Function	Pin	Symbol	Type	Description
Port	8 to 1	P0.0 to P0.7	I/O	8-bit Input-output port (port 0): Each of bits 0 to 7 is configured to be an input or an output by the direction register of port 0 (P0DIR). In addition to the basic function as the Input-output port, a secondary function is allocated to each of P0.0 through P0.7. Refer to the next table.
	63 to 56	P1.0 to P1.7	I/O	8-bit Input-output port (port 1): Each of bits 0 to 7 is configured to be input or output by the direction register of port 1 (P1DIR). In addition to the basic function as the Input-output port, a secondary function is allocated to each of P1.0 through P1.7. Refer to the next table.
	55	P2.0 (IN)	I	Input port (port 2.0)
	54	P2.1 ($\overline{\text{TEST}}$)	O	Output port (port 2.1) Pulled high at the time of reset. If this pin is set to the "0" level during reset, this IC goes into a test mode, disabling execution of the user program.
	53	P2.2	I/O	Input-output port (port 2.2)
	23 to 16	P3.0 to P3.7	I	8-bit input port (port 3): Each of P3.0 to P3.7 functions as analog input channel of A/D converter.
	49 to 52	P4.0 to P4.3	O	4-bit output port: These pins are valid only for the MSM65352.
LCD Driver	29 to 32	COM1 to COM4	O	LCD common signal output pins
	33 to 48	SEG0 to SEG15	O	LCD segment signal output pins In the case of MSM65352B, SEG0 to SEG19 and Pin 33 to Pin 52 are used.

Secondary Function

Function	Pin	Symbol	Type	Description
External Interrupt	8	INT0	I	Secondary function of P0.0: Input pin for external interrupt 0. This pin can receive an input at the rising edge, falling edge, or both the rising/falling edges.
	4	INT1	I	Secondary function of P0.4: Input pin for external interrupt 1. This pin can receive input at the rising edge, falling edge or both the rising/falling edges. Also used as a gate signal input pin to enable or disable the count of timer 0.
Control	7	$\overline{\text{HSTOP}}$	I	Secondary function of P0.1: Hardware stop mode input pin. When this pin is set to the "L" level while the HSTP bit in SBYCON is set to "1", the hardware stop mode is entered. In the hardware stop mode, oscillation on the OSC side is stopped for low power consumption.
Timer 0	5	T0CK	I	Secondary function of P0.3: External clock input pin for timer 0.
Timer 1	6	T1OUT	O	Secondary function of P0.2: Output pin that provides waveform with twice the cycle of the overflow of timer 1.
A/D Converter	23 to 16	AI0 to AI7	I	Secondary function of P3.0 to 3.7: These are used for analog channels during A/D conversion.
Clock Output	3	CLKOUT	O	Secondary function of P0.5: Output pin that provides clocks equal to OSCCLK divided by 2 or 4, and also clocks equal to XTCLK divided by 2 or 4.
Remote Control Input	59	RMCIN	I	Secondary function of P1.4: Input pin for remote control.
Shift Register	56	SFTO1	O	Secondary function of P1.7: Data output pin for shift register 1.
	57	SFTI1	I	Secondary function of P1.6: Data input pin for shift register 1.
	58	SFTCK1	I/O	Secondary function of P1.5: Sync clock I/O pin for shift register 1. This provides clock output when used as the master, while it functions as clock input when used as a slave.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to 7.0	V
Input Voltage	V_I		–0.3 to V_{DD}+0.3	
Output Voltage	V_O		–0.3 to V_{DD}+0.3	
Power Dissipation	P_D	Ta = 25°C, per package	400	mW
		Ta = 25°C, per output	50	
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	—	2.7 to 5.5	V
Memory Hold Voltage	V_{DDMH}	f_{OSC} = 0Hz	2.0 to 5.5	
Oscillation Frequency*1	f_{OSC}	—	1 to 10	MHz
	f_{XT}	V_{DD} = 2.7 to 5.5	32.768	kHz
External Clock Operating Frequency*2	f_{EXTCLK}	—	0 to 10	MHz
Operating Temparature	T_{op}	—	–20 to +70	°C

*1 Determined by the crystal oscillator or ceramic resonator to be used.
*2 External clock cannot be used in the XT pin.

ELECTRICAL CHARACTERISTICS

DC Characteristics 1 (V_{DD}=4.5 to 5.5V)

(GND = 0V, Ta = –20 to +70˚C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 *1	V_{IH1}	CPUCLK=1MHz	2.4	—	—	V
"H" Input Voltage 2 *2	V_{IH2}	CPUCLK=1MHz	$0.7V_{DD}$	—	—	
"L" Input Voltage	V_{IL}	CPUCLK=1MHz	—	—	0.8	
"H" Output Voltage 1 *3	V_{OH1}	I_{OH} = –200µA	$0.75V_{DD}$	—	—	
"H" Output Voltage 2 *4	V_{OH2}	I_{OH} = –400µA	$0.75V_{DD}$	—	—	
"L" Output Voltage 1 *3	V_{OL1}	I_{OL} = 1.6mA	—	—	0.4	
"L" Output Voltage 2 *4	V_{OL2}	I_{OL} = 3.2mA	—	—	0.4	
Input Leakage Current *5	I_{LI2}	V_I = V_{DD}/0V	—	—	±10	µA
"L" Input Current *6	I_{IL}	V_I = 0V, V_{DD} = 5V	–40	–200	–400	
Input Capacitance	C_I	f = 1MHz, Ta = 25˚C	—	5	—	pF
Operating Current Consumption V_{DD} = 5V XT = 32kHz OSC = 10MHz	I_{DD1}	Stop mode *7	—	15	30	µA
	I_{DD2}	CPUCLK = 32kHz, HALT mode *8	—	30	60	µA
	I_{DD3}	CPUCLK = 32kHz, no load. *9	—	80	160	µA
	I_{DD4}	CPUCLK = 10MHz, HALT mode *7	—	8	16	mA
	I_{DD5}	CPUCLK = 10MHz, no load.	—	20	40	mA

*1 Excluding OSC0 and $\overline{RESET}$
*2 Only for OSC0 and $\overline{RESET}$
*3 Excluding P4
*4 Only for P4
*5 Excluding $\overline{RESET}$
*6 Only for $\overline{RESET}$
*7 Measured when LCD is operated
*8 Measured when OSC clock is stopped but LCD is operated without load
*9 Measured when OSC clock is stopped

DC Characteristics 2 (2.7V≤V_{DD}<4.5V)

(GND = 0V, Ta = –20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 *1	V_{IH1}	CPUCLK=1MHz	$0.3V_{DD}$ +0.9	—	—	V
"H" Input Voltage 2 *2	V_{IH2}	CPUCLK=1MHz	$0.6V_{DD}$ +0.6 *10	—	—	
"L" Input Voltage	V_{IL}	CPUCLK=1MHz	—	—	$0.3V_{DD}$ –0.1 *11	
"H" Output Voltage 1 *3	V_{OH1}	I_{OH} = –10µA	$0.75V_{DD}$	—	—	
"H" Output Voltage 2 *4	V_{OH2}	I_{OH} = –20µA	$0.75V_{DD}$	—	—	
"L" Output Voltage 1 *3	V_{OL1}	I_{OL} = 10µA	—	—	0.1	
"L" Output Voltage 2 *4	V_{OL2}	I_{OL} = 20µA	—	—	0.1	
Input Leakage Current *5	I_{LI2}	V_I = V_{DD}/0V	—	—	±10	µA
"L" Input Current *6	I_{IL}	V_I = 0V, V_{DD} = 3V	–40	–125	–250	
Input Capacity	C_I	f = 1MHz, Ta = 25°C	—	5	—	pF
Operating Current Consumption V_{DD} = 3V XT = 32KHz OSC = 5MHz	I_{DD1}	Stop mode *7	—	4	8	µA
	I_{DD2}	CPUCLK = 32kHz, HALT mode *8	—	15	30	µA
	I_{DD3}	CPUCLK = 32kHz, no load. *9	—	45	90	µA
	I_{DD4}	CPUCLK = 5MHz, HALT mode *7	—	1.5	3	mA
	I_{DD5}	CPUCLK = 5MHz, no load.	—	5	14	mA

*1 Excluding OSC0 and $\overline{RESET}$
*2 Only for OSC0 and $\overline{RESET}$
*3 Excluding P4
*4 Only for P4
*5 Excluding $\overline{RESET}$
*6 Only for $\overline{RESET}$
*7 Measured when LCD is operated
*8 Measured when OSC clock is stopped but LCD is operated without load
*9 Measured when OSC clock is stopped
*10 More than 3.375V
*11 Less than 0.8V

A/D Converter Characteristics 1

(V_{DD}=A_{VDD}=5V, GND=AGND=0V, Ta=–20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
A/D Conversion Analog Input Detecting Voltage	AINFH	(ADOUT)=F_H	4.77	5.00	—	V
	AINEH	(ADOUT)=E_H	4.45	4.53	4.61	
	AINDH	(ADOUT)=D_H	4.14	4.22	4.30	
	AINCH	(ADOUT)=C_H	3.83	3.91	3.98	
	AINBH	(ADOUT)=B_H	3.52	3.59	3.67	
	AINAH	(ADOUT)=A_H	3.20	3.28	3.36	
	AIN9H	(ADOUT)=9_H	2.89	2.97	3.05	
	AIN8H	(ADOUT)=8_H	2.58	2.66	2.73	
	AIN7H	(ADOUT)=7_H	2.27	2.34	2.42	
	AIN6H	(ADOUT)=6_H	1.95	2.03	2.11	
	AIN5H	(ADOUT)=5_H	1.64	1.72	1.80	
	AIN4H	(ADOUT)=4_H	1.33	1.41	1.48	
	AIN3H	(ADOUT)=3_H	1.02	1.09	1.17	
	AIN2H	(ADOUT)=2_H	0.70	0.78	0.86	
	AIN1H	(ADOUT)=1_H	0.39	0.47	0.55	
	AIN0H	(ADOUT)=0_H	—	0.00	0.23	
A/D Conversion Settling Time	t_{SET}	—	—	60	200	µs

A/D Converter Characteristics 2

(V_{DD}=A_{VDD}=3V, GND=AGND=0V, Ta=–20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
A/D Conversion Analog Input Detecting Voltage	AINFH	(ADOUT)=F_H	2.88	3.00	—	V
	AINEH	(ADOUT)=E_H	2.69	2.72	2.75	
	AINDH	(ADOUT)=D_H	2.50	2.53	2.56	
	AINCH	(ADOUT)=C_H	2.32	2.34	2.37	
	AINBH	(ADOUT)=B_H	2.13	2.16	2.18	
	AINAH	(ADOUT)=A_H	1.94	1.97	2.00	
	AIN9H	(ADOUT)=9_H	1.75	1.78	1.81	
	AIN8H	(ADOUT)=8_H	1.57	1.59	1.62	
	AIN7H	(ADOUT)=7_H	1.38	1.41	1.43	
	AIN6H	(ADOUT)=6_H	1.19	1.22	1.25	
	AIN5H	(ADOUT)=5_H	1.00	1.03	1.06	
	AIN4H	(ADOUT)=4_H	0.82	0.89	0.87	
	AIN3H	(ADOUT)=3_H	0.63	0.66	0.68	
	AIN2H	(ADOUT)=2_H	0.44	0.47	0.50	
	AIN1H	(ADOUT)=1_H	0.25	0.28	0.31	
	AIN0H	(ADOUT)=0_H	—	0.00	0.12	
A/D Conversion Settling Time	t_{SET}	—	—	60	200	µs

AC Characteristics

• CPU control

(V_{DD} = 2.7 to 5.5V, GND = 0V, Ta = –20 to +70˚C)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{\text{RESET}}$ Pulse Width	t_{RESW}	—	20	—	ns

• Peripheral control 1

(V_{DD} = 2.7 to 5.5V, GND = 0V, Ta = –20 to +70˚C)

Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Cycle	t_C	V_{DD} = 4.5 to 5.5V	100	—	ns
			2.7V ≤ V_{DD} < 4.5V	200	—	
	Clock "L" Pulse Width	t_{CLW}	—	0.45 t_C	0.55 t_C	
EXI	External Interrupt Pulse Width	t_{EXIW}	—	4 t_C	—	

• Peripheral control 2

(V_{DD} = 2.7 to 5.5V, GND = 0V, Ta = –20 to +70˚C)

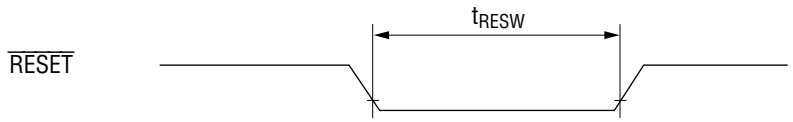
Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Cycle	t_C	V_{DD} = 4.5 to 5.5V	100	—	ns
			2.7V ≤ V_{DD} < 4.5V	200	—	
SFT1	SFTCK1 Cycle	t_{SFC}	C_L = 100 pF	8 t_C	—	
	SFTCK1 "L" Pulse Width	t_{SFCLW}		4 t_C –20	—	
	SFTCK1 "H" Pulse Width	t_{SFCHW}		4 t_C –20	—	
	SFTO1 Setup Time	t_{SFOS}		t_{SFCLW}–100	—	
	SFTO1 Hold Time	t_{SFOH}		t_{SFCHW}–100	—	
	SFTI1 Setup Time	t_{SFIS}		100	—	
	SFTI 1Hold Time	t_{SFIH}		100	—	

See Timing Diagram.

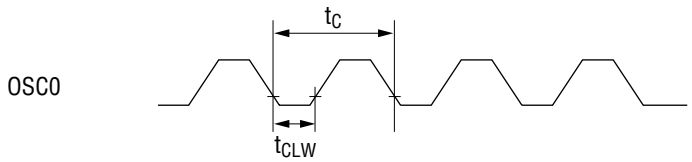
Timing Diagram

• CPU control

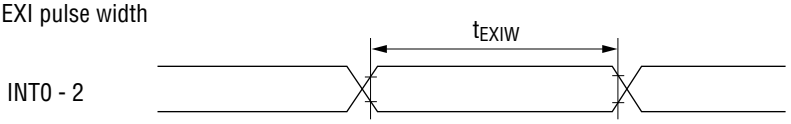
1) $\overline{\text{RESET}}$ pulse width



• Peripheral control 1

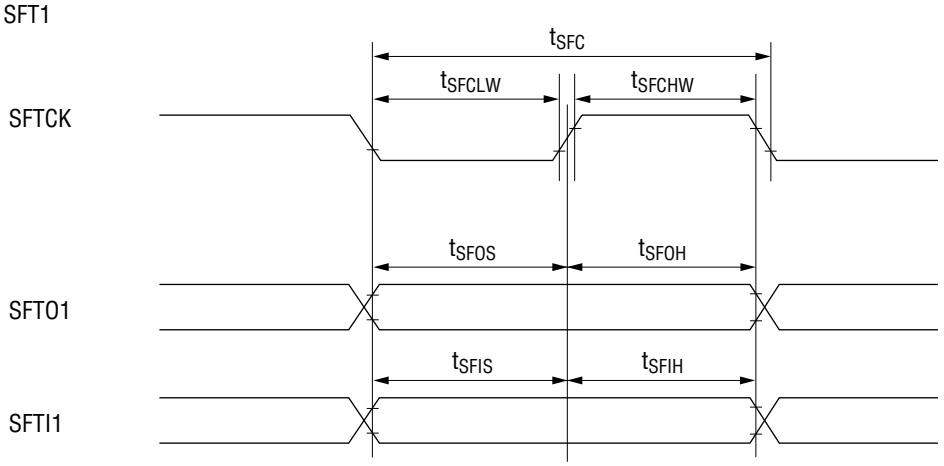


1) EXI pulse width



• Peripheral control 2

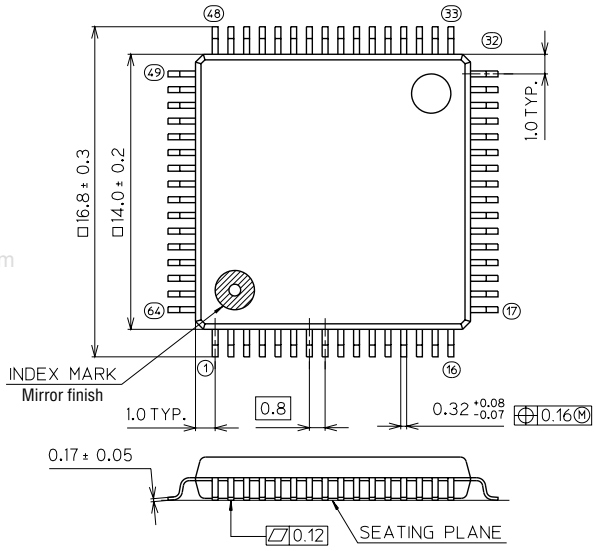
1) SFT1

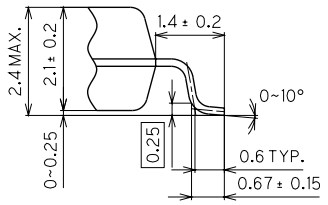


PACKAGE DIMENSIONS

(Unit : mm)

QFP64-P-1414-0.80-BK





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.87 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).