Discontinued Product

OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM65514/65P514

High Performance 8-Bit Microcontroller
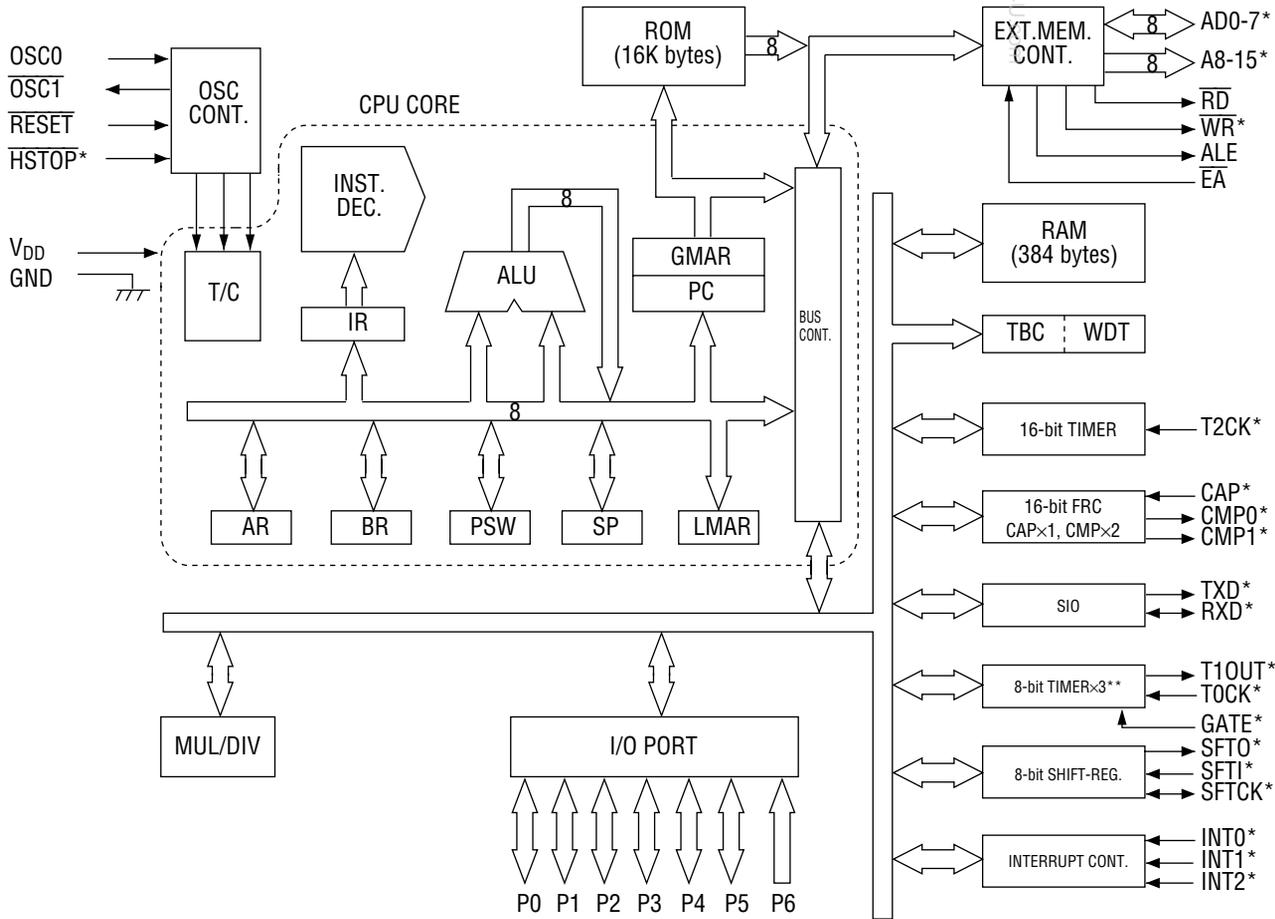
GENERAL DESCRIPTION

The MSM65514 is a high-performance 8-bit microcontroller that employs OKI original nX-8/50 CPU core. With a minimum instruction execution time of 400 ns (10MHz clock), the MSM65514 is capable of high-speed processing, and includes 16K bytes of program memory, 384 bytes of data memory, timers and serial ports on chip. Also available are the MSM65P514, which replaces the on-chip program memory with one-time PROM, and the MSM65X514, which uses external program memory.

FEATURES

- Operating range
  - Operating frequency : 0 to 10MHz (V_{DD}=4.5 to 5.5V)
    - 0 to 5MHz (V_{DD}=2.7 to 5.5V)
  - Operating voltage : 2.7 to 5.5V
  - Operating temperature : −40 to +85°C
- Memory space : 64K bytes
  - Internal program memory : 16K bytes
  - Internal data memory : 384 bytes
- Minimum instruction execution time : 400ns @ 10MHz
- Powerful instruction set : 83 basic instructions
  - 8/16-bit operation instructions
  - Bit manipulation instructions
  - Compound function instructions
- Abundant addressing modes
- Multiplication/division operation functions : $8 \times 8 \rightarrow 16$
  - $16 \div 8 \rightarrow 16 ... 8$
- I/O port
  - Input-output port : 6 ports × 8 bits
  - Input port : 1 port × 8 bits
- Timers : 8-bit auto-reload timer × 2
  - 16-bit auto-reload timer × 1
  - Watchdog timer × 1
- Counters : Time base counter × 1
  - 16-bit free-running counter × 1
- Capture input : 1 channel
- Compare output : 2 channels
- Serial ports : Shift register × 1
  - Serial port with baud rate generator (UART/synchronous) × 1
- External interrupts : 3
- Interrupt sources : 15
- Package
  - 64-pin plastic shrink DIP (SDIP64-P-750-1.78) : (MSM65514-×××SS, MSM65P514-×××SS)
  - 64-pin plastic QFP (QFP64-P-1414-0.80-BK) : (MSM65514-×××GS-BK, MSM65P514-×××GS-BK)
  - 68-pin plastic QFJ (PLCC) (QFJ68-P-S950-1.27): (MSM65514-×××JS, MSM65P514-×××JS)
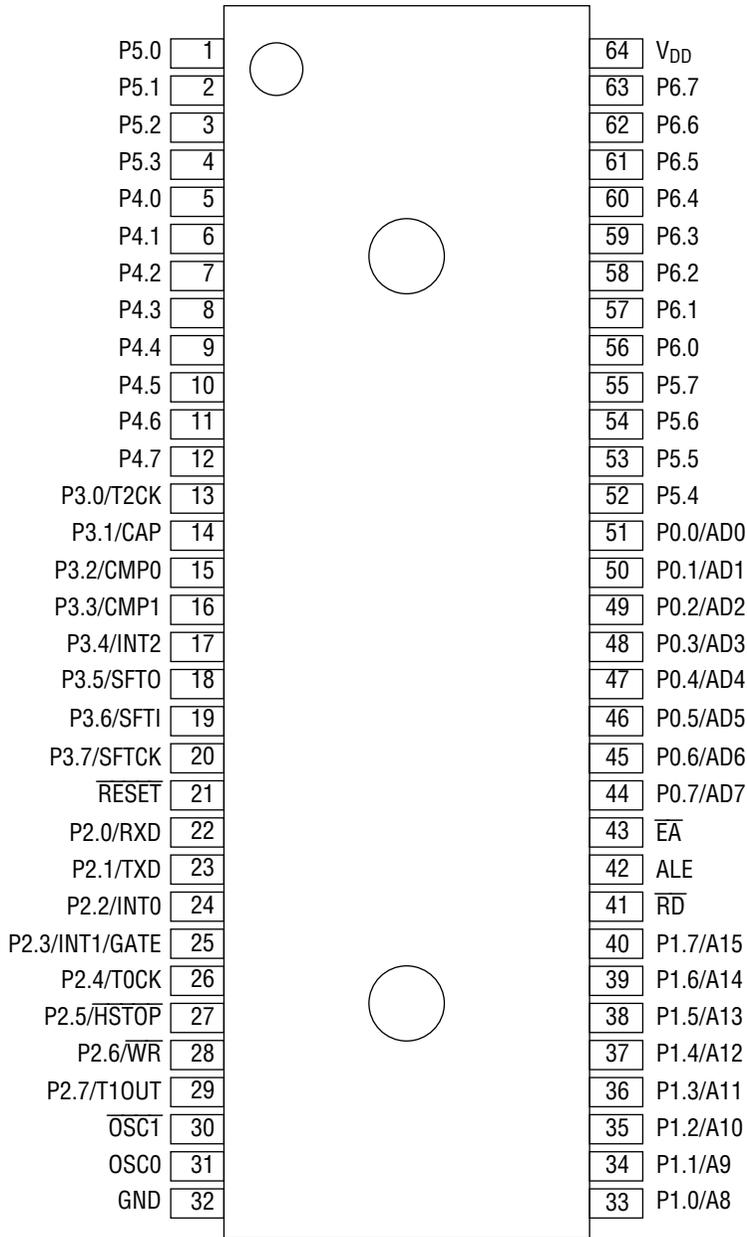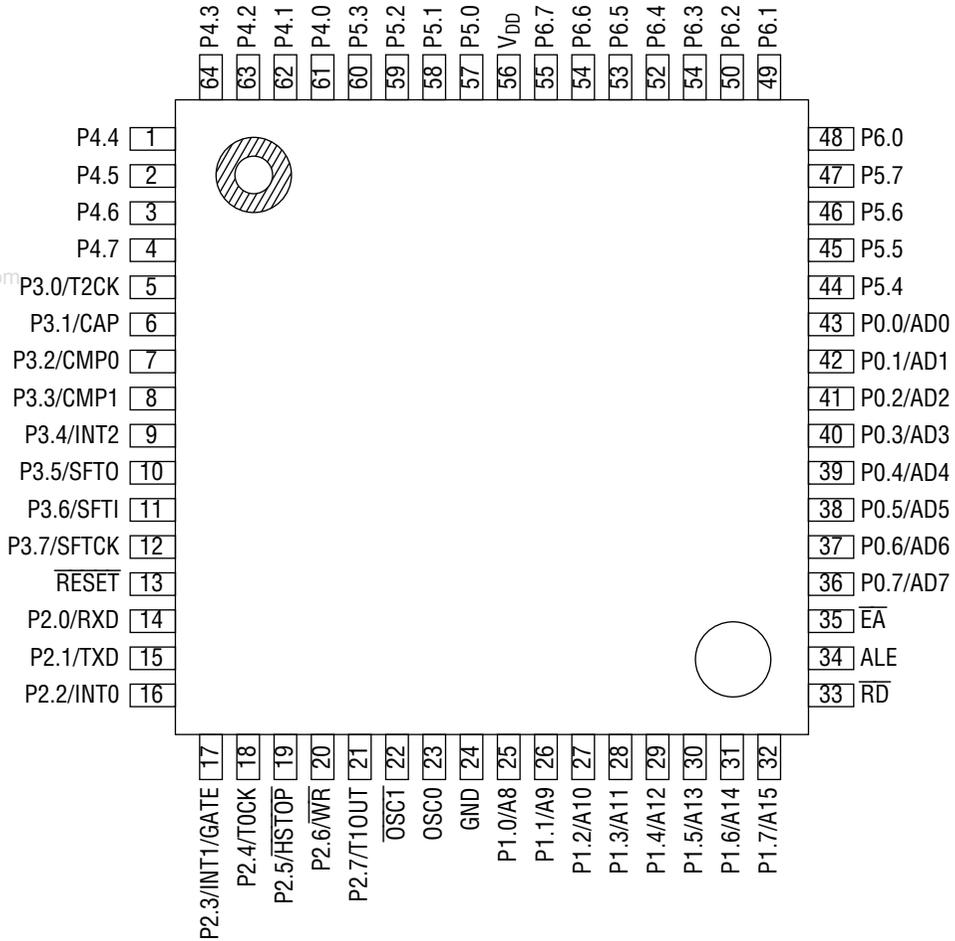   - ××× indicates the code number.

BLOCK DIAGRAM

OSC0
$\overline{OSC1}$
$\overline{RESET}$
$\overline{HSTOP}$*

OSC CONT.

V_{DD}
GND

CPU CORE

T/C

INST. DEC.

IR

ALU

8

GMAR
PC

8

AR   BR   PSW   SP   LMAR

BUS CONT.

ROM (16K bytes)

8

EXT.MEM. CONT.

8 AD0-7*
8 A8-15*
$\overline{RD}$
$\overline{WR}$*
ALE
$\overline{EA}$

RAM (384 bytes)

TBC | WDT

16-bit TIMER ← T2CK*

16-bit FRC
CAP×1, CMP×2
← CAP*
→ CMP0*
→ CMP1*

SIO
→ TXD*
← RXD*

8-bit TIMER×3**
→ T1OUT*
← T0CK*
← GATE*

8-bit SHIFT-REG.
→ SFT0*
← SFTI*
← SFTCK*

INTERRUPT CONT.
← INT0*
← INT1*
← INT2*

MUL/DIV

I/O PORT

P0 P1 P2 P3 P4 P5 P6

* Secondary functions of ports
** One timer is used for the SIO baud rate generator.

PIN CONFIGURATION (TOP VIEW)

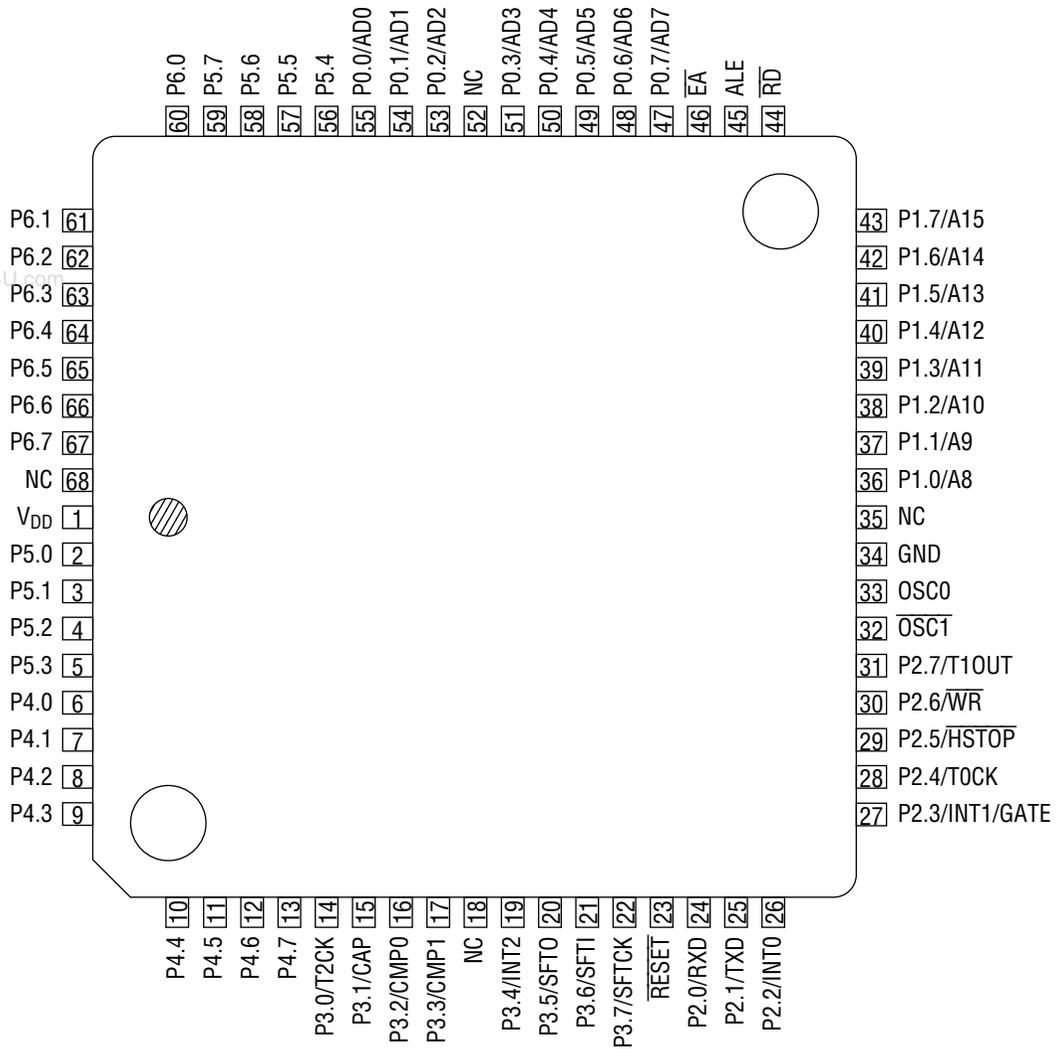| Left	Pin		Pin	Right
P5.0	1		64	V$_{DD}$
P5.1	2		63	P6.7
P5.2	3		62	P6.6
P5.3	4		61	P6.5
P4.0	5		60	P6.4
P4.1	6		59	P6.3
P4.2	7		58	P6.2
P4.3	8		57	P6.1
P4.4	9		56	P6.0
P4.5	10		55	P5.7
P4.6	11		54	P5.6
P4.7	12		53	P5.5
P3.0/T2CK	13		52	P5.4
P3.1/CAP	14		51	P0.0/AD0
P3.2/CMP0	15		50	P0.1/AD1
P3.3/CMP1	16		49	P0.2/AD2
P3.4/INT2	17		48	P0.3/AD3
P3.5/SFTO	18		47	P0.4/AD4
P3.6/SFTI	19		46	P0.5/AD5
P3.7/SFTCK	20		45	P0.6/AD6
$\overline{RESET}$	21		44	P0.7/AD7
P2.0/RXD	22		43	$\overline{EA}$
P2.1/TXD	23		42	ALE
P2.2/INT0	24		41	$\overline{RD}$
P2.3/INT1/GATE	25		40	P1.7/A15
P2.4/T0CK	26		39	P1.6/A14
P2.5/$\overline{HSTOP}$	27		38	P1.5/A13
P2.6/$\overline{WR}$	28		37	P1.4/A12
P2.7/T1OUT	29		36	P1.3/A11
$\overline{OSC1}$	30		35	P1.2/A10
OSC0	31		34	P1.1/A9
GND	32		33	P1.0/A8

64-Pin Plastic Shrink DIP

PIN CONFIGURATION (TOP VIEW) (Continued)

Top pins (left to right): 64 P4.3 | 63 P4.2 | 62 P4.1 | 61 P4.0 | 60 P5.3 | 59 P5.2 | 58 P5.1 | 57 P5.0 | 56 V$_{DD}$ | 55 P6.7 | 54 P6.6 | 53 P6.5 | 52 P6.4 | 51 P6.3 | 50 P6.2 | 49 P6.1

Left pins (top to bottom):
- P4.4 — 1
- P4.5 — 2
- P4.6 — 3
- P4.7 — 4
- P3.0/T2CK — 5
- P3.1/CAP — 6
- P3.2/CMP0 — 7
- P3.3/CMP1 — 8
- P3.4/INT2 — 9
- P3.5/SFTO — 10
- P3.6/SFTI — 11
- P3.7/SFTCK — 12
- $\overline{\text{RESET}}$ — 13
- P2.0/RXD — 14
- P2.1/TXD — 15
- P2.2/INT0 — 16

Right pins (top to bottom):
- 48 — P6.0
- 47 — P5.7
- 46 — P5.6
- 45 — P5.5
- 44 — P5.4
- 43 — P0.0/AD0
- 42 — P0.1/AD1
- 41 — P0.2/AD2
- 40 — P0.3/AD3
- 39 — P0.4/AD4
- 38 — P0.5/AD5
- 37 — P0.6/AD6
- 36 — P0.7/AD7
- 35 — $\overline{\text{EA}}$
- 34 — ALE
- 33 — $\overline{\text{RD}}$

Bottom pins (left to right): 17 P2.3/INT1/GATE | 18 P2.4/T0CK | 19 P2.5/$\overline{\text{HSTOP}}$ | 20 P2.6/$\overline{\text{WR}}$ | 21 P2.7/T1OUT | 22 OSC1 | 23 OSC0 | 24 GND | 25 P1.0/A8 | 26 P1.1/A9 | 27 P1.2/A10 | 28 P1.3/A11 | 29 P1.4/A12 | 30 P1.5/A13 | 31 P1.6/A14 | 32 P1.7/A15

64-Pin Plastic QFP

PIN CONFIGURATION (TOP VIEW) (Continued)

Top pins (left to right):

Pin	Signal
60	P6.0
59	P5.7
58	P5.6
57	P5.5
56	P5.4
55	P0.0/AD0
54	P0.1/AD1
53	P0.2/AD2
52	NC
51	P0.3/AD3
50	P0.4/AD4
49	P0.5/AD5
48	P0.6/AD6
47	P0.7/AD7
46	$\overline{EA}$
45	ALE
44	$\overline{RD}$

Left pins (top to bottom):

Pin	Signal
61	P6.1
62	P6.2
63	P6.3
64	P6.4
65	P6.5
66	P6.6
67	P6.7
68	NC
1	V_{DD}
2	P5.0
3	P5.1
4	P5.2
5	P5.3
6	P4.0
7	P4.1
8	P4.2
9	P4.3

Right pins (top to bottom):

Pin	Signal
43	P1.7/A15
42	P1.6/A14
41	P1.5/A13
40	P1.4/A12
39	P1.3/A11
38	P1.2/A10
37	P1.1/A9
36	P1.0/A8
35	NC
34	GND
33	OSC0
32	$\overline{OSC1}$
31	P2.7/T1OUT
30	P2.6/$\overline{WR}$
29	P2.5/$\overline{HSTOP}$
28	P2.4/T0CK
27	P2.3/INT1/GATE

Bottom pins (left to right):

Pin	Signal
10	P4.4
11	P4.5
12	P4.6
13	P4.7
14	P3.0/T2CK
15	P3.1/CAP
16	P3.2/CMP0
17	P3.3/CMP1
18	NC
19	P3.4/INT2
20	P3.5/SFT0
21	P3.6/SFTI
22	P3.7/SFTCK
23	$\overline{RESET}$
24	P2.0/RXD
25	P2.1/TXD
26	P2.2/INT0

NC: No-connection pin

68-Pin Plastic QFJ (PLCC)

PIN DESCRIPTION

Basic Functions

Function	Symbol	Type	Description
Power Supply	V_{DD}	—	+5V power supply
	GND	—	0V ground
Oscillation	OSC0	I	System clock input pin. Quartz oscillator or ceramic oscillator is connected between OSC0 and $\overline{OSC1}$. For external clock, input at OSC0, leaving $\overline{OSC1}$ open.
	$\overline{OSC1}$	O	System clock output pin
Control	$\overline{RESET}$	I	System reset input (program starts from address 0040H); internal pull-up resistance
	$\overline{EA}$	I	Program memory select input pin. "L" level input for external program memory; "H" level input for internal program memory.
	$\overline{RD}$	O	Read strobe signal during external memory access
	ALE	O	Address latch signal during external memory access
Port	PORT 0	I/O	8-bit Input-output port During external memory access, becomes address/data bus for address output, instruction fetch or data read/write along with ALE, $\overline{RD}$ and $\overline{WR}$ pins.
	PORT 1	I/O	8-bit Input-output port Address bus during external memory access
	PORT 2 PORT 3 PORT 4 PORT 5	I/O	8-bit Input-output port $\times$ 4. Secondary functions shown in following table are added for ports 2 and 3.
	PORT 6	I	8-bit Input port

Secondary Functions

Symbol	Type	Description
RXD	I/O	P2.0 secondary function UART: Input pin for serial port receive data. Synchronous: Input/output pin for serial port transmit/receive data.
TXD	O	P2.1 secondary function UART: Output pin for serial port transmit data. Synchronous: Output pin for serial port synchronizing clock.
INT0	I	P2.2 secondary function External interrupt 0 input pin.
INT1/GATE	I	P2.3 secondary functions External interrupt 1 input pin. Also used as input pin for gate signal for timer 0 count enable/disable.
T0CK	I	P2.4 secondary function Timer 0 external clock input pin.
$\overline{\text{HSTOP}}$	I	P2.5 secondary function Hard stop mode input pin; stops system clock oscillation with "L" level input.
$\overline{\text{WR}}$	O	P2.6 secondary function Write strobe signal output pin during external data memory access.
T1OUT	O	P2.7 secondary function Output pin for signal that 2-divided timer 1 overflow.
T2CK	I	P3.0 secondary function Timer 2 external clock input pin.
CAP	I	P3.1 secondary function Capture trigger input pin.
CMP0	O	P3.2 secondary function Compare output channel 0 output pin.
CMP1	O	P3.3 secondary function Compare output channel 1 output pin.
INT2	I	P3.4 secondary function External interrupt 2 input pin.
SFTO	O	P3.5 secondary function Shift register data output pin.
SFTI	I	P3.6 secondary function Shift register data input pin.
SFTCK	I/O	P3.7 secondary function Shift register synchronizing clock input/output pin.

Port Circuit Configuration

Type	Port	Circuit Configuration	Electrical Characteristics (V_{DD}=5V)
1	P0.0/AD0 to P0.7/AD7		"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=−400µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=3.2mA
2	P1.0/A8 to P1.7/A15		"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=−200µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=1.6mA
3	P2.0/RXD, P2.1/TXD, P2.6/$\overline{WR}$, P2.7/T1OUT, P3.2/CMP0, P3.3/CMP1, P3.5/SFTO, P3.7/SFTCK		"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V P2.6/$\overline{WR}$ "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=−400µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=3.2mA Excluding P2.6/$\overline{WR}$ "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=−200µA "L" Output Voltage: • V_{OL}=0.4V • I_{OL}=1.6mA

Port Circuit Configuration (Continued)

Type	Port	Circuit Configuration	Electrical Characteristics (V$_{DD}$=5V)
4	P2.2/INT0, P2.3/INT1/GATE, P2.4/T0CK, P2.5/$\overline{\text{HSTOP}}$, P3.0/T2CK, P3.1/CAP, P3.4/INT2, P3.6/SFTI, P4.0 to P4.7, P5.0 to P5.7	Data Bus — PxD — PORTx — Px DIR — Secondary Input Function (x=2 to 5)	"H" Input Voltage: • V$_{IH}$=2.4V "L" Input Voltage: • V$_{IL}$=0.8V "H" Output Voltage: • V$_{OH}$=3.75V • I$_{OH}$=−200µA "L" Output Voltage: • V$_{OL}$=0.4V • I$_{OL}$=1.6mA
5	P6.0 to P6.7	Data Bus — PORT6	"H" Input Voltage: • V$_{IH}$=2.4V "L" Input Voltage: • V$_{IL}$=0.8V
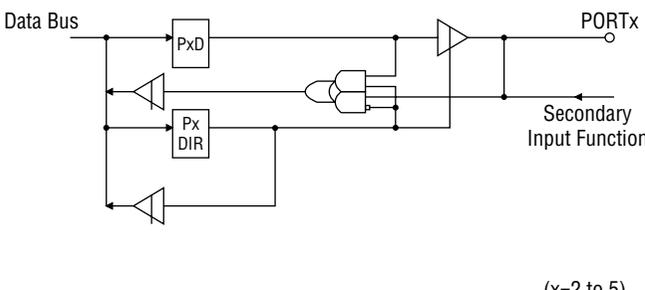
MEMORY MAPS

General Memory Space

Local Memory Space
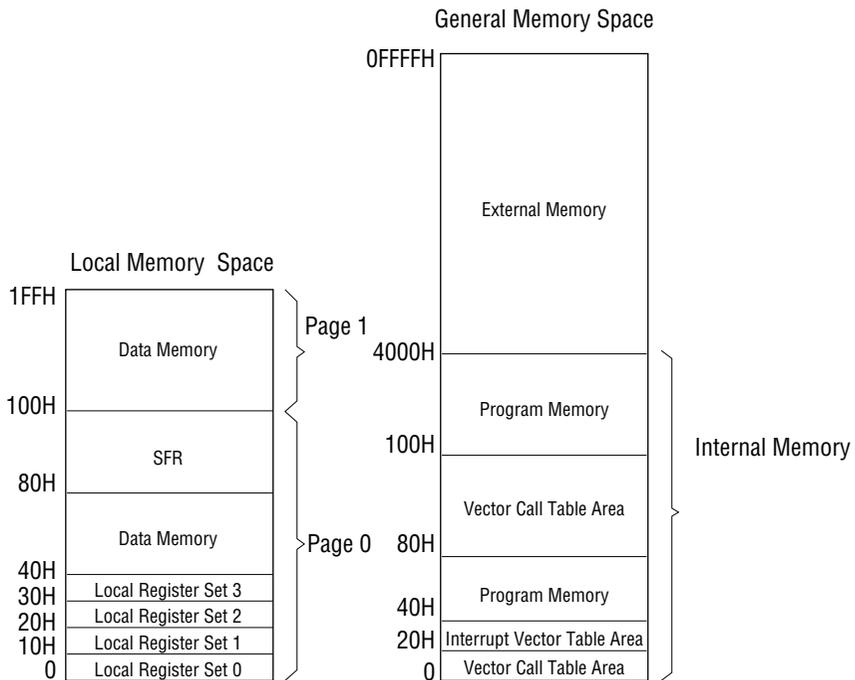
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}		-0.3 to 7.0	
Input Voltage	V_I	Ta=25°C	-0.3 to $V_{DD}+0.3$	V
Output Voltage	V_O		-0.3 to $V_{DD}+0.3$	
Power Dissipation	P_D	Ta=25°C per package	400	mW
		Ta=25°C per output	50	
Storage Temperature	T_{STG}	—	-55 to $+150$	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	Refer to Figure 1	2.7 to 5.5	V
Memory Hold Voltage	V_{DDMH}	f_{OSC}=0 Hz	2.0 to 5.5	
Oscillation Operating Frequency *1	f_{OSC}	Refer to Figure 1	1 to 10	MHz
External Clock Operating Frequency	f_{EXTCLK}	Refer to Figure 1	0 to 10	MHz
Operating Temperature	T_{op}	—	-40 to $+85$	°C

*1 This is due to the standard of a crystal oscillator or resonator.

Ta=−40 to +85°C

* Oscillates at 1MHz or more.
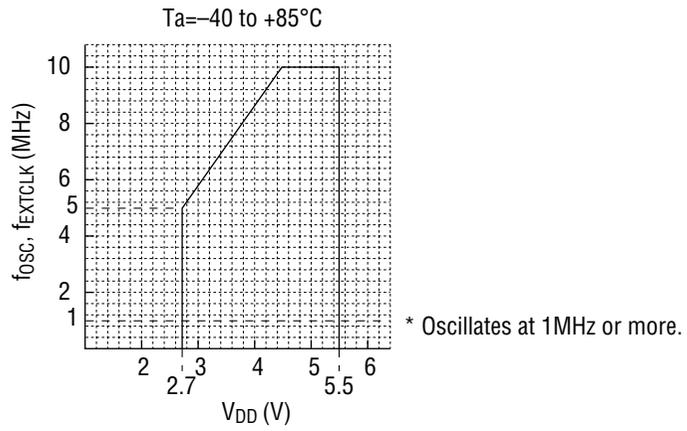
Figure 1.   Operating Frequency vs. Power Supply Voltage

ELECTRICAL CHARACTERISTICS

DC Characteristics 1 (V_{DD}=4.5 to 5.5V)

(GND=0V, Ta=−40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 [*1]	V_{IH1}	—	2.4	—	V_{DD}+0.3	V
"H" Input Voltage 2 [*2]	V_{IH2}	—	$0.7V_{DD}$	—	V_{DD}+0.3	
"L" Input Voltage	V_{IL}	—	−0.3	—	0.8	
"H" Output Voltage 1 [*3]	V_{OH1}	I_{OH}=−200µA	$0.75V_{DD}$	—	—	
"H" Output Voltage 2 [*4]	V_{OH2}	I_{OH}=−400µA	$0.75V_{DD}$	—	—	
"L" Output Voltage 1 [*3]	V_{OL1}	I_{OL}=1.6mA	—	—	0.4	
"L" Output Voltage 2 [*4]	V_{OL2}	I_{OL}=3.2mA	—	—	0.4	
Input Lack Current 1 [*5]	I_{LI1}	V_I=V_{DD}/0V	—	—	±1	µA
Input Lack Current 2 [*6]	I_{LI2}	V_I=V_{DD}/0V	—	—	±10	
"L" Input Current [*7]	I_{IL}	V_I=0V	−40	−200	−400	
Input Capacity	C_I	f=1MHz, Ta=25°C	—	5	—	pF
Still Current Consumption	I_{DDS}	5V, Stop mode [*8]	—	—	50	µA
Operating Current Consumption	I_{DD}	10MHz, 5V, no load Refer to Fig.2	—	20	40	mA

*1   Excluding OSC0 and $\overline{\text{RESET}}$

*2   OSC0 and $\overline{\text{RESET}}$

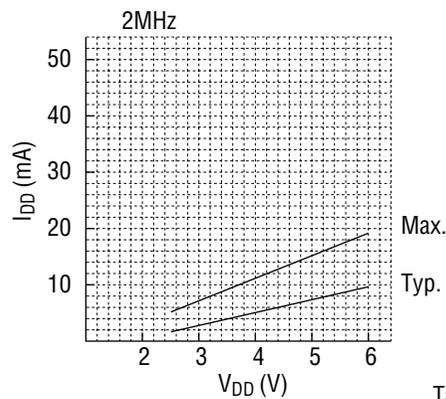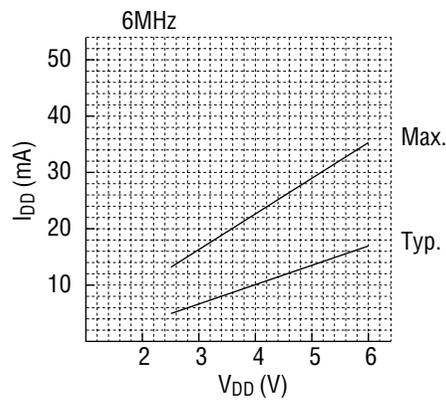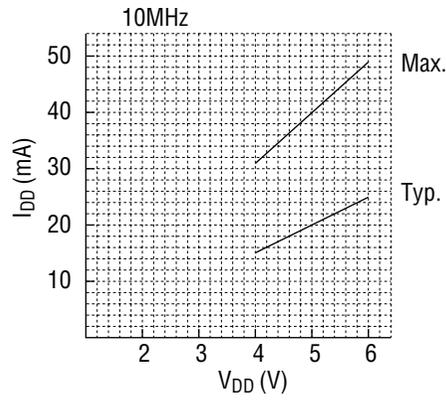*3   Excluding P0, ALE, $\overline{\text{RD}}$, P2.6/$\overline{\text{WR}}$

*4   P0, ALE, $\overline{\text{RD}}$, P2.6/$\overline{\text{WR}}$

*5 $\overline{\text{EA}}$, P6

*6   Excluding $\overline{\text{RESET}}$, $\overline{\text{EA}}$, P6

*7 $\overline{\text{RESET}}$

*8   The ports configured as inputs should be coupled to V_{DD} or 0V. Other ports should not be loaded.

## DC Characteristics 2 (2.7 ≤ V_{DD} < 4.5V)

(GND=0V, Ta=−40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 [*1]	V_{IH1}	—	$0.5V_{DD}+0.2$	—	$V_{DD}+0.3$	V
"H" Input Voltage 2 [*2]	V_{IH2}	—	$0.6V_{DD}+0.4$	—	$V_{DD}+0.3$	
"L" Input Voltage	V_{IL}	—	−0.3	—	$0.15V_{DD}+0.1$	
"H" Output Voltage 1 [*3]	V_{OH1}	$I_{OH}=-10\mu A$	$0.75V_{DD}$	—	—	
"H" Output Voltage 2 [*4]	V_{OH2}	$I_{OH}=-20\mu A$	$0.75V_{DD}$	—	—	
"L" Output Voltage 1 [*3]	V_{OL1}	$I_{OL}=10\mu A$	—	—	0.1	
"L" Output Voltage 2 [*4]	V_{OL2}	$I_{OL}=20\mu A$	—	—	0.1	
Input Lack Current 1 [*5]	I_{LI1}	$V_I=V_{DD}/0V$	—	—	±1	μA
Input Lack Current 2 [*6]	I_{LI2}	$V_I=V_{DD}/0V$	—	—	±10	
"L" Input Current [*7]	I_{IL}	V_{DD}=2.7 to 3.3V, V_I=0V	−40	−120	−240	
Input Capacity	C_I	f=1MHz, Ta=25°C	—	5	—	pF
Still Current Consumption	I_{DDS}	3V, Stop mode [*8]	—	—	25	μA
Operating Current Consumption	I_{DD}	5MHz, 3V, no load Refer to Fig.2	—	6	15	mA

*1   Excluding OSC0 and $\overline{\text{RESET}}$
*2   OSC0 and $\overline{\text{RESET}}$
*3   Excluding P0, ALE, $\overline{\text{RD}}$, P2.6/$\overline{\text{WR}}$
*4   P0, ALE, $\overline{\text{RD}}$, P2.6/$\overline{\text{WR}}$
*5 $\overline{\text{EA}}$, P6
*6   Excluding $\overline{\text{RESET}}$, $\overline{\text{EA}}$, P6
*7 $\overline{\text{RESET}}$
*8   The ports configured as inputs should be coupled to V_{DD} or 0V. Other ports should not be loaded.

Figure 2.   Operating Current Consumption vs. Power Supply Voltage

AC Characteristics

• External memory control

$(V_{DD}=2.7$ to $5.5V$, GND=0V, Ta=−40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Period	t_C		100	—	
"L" Clock Pulse Width	t_{CLW}	$V_{DD}=4.5$ to $5.5V$	45	—	
"H" Clock Pulse Width	t_{CHW}		45	—	
Clock Period	t_C		200	—	
"L" Clock Pulse Width	t_{CLW}	$V_{DD}=2.7$ to $5.5V$	90	—	
"H" Clock Pulse Width	t_{CHW}		90	—	
ALE Pulse Width	t_{AW}		$t_C+t_{CHW}-20$	—	
ALE Pulse Delay Time 1	t_{ALD1}		$t_{CLW}-20$	—	
ALE Pulse Delay Time 2	t_{ALD2}		$t_{CLW}-20$	—	
$\overline{RD}$ Pulse Width	t_{RW}		$t_C+t_{CHW}-20$	—	
$\overline{RD}$ Pulse Delay Time	t_{RD}		$t_{CLW}-40$	$t_{CLW}+20$	ns
$\overline{WR}$ Pulse Width	t_{WW}		$t_C+t_{CHW}-40$	—	
$\overline{WR}$ Pulse Delay Time	t_{WD}		$t_{CLW}-20$	$t_{CLW}+40$	
"L" Address Setup Time	t_{LAS}		t_C-40	—	
"H" Address Setup Time	t_{HAS}	$C_L=100pF$	t_C-40	—	
"L" Address Hold Time	t_{LAH}		$t_{CLW}-20$	—	
Bus Float Time	t_{LAZ}		—	20	
"H" Address Hold Time	t_{HAHR}		t_C-20	—	
"H" Address Hold Time	t_{HAHW}		t_C-20	—	
Read Data Access Time	t_{RDAA}		—	$t_C+t_{CLW}-15$	
Read Data Access Time	t_{RDAR}		—	$t_{CHW}+10$	
Read Data Hold Time	t_{RDH}		0	—	
Write Data Setup Time	t_{WDS}		$t_C+t_{CLH}-40$	—	
Write Data Hold Time	t_{WDH}		$t_{CLW}-20$	—	
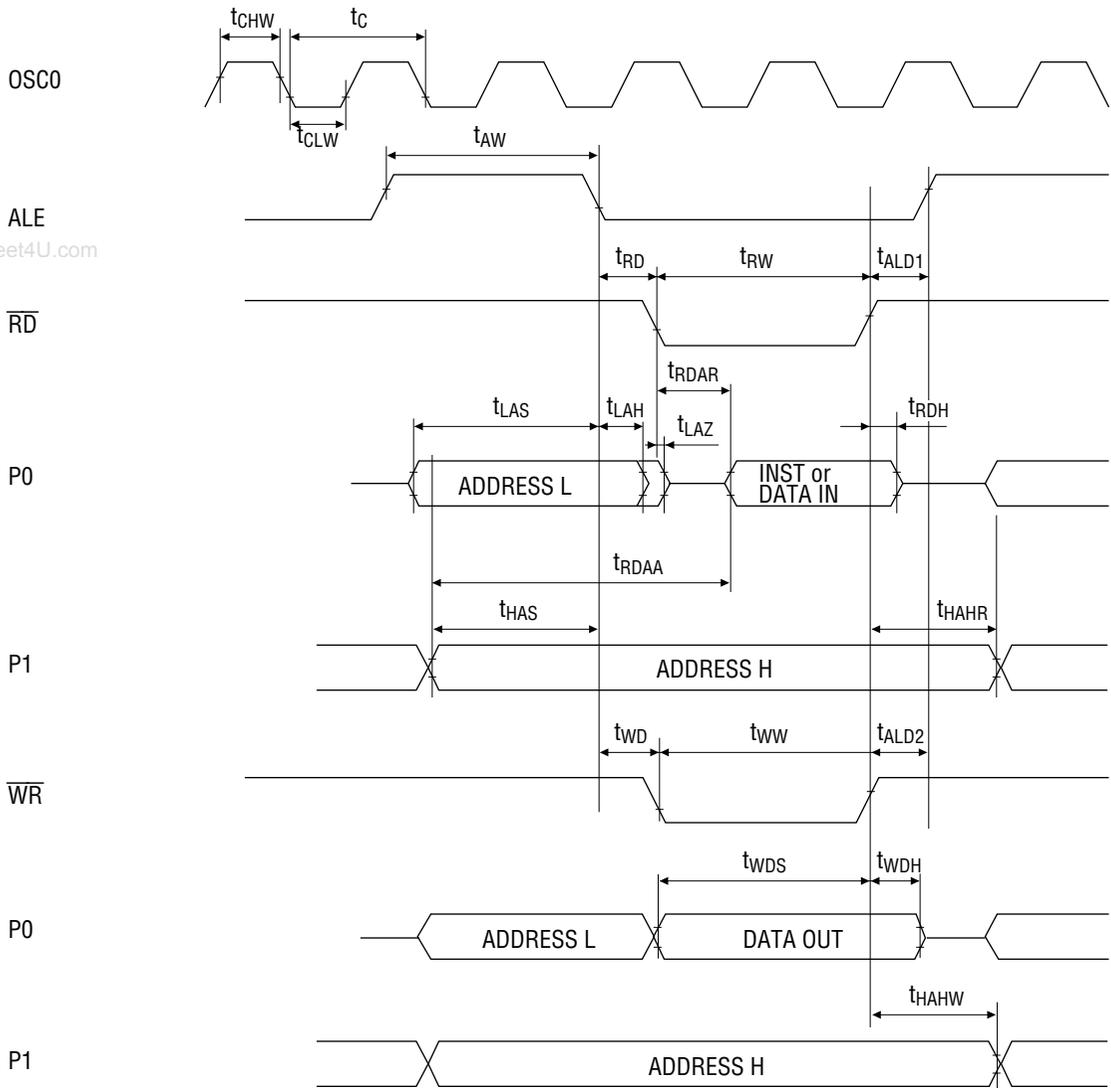
• CPU control

$(V_{DD}=2.7 \text{ to } 5.5V, \text{ GND}=0V, Ta=-40 \text{ to } +85°C)$

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{\text{RESET}}$ Pulse Width [*1]	t_{RESW1}	—	20	—	ns
$\overline{\text{RESET}}$ Pulse Width [*2]	t_{RESW2}	—	[*3]	—	—

*1 Excluding power ON, stop mode and hard stop mode.
*2 In power ON, stop mode and hard stop mode.
*3 Oscillation stabilization time depends on resonator.
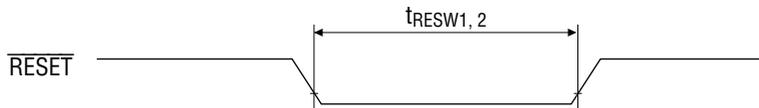
$\overline{\text{RESET}}$ pulse width

• Peripheral control 1

$(V_{DD}=2.7 \text{ to } 5.5V, \text{ GND}=0V, Ta=-40 \text{ to } +85°C)$

Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Period	t_C	$V_{DD}=4.5 \text{ to } 5.5V$	100	—	ns
			$V_{DD}=2.7 \text{ to } 5.5V$	200	—	
EXI	External Interrupt Pulse Width	t_{EXIW}		$4\ t_C$	—	
T0	External Clock Pulse Width	t_{T0CW}		$4\ t_C$	—	
	GATE Pulse Width	t_{T0GW}	—	$1\ t_{T0CLK}$ [*]	—	
T2	External Clock Pulse Width	t_{T2CW}		$4\ t_C$	—	
CAP	CAP Pulse Width	t_{CAPW}		$12\ t_C$	—	

* t_{T0CLK} : Timer 0 count clock period selected by T0CON.

OSC0

t_C

t_{CLW}

1) EXI pulse width

INT0-2

t_{EXIW}

2) T0

T0CK

t_{T0CW}

GATE

t_{T0GW}

3) T2

T2CK

t_{T2CW}

4) CAP

CAP

t_{CAPW}
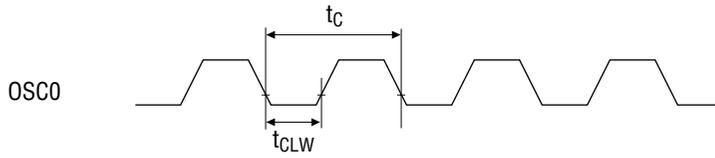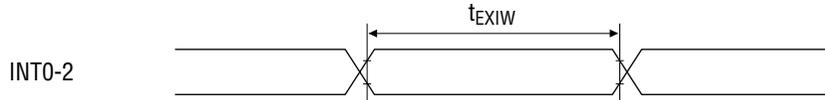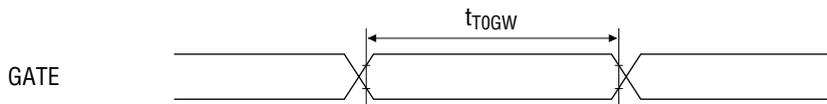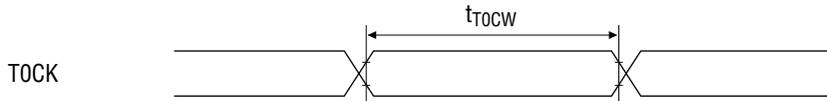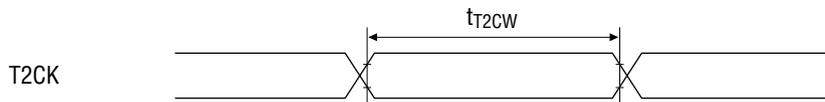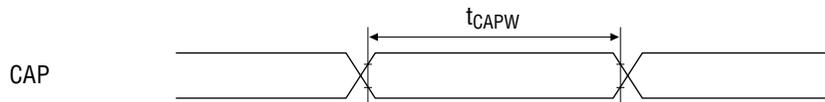
• Peripheral control 2

(V_{DD}=2.7 to 5.5V, GND=0V, Ta=−40 to +85°C)

Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Period	t_C	V_{DD}=4.5 to 5.5V	100	—	ns
			V_{DD}=2.7 to 5.5V	200	—	
SFT	SFTCK Period	t_{SFC}	C_L=100pF	8 t_C	—	
	SFTCK "L" Pulse Width	t_{SFCLW}		4 t_C−20	—	
	SFTCK "H" Pulse Width	t_{SFCHW}		4 t_C−20	—	
	SFTCK Setup Time	t_{SFOS}		t_{SFCLW}−100	—	
	SFTO Hold Time	t_{SFOH}		t_{SFCHW}−100	—	
	SFTI Setup Time	t_{SFIS}		100	—	
	SFTI Hold Time	t_{SFIH}		100	—	
SIO (Clock Synchronous Mode)	Synchronous Clock Period	t_{SIC}		8 t_C	—	
	Synchronous Clock "L" Pulse Width	t_{SICLW}		4 t_C−20	—	
	Synchronous Clock "H" Pulse Width	t_{SICHW}		4 t_C−20	—	
	Output Data Setup Time	t_{SIOS}		6 t_C−100	—	
	Output Data Hold Time	t_{SIOH}		2 t_C−100	—	
	Input Data Setup Time	t_{SIIS}		t_C+t_{CLW}+100	—	
	Input Data Hold Time	t_{SIIH}		0	—	

See TIMING DIAGRAM.

1) SFT
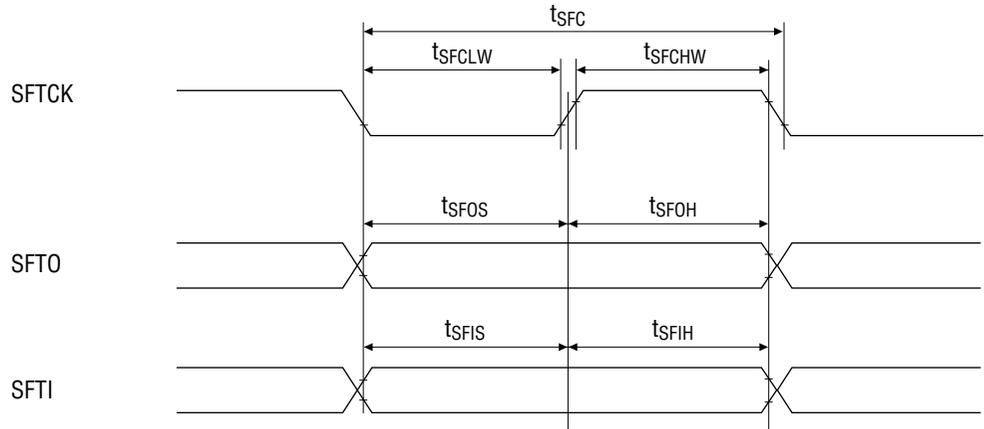
2) SIO
   (Clock synchronous mode)
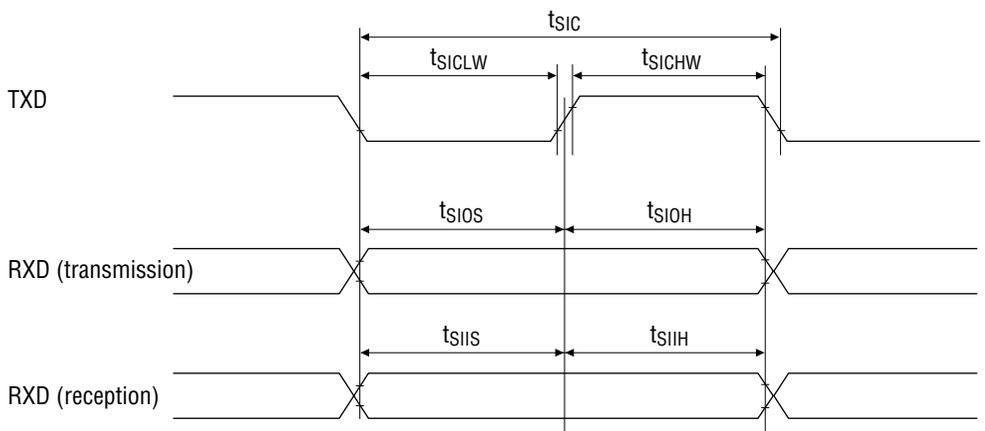
PACKAGE DIMENSIONS

(Unit : mm)

SDIP64-P-750-1.78

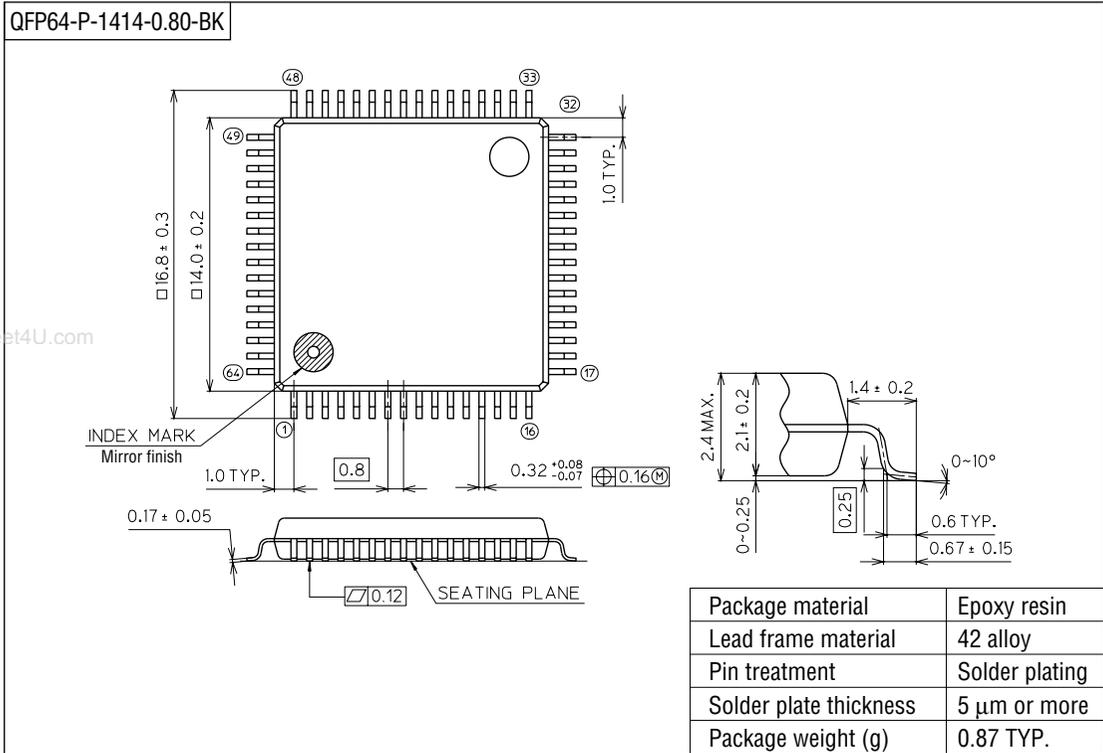| Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	8.70 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).
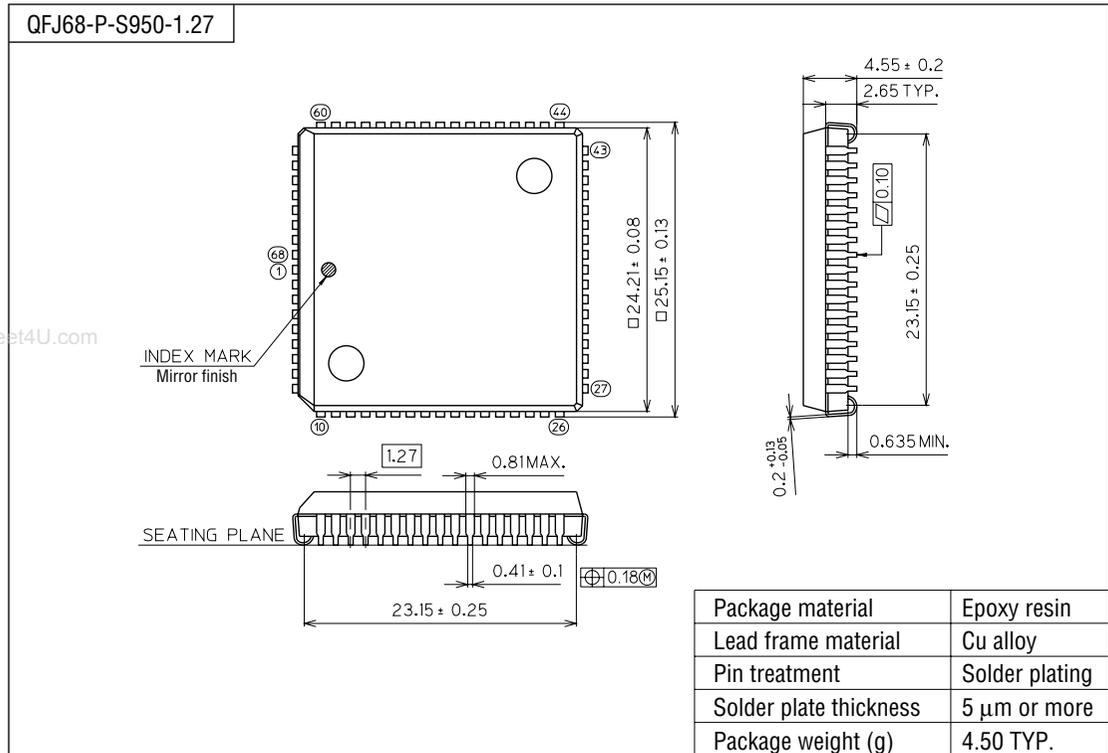
(Unit : mm)

QFP64-P-1414-0.80-BK

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.87 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFJ68-P-S950-1.27

Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	4.50 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).