

MSM6586**262,144-Word x 1-Bit Serial Register****GENERAL DESCRIPTION**

The MSM6586 is a serial register in 262,144 words x 1 bit configuration featuring medium speed operation with low power consumption.

The MSM6586 has a built-in internal address generator circuit allowing continuous serial read/write operation by external clock input. The internal address is automatically incremented or decremented by one by read/write operation. Address increment or decrement can be selected by external input.

Address designation in units of 1024 words in the direction of words is possible by an external serial address input.

A refresh timer and refresh counter are built in to eliminate the need of the external refresh circuit and to realize low power consumption.

18-pin plastic QFJ (PLCC) is used as the package and the operating temperature range is between 0°C and 70°C.

The MSM6586 is suitable for storing large capacity data with battery backup. A solid state recording and playback system can easily be constructed in combination with OKI's voice synthesizer ICs.

FEATURES

- Configuration : 262,144 x 1 bit
- Serial access operation
 - Serial access time : 1.5 μ s (3.0 μ s)
 - Serial read/write cycle time : 2.0 μ s (4.0 μ s)
 - Fast mode read/write cycle time : 0.4 μ s (0.4 μ s)
 - Times in parentheses indicate ones in self-refresh mode.
- Low current consumption : 100 μ A max.
(for data holding, $V_{CC} = 4.0$ V)
- Wide operating supply voltage range : Single 3.5 to 5.5 V
- Auto-refresh/self-refresh changeable
- Package: 18-pin plastic QFJ (PLCC) (QFJ18-P-R290-1.27) (Product name : MSM6586JS)

PIN DESCRIPTIONS

Pin	Symbol	Description
1	DIN	Data input
2	\overline{WE}	Write enable
3, 16	\overline{TEST}	Test input
4	\overline{CS}	Chip select
6	SAD	Serial address data
7	\overline{SAS}	Serial address strobe
8	\overline{TAS}	Transfer address strobe
9	V _{CC}	Power supply (+5V)
10	$\overline{RS/A}$ (TEST)	Self-refresh/auto-refresh select (Test input)
11	\overline{RFSH} (TEST)	Refresh clock input (Test input)
12	\overline{FAM} (TEST)	Fast access mode select (Test input)
13	\overline{RWCK}	Read/write clock
15	AU/D	Address up/down select
17	DOUT	Data output
18	V _{SS}	Ground (0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Terminal Voltage	V_T	$T_a = 25^\circ\text{C}$, relative to V_{SS}	-1.0 to +7.0	V
Output Short-Circuit Current	I_{OS}	$T_a = 25^\circ\text{C}$	50	mA
Power Dissipation	P_D	$T_a = 25^\circ\text{C}$	1	W
Operating Temperature	T_{op}	—	0 to 70	$^\circ\text{C}$
Storage Temperature	T_{STG}	—	-55 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

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(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
"H" Input Voltage	V_{IH}	$V_{CC} - 0.5$	V_{CC}	$V_{CC} + 0.5$	V
"L" Input Voltage	V_{IL}	-0.5	0	+0.5	V

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = 3.5V to 5.5V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" Output Voltage	V_{OH}	$I_{OH} = -0.5\text{mA}$	$V_{CC} - 0.5$	—	V
"L" Output Voltage	V_{OL}	$I_{OL} = 0.5\text{mA}$	—	0.4	V
Input Leakage Current	I_{LI}	$V_I = 0\text{V}$ to V_{CC}	-1	+1	μA
Output Leakage Current	I_{LO}	$V_O = 0\text{V}$ to V_{CC}	-1	+1	μA
Supply Current (in operating state)	I_{CC1}	$V_{CC} = 4\text{V}$, $t_{RWC} = 2\mu\text{s}$	—	5	mA
Supply Current (in standby state)	I_{CC2}	$V_{CC} = 4\text{V}$	—	100	μA
Supply Current (FAM)	I_{CC3}	$V_{CC} = 4\text{V}$, $t_{RWC} = 0.4\mu\text{s}$	—	15	mA

AC Characteristics

(V_{CC} = 3.5V to 5.5V, T_a = 0 to 70°C)

Parameter	Symbol	MSM6586-SELF		MSM6586-AUTO		Unit
		Min.	Max.	Min.	Max.	
Refresh Cycle	t _{REF}	—	—	—	100	ms
Read/Write Cycle Time	t _{RWC}	4,000	—	2,000	—	ns
Access Time	t _{ACC}	—	3,000	—	1500	ns
Output Turn-off Delay Time	t _{OFF}	0	50	0	50	ns
Input Signal Rise/Fall Time	t _T	3	50	3	50	ns
RWCK Precharge Time	t _{RWP}	1,000	—	500	—	ns
RWCK Pulse Width	t _{RW}	3,000	10,000	1,500	10,000	ns
SAS Cycle Time	t _{SSC}	100	—	100	—	ns
SAS Pulse Width	t _{SAS}	50	—	50	—	ns
SAS Precharge Time	t _{SAP}	50	—	50	—	ns
Address Setup Time	t _{AS}	0	—	0	—	ns
Address Hold Time	t _{AH}	50	—	50	—	ns
TAS Setup Time	t _{ATS}	50	—	50	—	ns
TAS to RWCK Setup Time	t _{TRS}	50	—	50	—	ns
TAS Pulse Width	t _{TAS}	50	—	50	—	ns
Read Command Setup Time	t _{RRS}	0	—	0	—	ns
Read Command Hold Time	t _{RRH}	250	—	250	—	ns
Write Command Setup Time	t _{WRS}	0	—	0	—	ns
Write Command Hold Time	t _{WRH}	50	—	50	—	ns
Write Command Pulse Width	t _{WP}	50	—	50	—	ns
WE to RWCK Lead Time	t _{RWL}	50	—	50	—	ns
Data Setup Time	t _{DS}	0	—	0	—	ns
Data Hold Time	t _{DH}	50	—	50	—	ns
RWCK to WE Delay Time	t _{RWD}	100	—	100	—	ns
AU/D Setup Time	t _{UDS}	0	—	0	—	ns
AU/D Hold Time	t _{UDH}	50	—	50	—	ns
AU/D to TAS Setup Time	t _{UDTS}	0	—	0	—	ns
RFSH Setup Time	t _{RFS}	—	—	500	—	ns
RFSH Precharge Time	t _{RFP}	—	—	500	—	ns
RFSH Pulse Width	t _{RF}	—	—	1,500	10,000	ns
RFSH RWCK Precharge Time	t _{RRP}	—	—	500	—	ns
Fast RWCK Mode Cycle	t _{FC}	400	—	400	—	ns
Fast Mode Access Time	t _{FAC}	—	300	—	300	ns
Fast RWCK Precharge Time	t _{FCP}	100	—	100	—	ns
Fast Mode RWCK Pulse Width	t _{FR}	300	—	300	—	ns
Fast Mode Setup Time	t _{FS}	0	—	0	—	ns
Fast Mode Hold Time	t _{FH}	50	—	50	—	ns

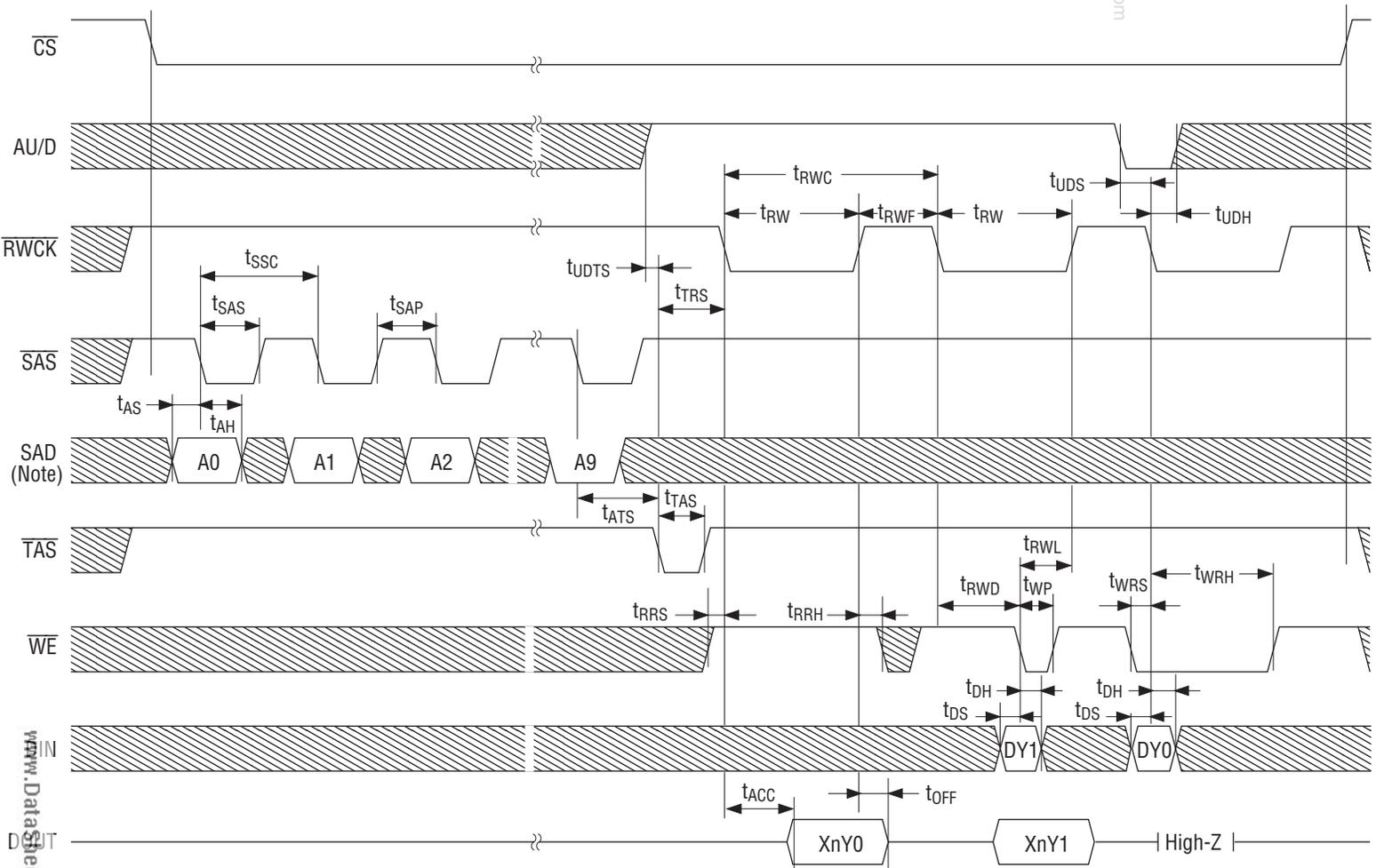
AC Characteristics (Continued)

Parameter	Symbol	MSM6586-SELF		MSM6586-AUTO		Unit
		Min.	Max.	Min.	Max.	
Fast Mode Width	t_{FCC}	4,000	100,000	2,000	100,000	ns
Slow Mode Setup Time	t_{SS}	0	—	0	—	ns
Slow Mode Hold Time	t_{SH}	50	—	50	—	ns

- Note: 1. Up/down switching for internal addresses is not available in fast mode.
 2. Switching to the fast mode should be made satisfying the timings of t_{FS} and t_{SS} at the "L" level of RWCK.

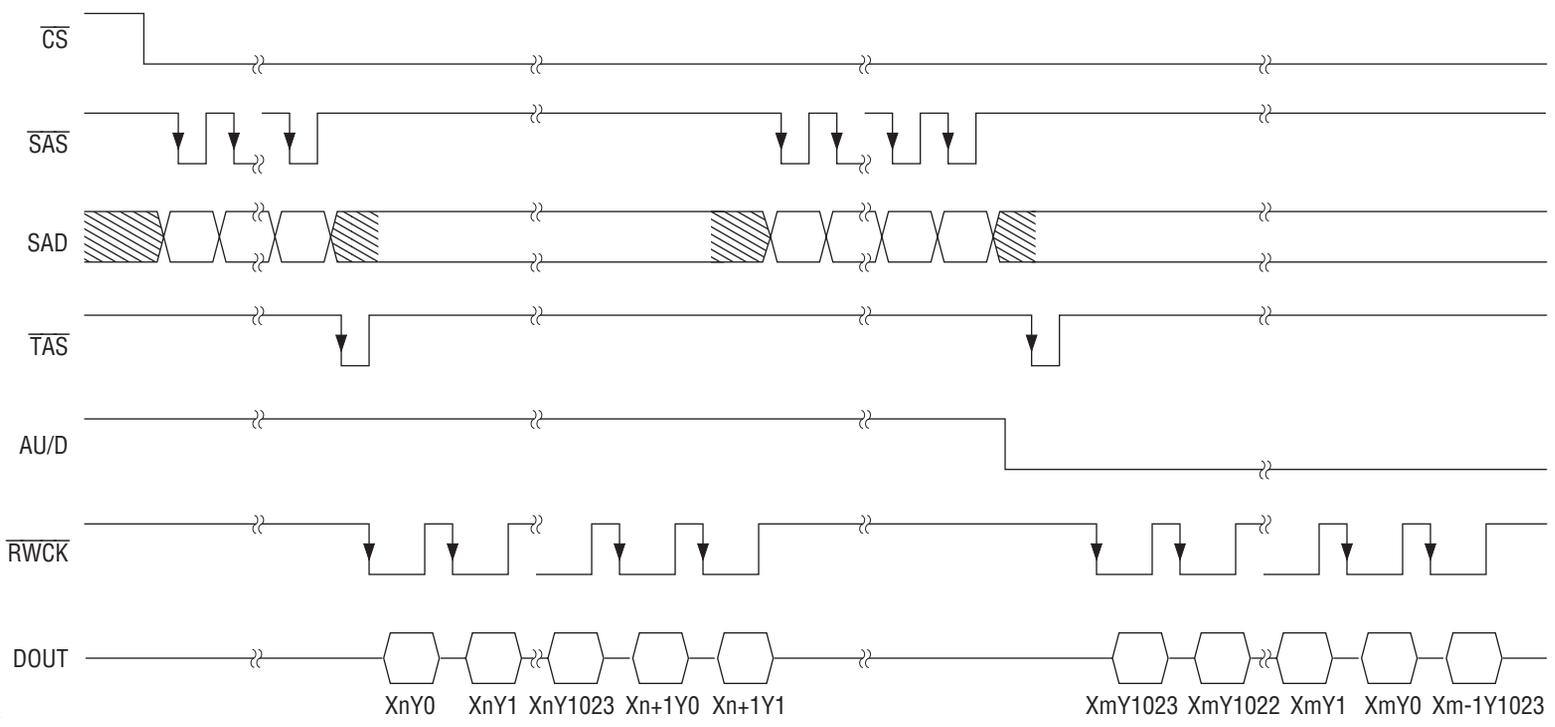
TIMING DIAGRAMS

Read/Write/Read Modify Write Cycle



Note: Out of ten bits from A0 to A9, only the eight bits from A0 to A7 are effective. Fix A8 and A9 to "L".

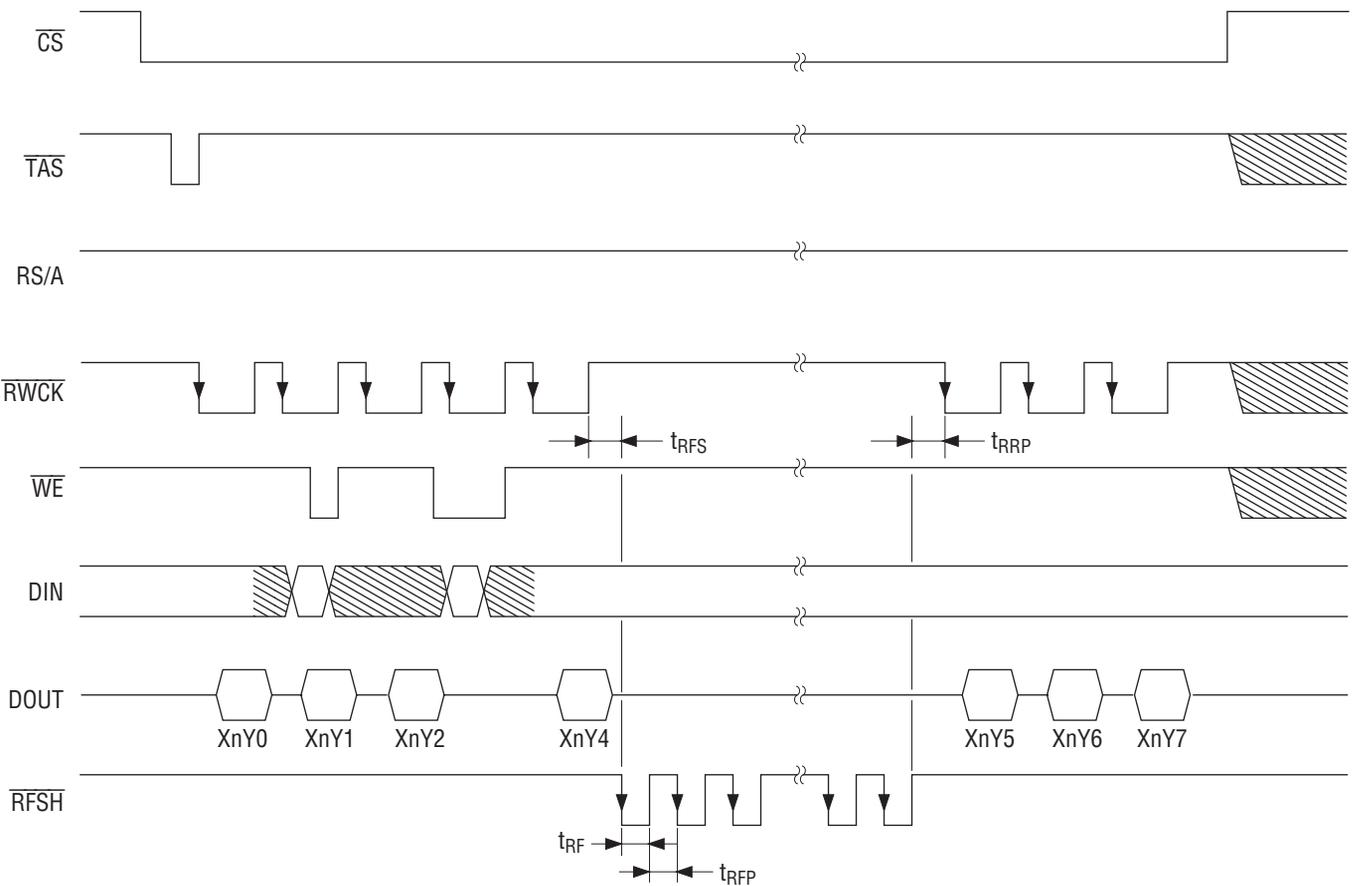
Address Up/Down Select Mode



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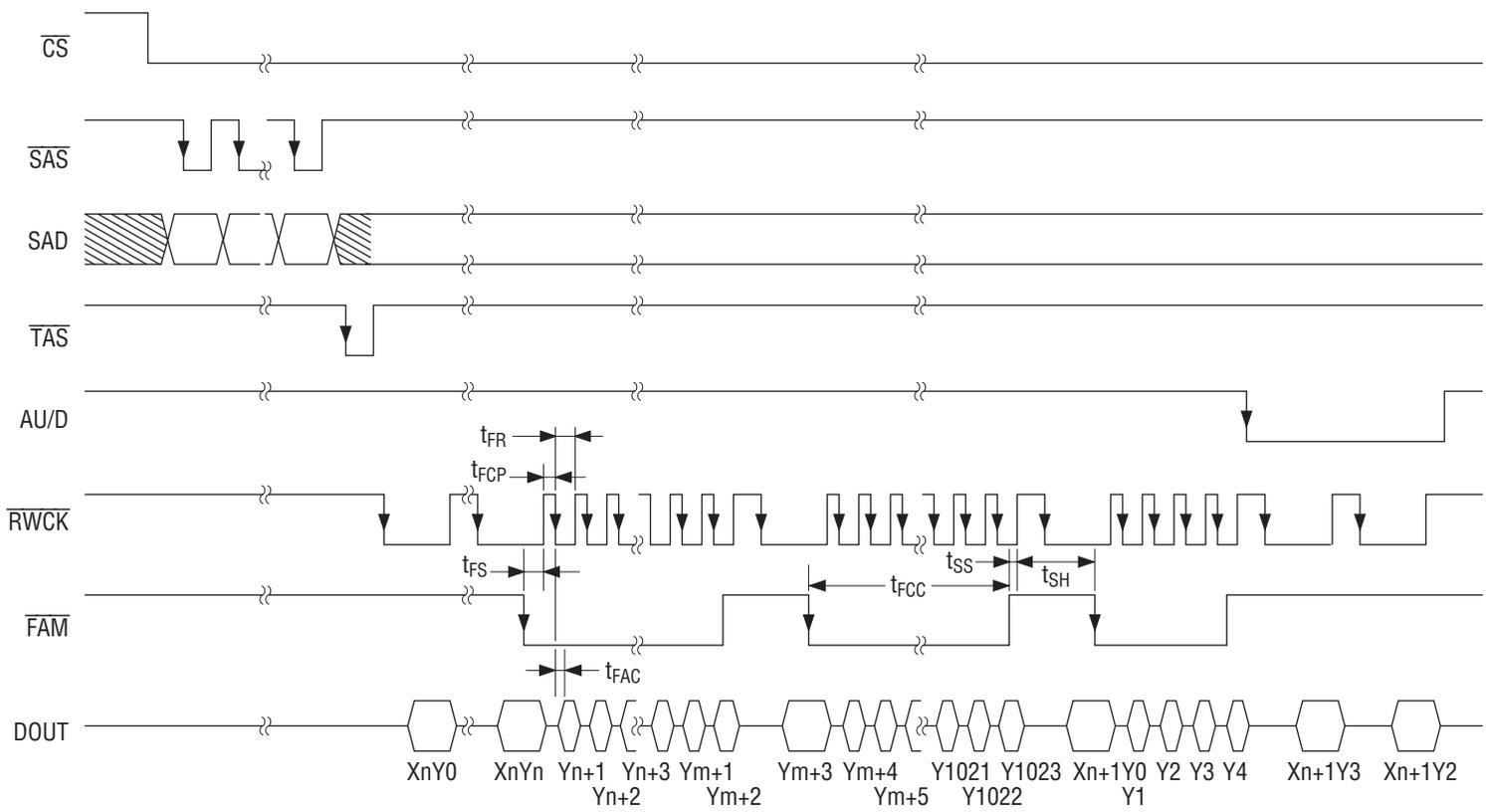
Auto-Refresh Mode



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Fast Access Mode

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FUNCTIONAL DESCRIPTION

Serial Address Input (SAD)

Pin for inputting the read/write starting address. Designation in units of 1024 words is possible. The 512 address data can be input as 10-bit (A0-A9) serial from the SAD pin. (A0-A7 has enable address, A8 and A9 keep "L".)

Serial Address Strobe ($\overline{\text{SAS}}$)

Pin for the clock used to store the serial address data into the internal register.

Address Transfer Strobe ($\overline{\text{TAS}}$)

Input pin for setting the serial address data stored in the address register to the internal address counter.

When the $\overline{\text{TAS}}$ falls, and the Y address is set to address 0 in the increment mode or to address 1023 in the decrement mode.

Read/Write Clock ($\overline{\text{RWCK}}$)

Input pin for the data register information read/write clock.

Internal operation starts at the falling edge of $\overline{\text{RWCK}}$. The information in the data register is output to the DOUT pin in the read mode, and the information at the DIN pin is written into the data register in the write mode. The internal address counter is automatically incremented or decremented also when $\overline{\text{RWCK}}$ falls.

Write Enable ($\overline{\text{WE}}$)

Input pin for selecting the read mode, write mode or read modify write mode.

The read mode is set when $\overline{\text{WE}}$ is "H", and the write mode is set when $\overline{\text{WE}}$ is "L". When $\overline{\text{WE}}$ falls from "H" to "L" while $\overline{\text{RWCK}}$ is active, the read modify write mode is set.

Data Input (DIN)

Input pin for write data.

The information at the data input pin is stored at the falling edge of $\overline{\text{RWCK}}$ in the write mode, and at the falling edge of $\overline{\text{WE}}$ in the modify write mode.

Data Output (DOUT)

The data output pin is always kept in the high impedance state when $\overline{\text{RWCK}}$ or $\overline{\text{CS}}$ is kept at "H". When "H" or "L" information is read in the read operation, the output pin is set to "H" or "L" and holds the read information until $\overline{\text{RWCK}}$ is again set to "H". In the early write mode the output pin maintains the high impedance state, so I/O common operation by connecting DIN and DOUT is possible.

Address Up/Down Select (AU/D)

Input pin for selecting the direction of automatic address updating.

When the $\overline{\text{TAS}}$ signal is input with the AU/D pin set to "H", the internal address counters are set to the externally set address for X and to address 0 for Y. Then the address is incremented by 1 every time $\overline{\text{RWCK}}$ is input.

When the $\overline{\text{TAS}}$ signal is input with the AU/D pin set to "L", the internal address counters are set to the externally set address in the same way for X but set to address 1023 for Y.

Then the address is decremented by 1 every time $\overline{\text{RWCK}}$ is input. In either case, the X address is automatically incremented or decremented by 1 when read/write operation for 1024 words ends. The AU/D pin setting change is possible in any read/write cycle so long as the timing specifications for t_{UDS} , t_{UDH} are satisfied.

Chip Select ($\overline{\text{CS}}$)

Input pin for disabling all input and output pins. This pin enables parallel use of multiple MSM6586s by connecting the data input and output pins.

Self/Auto Refresh Select ($\overline{\text{RS/A}}$ (TEST))

Pin for selecting a refresh mode in order to retain memory cell data.

If the $\overline{\text{RS/A}}$ pin is set to "L" level, the self-refresh mode is selected and no external refresh control is required. If the $\overline{\text{RS/A}}$ pin is set to "H" level, the auto-refresh mode is selected and refresh operation is required to retain memory cell data.

Refresh Clock Input ($\overline{\text{RFSH}}$ (TEST))

Input pin for controlling the external refresh when the auto refresh mode is selected.

When the auto-refresh mode is selected, 1024 refresh operations are required within 100ms via the $\overline{\text{RFSH}}$ pin while the $\overline{\text{RWCK}}$ is at "H" level.

Fast Access Mode Select ($\overline{\text{FAM}}$ (TEST))

Pin for fast read/write operations.

Fast read/write is possible by keeping the $\overline{\text{FAM}}$ pin at "L" level. The fast access mode is set or released by inputting "L" level or "H" level to the $\overline{\text{FAM}}$ pin when the $\overline{\text{RWCK}}$ pin is at "L" level, and when t_{FG} and t_{GS} are satisfied.

When 1024-word data access is complete, be sure to insert a normal cycle in order to increment or decrement the X address.

When the fast access mode is set, the address increment/decrement switching with the AU/D pin is not available.

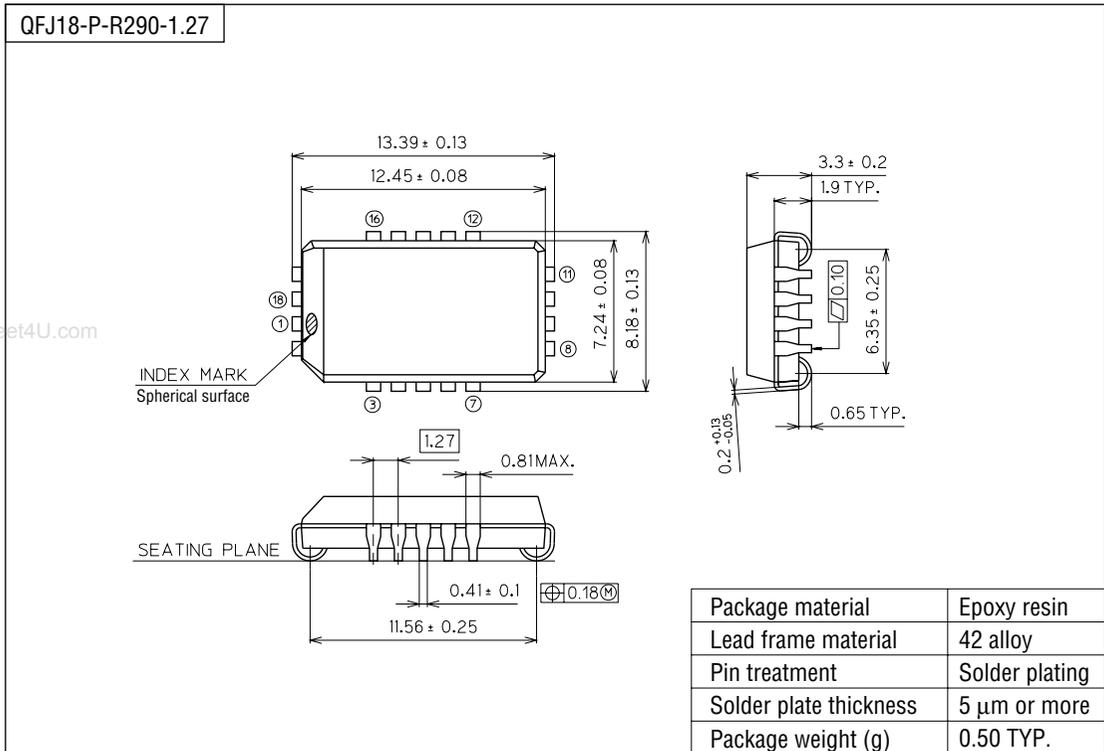
Test (TEST, $\overline{\text{TEST}}$)

The TEST pin is fixed to "L" level.

The $\overline{\text{TEST}}$ pin is fixed to "H" level.

PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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