3-Channel 25mA Linear LED Driver

Features

- ±6% current accuracy @ 4.0 -15V
- 90V standoff voltage
- Separate enable pins for each channel allow for PWM dimming
- Over-temperature protection
- 8-Lead SOIC (w/Heat Slug) package

Applications

- LCD backlighting
- Indicator lamps

General Description

The CL325 is designed to drive 3 strings of LEDs at a constant current of 25mA.

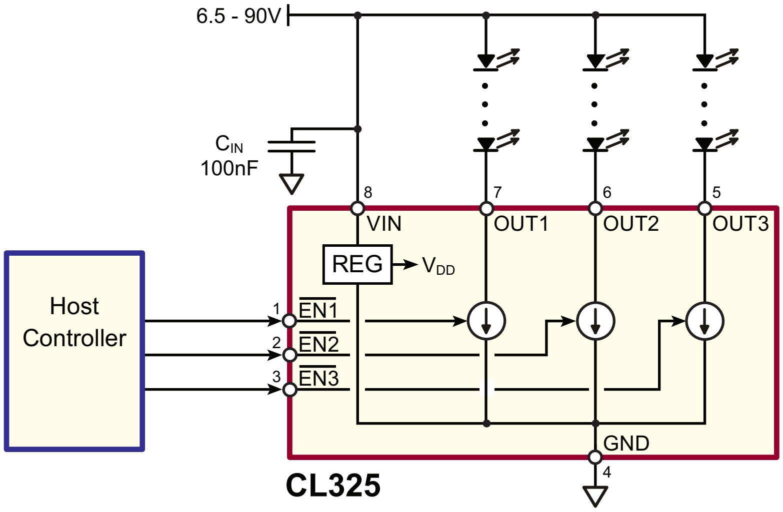
Other drivers with currents in the range of 20 - 30mA are available. The drive current is fixed, with a ±6% tolerance over a V_{OUT} range of 4 - 15V.

Separate enable pins for each channel allow for PWM dimming, 3-step linear dimming, or individual disconnection of faulty LED strings.

Over-temperature protection circuitry shuts down all 3 channels when the nominal die temperature reaches 135°C. Normal operation resumes when the die temperature drops by 30°C.

The CL325 is available in the 8-Lead SOIC (w/Heat Slug) package and requires a single ceramic bypass capacitor which may be shared among several drivers.

Block Diagram and Typical Application Circuit

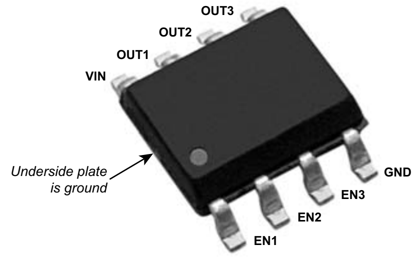


Ordering Information

Device	8-Lead SOIC (w/Heat Slug)
CL325	CL325SG-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



8-Lead SOIC (w/Heat Slug) (SG)

Absolute Maximum Ratings

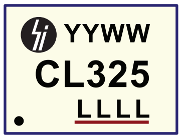
Parameter	Value
Supply voltage, V_{IN}	-0.5V to +100V
Output voltage, V_{OUT}	-0.5V to +100V
Enable voltage, V_{EN}	-0.5V to +6.5V
Operating temperature(1)	-40°C
Storage temperature	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Note:

(1) Maximum junction temperature internally limited.

Product Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
______ = "Green" Packaging

8-Lead SOIC (w/Heat Slug) (SG)

Recommended Operating Conditions *(all voltages with respect to GND pin)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IN}	Supply voltage	6.5	-	90	V	---
V_{OUT}	Output voltage	4.0	-	15	V	$\overline{EN} = 0$
				90	V	$\overline{EN} = 1$
f_{EN}	Enable toggling frequency	0	-	100	kHz	---
T_J	Junction temperature	-40	-	119	°C	---
C_{IN}	V_{IN} capacitor	-	100	-	nF	---

Thermal Characteristics

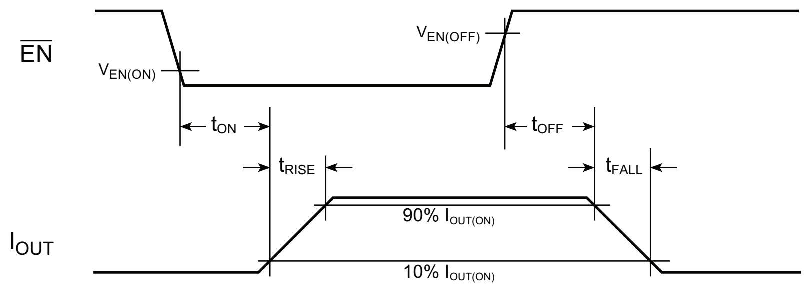
Sym	Parameter	Min	Typ	Max	Units	Conditions
θ_{JA}	Thermal resistance, junction to ambient	-	48	-	°C/W	Mounted on JEDEC test PCB (2s 2p)
T_{LIM}	Over-temperature limit	120	135	150	°C	---
T_{HYS}	Over-temperature hysteresis	-	30	-	°C	---

Electrical Characteristics

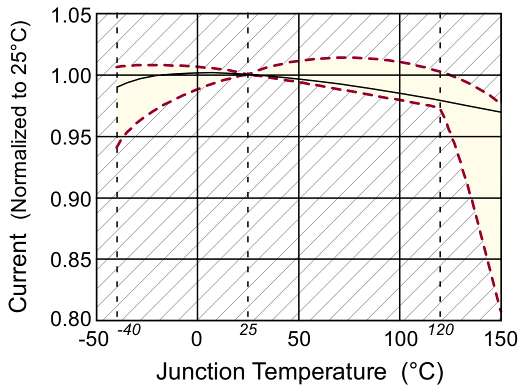
(Over recommended operating conditions. T_J @ 25°C unless otherwise specified.)

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{IN}	V_{IN} supply current	-	220	250	μA	$\overline{EN}_{1-3} = 1$
		-	2.2	2.3	mA	$\overline{EN}_{1-3} = 0$
$I_{OUT(OFF)}$	Output current, off	-	4.0	10	μA	$\overline{EN}_X = 1$
$I_{OUT(ON)}$	Output current, on	-	-	26.5	mA	$\overline{EN}_X = 0$, $V_{OUT} = 0 - 4.0V$
		23.5	25.0	26.5		$\overline{EN}_X = 0$, $V_{OUT} = 4.0 - 15V$
		22.5	25.0	27.5		$\overline{EN}_X = 0$, $V_{OUT} = 15 - 90V$
$V_{EN(ON)}$	Enable voltage, on	-	-	0.8	V	---
$V_{EN(OFF)}$	Enable voltage, off	2.4	-	-	V	---
C_{EN}	Enable input capacitance	-	5.0	10	pF	---
I_{ENL}	Enable low input current	-	-	1.0	μA	$V_{EN} = 0V$
I_{ENH}	Enable high input current	-	-	1.0	μA	$V_{EN} = 5.0V$
t_{ON}	Enable on delay	-	2.0	2.4	μs	---
t_{RISE}	Output current rise time	-	1.0	1.2	μs	---
t_{OFF}	Enable off delay	-	440	800	ns	---
t_{FALL}	Output current fall time	-	170	250	ns	---

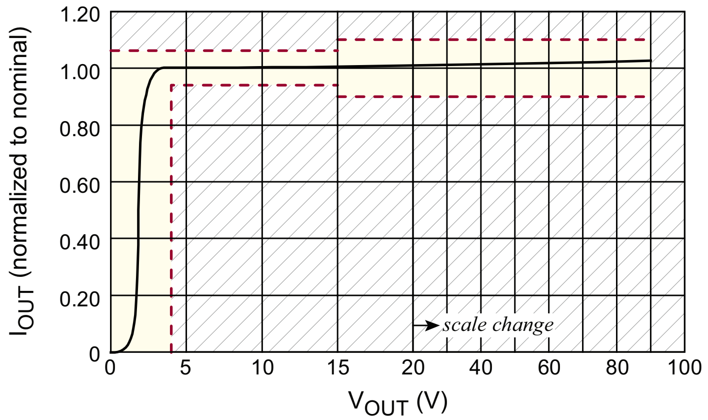
Timing



Temperature Effects



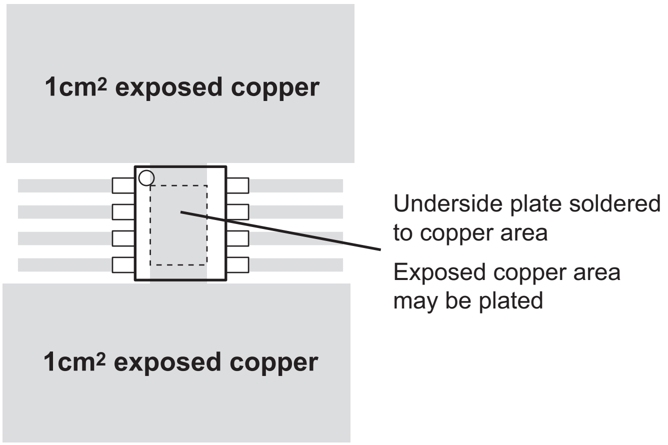
Load Regulation



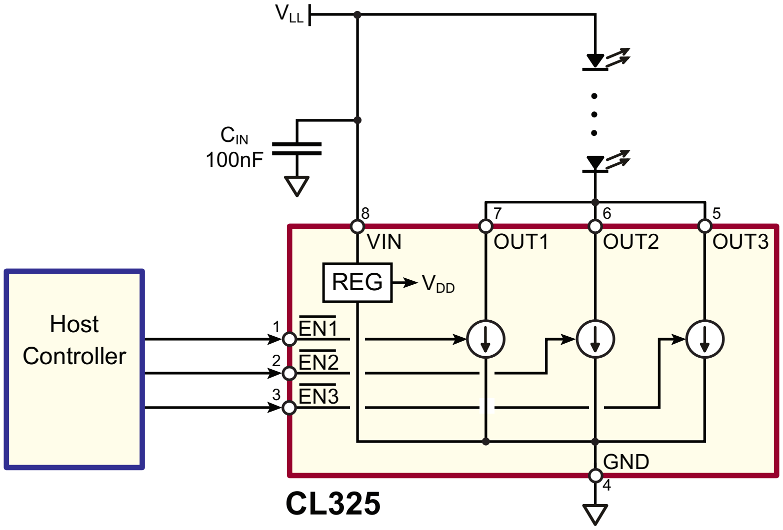
Pin Description

Pin #	Name	Description
1,2,3	$\overline{\text{EN}}1$, $\overline{\text{EN}}2$, $\overline{\text{EN}}3$	Output enable, active low.
4	GND	Circuit common.
5,6,7	OUT1, OUT2, OUT3	Constant current output (sinking). Connect the cathodes of the LEDs to these pins.
8	VIN	Supply voltage. 6.5V to 90V. Bypass locally with a 100nF capacitor to ground.
Underside Plate	GND	The exposed underside plate is internally connected to the GND pin. The plate may either be left floating or connected to ground. Solder the plate to an exposed copper area on the PCB for heatsinking purposes (see recommended layout).

Recommended PCB Layout

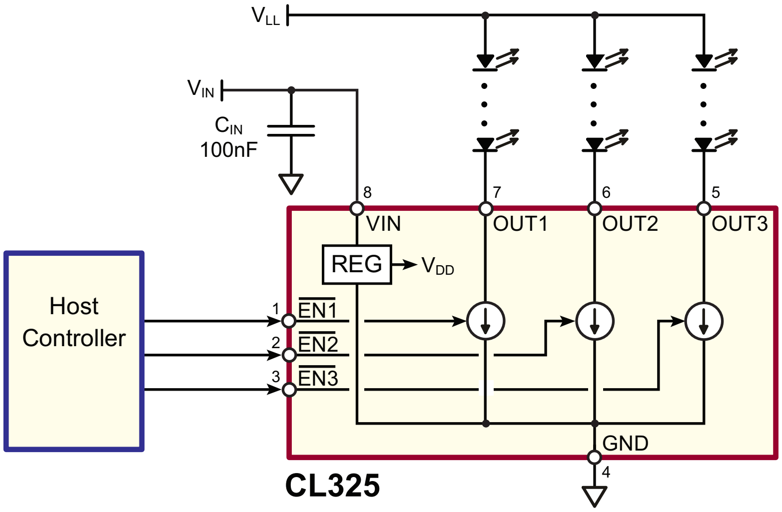


Higher LED Current



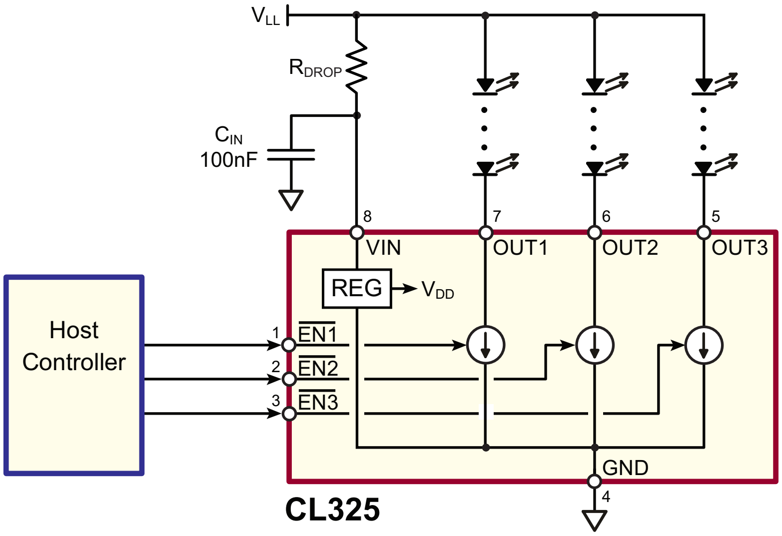
By paralleling outputs, higher LED currents can be achieved. In addition, linear dimming in 3 discrete steps may be obtained by enabling 1, 2, or 3 outputs.

Lowering CL325 Power Dissipation: Separate V_{IN} Supply



CL325 power dissipation may be lowered by supplying the CL325 from a voltage source (V_{IN}) that is lower in voltage than the LED supply (V_{LL}).

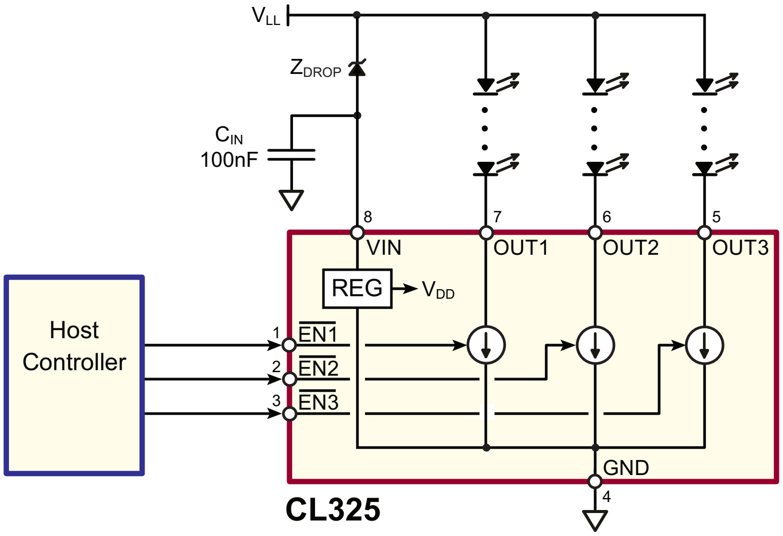
Lowering CL325 Power Dissipation: Dropping Resistor



$$R_{DROP} < \frac{V_{LL(MIN)} - 6.5V}{2.3mA}$$

where: R_{DROP} *= Dropping resistance*
$V_{LL(MIN)}$ *= minimum supply voltage*

Lowering CL325 Power Dissipation: Zener Diode

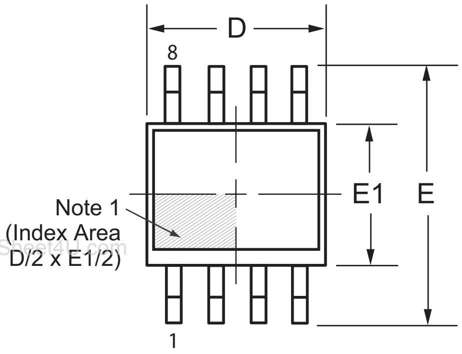


$$V_Z < (V_{LL(MIN)} - 6.5V)$$

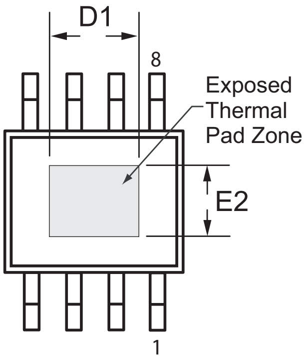
where: V_Z *= Zener Voltage*
$V_{LL(MIN)}$ *= minimum supply voltage*

8-Lead SOIC (w/Heat Slug) Package Outline (SG)

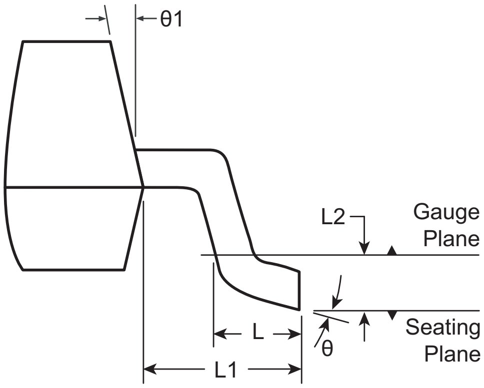
4.90x3.90mm body, 1.70mm height (max), 1.27mm pitch



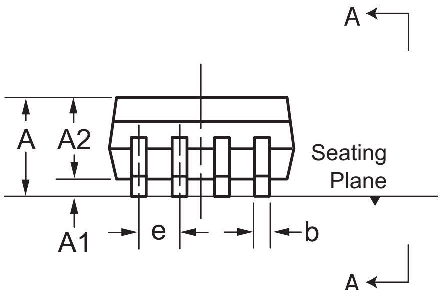
Top View



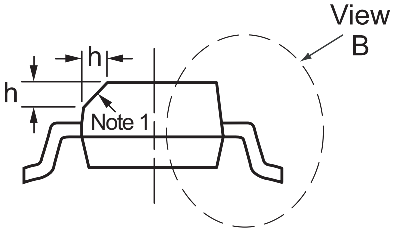
Bottom View



View B



Side View



View A-A

Note 1:
This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	D1	E	E1	E2	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.25	0.00	1.25	0.31	4.80	3.30*	5.80	3.80	2.29*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	-	6.00	3.90	-		-	-			-	-
	MAX	1.70	0.15	1.70	0.51	5.00	3.81*	6.20	4.00	2.79*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation BA, Issue E, Sept. 2005.
Dimensions marked with (*) are non-JEDEC dimensions.
Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)