

ALi M3328C DVB-S Solution

CB-M3328c-TC-01V01

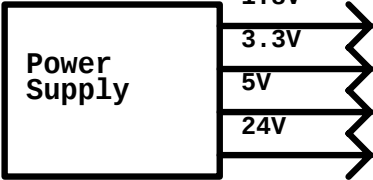
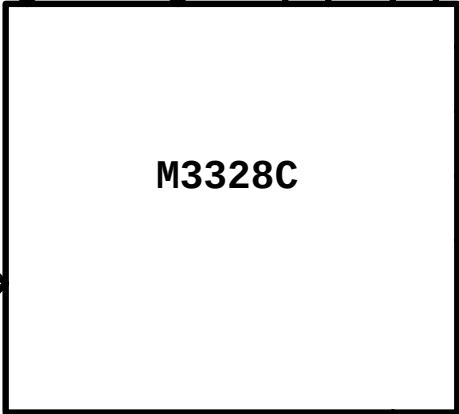
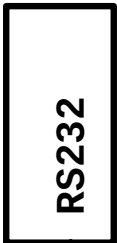
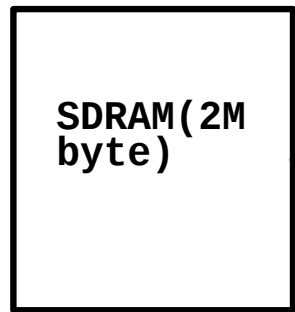
Change List:

ITEM	Change	DATE	BY
1	Created CB-M3328C-TC-01V01	2005-06-10	qinhe
2	Changed some GPIO of panel.	2005-06-20	Tom
3	Changed DiSEqC Control Circuit	2005-06-20	Tom
4	Add a FLASH as 39LV040	2005-07-6	Tom

GPIO MAPPING:

Number	USAGE	USAGE DETAIL	NOTE
GPIO0	F_LOCK	PANEL LOCK LED(0:LIGHT)	
GPIO2	F_KEY2	PANEL KEY DETECT 2	NEED PULL HIGH
GPIO3	F_KEY1	PANEL KEY DETECT 1	NEED PULL HIGH
GPIO4	F_CLOCK	PANEL CLOCK	
GPIO5	F_DATA	PANEL DATA	
GPIO8	F_COM1	PANEL COM1	NEED PULL HIGH
GPIO9	F_COM2	PANEL COM2	NEED PULL HIGH
GPIO17	F_COM3	PANEL COM3	NEED PULL HIGH
GPIO18	LNB_CUT	LNB POWER CUT(1: OFF)	

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Title Module		
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SDRAM I/F

[4] P_D_DQ[0..15]	← P_D_DQ[0..15]
[4,6] P_D_ADDR[0..10]	← P_D_ADDR[0..10]
[4] P_D_DQM0	← P_D_DQM0
[4] P_D_BADDR0	← P_D_BADDR0
[4] P_D_CS0	← P_D_CS0
[4] P_D_CAS1	← P_D_CAS1
[4] P_D_RAS1	← P_D_RAS1
[4] P_D_WE1	← P_D_WE1
[4] P_D_CLK	← P_D_CLK

FLASH I/F

[4]	ROM_AD[0..18]	ROM_AD[0..18]
[4]	ROM_DA[0..7]	ROM_DA[0..7]
[4,6]	ROM_OE $\overline{\text{J}}$	ROM_OE $\overline{\text{J}}$
[4]	ROM_WE $\overline{\text{J}}$	ROM_WE $\overline{\text{J}}$

EJTAG I/F	
[4]	TRSTJ
[4]	TDI
[4]	TDO
[4]	TMS
[4]	TCK

RESET CIRCUIT

5VDC

R3 330R

D1 1N4148

TC9 10uF/16V

R6 3K

Q1 2N3906

R7 1K

R5 10K

D2 4.3V(ZENER Diode)

CPURSTJ

2N3906 (SOT-23)

PNP

1 B E 2

3 C



The schematic shows two power supply rails: RXADC_VDD and RXADC_VDDA. Both are connected to VDD033. The RXADC_VDD rail includes a series resistor R1 and a parallel combination of capacitor C1 (10µF/16V) and inductor L1. The RXADC_VDDA rail includes a series resistor R2 and a parallel combination of capacitors C2 (10µF/16V) and C3 (0.01µF). A common ground connection is shown at the bottom.

Audio-DAC

The schematic diagram illustrates the Audio-DAC circuit. It features a VDD33 supply connected to an L3 inductor, which is connected to a BEAD. The BEAD is connected to the ADAC_VDD pin of the ADAC chip. The ADAC chip has a TC5 capacitor (33uF/16V) connected to its ADAC_VDD pin and a TC12 capacitor (0.1uF) connected to its ADAC_VDD pin. The ADAC chip is connected to a 20K resistor R1, which is connected to the A_IREF pin. The A_IREF pin is connected to the A_V15R pin (TC3), the A_V15L pin (TC4), and the ANA_TST pin (TC6). All these pins are connected to a common A-GND point.

[illegible]

The diagram shows a PLLAVSS decoupling circuit. A red line represents the PLLAVSS signal path. It starts from a terminal labeled 'PLLAVSS' at the bottom, goes up to a capacitor labeled '10uF/16V' with 'TCB' above it. From the top of this capacitor, the path goes left through a 1.5 ohm resistor labeled 'BEAD' to a terminal labeled 'VDD33'. From the junction between the capacitor and the bead, the path continues right through a 50nH inductor labeled 'L6' to a terminal labeled 'DVDD'. From 'DVDD', the path goes up to a capacitor labeled '0.1uF' with 'BC15' above it. From the top of this capacitor, the path goes left through a 1 ohm resistor labeled 'R1' to a terminal labeled 'PLLAVSS' at the top.

TUNER I/F		PERIPHERAL		
		IC-SCK	IC-SCK	[6]
		IC-DA	IC-DA	[6]
DISEQC_HV	DISEQC_HV			
DISEQC_OUT	DISEQC_OUT	RXD	RXD	[4]
		TXD	TXD	[4]
XAGC	XAGC			
GPIO18	UNB_CUT			

IIC-SCK	≡	IIC-SCK	[6]
IIC-DA	≡	IIC-DA	[6]
RXD	≡	RXD	[4]
TXD	≡	TXD	[4]

Crystal

X27OUT

R8 1M

Y1 27MHZ

C6 27pF

C7 27pF

X27IN

PLLAVSS

AV I/F

AUDIO_DR

AUDIO_DL

VIDEOA0

VIDEOA1

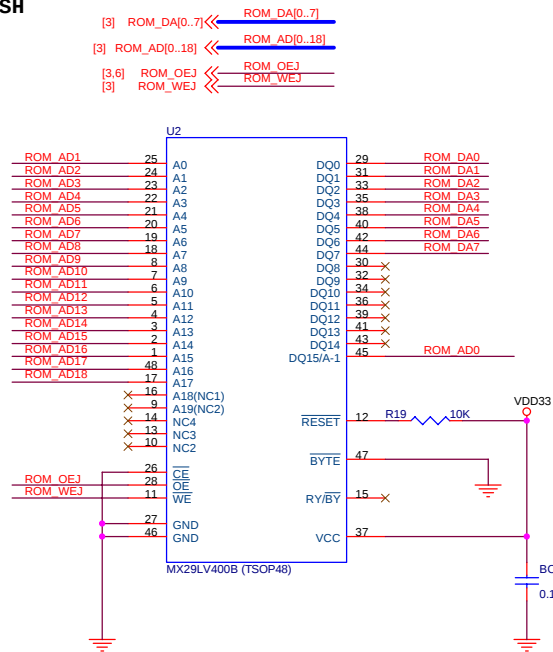
VIDEOA2

VIDEOA3

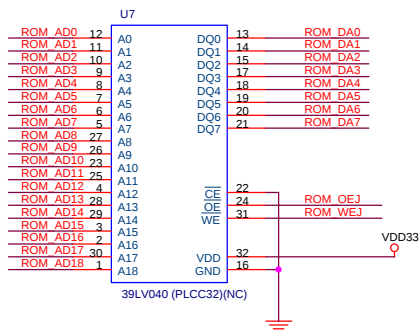
AUDIO_DR << AUDIO_DR [5]
 AUDIO_DL << AUDIO_DL [5]

VIDEOA0 << VIDEOA0 [5]
 VIDEOA1 << VIDEOA1 [5]
 VIDEOA2 << VIDEOA2 [5]
 VIDEOA3 << VIDEOA3 [5]

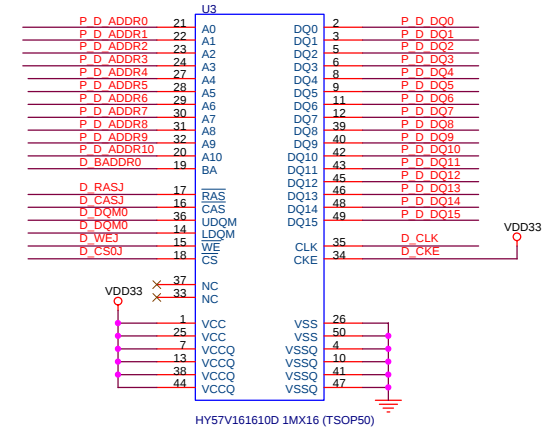
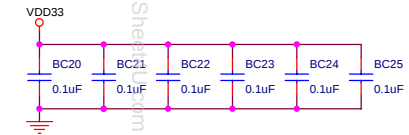
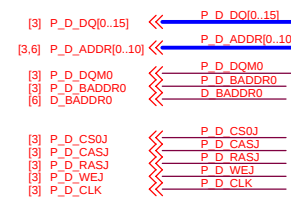
FLASH



OPTIONAL

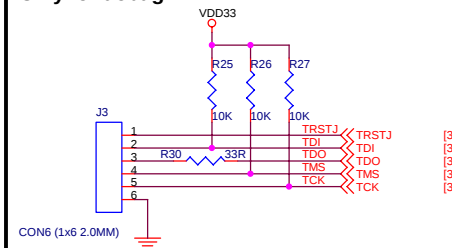


SDRAM

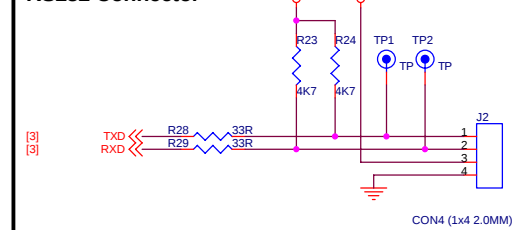


EJTAG Connector

Only for debug

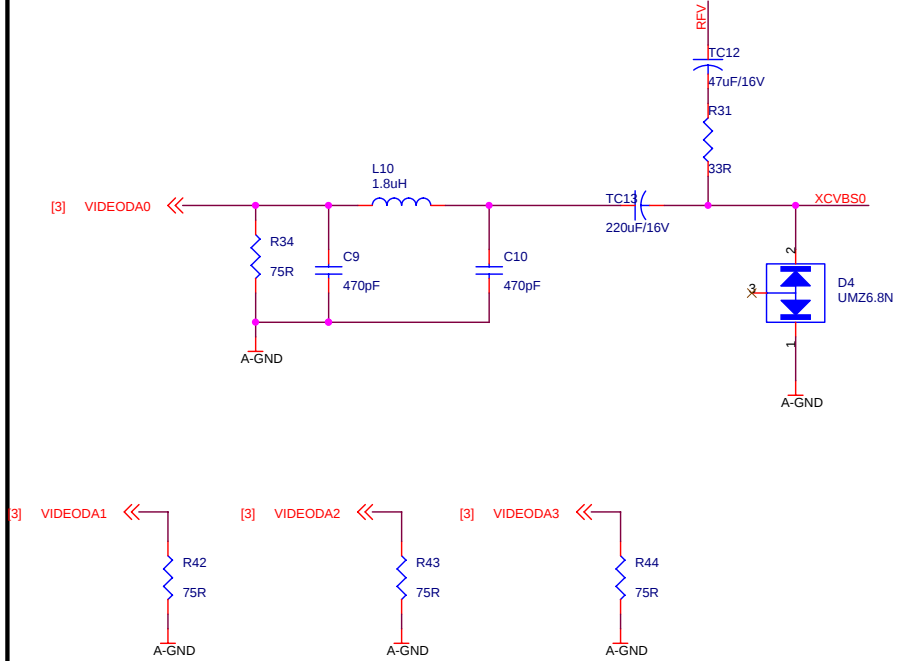


RS232 Connector

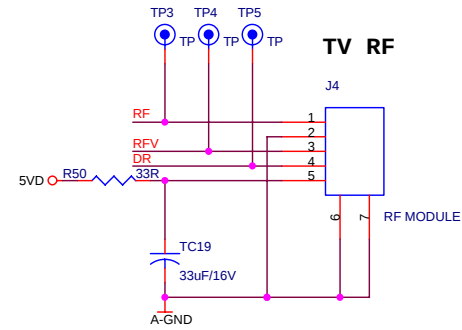
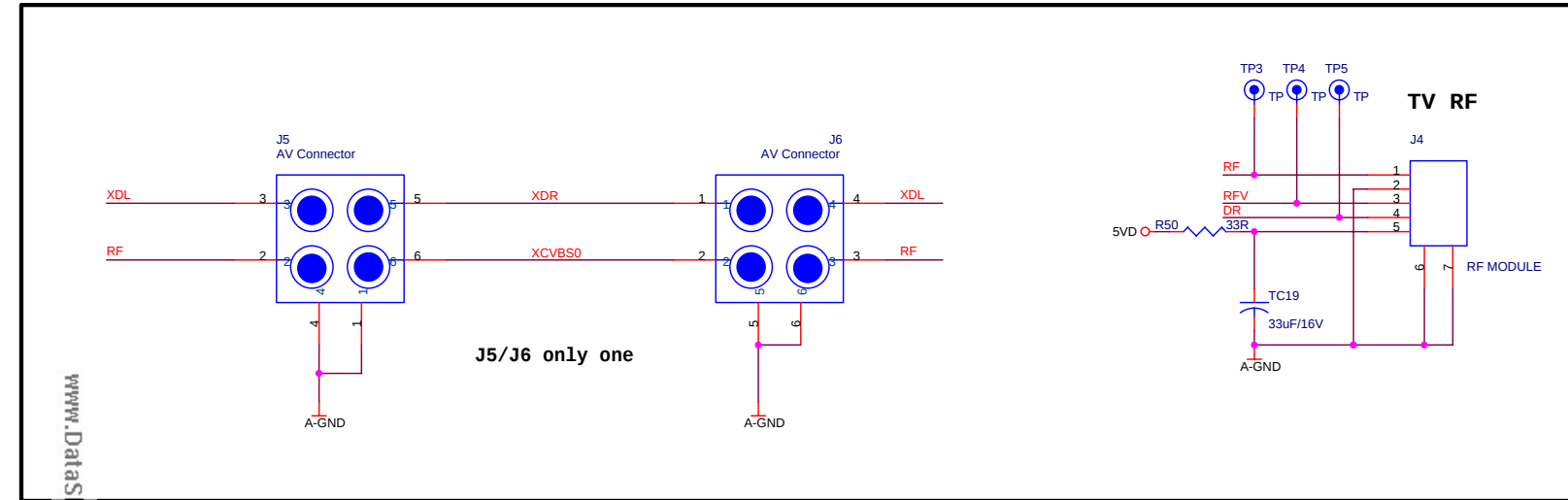
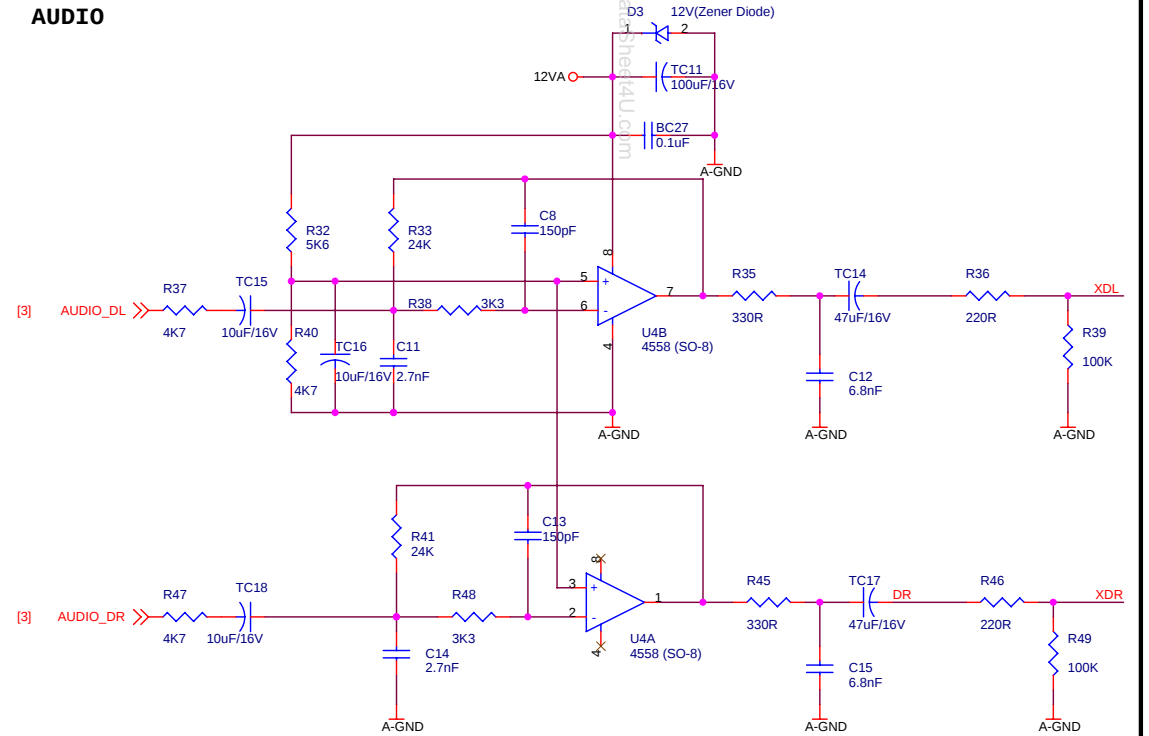


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VIDEO

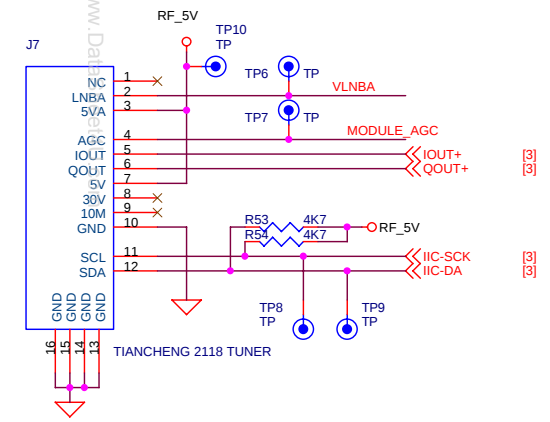
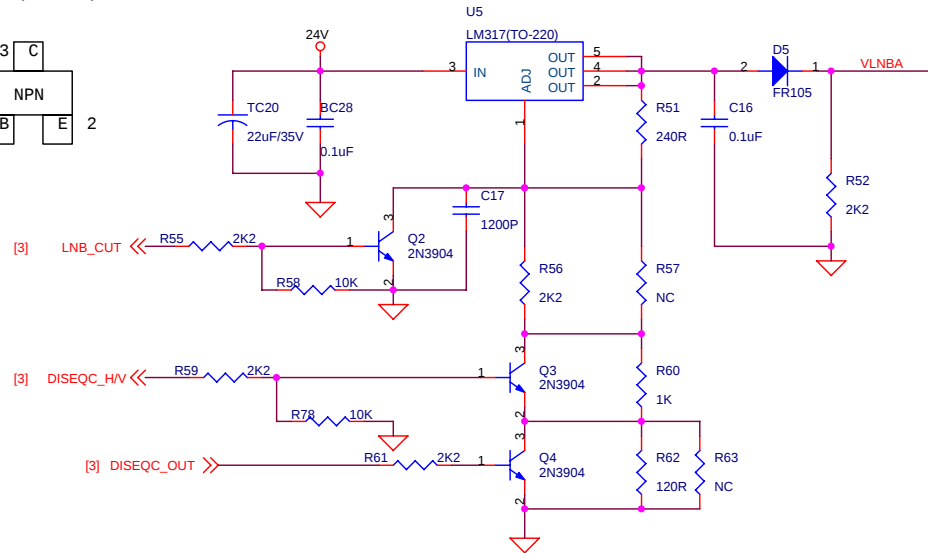
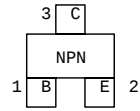


AUDIO



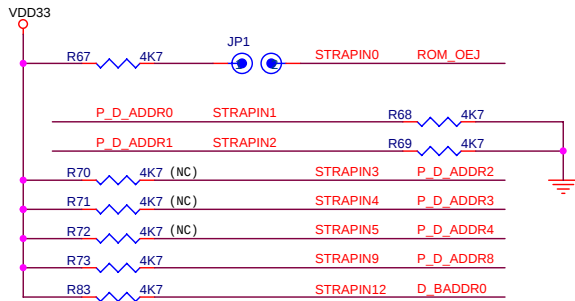
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2N3904(SOT-23)



M3328c Hardware Config

P_D_ADDR0,101 << P_D_ADDR[0..10] [3,4]
D_BADDR0 >> D_BADDR0 [4]
ROM_OEJ << ROM_OEJ [3,4]



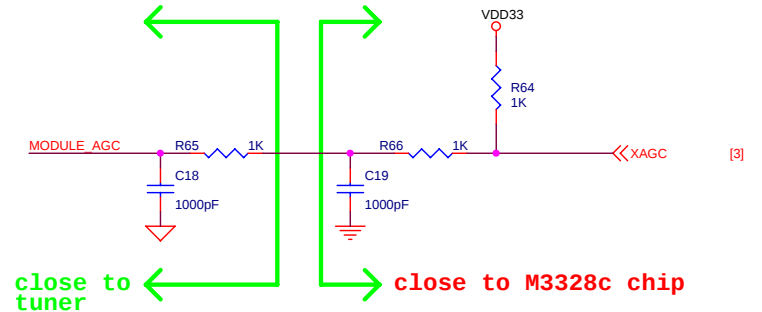
1. CPU_PROBE_EN
STRAPIN[0]: ROM_OEJ
0: Disable(DEFAULT)
1: Enable

2. CPU_PLL_M
STRAPIN[3:1]: P_D_ADDR[2..0]
011: 216M (DEFAULT)
100: 180M
101: 154M

3. MEM_PLL_M
STRAPIN[6:4]: P_D_ADDR[5..3]
000: 135M (DEFAULT)
001: 120M
010: 98M
011: 108M

4. CHIP_MODE
STRAPIN[11:9]: [P_D_ADDR10:8]
000: Mode0(Flash muxed 8-bit MODE) (DEFAULT)
001: Mode1(Flash and GPIO muxed MODE)

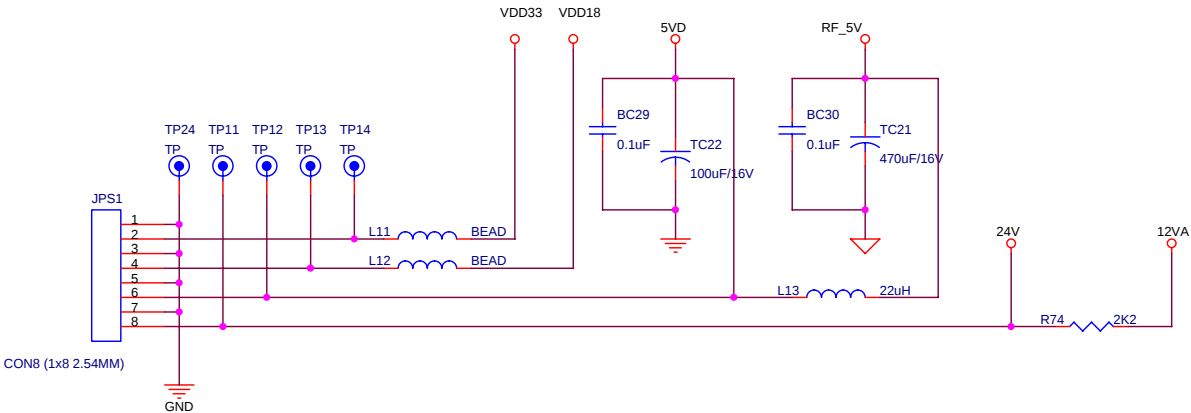
5. CRYSTAL SELECT
STRAPIN[12]: [P_D_BADDR0]
0: 27MHz (DEFAULT)
1: 13.5MHz



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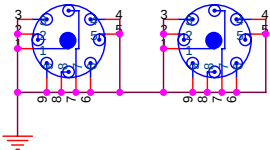
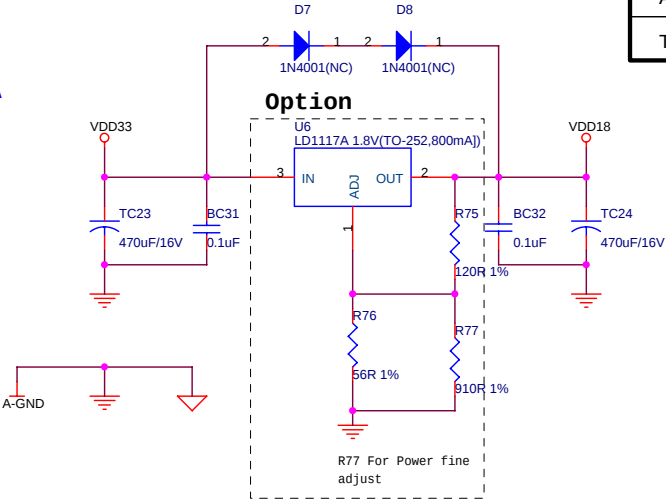
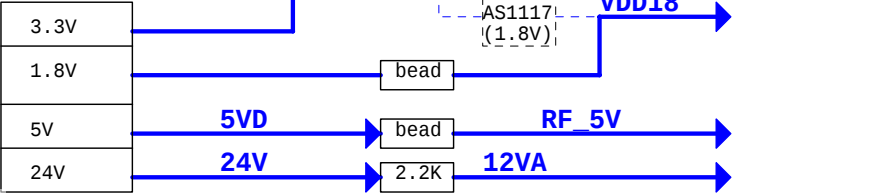
System Board Power Connector



VDD33	M3328C IO PART 3.3V
TVDAC3V3	M3328C VIDEO DAC 3.3V
RXADC_VDD	M3328C QPSK DIGITAL 3.3V
RXADC_VDDA	M3328C QPSK ANALOG 3.3V
VDD18	M3328C CORE 1.8V
5VD	DIGITAL 5V
RF_5V	TUNER POWER 5V
12VA	Audio OP POWER 12V
24V	LNB POWER 24V

GND	Digital GND
A-GND	ANALOG GND
TGND	TUNER RF GND

STB POWER SUPPLY





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POWER		
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