ALi M3328C DVB-S Solution

CB-M3328c-TC-01V01

Change List:

ITEM	Change	DATE	BY
1	Created CB-M3328C-TC-01V01	2005-06-10	qinhe
2	Changed some GPIO of panel.	2005-06-20	Tom
3	Changed DiSEqC Control Circuit	2005-06-20	Tom
4	Add a FLASH as 39LV040	2005-07-6	Tom

GPIO MAPPING:

Number	USAGE	USAGE DETAIL	NOTE
GPIO0	F_LOCK	PANEL LOCK LED(0:LIGHT)	
GPIO2	F_KEY2	PANEL KEY DETECT 2	NEED PULL HIGH
GPIO3	F_KEY1	PANEL KEY DETECT 1	NEED PULL HIGH
GPIO4	F_CLOCK	PANEL CLOCK	
GPIO5	F_DATA	PANEL DATA	
GPIO8	F_COM1	PANEL COM1	NEED PULL HIGH
GPIO9	F_COM2	PANEL COM2	NEED PULL HIGH
GPIO17	F_COM3	PANEL COM3	NEED PULL HIGH
GPIO18	LNB_CUT	LNB POWER CUT(1: OFF)	

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Title: COVER		
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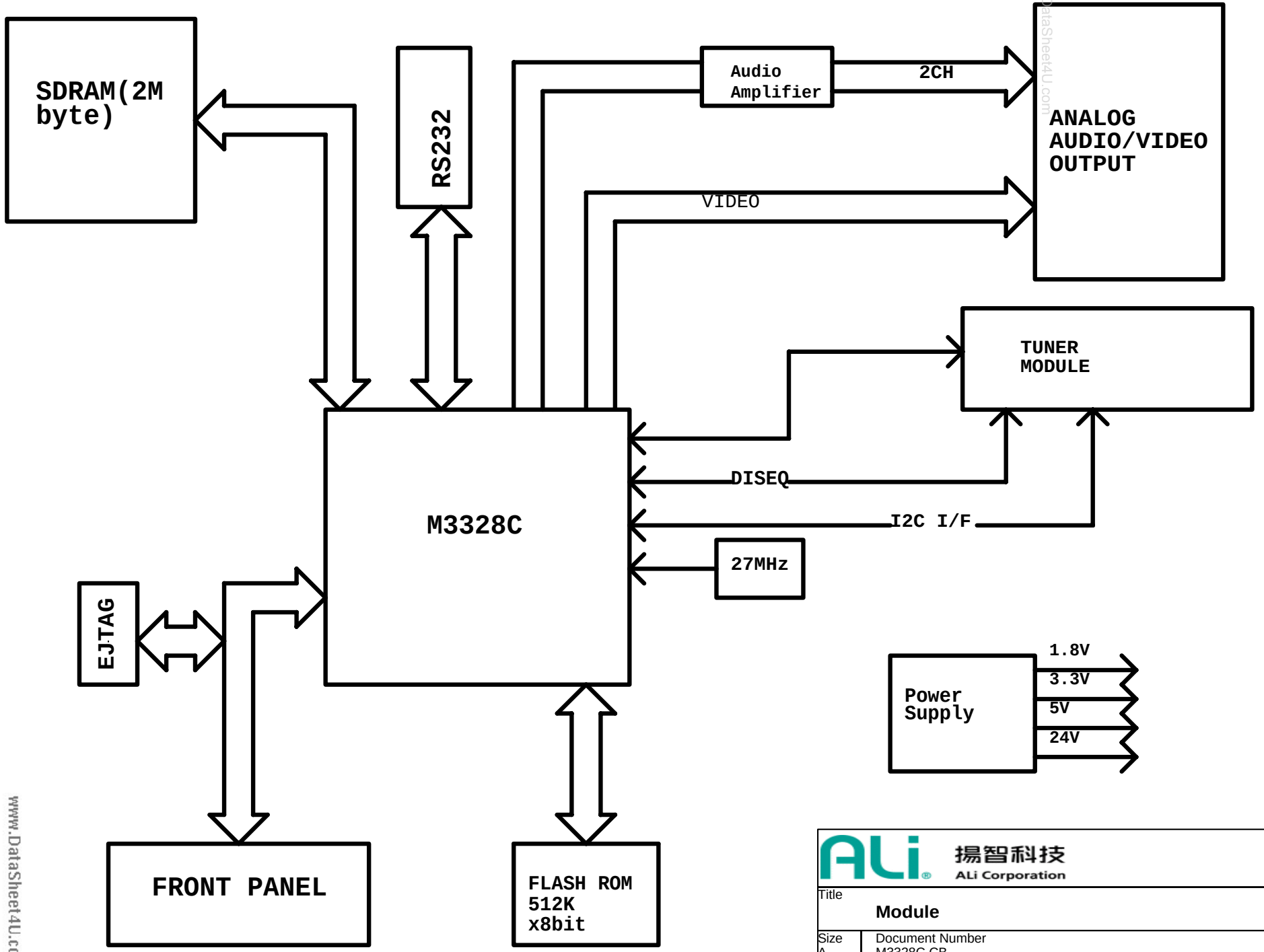

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SDRAM I/F

[4] P_D_DQ[0..15] — P_D_DQ[0..15]
[4,6] P_D_ADDR[0..10] — P_D_ADDR[0..10]
[4] P_D_DQM0 — P_D_DQM0
[4] P_D_BADDR0 — P_D_BADDR0
[4] P_D_CS0J — P_D_CS0J
[4] P_D_CASJ — P_D_CASJ
[4] P_D_RASJ — P_D_RASJ
[4] P_D_WEJ — P_D_WEJ
[4] P_D_CLK — P_D_CLK

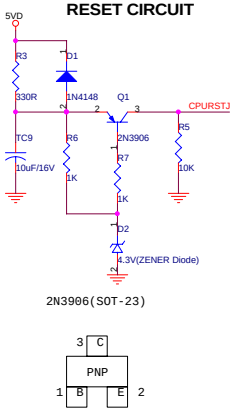
FLASH I/F

[4] ROM_AD[0..18] — ROM_AD[0..18]
[4] ROM_DA[0..7] — ROM_DA[0..7]
[4,6] ROM_OEJ — ROM_OEJ
[4] ROM_WEJ — ROM_WEJ

EJTAG I/F

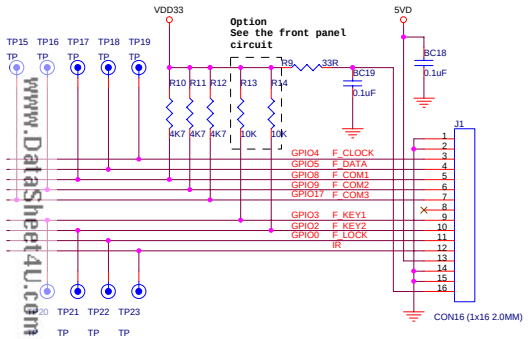
[4] TRSTJ — TRSTJ
[4] TDI — TDI
[4] TDO — TDO
[4] TMS — TMS
[4] TCK — TCK

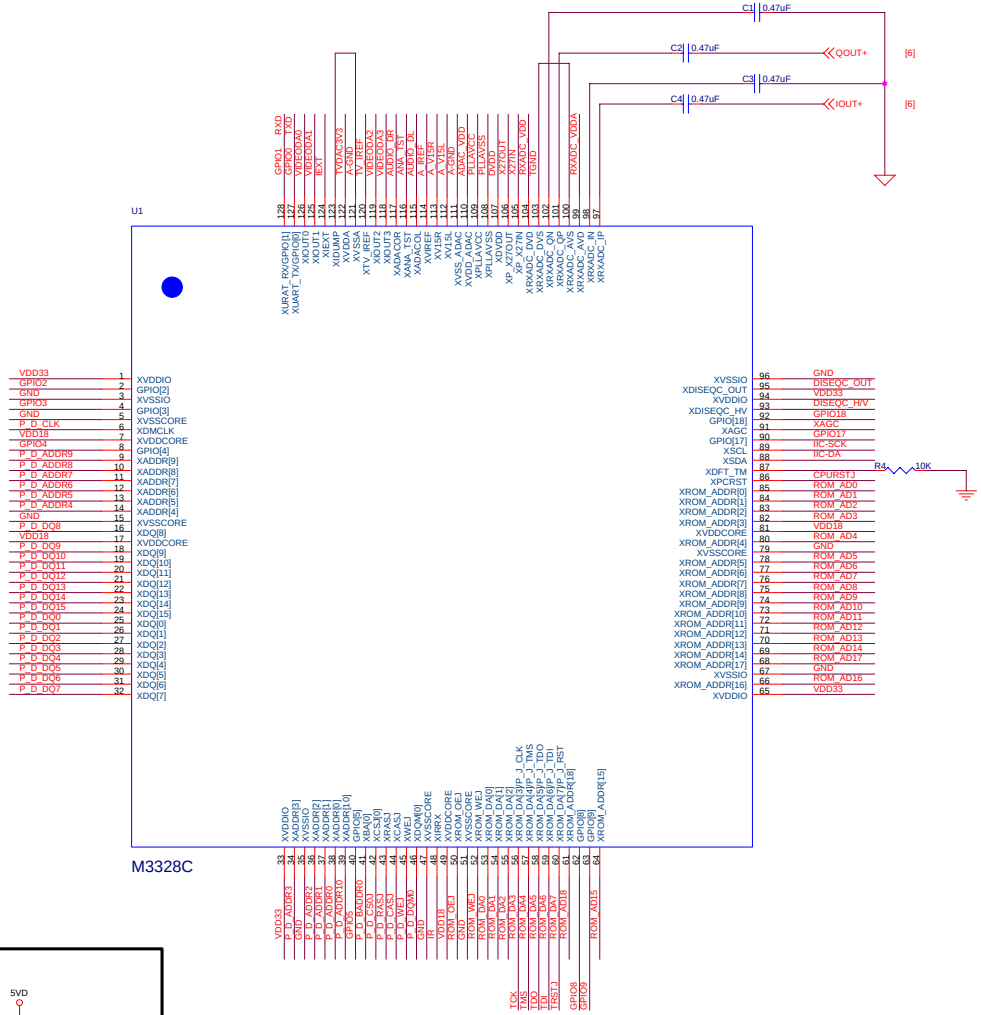
RESET CIRCUIT

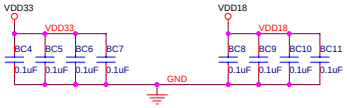


2N3906(SOT-23)

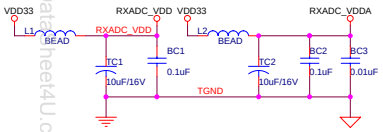
FRONT PANEL I/F



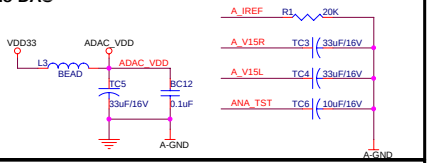




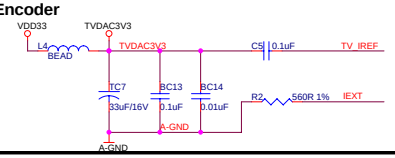
QPSK-ADC



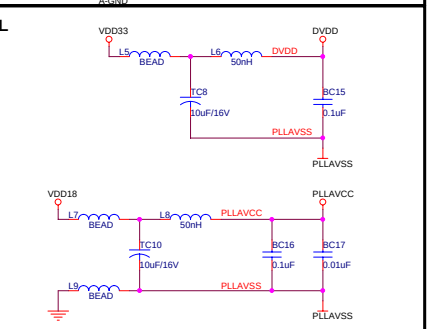
Audio-DAC



TV-Encoder



PLL



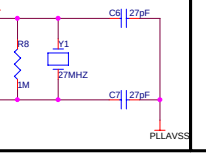
TUNER I/F

DISEQC_H/V — DISEQC_H/V [6]
DISEQC_OUT — DISEQC_OUT [6]
XAGC — XAGC [6]
GPIO18 — LNB_CUT [6]

PERIPHERAL

IIC-SCK — IIC-SCK [6]
IIC-DA — IIC-DA [6]
RXD — RXD [4]
TXD — TXD [4]

Crystal



AV I/F

AUDIO_DR — AUDIO_DR [5]
AUDIO_DL — AUDIO_DL [5]
VIDEODA0 — VIDEODA0 [5]
VIDEODA1 — VIDEODA1 [5]
VIDEODA2 — VIDEODA2 [5]
VIDEODA3 — VIDEODA3 [5]

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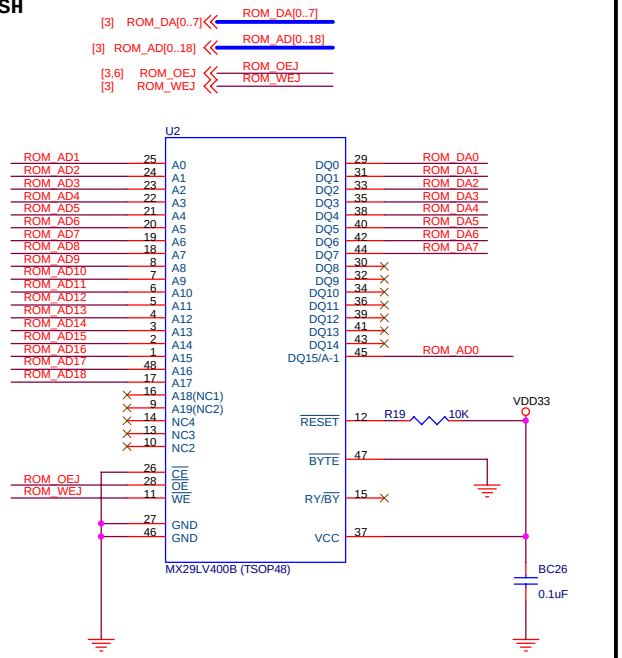
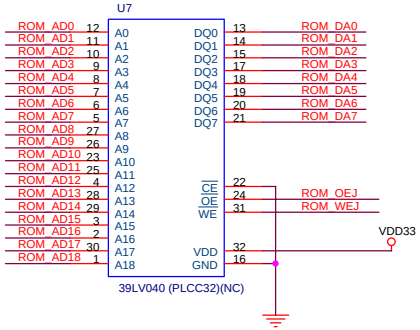
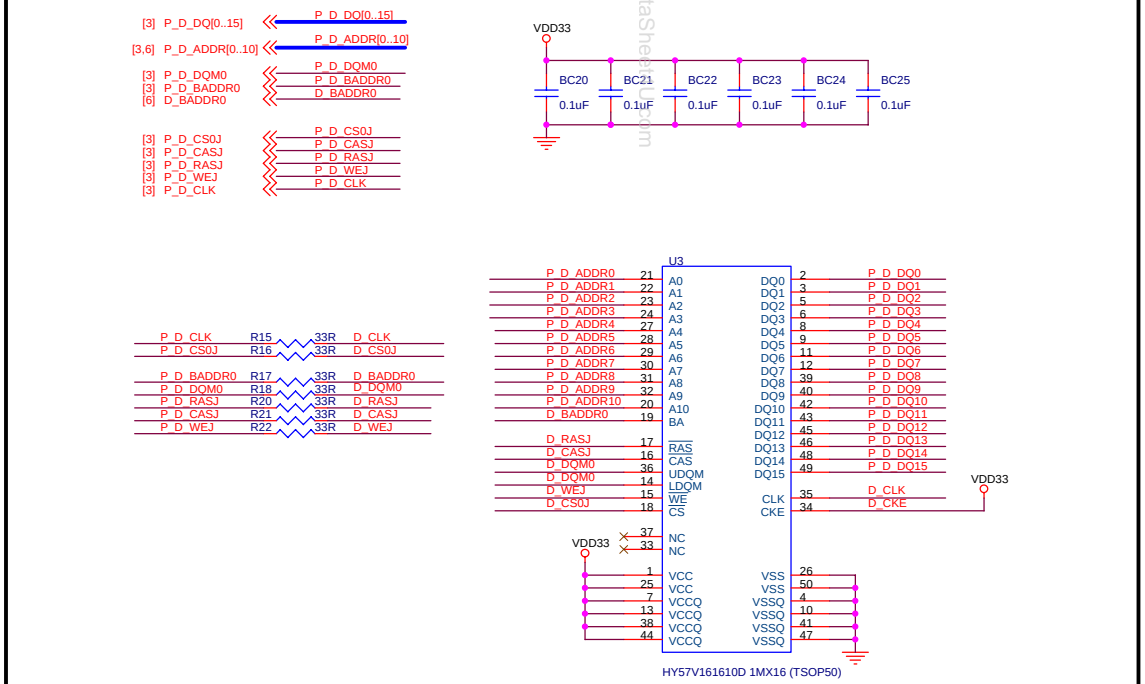
FLASH



OPTIONAL

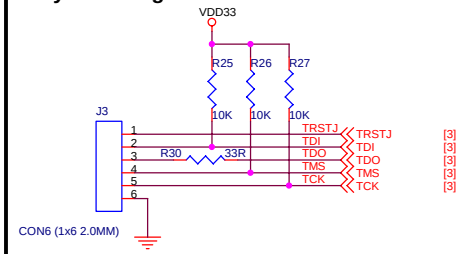


SDRAM

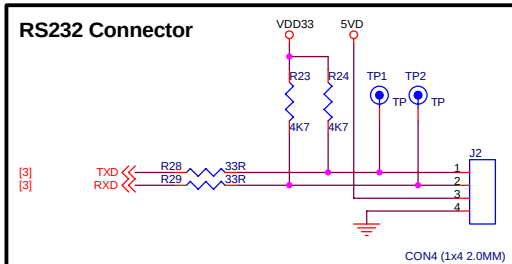


EJTAG Connector

Only for debug



RS232 Connector



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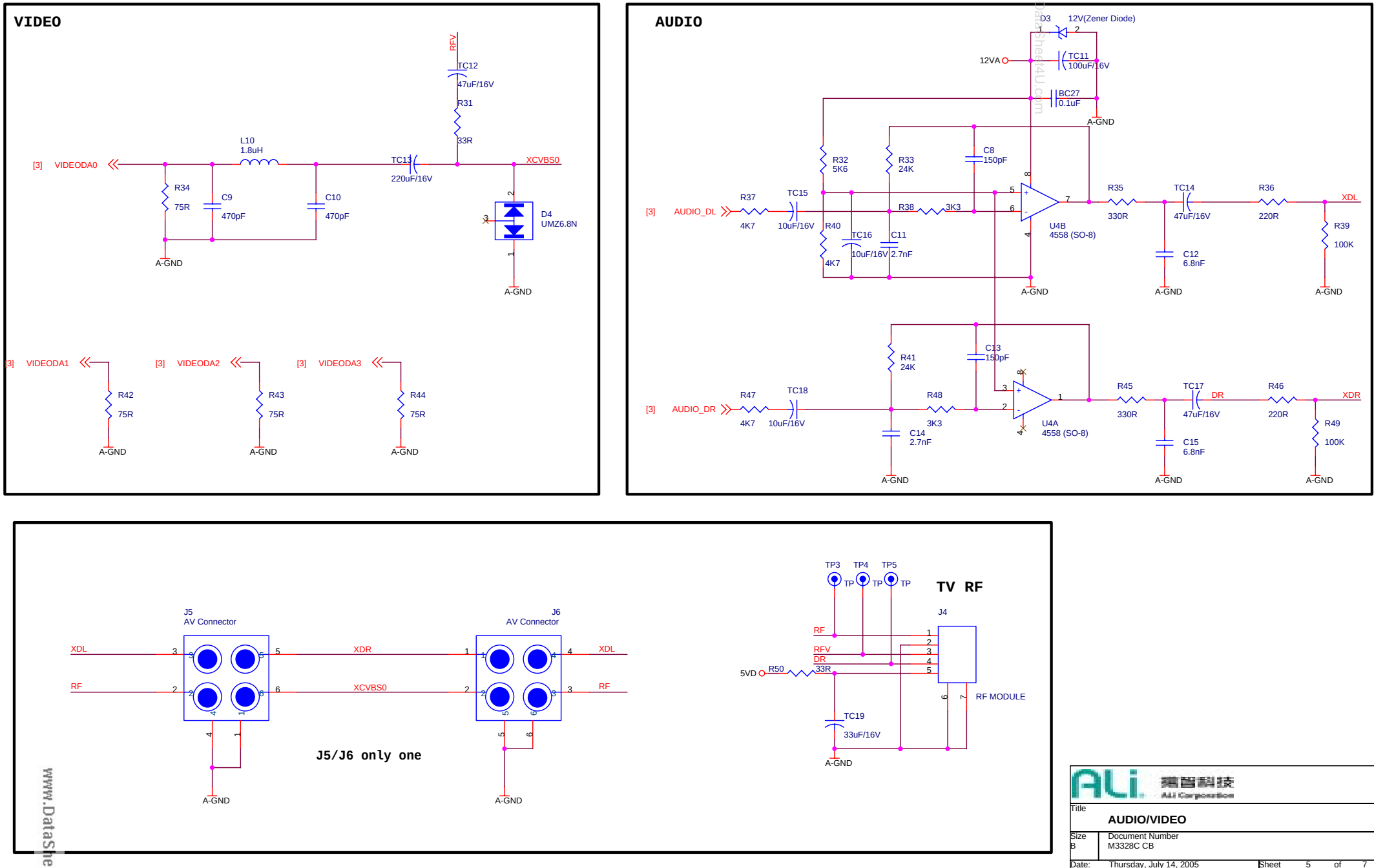

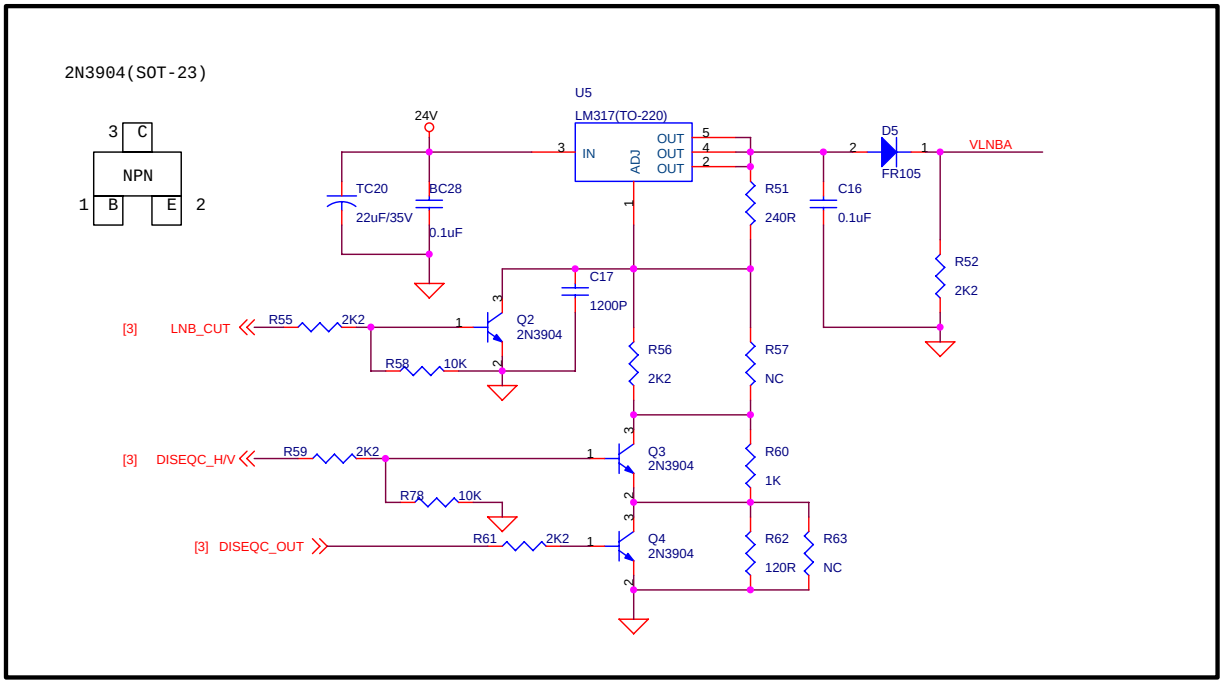

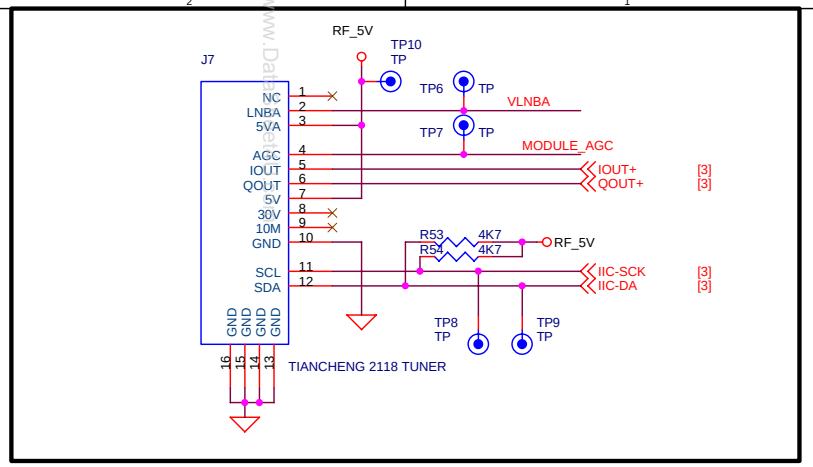

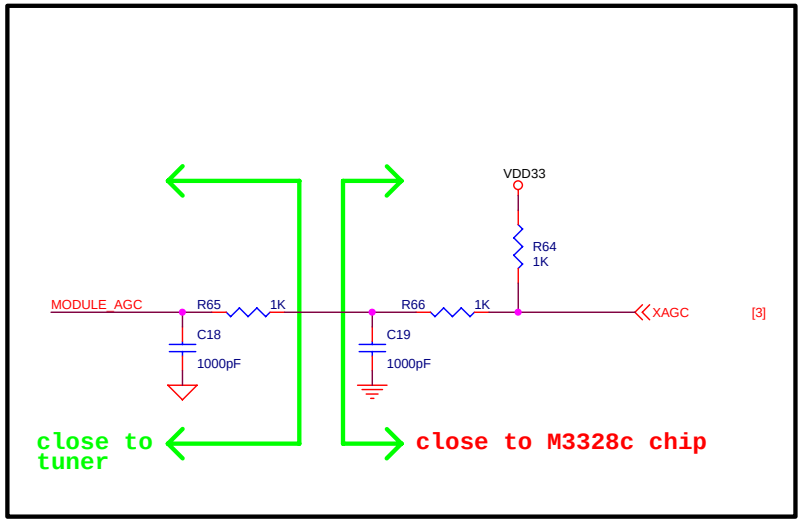

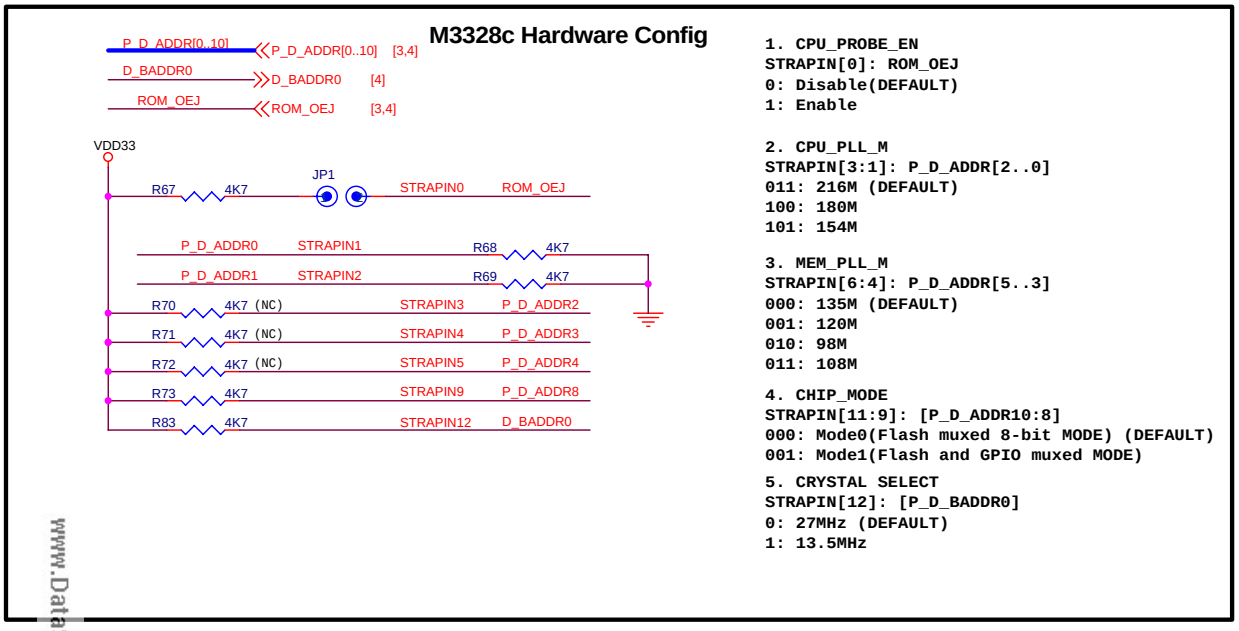

1. CPU_PROBE_EN
STRAPIN[0]: ROM_OEJ
0: Disable(DEFAULT)
1: Enable

2. CPU_PLL_M
STRAPIN[3:1]: P_D_ADDR[2..0]
011: 216M (DEFAULT)
100: 180M
101: 154M

3. MEM_PLL_M
STRAPIN[6:4]: P_D_ADDR[5..3]
000: 135M (DEFAULT)
001: 120M
010: 98M
011: 108M

4. CHIP_MODE
STRAPIN[11:9]: [P_D_ADDR10:8]
000: Mode0(Flash muxed 8-bit MODE) (DEFAULT)
001: Mode1(Flash and GPIO muxed MODE)

5. CRYSTAL SELECT
STRAPIN[12]: [P_D_BADDR0]
0: 27MHz (DEFAULT)
1: 13.5MHz

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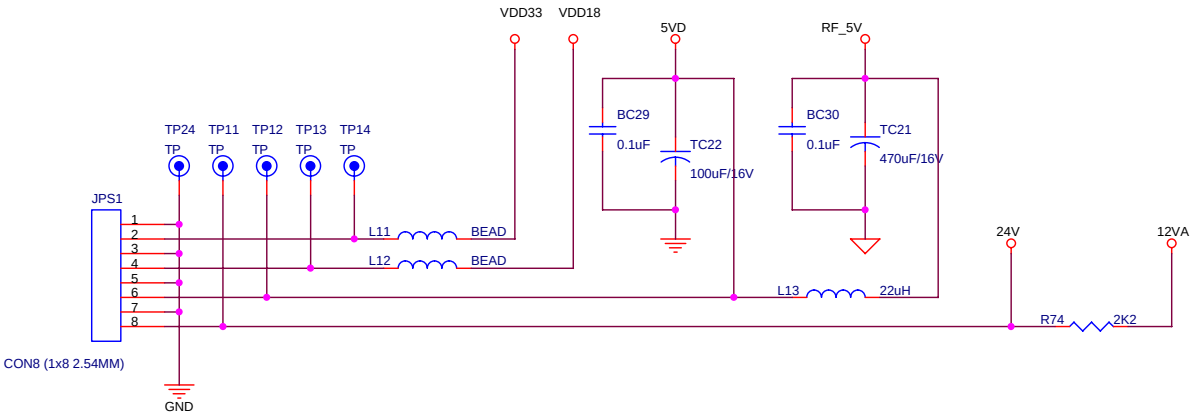
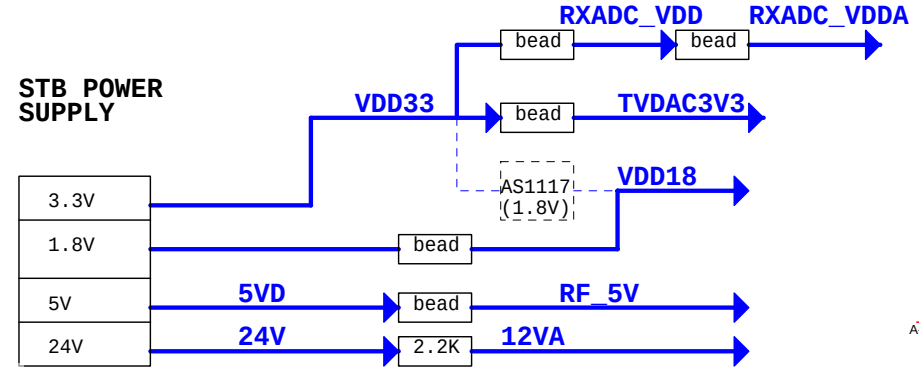
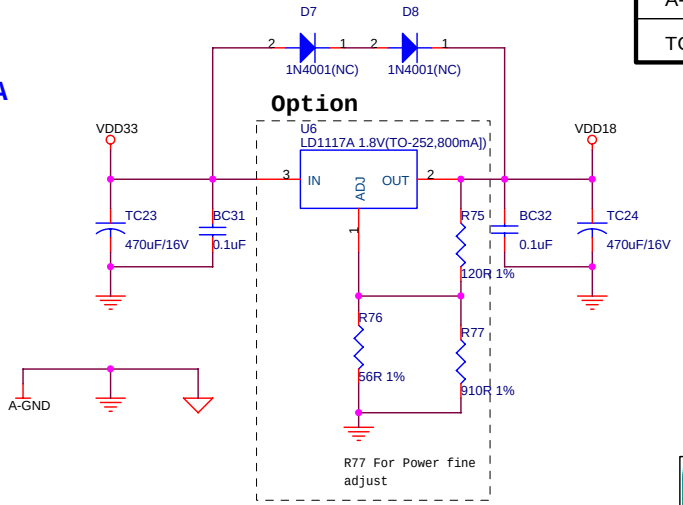
System Board Power Connector

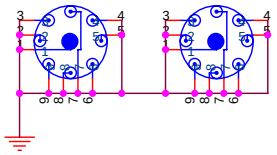


VDD33	M3328C IO PART 3.3V
TVDAC3V3	M3328C VIDEO DAC 3.3V
RXADC_VDD	M3328C QPSK DIGITAL 3.3V
RXADC_VDDA	M3328C QPSK ANALOG 3.3V
VDD18	M3328C CORE 1.8V
5VD	DIGITAL 5V
RF_5V	TUNER POWER 5V
12VA	Audio OP POWER 12V
24V	LNB POWER 24V

GND	Digital GND
A-GND	ANALOG GND
TGND	TUNER RF GND







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