

Revision History

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Revision 1 (Dec. 2001)

1. Fister release.

Revision 2 (Apr. 2002)

1. Changed module current specification.
2. Add Performance range.
3. Changed AC Characteristics.
4. Changed typo size on module PCB in package dimensions.

DDR SDRAM 200pin DIMM

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16Mx64bits DDR SDRAM 200pin SODIMM based on 16Mx8

General Description

The ADECB1608 is 16Mx64 bits Double Data Rate SDRAM Modules, The modules are composed of eight 16Mx8 bits CMOS Double Data Rate SDRAMs in TSOP-II 400mil 66pin package and one 2Kbit EEPROM in 8pin TSSOP(TSOP) package on a 200pin glass-epoxy printed circuit board.

The A-Data is a Dual In-line Memory Module and is intended for mounting onto 200-pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS.

Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- DLL aligns DQ and DQS transition with CK transition
- Double-data-rate architecture.
- Bi-directional data strobe (DQS)
- Differential clock inputs(CK and /CK)
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Power supply: Vdd,Vddq:2.5V±0.2V
- Programmable Burst length (2,4,8)
- Serial Presence Detect with EEPROM
- Module bank : one physical bank
- PCB : SO200RCB,Height (12.5mm),single sided component, Six layers

Performance range

Part No.	Max Freq.	Interface
ADECB1608-75B	133MHz (7.5ns /CL=2.5)	SSTL_2

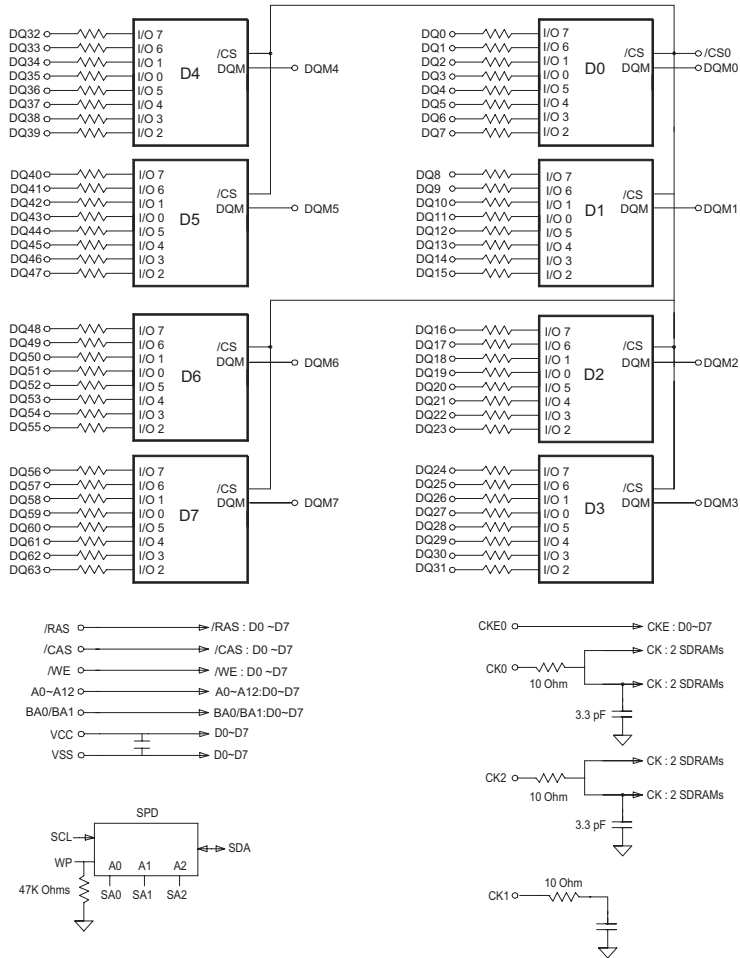
Pin Assignment

FRONT SIDE								BACK SIDE							
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	VREF	26	DM1	51	VSS	76	VSS	101	A9	126	VSS	151	DQ42	176	DQ55
2	VREF	27	VSS	52	VSS	77	DQS8	102	A8	127	DQ32	152	DQ46	177	DQ56
3	VSS	28	VSS	53	DQ19	78	DM8	103	VSS	128	DQ36	153	DQ43	178	DQ60
4	VSS	29	DQ10	54	DQ23	79	CB2	104	VSS	129	DQ33	154	DQ47	179	VDD
5	DQ0	30	DQ14	55	DQ24	80	CB6	105	A7	130	DQ37	155	VDD	180	VDD
6	DQ4	31	DQ11	56	DQ28	81	VDD	106	A6	131	VDD	156	VDD	181	DQ57
7	DQ1	32	DQ15	57	VDD	82	VDD	107	A5	132	VDD	157	VDD	182	DQ61
8	DQ5	33	VDD	58	VDD	83	VBS3	108	A4	133	DQS4	158	/CK1	183	DQS7
9	VDD	34	VDD	59	DQ25	84	CB7	109	A3	134	DM4	159	VSS	184	DM7
10	VDD	35	CK0	60	DQ29	85	DU	110	A2	135	DQ34	160	CK1	185	VSS
11	DQS0	36	VDD	61	DQS3	86	DU	111	A1	136	DQ38	161	VSS	186	VSS
12	DM0	37	/CK0	62	DM3	87	VSS	112	A0	137	VSS	162	VSS	187	DQ58
13	DQ2	38	VSS	63	VSS	88	VSS	113	VDD	138	VSS	163	DQ48	188	DQ62
14	DQ6	39	VSS	64	VSS	89	CK2	114	VDD	139	DQ35	164	DQ52	189	DQ59
15	VSS	40	VSS	65	DQ26	90	VSS	115	A10	140	DQ39	165	DQ49	190	DQ63
16	VSS	41	DQ16	66	DQ30	91	/CK2	116	BA1	141	DQ40	166	DQ53	191	VDD
17	DQ3	42	DQ20	67	DQ27	92	VDD	117	BA0	142	DQ44	167	VDD	192	VDD
18	DQ7	43	DQ17	68	DQ31	93	VDD	118	/RAS	143	VDD	168	VDD	193	SDA
19	DQ8	44	DQ21	69	VDD	94	VDD	119	/WE	144	VDD	169	DQS6	194	SA0
20	DQ12	45	VDD	70	VDD	95	CKE1	120	/CAS	145	DQ41	170	DM6	195	SCL
21	VDD	46	VDD	71	CB0	96	CKE0	121	/S0	146	DQ45	171	DQ50	196	SA1
22	VDD	47	DQS2	72	CB4	97	DU	122	/S1	147	DQS5	172	DQ54	197	VDDS
23	DQ9	48	DM2	73	CB3	98	DU	123	DU	148	DM5	173	VSS	198	SA2
24	DQ13	49	DQ18	74	CB5	99	A12	124	DU	149	VSS	174	VSS	199	VDDI
25	DQS1	50	DQ22	75	VSS	100	A11	125	VSS	150	VSS	175	DQ51	200	DU

Pin Description

PIN	NAME	FUNCTION
CK0~CK2,/CK0~/CK02	System Clock	Active on the positive edge to sample all inputs.
CKE0	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least on cycle prior new command. Disable input buffers for power down in standby
/CS0	Chip Select	Disables or Enables device operation by masking or enabling all input except CK, CKE and L(U)DQM
A0~A11	Address	Row / Column address are multiplexed on the same pins.
BA0~BA1	Banks Select	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
DQ0~DQ63	Data	Data inputs / outputs are multiplexed on the same pins.
DQS0~DQS7	Data Strobe	Bi-directional Data Strobe
DM0~7	Data Mask	Makes data output Hi-Z,
/RAS	Row Address Strobe	Latches row addresses on the positive edge of the CLK with /RAS low
/CAS	Column Address Strobe	Latches Column addresses on the positive edge of the CLK with /CAS low
/WE	Write Enable	Enables write operation and row recharge.
VDD/VSS	Power Supply/Ground	Power and Ground for the input buffers and the core logic.
VDDQ	Power Supply	Power Supply for DQS
VREF	Power Supply reference	Power Supply for reference
VDDS	SPD Power Supply	Serial EEPROM power Supply
SDA	Serial data I/O	EEPROM serial data I/O
SCL	Serial clock	EEPROM clock input
SA0~2	Address in EEPROM	EEPROM address input
VDDID	VDD identification	VDD identification flag
NC	No Connection	This pin is recommended to be left No Connection on the device.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{out}	-0.5~3.6	V
Voltage on VDD supply relative to Vss	V _{DD}	-1.0~3.6	V
Voltage on VDDQ supply relative to Vss	V _{DDQ}	-0.5~3.6	V
Storage temperature	T _{STG}	-55~+150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Condition

Voltage referenced to Vss = 0V, T_A = 0 to 70 °C

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	2.3	2.7	V	
Reference voltage	V _{REF}	V _{DDQ} /2-50mV	V _{DDQ} /2+50mV	V	1
Termination voltage	V _{TT}	V _{REF} -0.04	V _{REF} +0.04		2
Input logic high voltage	V _{IH}	V _{REF} +0.15	V _{DDQ} +0.3	V	3
Input logic low voltage	V _{IL}	-0.3	V _{REF} -0.15	V	3
Output logic high voltage	V _{OH}	V _{TT} +0.84	-	V	I _{OH} =-16.8mA
Output logic low voltage	V _{OL}	-	V _{TT} -0.84	V	I _{OL} =16.8mA
Input voltage Level	V _{IN}	-0.3	V _{DDQ} +0.3	V	
Input Differential Voltage	V _{ID}	0.3	V _{DDQ} +0.6	V	4
Input crossing point voltage	V _{IX}	1.15	1.35	V	5
Input leakage current	I _{IL}	-2	2	uA	
Output leakage current	I _{OL}	-5	5	uA	

Note : 1. Includes ±25mV margin for DC offset on V_{REF}, and a combined total of ±50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤ 3nH.

2.V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}

3.These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHz.

4.V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK.

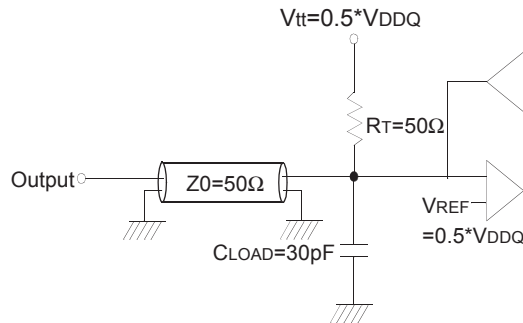
5.The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Capacitance

TA=25°C, VDDQ=2.5V, VDD=2.5V

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CKE0,A0~A11,BA0,BA1,/RAS,/CAS,/WE	CI1	36	44	pF
Input capacitance	/CS0	CI2	34	42	pF
Input capacitance	CLK0~CLK1	CI3	34	38	PF
Data input / output capacitance	DQM	CI4	8	9	pF
Input capacitance	DM0~DM8	CI5	8	9	pF

Output load circuit



Output Load Circuit (SSTL_2)

DC Characteristics II

TA=0 to 70°C

Symbol	Condition	Typical	Unit	Note
IDD0	One bank Active-Precharge	800	mA	
IDD1	One bank operation	1000	mA	
IDD2P	Precharge power-down standby current	200	mA	
IDD2F	Precharge floating standby current	360	mA	
IDD2Q	Precharge quiet standby current	280	mA	
IDD3P	Active power-down standby current	240	mA	
IDD3N	Active standby current	400	mA	
IDD4R	Operating current-burst read	1,360	mA	
IDD4W	Operating current-burst write	1,480	mA	
IDD5	Auto refresh current	1,480	mA	
IDD6	Self refresh current	16	mA	
IDD7A	Operating current-Four bank operation	2,600	mA	

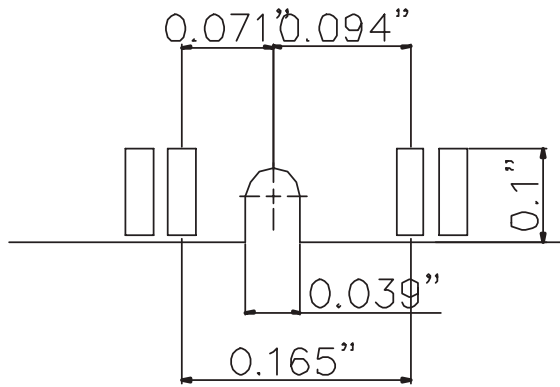
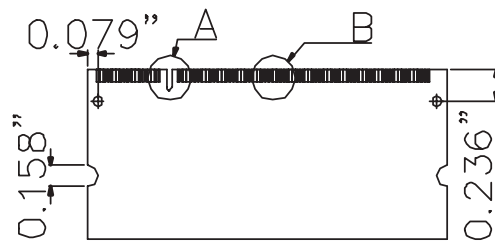
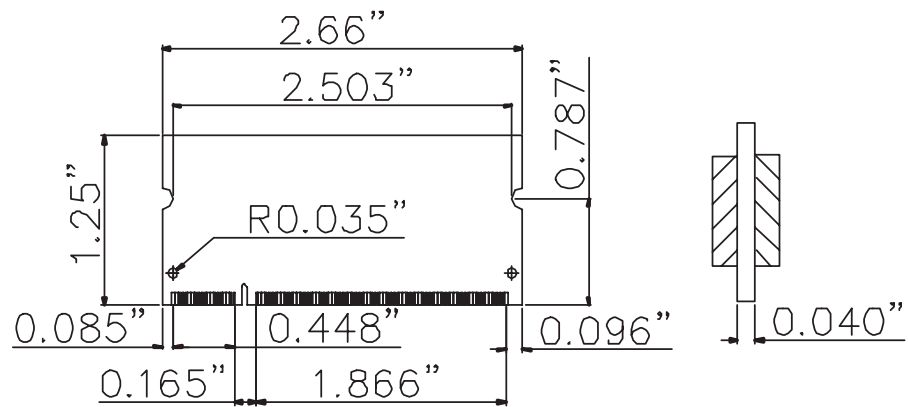
AC Characteristics

Parameter		Symbol	ADECB1608		Unit	Note
			Min	Max		
System clock	/CAS Latency = 2.5	tCK2.5	7.5	12	ns	
Cycle time	/CAS Latency = 2	tCK2	10			
Clock high pulse width		tCHW	0.45	0.55	tCK	
Clock low pulse width		tCLW	0.45	0.55	tCK	
Access time form clock		tAC	-0.75	0.75	ns	
ROW cycle time		tRC	65		ns	
/RAS to /CAS delay		tRCD	20		ns	
ROW active time		tRAS	45	120K	ns	
ROW precharge time		tRP	20		ns	
ROW to ROW bank active delay		tRRD	15		ns	
Write recovery time		Twr	2		tCK	
Refresh row cycle time		tRFC	75		ns	
Col. Address to Col. Address delay		tCCD	1		tCK	
DQS out access time from CK /CK		tDQSK	-0.751	+0.75	ns	
Data strobe edge to output data edge		tDQSQ		+0.5	ns	
CK to valid DQS-in		tDQSS	0.75	1.25	tCK	
DQS – input setup time		tWPRES	0		ns	
DQS – input hold time		tWPREH	0.25		tCK	
Address/Command setup time		tIS	0.9		ns	
Address/Command hold time		tIH	0.9		ns	
DQS falling edge to CK rising-setup time		tDDS	0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		tCK	
DQS in high level width		tDQSH	0.35		tCK	
DQS in low level width		tDQSL	0.35		tCK	
DQS in cycle time		tDSC	0.9	1.1	tCK	
Read Preamble		tRPRE	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	tCK	
Mode register set cycle time		tMRD	15		ns	
Power down exit time		tPDEX	10		ns	

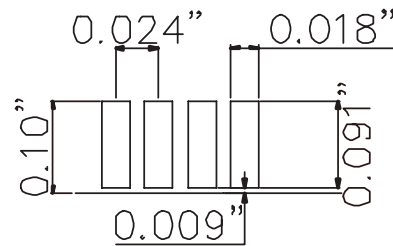
Command Truth-Table

Command		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	ADDR	A10/AP	BA
Mode Register Set		H	X	L	L	L	L	OP code		
No Operation		H	X	L	H	H	H	X		
Bank Active		H	X	L	L	H	H	RA		V
Read		H	X	L	H	L	H	CA	L	V
Read with Auto Precharge									H	
Write		H	X	L	H	L	L	CA	L	V
Write with Auto Precharge									H	
Precharge All Bank		H	X	L	L	H	L	X	H	X
Precharge select Bank									L	V
Burst Stop		H	X	L	H	H	L	X		
Auto Refresh		H	H	L	L	L	H	X		
Self Refresh	Entry	H	L	L	L	L	H	X		
	Exit	L	H	L	H	H	H			
Precharge	Entry	H	L	H	X	X	X	X		
				L	H	H	H			
Power down	Exit	L	H	H	X	X	X			
				L	V	V	V			
Active Power Down	Entry	H	L	H	X	X	X	X		
				L	V	V	V			
	Exit	L	H	X	X	X	X			

Package Information



Detail A



Detail B