

**Low Phase Noise VCXO (9.5-65MHz)**

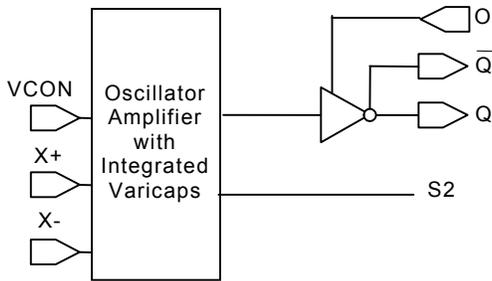
**FEATURES**

- 19MHz to 65MHz fundamental crystal input.
- Output range: 9.5MHz – 65MHz
- Complementary outputs: PECL or LVDS output.
- Selectable OE Logic (enable high or enable low).
- Integrated variable capacitors.
- Supports 2.5V or 3.3V Power Supply.
- Available in 16 pin TSSOP package.

**DESCRIPTION**

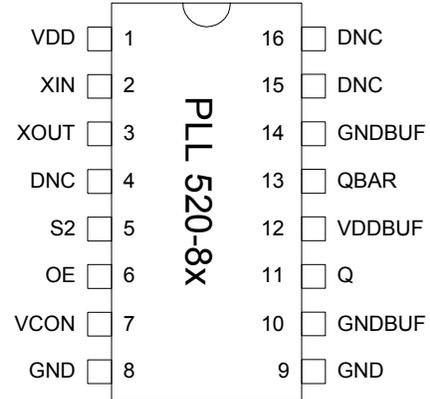
The PLL520-88 (PECL) and PLL520-89 (LVDS) are VCXO ICs specifically designed to work with fundamental crystals between 19MHz and 65MHz. The selectable divide by two feature extends the operation range from 9.5MHz to 65MHz. They require very low current into the crystal resulting in better overall stability. The OE logic feature allows selection of enable high or enable low.

**BLOCK DIAGRAM**



**PLL520-8X Block Diagram**

**PIN CONFIGURATION**



**OUTPUT SELECTION AND ENABLE**

OE_SELECT	OE_CTRL	State
0	0	Tri-state
	1 (Default)	Output enabled
1 (Default)	0 (Default)	Output enabled
	1	Tri-state

Input selection: Bond to GND to set to "0", bond to VDD to set to "1"  
No connection results to "default" setting through internal pull-up/-down.

OE\_CTRL: Logical states defined by PECL levels if OE\_SELECT is "1"  
Logical states defined by CMOS levels if OE\_SELECT is "0"

**OUTPUT FREQUENCY DIVIDE BY TWO SELECTOR**

S2	Output
0	Input/2
1	Input

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**PIN AND PAD ASSIGNMENT**

Name	Pin#	Description
VDD	1	Power Supply.
XIN	2	Crystal input. See Crystal Specification on page 3.
XOUT	3	Crystal output. See Crystal Specification on page 3.
DNC	4	Do Not Connect.
S2	5	Output Divide by Two selector pin. See the OUTPUT DIVIDE BY TWO SELECTOR Table on page 1.
OE_CTRL	6	Output Enable input. See OUTPUT SELECTION AND ENABLE TABLE on page 1.
VCON	8	Voltage control input.
GND	9	Ground.
GNDBUF	10	Ground for output buffer circuitry.
Q	11	PECL or LVDS output.
VDDBUF	12	Power supply for output buffer circuitry.
QBAR	13	Complementary PECL or LVDS output.
GNDBUF	14	Ground for output buffer circuitry.
DNC	15	Do Not Connect.
DNC	16	Do Not Connect.

**ELECTRICAL SPECIFICATIONS**
**1. Absolute Maximum Ratings**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		4.6	V
Input Voltage, dc	$V_I$	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature*	$T_A$	-40	85	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

\* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

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**2. Crystal Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	$F_{XIN}$	Fundamental	19		65	MHz
Crystal Loading Rating	$C_L (xtal)$	Die		8*		pF
Interelectrode Capacitance	$C_0$				5	pF
Recommended ESR	$R_E$	AT cut			30	$\Omega$

Note: Parameters denoted with an asterisk (\*) represent nominal characterization data and are not production tested to any specific limits.

**3. Voltage Control Crystal Oscillator (3.3V)**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		$F_{XIN} = 19 - 65\text{MHz};$ XTAL $C_0/C_1 < 250$ $0V \leq VCON \leq 3.3V$		200*		ppm
CLK output pullability		$VCON = 1.65V, \pm 1.65V$	$\pm 100^*$			ppm
On-chip Varicaps control range		$VCON = 0 \text{ to } 3.3V$		4 - 18*		pF
Linearity					10*	%
VCXO Tuning Characteristic				65		ppm/V
VCON input impedance				60		k $\Omega$
VCON modulation BW		$0V \leq VCON \leq 3.3V, -3\text{dB}$	25			kHz

Note: Parameters denoted with an asterisk (\*) represent nominal characterization data and are not production tested to any specific limits.

**4. General Electrical Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	$I_{DD}$	PECL/LVDS			100/80	mA
Operating Voltage	$V_{DD}$		2.97		3.63	V
Output Clock Duty Cycle		@ 50% $V_{DD}$ (CMOS) @ 1.25V (LVDS) @ $V_{DD} - 1.3V$ (PECL)	45 45 45	50 50 50	55 55 55	%
Short Circuit Current				$\pm 50$		mA

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**5. Jitter Specifications**

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS at 27MHz	With capacitive decoupling between VDD and GND. Over 10,000 cycles		2.3		ps
Period jitter peak-to-peak at 27MHz			18.5	20	
Accumulated jitter RMS at 27MHz	With capacitive decoupling between VDD and GND. Over 1,000,000 cycles.		2.3		ps
Accumulated jitter peak-to-peak at 27MHz			24	25	
Random Jitter	"RJ" measured on Wavecrest SIA 3000		2.3		ps

Measured on Wavecrest SIA 3000

**6. Phase Noise Specifications**

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	27MHz	-75	-100	-125	-140	-145	dBc/Hz

Note: Phase Noise measured on Agilent E5500

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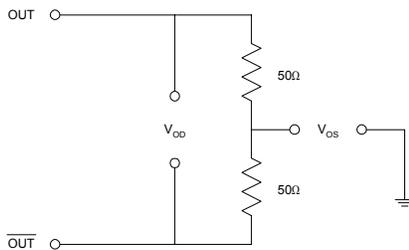
**7. LVDS Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	$V_{OD}$	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
$V_{DD}$ Magnitude Change	$\Delta V_{OD}$		-50		50	mV
Output High Voltage	$V_{OH}$			1.4	1.6	V
Output Low Voltage	$V_{OL}$		0.9	1.1		V
Offset Voltage	$V_{OS}$		1.125	1.2	1.375	V
Offset Magnitude Change	$\Delta V_{OS}$		0	3	25	mV
Power-off Leakage	$I_{OXD}$	$V_{out} = V_{DD}$ or $GND$ $V_{DD} = 0V$		$\pm 1$	$\pm 10$	$\mu A$
Output Short Circuit Current	$I_{OSD}$			-5.7	-8	mA

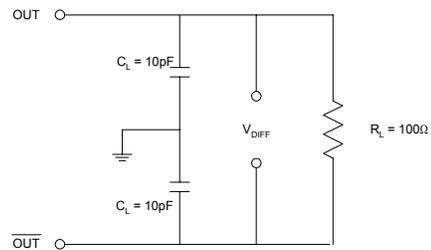
**8. LVDS Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	$t_r$	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	$t_f$		0.2	0.7	1.0	ns

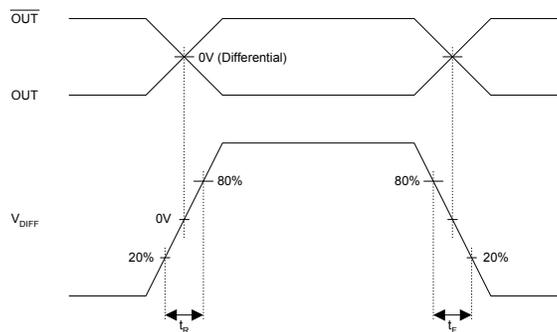
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



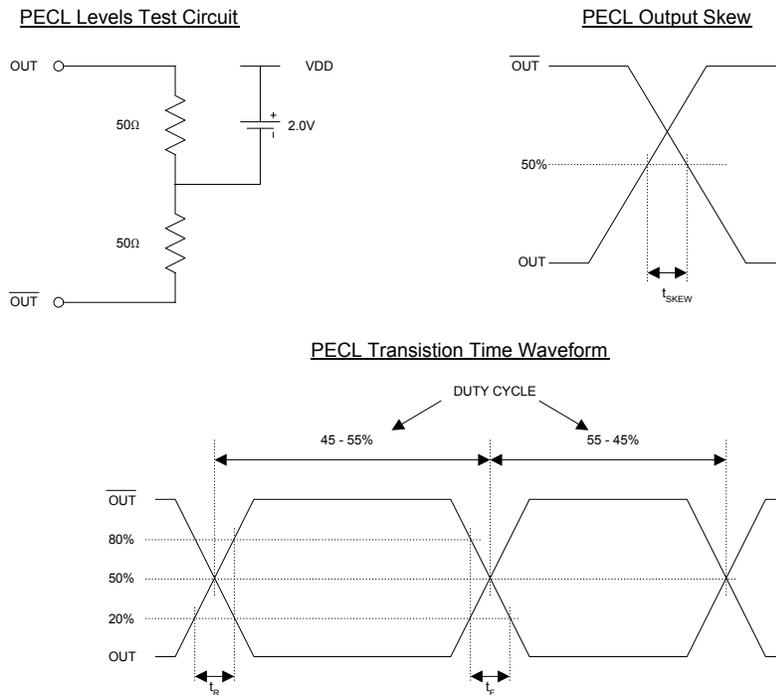
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**9. PECL Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	$V_{OH}$	$R_L = 50 \Omega$ to $(V_{DD} - 2V)$ (see figure)	$V_{DD} - 1.025$		V
Output Low Voltage	$V_{OL}$			$V_{DD} - 1.620$	V

**11. PECL Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	$t_r$	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	$t_f$	@80/20% - PECL		0.5	1.5	ns

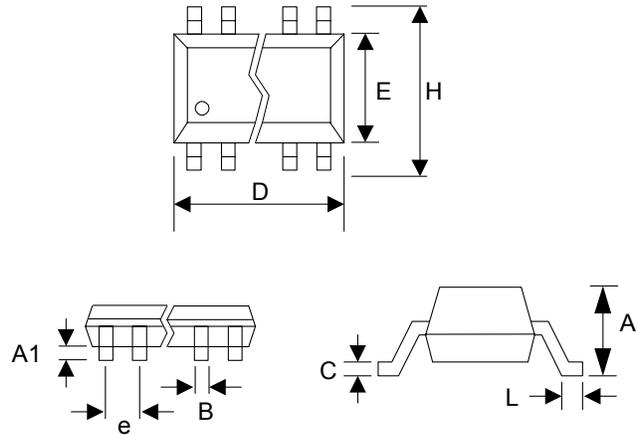


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**PACKAGE INFORMATION**

16 PIN TSSOP ( mm )		
Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



**ORDERING INFORMATION**

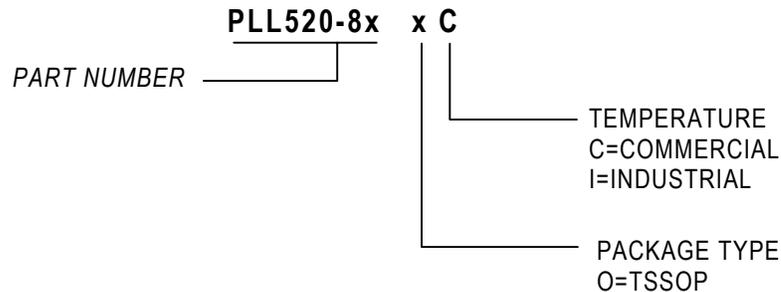
**For part ordering, please contact our Sales Department:**

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:  
Device number, Package type and Operating temperature range



<u>Order Number</u>	<u>Marking</u>	<u>Package Option</u>
PLL520-88OC-R	P520-88 OC	TSSOP – Tape and Reel
PLL520-88OC	P520-88 OC	TSSOP – Tube
PLL520-89OC-R	P520-89 OC	TSSOP – Tape and Reel
PLL520-89OC	P520-89 OC	TSSOP – Tube

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