REJ09B0069-0100

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32

SH7108, SH7109 Group

Hardware Manual

Renesas 32-Bit RISC Microcomputer
SuperH™ RISC engine Family / SH7108 Series

SH7108 Group	SH7108	HD6437108
	SH7106	HD6437106
	SH7104	HD6437104
	SH7101	HD6437101
SH7109 Group	SH7109	HD6437109
	SH7107	HD6437107
	SH7105	HD6437105

User's Manual

Rev.1.00
Revision Date: Sep. 18, 2008

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions may occur due to the false recognition of the pin state as an input signal. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

Configuration of This Manual

This manual comprises the following items:

1. General Precautions in the Handling of MPU/MCU Products
2. Configuration of This Manual
3. Preface
4. Contents
5. Overview
6. Description of Functional Modules
   - CPU and System-Control Modules
   - On-Chip Peripheral Modules

   The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

   i) Feature
   ii) Input/Output Pin
   iii) Register Description
   iv) Operation
   v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

7. List of Registers
8. Electrical Characteristics
9. Appendix
10. Main Revisions and Additions in this Edition (only for revised versions)

The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.

11. Index

Preface

The SH7108 Series single-chip RISC microprocessor integrates a Renesas Technology original RISC CPU core with peripheral functions required for system configuration.

Target users: This manual was written for users who will be using the SH7108 Series Micro-Computer Unit (MCU) in the design of application systems. Users of this manual are expected to understand the fundamentals of electrical circuits, logical circuits, and microcomputers.

Objective: This manual was written to explain the hardware functions and electrical characteristics of the SH7108 Series MCU to the above users.
Refer to the SH-1, SH-2, SH-DSP Software Manual for a detailed description of the instruction set.

Notes on reading this manual:

- Product names
  The following products are covered in this manual.

Product Classifications and Abbreviations

Basic Classification	On-Chip ROM Classification		Part No.
SH7108 (80-pin version)	SH7108	Masked ROM version (ROM: 128 kbytes)	HD6437108
	SH7106	Masked ROM version (ROM: 64 kbytes)	HD6437106
	SH7104	Masked ROM version (ROM: 256 kbytes)	HD6437104
	SH7101	Masked ROM version (ROM: 32 kbytes)	HD6437101
SH7109 (100-pin version)	SH7109	Masked ROM version (ROM: 128 kbytes)	HD6437109
	SH7107	Masked ROM version (ROM: 64 kbytes)	HD6437107
	SH7105	Masked ROM version (ROM: 256 kbytes)	HD6437105

In this manual, the product abbreviations are used to distinguish products. For example, 80-pin products are collectively referred to as the SH7108, an abbreviation of the basic type's classification code, and 100-pin products are referred to as the SH7109.

- The typical product

  The HD6437108 is taken as the typical product for the descriptions in this manual. Accordingly, when using an HD6437101, HD6437104, HD6437105, HD6437106, HD6437109, or HD6437107 simply replace the HD6437108 in those references where no differences between products are pointed out with HD6437101, HD6437104, HD6437105, HD6437106, HD6437109, or HD6437107. Where differences are indicated, be aware that each specification applies to the products as indicated.
- In order to understand the overall functions of the chip

  Read the manual according to the contents. This manual can be roughly categorized into parts on the CPU, system control functions, peripheral functions and electrical characteristics.
- In order to understand the details of the CPU's functions

  Read the SH-1, SH-2, SH-DSP Software Manual.
- In order to understand the details of a register when the user knows its name

  Read the index that is the final part of the manual to find the page number of the entry on the register. The addresses, bit names, and initial values of the registers are summarized in Appendix A, On-chip I/O Register.

Rules:	Register name:	The following notation is used for cases when the same or a similar function, e.g. serial communication, is implemented on more than one channel: XXX_N (XXX is the register name and N is the channel number)
	Bit order:	The MSB (most significant bit) is on the left and the LSB (least significant bit) is on the right.

Related Manuals: The latest versions of all related manuals are available from our web site. Please ensure you have the latest versions of all documents you require.
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SH7108 Series Manuals:

Document Title	ADE No.
SH7108, SH7109 Group Hardware Manual	This manual
SH-1, SH-2, SH-DSP Software Manual	REJ09B0171

Users Manuals for Development Tools:

Document Title	ADE No.
C/C++ Compiler, Assembler, Optimized Linkage Editor Users Manual	REJ10B0047
Simulator Debugger (for Windows) Users Manual	ADE-702-186
Simulator Debugger (for UNIX) Users Manual	ADE-702-149
High-performance Embedded Workshop Users Manual	REJ10J1737

Application Notes:

Document Title	ADE No.
C/C++ Compiler Edition	REJ05B0463

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Section 1 Overview

The SH7108 Series single-chip RISC microprocessor integrates a Renesas Technology original RISC CPU core with peripheral functions required for system configuration.

The SH7108 Series CPU has a RISC-type instruction set. Most instructions can be executed in one state (one system clock cycle), which greatly improves instruction execution speed. In addition, the 32-bit internal-bus architecture enhances data processing power. With this CPU, it has become possible to assemble low cost, high performance/high-functioning systems, even for applications that were previously impossible with microprocessors, such as realtime control, which demands high speeds.

In addition, the SH7108 Series includes on-chip peripheral functions necessary for system configuration, such as ROM, RAM, timers, a serial communication interface (SCI), an A/D converter, an interrupt controller (INTC), and I/O ports.

As the on-chip ROM, only masked ROM version is available. However, when F-ZTAT (Flexible Zero Turn Around Time) version is required, the SH7046F (80 pins) or SH7047F (100 pins) can be used.

1.1 Features

- Central processing unit with an internal 32-bit RISC (Reduced Instruction Set Computer) architecture
  - Instruction length: 16-bit fixed length for improved code efficiency
  - Load-store architecture (basic operations are executed between registers)
  - Sixteen 32-bit general registers
  - Five-stage pipeline
  - On-chip multiplier: multiplication operations (32 bits × 32 bits → 64 bits) executed in two to four cycles
  - C language-oriented 62 basic instructions
- Various peripheral functions
  - Multifunction timer/pulse unit (MTU)
  - Motor management timer(MMT)
  - Compare match timer (CMT)
  - Watchdog timer (WDT)
  - Asynchronous or clocked synchronous serial communication interface (SCI)
  - 10-bit A/D converter
  - Clock pulse generator

- On-chip memory

ROM	Model	ROM	RAM	Remarks
Mask ROM version	HD6437108	128 kbytes	4 kbytes	
	HD6437106	64 kbytes	4 kbytes	
	HD6437104	256 kbytes	8 kbytes	
	HD6437101	32 kbytes	2 kbytes	
	HD6437109	128 kbytes	4 kbytes	
	HD6437107	64 kbytes	4 kbytes	
	HD6437105	256 kbytes	8 kbytes	

- Maximum operating frequency and operating temperature range

Model	Maximum Operating Frequency (MHz) (System Clock (ϕ) and Peripheral Clock (Pϕ))	Operating Temperature Range (°C)
HD6437108F50/HD6437106F50 HD6437104F50/HD6437101F50 HD6437109F50/HD6437107F50/ HD6437105F50	(50, 25) or (40, 40)	-20 to +75
HD6437108FW50/HD6437106FW50 HD6437104FW50/HD6437101FW50 HD6437109FW50/HD6437107FW50/ HD6437105FW50	(50, 25) or (40, 40)	-40 to +85
HD6437101F40	(40, 40)	-40 to +75
HD6437101FW40	(40, 40)	-40 to +85

- I/O ports

Model	No. of I/O Pins	No. of Input-only Pins
HD6437108/HD6437106 HD6437104/HD6437101	42	12
HD6437109/HD6437107/HD6437105	53	16

- Supports various power-down states
- Compact package

Model	Package	(Code)	Body Size	Pin Pitch
HD6437108/HD6437106/ HD6437104/HD6437101	QFP-80	FP-80Q	14.0 × 14.0 mm	0.65 mm
HD6437109/HD6437107/ HD6437105	QFP-100	FP-100M	14.0 × 14.0 mm	0.50 mm

1.2 Internal Block Diagram

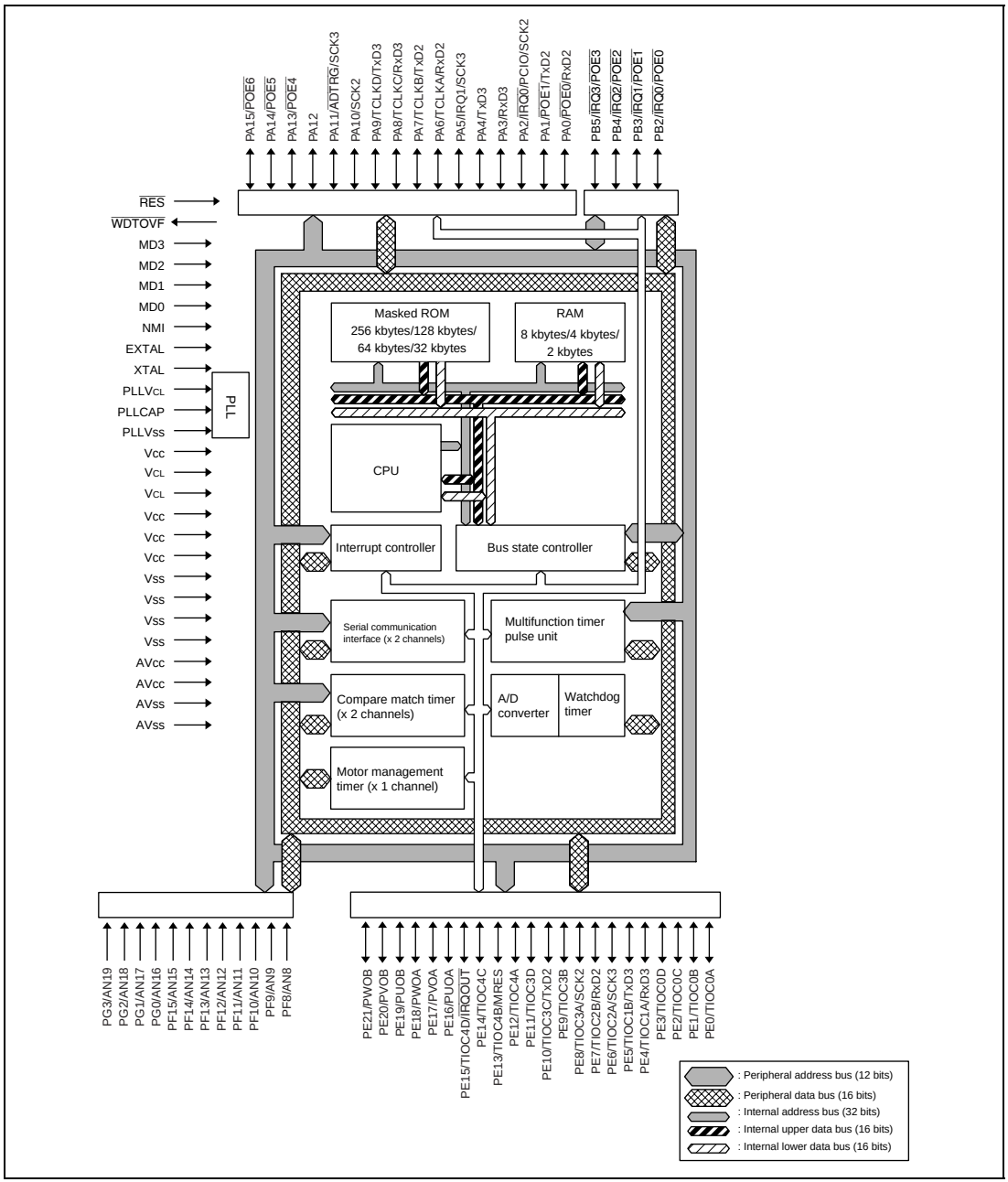


Figure 1.1 Internal Block Diagram of SH7108/SH7106/SH7104/SH7101

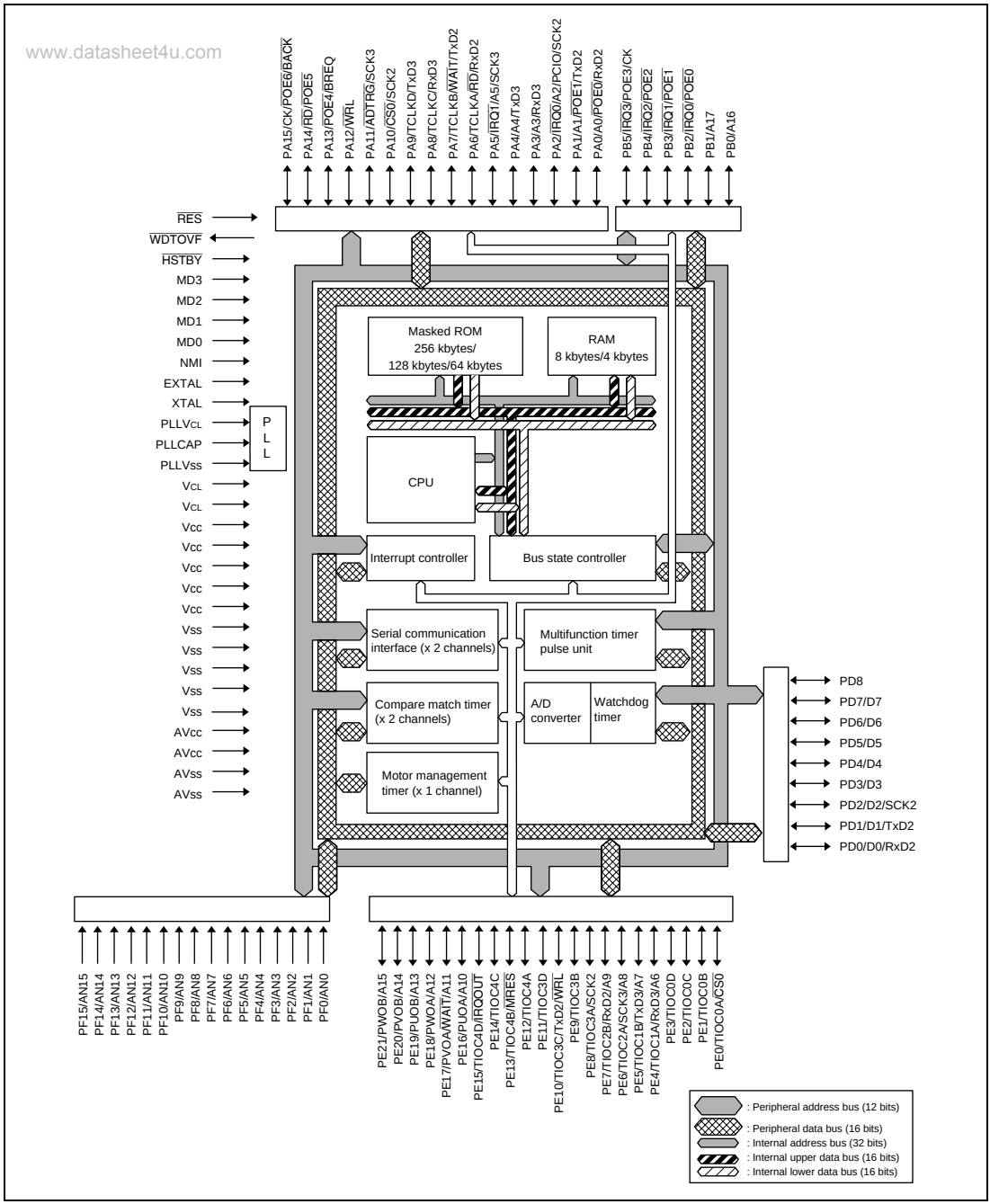


Figure 1.2 Internal Block Diagram of SH7109/SH7107/SH7105

1.3 Pin Assignment

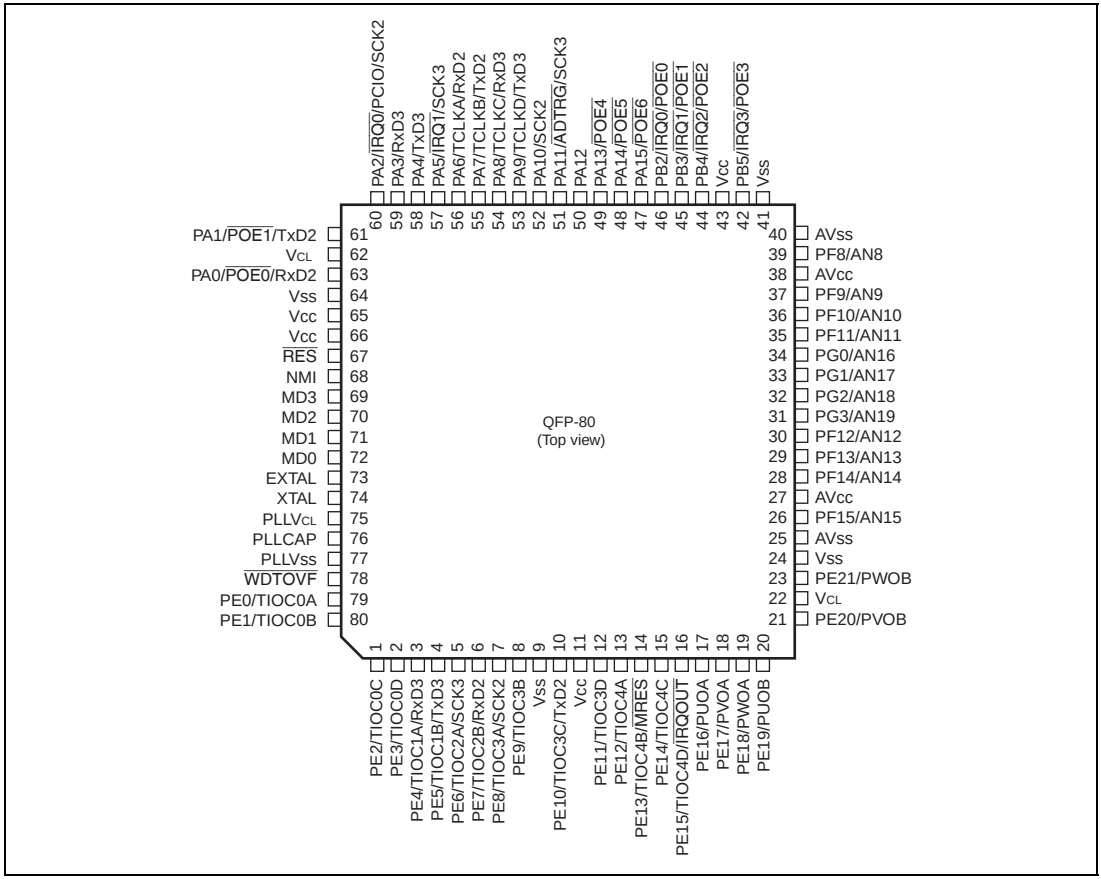
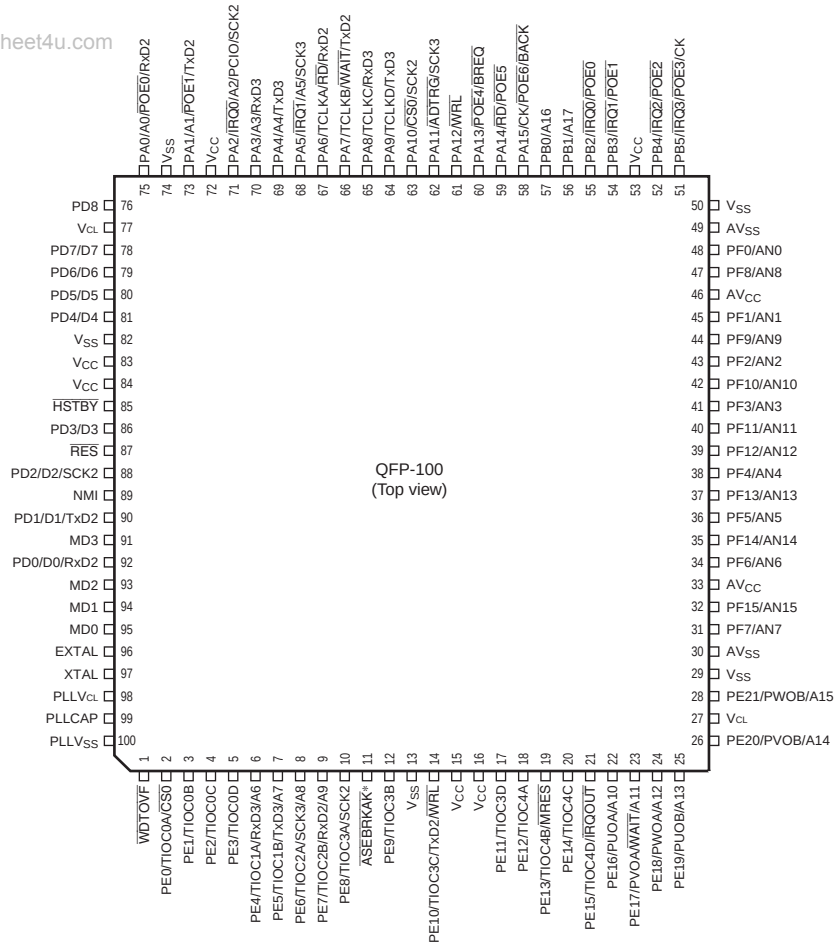


Figure 1.3 SH7108/SH7106/SH7104/SH7101 Pin Assignment



Note: * ASEBRKAK:

Handling procedure				
Vcc fixed	Vss fixed	Pull-up	Pull-down	NC
Enabled	Enabled	Enabled	Enabled	Enabled

Figure 1.4 SH7109/SH7107/SH7105 Pin Assignment

1.4 Pin Functions

Table 1.1 Pin Functions

Type	Symbol	I/O	Name	Function
Power Supply	V_{CC}	Input	Power supply	Power supply pins. Connect all these pins to the system power supply. The chip does not operate normally when some of these pins are open.
	V_{SS}	Input	Ground	Ground pins. Connect all these pins to the system power supply (0 V). The chip does not operate normally when some of these pins are open.
	V_{CL}	Output	Power supply for internal power-down	External capacitance pins for internal power-down power supply. Connect these pins to V_{SS} via a 0.47 µF (–10%/+100%) capacitor (placed close to the pin).
Clock	PLLV_{CL}	Output	Power supply for PLL	External capacitance pin for internal power-down power supply for an on-chip PLL oscillator. Connect this pin to PLLV_{SS} via a 0.47 µF (–10%/+100%) capacitor (placed close to the pin).
	PLLV_{SS}	Input	Ground for PLL	On-chip PLL oscillator ground pin.
	PLLCAP	Input	Capacitance for PLL	External capacitance pin for an on-chip PLL oscillator. This is an NC (no connection) pin in the SH7105.
	EXTAL	Input	External clock	For connection to a crystal resonator. An external clock can be supplied from the EXTAL pin. For examples of crystal resonator connection and external clock input, see section 4, Clock Pulse Generator.
	XTAL	Input	Crystal	For connection to a crystal resonator. For examples of crystal resonator connection and external clock input, see section 4, Clock Pulse Generator.
	CK	Output	System clock	Supplies the system clock to external devices.

Type	Symbol	I/O	Name	Function
Operating mode control	MD3 to MD0	Input	Set the mode	Set the operating mode. Inputs at these pins should not be changed during operation.
	FWP	Input	Protection against write operation into flash memory	Pin for the flash memory. This pin is only used in the flash memory version. Writing or erasing of flash memory can be protected. This pin becomes the V_{CC} pin for the masked ROM version.
System control	$\overline{RES}$	Input	Power-on reset	When this pin is driven low, the chip becomes to power-on reset state.
	$\overline{MRES}$	Input	Manual reset	When this pin is driven low, the chip becomes to manual reset state.
	$\overline{HSTBY}$	Input	Standby	When this pin is driven low, the chip shifts to standby mode.
	$\overline{WDTOVF}$	Output	Watchdog timer overflow	Output signal for the watchdog timer overflow. If this pin need to be pulled-down, use the resistor larger than 1 MΩ to pull the pin down.
	$\overline{BREQ}$	Input	Bus request	Driven low when an external device request the bus to be released.
	$\overline{BACK}$	Output	Bus request acknowledge	Indicates that the bus is released to the external device. The device output the $\overline{BREQ}$ signal controls the bus after it has received the $\overline{BACK}$ signal.
Interrupts	NMI	Input	Non-maskable interrupt	Non-maskable interrupt pin. If this pin is not used, it should be fixed high or low.
	$\overline{IRQ3}$ to $\overline{IRQ0}$	Input	Interrupt request 3 to 0	These pins request a maskable interrupt. One of the level input or edge input can be selected. In case of the edge input, one of the rising edge, falling edge, or both can be selected.
	$\overline{IRQOUT}$	Output	Interrupt request output	Shows that an interrupt cause has occurred. It is informed of an interrupt even when the bus is released.
Address bus	A17 to A0	Output	Address bus	These pins output addresses.
Data bus	D7 to D0	I/O	Data bus	8-bit bidirectional bus.

Type	Symbol	I/O	Name	Function
Bus control	CS0	Output	Chip select 0	Chip-select signal for external memory or devices.
	$\overline{RD}$	Output	Read	Indicates reading of data from external devices.
	$\overline{WRL}$	Output	Write to lower byte	Indicates that lower eight bits (bits 7 to 0) of external data are to be written.
	$\overline{WAIT}$	Input	Wait	Inserts waits to the bus cycle for accessing an external space.
Multifunction timer pulse unit (MTU)	TCLKA TCLKB TCLKC TCLKD	Input	External clock input for MTU timer	These pins input an external clock.
	TIOC0A TIOC0B TIOC0C TIOC0D	Input/ output	MTU input capture/output compare (channel 0)	The TGRA_0 to TGRD_0 input capture input/output compare output/PWM output pins.
	TIOC1A TIOC1B	Input/ output	MTU input capture/output compare (channel 1)	The TGRA_1 and TGRB_1 input capture input/output compare output/PWM output pins.
	TIOC2A TIOC2B	Input/ output	MTU input capture/output compare (channel 2)	The TGRA_2 and TGRB_2 input capture input/output compare output/PWM output pins.
	TIOC3A TIOC3B TIOC3C TIOC3D	Input/ output	MTU input capture/output compare (channel 3)	The TGRA_3 to TGRD_3 input capture input/output compare output/PWM output pins.
	TIOC4A TIOC4B TIOC4C TIOC4D	Input/ output	MTU input capture/output compare (channel 4)	The TGRA_4 to TGRD_4 input capture input/output compare output/PWM output pins.

Type	Symbol	I/O	Name	Function
Serial communication interface (SCI)	TxD2 TxD3	Output	Transmit data	Data output pins.
	RxD2 RxD3	Input	Receive data	Data input pins.
	SCK2 SCK3	Input/ output	Serial clock	Clock input/output pins.
Motor management timer (MMT)	PUOA	Output	U-phase of PWM	U-phase output pin for 6-phase non-overlap PWM waveforms.
	PUOB	Output	$\overline{\text{U}}$-phase of PWM	$\overline{\text{U}}$-phase output pin for 6-phase non-overlap PWM waveforms.
	PVOA	Output	V-phase of PWM	V-phase output pin for 6-phase non-overlap PWM waveforms.
	PVOB	Output	$\overline{\text{V}}$-phase of PWM	$\overline{\text{V}}$-phase output pin for 6-phase non-overlap PWM waveforms.
	PWOA	Output	W-phase of PWM	W-phase output pin for 6-phase non-overlap PWM waveforms.
	PWOB	Output	$\overline{\text{W}}$-phase of PWM	$\overline{\text{W}}$-phase output pin for 6-phase non-overlap PWM waveforms.
	PCIO	Input/ output	PWM control	Counter clear input pin by external input or output pin, or toggle output pin synchronized with PWM period.
Output control for MTU and MMT	$\overline{\text{POE6}}$ to $\overline{\text{POE0}}$	Input	Port output control	Input pins for the signal to request the output pins of MTU or MMT to become high impedance state.
A/D converter	AN19 to AN0	Input	Analog input pins	Analog input pins.
	$\overline{\text{ADTRG}}$	Input	Input of trigger for A/D conversion	Pin for input of an external trigger to start A/D conversion.
	AVCC	Input	Analog power supply	Power supply pin for the A/D converter. When the A/D converter is not used, connect this pin to the system power supply (+5 V). Connect all AVCC pins to the power supply. The chip does not operate normally when some of these pins are open.

Type	Symbol	I/O	Name	Function
A/D converter	AVSS	Input	Analog ground	The ground pin for the A/D converter. Connect this pin to the system power supply (0 V). Connect all AVSS pins to the system power supply. The chip does not operate normally when some of these pins are open.
I/O ports	PA15 to PA0	Input/ output	General purpose port	16-bit general-purpose input/output pins.
	PB5 to PB0	Input/ output	General purpose port	6-bit general-purpose input/output pins.
	PD8 to PD0	Input/ output	General purpose port	9-bit general-purpose input/output pins.
	PE21 to PE0	Input/ output	General purpose port	22-bit general-purpose input/output pins.
	PF15 to PF0	Input	General purpose port	16-bit general-purpose input/output pins.
	PG3 to PG0	Input	General purpose port	4-bit general-purpose input/output pins.

1.5 Differences from SH7046 Group

Table 1.2 Differences from SH7046 Group

Item	SH7046F	SH7108/SH7106/SH7104/SH7101
DTC, UBC	Incorporated	Not incorporated
BSC	—	Register RAMER deleted
I/O ports, PFC	PA3/$\overline{\text{POE4}}$/RxD3	PA3/RxD3
	PA3/$\overline{\text{POE5}}$/RxD3	PA4/TxD3
	PA5/$\overline{\text{IRQ1}}$/$\overline{\text{POE6}}$/SCK3	PA5/$\overline{\text{IRQ1}}$/SCK3
	PA8/TCLKC/$\overline{\text{IRQ2}}$/RxD3	PA8/TCLKC/RxD3
	PA9/TCLKC/$\overline{\text{IRQ3}}$/RxD3	PA9/TCLKD/TxD3
	PA12/$\overline{\text{UBCTRG}}$	PA12
	PE16/PUOA/$\overline{\text{UBCTRG}}$	PE16/PUOA
ROM	Flash: 256 kbytes	Masked ROM: 256 kbytes/128 kbytes/64 kbytes/32 kbytes
RAM	12 kbytes	8 kbytes/4 kbytes/2 kbytes
Operating frequency	4 to 50 MHz	10 to 50 MHz

1.6 Differences from SH7047 Group

Table 1.3 Differences from SH7047 Group

Item	SH7047F	SH7109/SH7107/SH7105
DTC, UBC, AUD, H-UDI, HCAN2, SCI (channel 4)	Incorporated	Not incorporated
BSC	—	Register RAMER deleted
I/O ports, PFC	PA3/A3/$\overline{\text{POE4}}$/RxD3	PA3/A3/RxD3
	PA4/A4/$\overline{\text{POE5}}$/TxD3	PA4/A4/TxD3
	PA5/$\overline{\text{IRQ1}}$/A5/$\overline{\text{POE6}}$/SCK3	PA5/$\overline{\text{IRQ1}}$/A5/SCK3
	PA8/TCLKC/$\overline{\text{IRQ2}}$/RxD3	PA8/TCLKC/RxD3
	PA9/TCLKD/$\overline{\text{IRQ3}}$/TxD3	PA9/TCLKD/TxD3
	PA10/$\overline{\text{CS0}}$/$\overline{\text{RD}}$/TCK/SCK2	PA10/$\overline{\text{CS0}}$/SCK2
	PA12/$\overline{\text{WRL}}$/$\overline{\text{UBCTRG}}$/TDI	PA12/$\overline{\text{WRL}}$
	PA13/$\overline{\text{POE4}}$/TDO/$\overline{\text{BREQ}}$	PA13/$\overline{\text{POE4}}$/$\overline{\text{BREQ}}$
	PA14/$\overline{\text{RD}}$/$\overline{\text{POE5}}$/TMS	PA14/$\overline{\text{RD}}$/$\overline{\text{POE5}}$
	PA15/CK/$\overline{\text{POE6}}$/$\overline{\text{TRST}}$/$\overline{\text{BACK}}$	PA15/CK/$\overline{\text{POE6}}$/$\overline{\text{BACK}}$
	PB0/A16/HTxD1	PB0/A16
	PB1/A17/HRxD1/SCK4	PB1/A17
	PB2/$\overline{\text{IRQ0}}$/$\overline{\text{POE0}}$/RxD4	PB2/$\overline{\text{IRQ0}}$/$\overline{\text{POE0}}$
	PB3/$\overline{\text{IRQ1}}$/$\overline{\text{POE1}}$/TxD4	PB3/$\overline{\text{IRQ1}}$/$\overline{\text{POE1}}$
	PB4/$\overline{\text{IRQ2}}$/$\overline{\text{POE2}}$/SCK4	PB4/$\overline{\text{IRQ2}}$/$\overline{\text{POE2}}$
	PD0/D0/RxD2/AUDATA0	PD0/D0/RxD2
	PD1/D1/TxD2/AUDATA1	PD1/D1/TxD2
	PD2/D2/SCK2/AUDATA2	PD2/D2/SCK2
	PD3/D3/AUDATA3	PD3/D3
	PD4/D4/$\overline{\text{AUDRST}}$	PD4/D4
	PD5/D5/AUDMD	PD5/D5
	PD6/D6/AUDCK	PD6/D6
	PD7/D7/$\overline{\text{AUDSYNC}}$	PD7/D7
	PD8/$\overline{\text{UBCTRG}}$	PD8
	PE16/PUOA/$\overline{\text{UBCTRG}}$/A10	PE16/PUOA/A10
	PE19/PUOB/RxD4/A13	PE19/PUOB/A13
	PE20/PVOB/TxD4/A14	PE20/PVOB/A14
	PE21/PWOB/SCK4/A15	PE21/PWOB/A15

Item	SH7047F	SH7109/SH7107/SH7105
ROM	Flash: 256 kbytes	Masked ROM: 256 kbytes/128 kbytes/64 kbytes
RAM	12 kbytes	8 kbytes/4 kbytes
Operating frequency	4 to 50 MHz	10 to 50 MHz

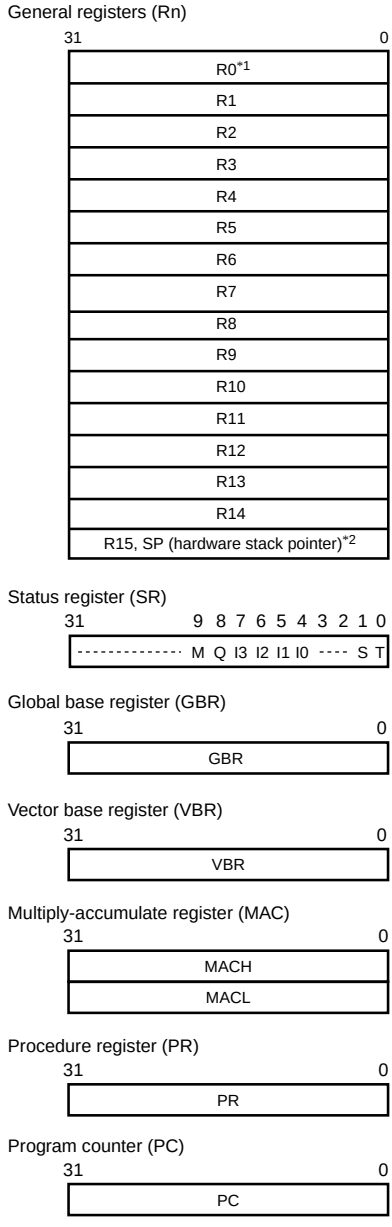
Section 2 CPU

2.1 Features

- General-register architecture
  - Sixteen 32-bit general registers
- Sixty-two basic instructions
- Eleven addressing modes
  - Register direct [Rn]
  - Register indirect [@Rn]
  - Register indirect with post-increment [@Rn+]
  - Register indirect with pre-decrement [@-Rn]
  - Register indirect with displacement [@disp:4,Rn]
  - Register indirect with index [@R0, Rn]
  - GBR indirect with displacement [@disp:8,GBR]
  - GBR indirect with index [@R0,GBR]
  - Program-counter relative with displacement [@disp:8,PC]
  - Program-counter relative [disp:8/disp:12/Rn]
  - Immediate [#imm:8]

2.2 Register Configuration

The register set consists of sixteen 32-bit general registers, three 32-bit control registers, and four 32-bit system registers.



Notes: 1. R0 functions as an index register in the indirect indexed register addressing mode and indirect indexed GBR addressing mode. In some instructions, R0 functions as a fixed source register or destination register.
2. R15 functions as a hardware stack pointer (SP) during exception processing.

Figure 2.1 CPU Internal Registers

2.2.1 General Registers (Rn)

The sixteen 32-bit general registers (Rn) are numbered R0 to R15. General registers are used for data processing and address calculation. R0 is also used as an index register. Several instructions have R0 fixed as their only usable register. R15 is used as the hardware stack pointer (SP). Saving and recovering the status register (SR) and program counter (PC) in exception processing is accomplished by referencing the stack using R15.

2.2.2 Control Registers

The control registers consist of three 32-bit registers: status register (SR), global base register (GBR), and vector base register (VBR). The status register indicates processing states. The global base register functions as a base address for the indirect GBR addressing mode to transfer data to the registers of on-chip peripheral modules. The vector base register functions as the base address of the exception processing vector area (including interrupts).

Status Register (SR):

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
9	M	Undefined	R/W	Used by the DIV0U, DIV0S, and DIV1 instructions.
8	Q	Undefined	R/W	Used by the DIV0U, DIV0S, and DIV1 instructions.
7	I3	1	R/W	Interrupt Mask Bits
6	I2	1	R/W	
5	I1	1	R/W	
4	I0	1	R/W	
3, 2	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
1	S	Undefined	R/W	S Bit Used by the MAC instruction.
0	T	Undefined	R/W	T Bit The MOVT, CMP/cond, TAS, TST, BT (BT/S), BF (BF/S), SETT, and CLRT instructions use the T bit to indicate true (1) or false (0). The ADDV, ADDC, SUBV, SUBC, DIV0U, DIV0S, DIV1, NEGC, SHAR, SHAL, SHLR, SHLL, ROTR, ROTL, ROTCR, and ROTCL instructions also use the T bit to indicate carry/borrow or overflow/underflow.

Global Base Register (GBR): Indicates the base address of the indirect GBR addressing mode. The indirect GBR addressing mode is used in data transfer for on-chip peripheral modules register areas and in logic operations.

Vector Base Register (VBR): Indicates the base address of the exception processing vector area.

2.2.3 System Registers

System registers consist of four 32-bit registers: high and low multiply and accumulate registers (MACH and MACL), the procedure register (PR), and the program counter (PC).

Multiply-and-Accumulate Registers (MAC): Registers to store the results of multiply-and-accumulate operations.

Procedure Register (PR): Registers to store the return address from a subroutine procedure.

Program Counter (PC): Registers to indicate the sum of current instruction addresses and four, that is, the address of the second instruction after the current instruction.

2.2.4 Initial Values of Registers

Table 2.1 lists the values of the registers after reset.

Table 2.1 Initial Values of Registers

Classification	Register	Initial Value
General registers	R0 to R14	Undefined
	R15 (SP)	Value of the stack pointer in the vector address table
Control registers	SR	Bits I3 to I0 are 1111 (H'F), reserved bits are 0, and other bits are undefined
	GBR	Undefined
	VBR	H'00000000
System registers	MACH, MACL, PR	Undefined
	PC	Value of the program counter in the vector address table

2.3 Data Formats

2.3.1 Data Format in Registers

Register operands are always longwords (32 bits). If the size of memory operand is a byte (8 bits) or a word (16 bits), it is changed into a longword by expanding the sign-part when loaded into a register.

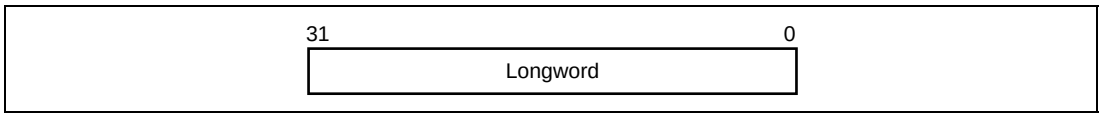


Figure 2.2 Data Format in Registers

2.3.2 Data Formats in Memory

Memory data formats are classified into bytes, words, and longwords. Byte data can be accessed from any address. Locate, however, word data at an address 2n, longword data at 4n. Otherwise, an address error will occur if an attempt is made to access word data starting from an address other than 2n or longword data starting from an address other than 4n. In such cases, the data accessed cannot be guaranteed. The hardware stack area, pointed by the hardware stack pointer (SP, R15), uses only longword data starting from address 4n because this area holds the program counter and status register.

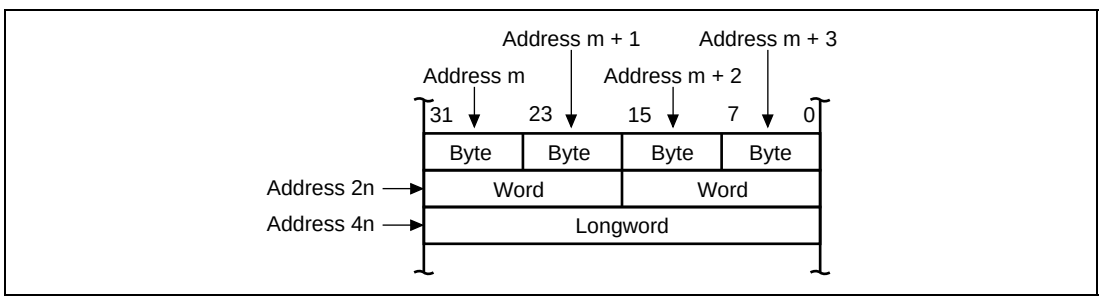


Figure 2.3 Data Formats in Memory

2.3.3 Immediate Data Format

Byte (8 bit) immediate data resides in an instruction code. Immediate data accessed by the MOV, ADD, and CMP/EQ instructions is sign-extended and handled in registers as longword data. Immediate data accessed by the TST, AND, OR, and XOR instructions is zero-extended and handled as longword data. Consequently, AND instructions with immediate data always clear the upper 24 bits of the destination register.

Word or longword immediate data is not located in the instruction code, but instead is stored in a memory table. An immediate data transfer instruction (MOV) accesses the memory table using the PC relative addressing mode with displacement.

2.4 Instruction Features

2.4.1 RISC-Type Instruction Set

All instructions are RISC type. This section details their functions.

16-Bit Fixed Length: All instructions are 16 bits long, increasing program code efficiency.

One Instruction per State: The microprocessor can execute basic instructions in one state using the pipeline system. One state is 25 ns at 40 MHz.

Data Length: Longword is the standard data length for all operations. Memory can be accessed in bytes, words, or longwords. Byte or word data accessed from memory is sign-extended and handled as longword data. Immediate data is sign-extended for arithmetic operations or zero-extended for logic operations. It also is handled as longword data.

Table 2.2 Sign Extension of Word Data

CPU of This LSI		Description	Example of Conventional CPU
`MOV.W`	`@(disp,PC),R1`	Data is sign-extended to 32 bits, and R1 becomes H'00001234. It is next operated upon by an ADD instruction.	`ADD.W #H'1234,R0`
`ADD`	`R1,R0`		
	`.........`		
`.DATA.W`	`H'1234`		

Note: @(disp, PC) accesses the immediate data.

Load-Store Architecture: Basic operations are executed between registers. For operations that involve memory access, data is loaded to the registers and executed (load-store architecture). Instructions such as AND that manipulate bits, however, are executed directly in memory.

Delayed Branch Instructions: Unconditional branch instructions are delayed branch instructions. With a delayed branch instruction, the branch is taken after execution of the instruction following the delayed branch instruction. This reduces the disturbance of the pipeline control in case of branch instructions. There are two types of conditional branch instructions: delayed branch instructions and ordinary branch instructions.

Table 2.3 Delayed Branch Instructions

CPU of This LSI		Description	Example of Conventional CPU	
BRA	TRGET	Executes the ADD before branching to TRGET.	ADD.W	R1,R0
ADD	R1,R0		BRA	TRGET

Multiply/Multiply-and-Accumulate Operations: 16-bit × 16-bit → 32-bit multiply operations are executed in one to two states. 16-bit × 16-bit + 64-bit → 64-bit multiply-and-accumulate operations are executed in two to three states. 32-bit × 32-bit → 64-bit multiply and 32-bit × 32-bit + 64-bit → 64-bit multiply-and-accumulate operations are executed in two to four states.

T Bit: The T bit in the status register changes according to the result of the comparison. Whether a conditional branch is taken or not taken depends upon the T bit condition (true/false). The number of instructions that change the T bit is kept to a minimum to improve the processing speed.

Table 2.4 T Bit

CPU of This LSI		Description	Example of Conventional CPU	
CMP/GE	R1,R0	T bit is set when R0 ≥ R1. The program branches to TRGET0 when R0 ≥ R1 and to TRGET1 when R0 < R1.	CMP.W	R1,R0
BT	TRGET0		BGE	TRGET0
BF	TRGET1		BLT	TRGET1
ADD	#–1,R0	T bit is not changed by ADD. T bit is set when R0 = 0. The program branches if R0 = 0.	SUB.W	#1,R0
CMP/EQ	#0,R0		BEQ	TRGET
BT	TRGET			

Immediate Data: Byte (8-bit) immediate data is located in an instruction code. Word or longword immediate data is not located in instruction codes but in a memory table. An immediate data transfer instruction (MOV) accesses the memory table using the PC relative addressing mode with displacement.

Table 2.5 Immediate Data Accessing

Classification	CPU of This LSI		Example of Conventional CPU	
8-bit immediate	MOV	#H'12,R0	MOV.B	#H'12,R0
16-bit immediate	MOV.W	@(disp,PC),R0	MOV.W	#H'1234,R0
		.....		
	.DATA.W	H'1234		
32-bit immediate	MOV.L	@(disp,PC),R0	MOV.L	#H'12345678,R0
		.....		
	.DATA.L	H'12345678		

Note: @(disp, PC) accesses the immediate data.

Absolute Address: When data is accessed by absolute address, the value in the absolute address is placed in the memory table in advance. That value is transferred to the register by loading the immediate data during the execution of the instruction, and the data is accessed in the indirect register addressing mode.

Table 2.6 Absolute Address Accessing

Classification	CPU of This LSI		Example of Conventional CPU
Absolute address	MOV.L	@(disp,PC),R1	MOV.B @H'12345678,R0
	MOV.B	@R1,R0	
		.....	
	.DATA.L	H'12345678	

Note: @(disp,PC) accesses the immediate data.

16-Bit/32-Bit Displacement: When data is accessed by 16-bit or 32-bit displacement, the displacement value is placed in the memory table in advance. That value is transferred to the register by loading the immediate data during the execution of the instruction, and the data is accessed in the indirect indexed register addressing mode.

Table 2.7 Displacement Accessing

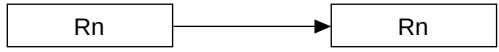
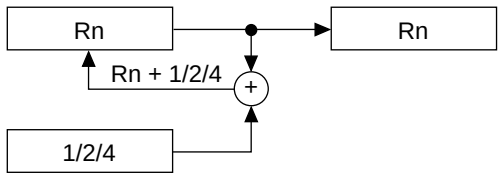
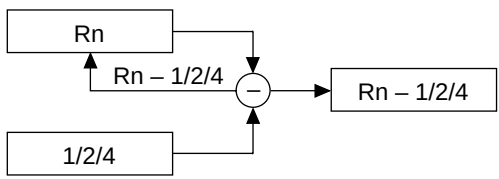
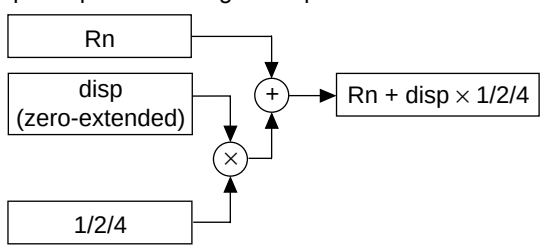
Classification	CPU of This LSI		Example of Conventional CPU
16-bit displacement	MOV.W	@(disp,PC),R0	MOV.W @(H'1234,R1),R2
	MOV.W	@(R0,R1),R2	
		.....	
	.DATA.W	H'1234	

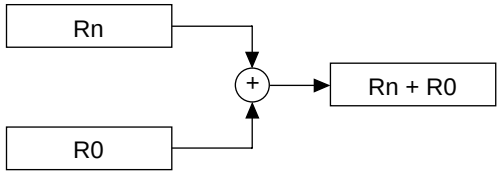
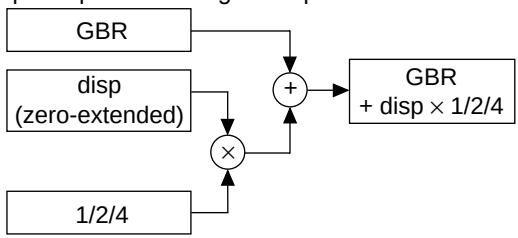
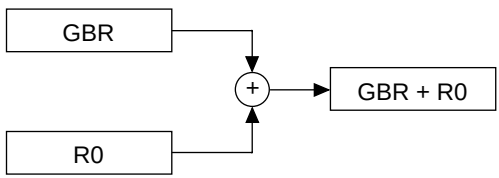
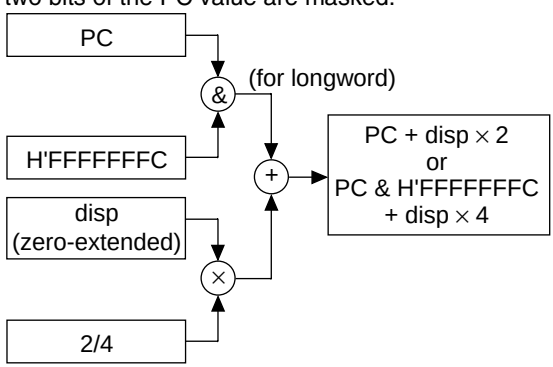
Note: @(disp,PC) accesses the immediate data.

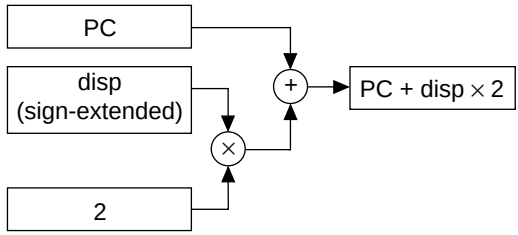
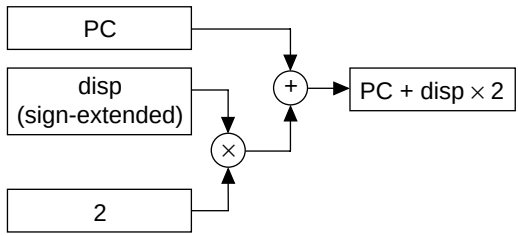
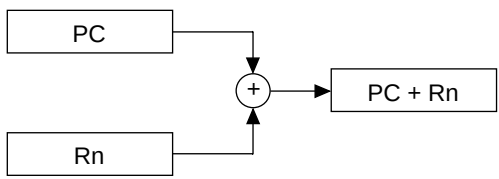
2.4.2 Addressing Modes

Table 2.8 describes addressing modes and effective address calculation.

Table 2.8 Addressing Modes and Effective Addresses

Addressing Mode	Instruction Format	Effective Address Calculation	Equation
Direct register addressing	`Rn`	The effective address is register Rn. (The operand is the contents of register Rn.)	—
Indirect register addressing	`@Rn`	The effective address is the contents of register Rn. 	Rn
Post-increment indirect register addressing	`@Rn+`	The effective address is the contents of register Rn. A constant is added to the content of Rn after the instruction is executed. 1 is added for a byte operation, 2 for a word operation, and 4 for a longword operation. 	Rn (After the instruction executes) Byte: Rn + 1 → Rn Word: Rn + 2 → Rn Longword: Rn + 4 → Rn
Pre-decrement indirect register addressing	`@-Rn`	The effective address is the value obtained by subtracting a constant from Rn. 1 is subtracted for a byte operation, 2 for a word operation, and 4 for a longword operation. 	Byte: Rn – 1 → Rn Word: Rn – 2 → Rn Longword: Rn – 4 → Rn (Instruction is executed with Rn after this calculation)
Indirect register addressing with displacement	`@(disp:4, Rn)`	The effective address is the sum of Rn and a 4-bit displacement (disp). The value of disp is zero-extended, and remains unchanged for a byte operation, is doubled for a word operation, and is quadrupled for a longword operation. 	Byte: Rn + disp Word: Rn + disp × 2 Longword: Rn + disp × 4

Addressing Mode	Instruction Format	Effective Address Calculation	Equation
Indirect indexed register addressing	@(R0, Rn)	The effective address is the sum of Rn and R0. 	Rn + R0
Indirect GBR addressing with displacement	@(disp:8, GBR)	The effective address is the sum of GBR value and an 8-bit displacement (disp). The value of disp is zero-extended, and remains unchanged for a byte operation, is doubled for a word operation, and is quadrupled for a longword operation. 	Byte: GBR + disp Word: GBR + disp × 2 Longword: GBR + disp × 4
Indirect indexed GBR addressing	@(R0, GBR)	The effective address is the sum of GBR value and R0. 	GBR + R0
Indirect PC addressing with displacement	@(disp:8, PC)	The effective address is the sum of PC value and an 8-bit displacement (disp). The value of disp is zero-extended, and is doubled for a word operation, and quadrupled for a longword operation. For a longword operation, the lowest two bits of the PC value are masked. 	Word: PC + disp × 2 Longword: PC & H'FFFFFFFC + disp × 4

Addressing Mode	Instruction Format	Effective Address Calculation	Equation
PC relative addressing	`disp:8`	The effective address is the sum of PC value and the value that is obtained by doubling the sign-extended 8-bit displacement (disp). 	PC + disp × 2
	`disp:12`	The effective address is the sum of PC value and the value that is obtained by doubling the sign-extended 12-bit displacement (disp). 	PC + disp × 2
	`Rn`	The effective address is the sum of the register PC and Rn. 	PC + Rn
Immediate addressing	`#imm:8`	The 8-bit immediate data (imm) for the TST, AND, OR, and XOR instructions is zero-extended.	—
	`#imm:8`	The 8-bit immediate data (imm) for the MOV, ADD, and CMP/EQ instructions is sign-extended.	—
	`#imm:8`	The 8-bit immediate data (imm) for the TRAPA instruction is zero-extended and then quadrupled.	—

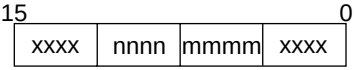
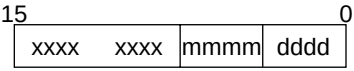
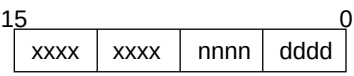
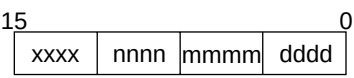
2.4.3 Instruction Format

The instruction formats and the meaning of source and destination operand are described below. The meaning of the operand depends on the instruction code. The symbols used are as follows:

- xxxx: Instruction code
- mmmm: Source register
- nnnn: Destination register
- iiii: Immediate data
- dddd: Displacement

Table 2.9 Instruction Formats

Instruction Formats	Source Operand	Destination Operand	Example
0 format 15 0 xxxx xxxx xxxx xxxx	—	—	`NOP`
n format 15 0 xxxx nnnn xxxx xxxx	—	nnnn: Direct register	`MOVT Rn`
	Control register or system register	nnnn: Direct register	`STS MACH,Rn`
	Control register or system register	nnnn: Indirect pre-decrement register	`STC.L SR,@-Rn`
m format 15 0 xxxx mmmm xxxx xxxx	mmmm: Direct register	Control register or system register	`LDC Rm,SR`
	mmmm: Indirect post-increment register	Control register or system register	`LDC.L @Rm+,SR`
	mmmm: Indirect register	—	`JMP @Rm`
	mmmm: PC relative using Rm	—	`BRAF Rm`

Instruction Formats	Source Operand	Destination Operand	Example
nm format 	mmmm: Direct register	nnnn: Direct register	`ADD Rm,Rn`
	mmmm: Direct register	nnnn: Indirect register	`MOV.L Rm,@Rn`
	mmmm: Indirect post-increment register (multiply-and-accumulate) nnnn*: Indirect post-increment register (multiply-and-accumulate)	MACH, MACL	`MAC.W @Rm+,@Rn+`
	mmmm: Indirect post-increment register	nnnn: Direct register	`MOV.L @Rm+,Rn`
	mmmm: Direct register	nnnn: Indirect pre-decrement register	`MOV.L Rm,@-Rn`
	mmmm: Direct register	nnnn: Indirect indexed register	`MOV.L Rm,@(R0,Rn)`
md format 	mmmmdddd: Indirect register with displacement	R0 (Direct register)	`MOV.B @(disp,Rn),R0`
nd4 format 	R0 (Direct register)	nnnndddd: Indirect register with displacement	`MOV.B R0,@(disp,Rn)`
nmd format 	mmmm: Direct register	nnnndddd: Indirect register with displacement	`MOV.L Rm,@(disp,Rn)`
	mmmmdddd: Indirect register with displacement	nnnn: Direct register	`MOV.L @(disp,Rm),Rn`

Instruction Formats	Source Operand	Destination Operand	Example
d format 15 0 xxxx xxxx dddd dddd	ddddddddd: Indirect GBR with displacement	R0 (Direct register)	MOV.L @(disp,GBR),R0
	R0 (Direct register)	ddddddddd: Indirect GBR with displacement	MOV.L R0,@(disp,GBR)
	ddddddddd: PC relative with displacement	R0 (Direct register)	MOVA @(disp,PC),R0
	—	ddddddddd: PC relative	BF label
d12 format 15 0 xxxx dddd dddd dddd	—	ddddddddddddd: PC relative	BRA label (label = disp + PC)
nd8 format 15 0 xxxx nnnn dddd dddd	ddddddddd: PC relative with displacement	nnnn: Direct register	MOV.L @(disp,PC),Rn
i format 15 0 xxxx xxxx iiii iiii	iiiiiiii: Immediate	Indirect indexed GBR	AND.B #imm,@(R0,GBR)
	iiiiiiii: Immediate	R0 (Direct register)	AND #imm,R0
	iiiiiiii: Immediate	—	TRAPA #imm
ni format 15 0 xxxx nnnn iiii iiii	iiiiiiii: Immediate	nnnn: Direct register	ADD #imm,Rn

Note: * In multiply-and-accumulate instructions, nnnn is the source register.

2.5 Instruction Set

2.5.1 Instruction Set by Classification

Table 2.10 lists the instructions according to their classification.

Table 2.10 Classification of Instructions

Classification	Types	Operation Code	Function	No. of Instructions
Data transfer	5	MOV	Data transfer, immediate data transfer, peripheral module data transfer, structure data transfer	39
		MOVA	Effective address transfer	
		MOVT	T bit transfer	
		SWAP	Swap of upper and lower bytes	
		XTRCT	Extraction of the middle of registers connected	
Arithmetic operations	21	ADD	Binary addition	33
		ADDC	Binary addition with carry	
		ADDV	Binary addition with overflow check	
		CMP/cond	Comparison	
		DIV1	Division	
		DIV0S	Initialization of signed division	
		DIV0U	Initialization of unsigned division	
		DMULS	Signed double-length multiplication	
		DMULU	Unsigned double-length multiplication	
		DT	Decrement and test	
		EXTS	Sign extension	
		EXTU	Zero extension	
		MAC	Multiply-and-accumulate, double-length multiply-and-accumulate operation	
		MUL	Double-length multiply operation	
		MULS	Signed multiplication	
		MULU	Unsigned multiplication	
		NEG	Negation	
		NEGC	Negation with borrow	
		SUB	Binary subtraction	
		SUBC	Binary subtraction with borrow	
		SUBV	Binary subtraction with underflow	

Classification	Types	Operation Code	Function	No. of Instructions
Logic operations	6	AND	Logical AND	14
		NOT	Bit inversion	
		OR	Logical OR	
		TAS	Memory test and bit set	
		TST	Logical AND and T bit set	
		XOR	Exclusive OR	
Shift	10	ROTL	One-bit left rotation	14
		ROTR	One-bit right rotation	
		ROTCL	One-bit left rotation with T bit	
		ROTCR	One-bit right rotation with T bit	
		SHAL	One-bit arithmetic left shift	
		SHAR	One-bit arithmetic right shift	
		SHLL	One-bit logical left shift	
		SHLLn	n-bit logical left shift	
		SHLR	One-bit logical right shift	
		SHLRn	n-bit logical right shift	
Branch	9	BF	Conditional branch, conditional branch with delay (Branch when T = 0)	11
		BT	Conditional branch, conditional branch with delay (Branch when T = 1)	
		BRA	Unconditional branch	
		BRAF	Unconditional branch	
		BSR	Branch to subroutine procedure	
		BSRF	Branch to subroutine procedure	
		JMP	Unconditional branch	
		JSR	Branch to subroutine procedure	
		RTS	Return from subroutine procedure	

Classification	Types	Operation Code	Function	No. of Instructions
System control	11	CLRT	T bit clear	31
		CLRMAC	MAC register clear	
		LDC	Load to control register	
		LDS	Load to system register	
		NOP	No operation	
		RTE	Return from exception processing	
		SETT	T bit set	
		SLEEP	Transition to power-down mode	
		STC	Store control register data	
		STS	Store system register data	
		TRAPA	Trap exception handling	
Total:	62			142

The table below shows the format of instruction codes, operation, and execution states. They are described by using this format according to their classification.

Table 2.11 Symbols Used in Instruction Code, Operation, and Execution States Tables

Item	Format	Explanation
Instruction	Described in mnemonic. `OP.Sz SRC,DEST`	OP: Operation code Sz: Size SRC: Source DEST: Destination Rm: Source register Rn: Destination register imm: Immediate data disp: Displacement*2
Instruction code	Described in MSB ↔ LSB order	mmmm: Source register nnnn: Destination register 0000: R0 0001: R1 . . . 1111: R15 iiii: Immediate data dddd: Displacement
Outline of the Operation	→, ←	Direction of transfer
	(xx)	Memory operand
	M/Q/T	Flag bits in the SR
	&	Logical AND of each bit
	|	Logical OR of each bit
	^	Exclusive OR of each bit
	~	Logical NOT of each bit
	<<n	n-bit left shift
	>>n	n-bit right shift
Execution states	—	Value when no wait states are inserted*1
T bit	—	Value of T bit after instruction is executed. An em-dash (—) in the column means no change.

Notes: 1. Instruction execution states: The execution states shown in the table are minimums. The actual number of states may be increased when (1) contention occurs between instruction fetches and data access, or (2) when the destination register of the load instruction (memory → register) equals to the register used by the next instruction.

2. Depending on the operand size, displacement is scaled by ×1, ×2, or ×4. For details, refer the *SH-1/SH-2/SH-DSP Software Manual*.

Data Transfer Instructions

Table 2.12 Data Transfer Instructions

Instruction		Instruction Code	Operation	Execution States	T Bit
MOV	#imm,Rn	1110nnnniiiiiiii	#imm → Sign extension → Rn	1	—
MOV.W	@(disp,PC),Rn	1001nnnndddddddd	(disp × 2 + PC) → Sign extension → Rn	1	—
MOV.L	@(disp,PC),Rn	1101nnnndddddddd	(disp × 4 + PC) → Rn	1	—
MOV	Rm,Rn	0110nnnnmmmm0011	Rm → Rn	1	—
MOV.B	Rm,@Rn	0010nnnnmmmm0000	Rm → (Rn)	1	—
MOV.W	Rm,@Rn	0010nnnnmmmm0001	Rm → (Rn)	1	—
MOV.L	Rm,@Rn	0010nnnnmmmm0010	Rm → (Rn)	1	—
MOV.B	@Rm,Rn	0110nnnnmmmm0000	(Rm) → Sign extension → Rn	1	—
MOV.W	@Rm,Rn	0110nnnnmmmm0001	(Rm) → Sign extension → Rn	1	—
MOV.L	@Rm,Rn	0110nnnnmmmm0010	(Rm) → Rn	1	—
MOV.B	Rm,@–Rn	0010nnnnmmmm0100	Rn–1 → Rn, Rm → (Rn)	1	—
MOV.W	Rm,@–Rn	0010nnnnmmmm0101	Rn–2 → Rn, Rm → (Rn)	1	—
MOV.L	Rm,@–Rn	0010nnnnmmmm0110	Rn–4 → Rn, Rm → (Rn)	1	—
MOV.B	@Rm+,Rn	0110nnnnmmmm0100	(Rm) → Sign extension → Rn,Rm + 1 → Rm	1	—
MOV.W	@Rm+,Rn	0110nnnnmmmm0101	(Rm) → Sign extension → Rn,Rm + 2 → Rm	1	—
MOV.L	@Rm+,Rn	0110nnnnmmmm0110	(Rm) → Rn,Rm + 4 → Rm	1	—
MOV.B	R0,@(disp,Rn)	10000000nnnndddd	R0 → (disp + Rn)	1	—
MOV.W	R0,@(disp,Rn)	10000001nnnndddd	R0 → (disp × 2 + Rn)	1	—
MOV.L	Rm,@(disp,Rn)	0001nnnnmmmmdddd	Rm → (disp × 4 + Rn)	1	—
MOV.B	@(disp,Rm),R0	10000100mmmmdddd	(disp + Rm) → Sign extension → R0	1	—
MOV.W	@(disp,Rm),R0	10000101mmmmdddd	(disp × 2 + Rm) → Sign extension → R0	1	—
MOV.L	@(disp,Rm),Rn	0101nnnnmmmmdddd	(disp × 4 + Rm) → Rn	1	—
MOV.B	Rm,@(R0,Rn)	0000nnnnmmmm0100	Rm → (R0 + Rn)	1	—

Instruction	Instruction Code	Operation	Execution States	T Bit
MOV.W Rm,@(R0,Rn)	0000nnnnmmmm0101	Rm → (R0 + Rn)	1	—
MOV.L Rm,@(R0,Rn)	0000nnnnmmmm0110	Rm → (R0 + Rn)	1	—
MOV.B @(R0,Rm),Rn	0000nnnnmmmm1100	(R0 + Rm) → Sign extension → Rn	1	—
MOV.W @(R0,Rm),Rn	0000nnnnmmmm1101	(R0 + Rm) → Sign extension → Rn	1	—
MOV.L @(R0,Rm),Rn	0000nnnnmmmm1110	(R0 + Rm) → Rn	1	—
MOV.B R0,@(disp,GBR)	11000000dddddddd	R0 → (disp + GBR)	1	—
MOV.W R0,@(disp,GBR)	11000001dddddddd	R0 → (disp × 2 + GBR)	1	—
MOV.L R0,@(disp,GBR)	11000010dddddddd	R0 → (disp × 4 + GBR)	1	—
MOV.B @(disp,GBR),R0	11000100dddddddd	(disp + GBR) → Sign extension → R0	1	—
MOV.W @(disp,GBR),R0	11000101dddddddd	(disp × 2 + GBR) → Sign extension → R0	1	—
MOV.L @(disp,GBR),R0	11000110dddddddd	(disp × 4 + GBR) → R0	1	—
MOVA @(disp,PC),R0	11000111dddddddd	disp × 4 + PC → R0	1	—
MOVT Rn	0000nnnn00101001	T → Rn	1	—
SWAP.B Rm,Rn	0110nnnnmmmm1000	Rm → Swap bottom two bytes → Rn	1	—
SWAP.W Rm,Rn	0110nnnnmmmm1001	Rm → Swap two consecutive words → Rn	1	—
XTRCT Rm,Rn	0010nnnnmmmm1101	Rm: Middle 32 bits of Rn → Rn	1	—

Arithmetic Operation Instructions

Table 2.13 Arithmetic Operation Instructions

Instruction		Instruction Code	Operation	Execution States	T Bit
ADD	Rm,Rn	0011nnnnmmmm1100	Rn + Rm → Rn	1	—
ADD	#imm,Rn	0111nnnniiiiiiii	Rn + imm → Rn	1	—
ADDC	Rm,Rn	0011nnnnmmmm1110	Rn + Rm + T → Rn, Carry → T	1	Carry
ADDV	Rm,Rn	0011nnnnmmmm1111	Rn + Rm → Rn, Overflow → T	1	Overflow
CMP/EQ	#imm,R0	10001000iiiiiiii	If R0 = imm, 1 → T	1	Comparison result
CMP/EQ	Rm,Rn	0011nnnnmmmm0000	If Rn = Rm, 1 → T	1	Comparison result
CMP/HS	Rm,Rn	0011nnnnmmmm0010	If Rn ≥ Rm with unsigned data, 1 → T	1	Comparison result
CMP/GE	Rm,Rn	0011nnnnmmmm0011	If Rn ≥ Rm with signed data, 1 → T	1	Comparison result
CMP/HI	Rm,Rn	0011nnnnmmmm0110	If Rn > Rm with unsigned data, 1 → T	1	Comparison result
CMP/GT	Rm,Rn	0011nnnnmmmm0111	If Rn > Rm with signed data, 1 → T	1	Comparison result
CMP/PL	Rn	0100nnnn00010101	If Rn > 0, 1 → T	1	Comparison result
CMP/PZ	Rn	0100nnnn00010001	If Rn ≥ 0, 1 → T	1	Comparison result
CMP/STR	Rm,Rn	0010nnnnmmmm1100	If Rn and Rm have an equivalent byte, 1 → T	1	Comparison result
DIV1	Rm,Rn	0011nnnnmmmm0100	Single-step division (Rn ÷ Rm)	1	Calculation result
DIV0S	Rm,Rn	0010nnnnmmmm0111	MSB of Rn → Q, MSB of Rm → M, M ^ Q → T	1	Calculation result
DIV0U		0000000000011001	0 → M/Q/T	1	0
DMULS.L	Rm,Rn	0011nnnnmmmm1101	Signed operation of Rn × Rm → MACH, MACL 32 × 32 → 64 bits	2 to 4*	—

Instruction		Instruction Code	Operation	Execution States	T Bit
DMULU.L	Rm,Rn	0011nnnnmmmm0101	Unsigned operation of Rn × Rm → MACH, MACL 32 × 32 → 64 bits	2 to 4*	—
DT	Rn	0100nnnn00010000	Rn – 1 → Rn, when Rn is 0, 1 → T. When Rn is nonzero, 0 → T	1	Comparison result
EXTS.B	Rm,Rn	0110nnnnmmmm1110	Byte in Rm is sign-extended → Rn	1	—
EXTS.W	Rm,Rn	0110nnnnmmmm1111	Word in Rm is sign-extended → Rn	1	—
EXTU.B	Rm,Rn	0110nnnnmmmm1100	Byte in Rm is zero-extended → Rn	1	—
EXTU.W	Rm,Rn	0110nnnnmmmm1101	Word in Rm is zero-extended → Rn	1	—
MAC.L	@Rm+,@Rn+	0000nnnnmmmm1111	Signed operation of (Rn) × (Rm) + MAC → MAC 32 × 32 + 64 → 64 bits	3/ (2 to 4)*	—
MAC.W	@Rm+,@Rn+	0100nnnnmmmm1111	Signed operation of (Rn) × (Rm) + MAC → MAC 16 × 16 + 64 → 64 bits	3/(2)*	—
MUL.L	Rm,Rn	0000nnnnmmmm0111	Rn × Rm → MACL, 32 × 32 → 32 bits	2 to 4*	—
MULS.W	Rm,Rn	0010nnnnmmmm1111	Signed operation of Rn × Rm → MACL 16 × 16 → 32 bits	1 to 3*	—
MULU.W	Rm,Rn	0010nnnnmmmm1110	Unsigned operation of Rn × Rm → MACL 16 × 16 → 32 bits	1 to 3*	—
NEG	Rm,Rn	0110nnnnmmmm1011	0 – Rm → Rn	1	—
NEGC	Rm,Rn	0110nnnnmmmm1010	0 – Rm – T → Rn, Borrow → T	1	Borrow
SUB	Rm,Rn	0011nnnnmmmm1000	Rn – Rm → Rn	1	—
SUBC	Rm,Rn	0011nnnnmmmm1010	Rn – Rm – T → Rn, Borrow → T	1	Borrow
SUBV	Rm,Rn	0011nnnnmmmm1011	Rn – Rm → Rn, Underflow → T	1	Overflow

Note: * The normal number of execution states is shown. (The number in parentheses is the number of states when there is contention with the preceding or following instructions.)

Logic Operation Instructions

Table 2.14 Logic Operation Instructions

Instruction		Instruction Code	Operation	Execution States	T Bit
AND	Rm,Rn	0010nnnnmmmm1001	Rn & Rm → Rn	1	—
AND	#imm,R0	11001001iiiiiiii	R0 & imm → R0	1	—
AND.B	#imm,@(R0,GBR)	11001101iiiiiiii	(R0 + GBR) & imm → (R0 + GBR)	3	—
NOT	Rm,Rn	0110nnnnmmmm0111	~Rm → Rn	1	—
OR	Rm,Rn	0010nnnnmmmm1011	Rn | Rm → Rn	1	—
OR	#imm,R0	11001011iiiiiiii	R0 | imm → R0	1	—
OR.B	#imm,@(R0,GBR)	11001111iiiiiiii	(R0 + GBR) | imm → (R0 + GBR)	3	—
TAS.B	@Rn	0100nnnn00011011	If (Rn) is 0, 1 → T; 1 → MSB of (Rn)	4	Test result
TST	Rm,Rn	0010nnnnmmmm1000	Rn & Rm; if the result is 0, 1 → T	1	Test result
TST	#imm,R0	11001000iiiiiiii	R0 & imm; if the result is 0, 1 → T	1	Test result
TST.B	#imm,@(R0,GBR)	11001100iiiiiiii	(R0 + GBR) & imm; if the result is 0, 1 → T	3	Test result
XOR	Rm,Rn	0010nnnnmmmm1010	Rn ^ Rm → Rn	1	—
XOR	#imm,R0	11001010iiiiiiii	R0 ^ imm → R0	1	—
XOR.B	#imm,@(R0,GBR)	11001110iiiiiiii	(R0 + GBR) ^ imm → (R0 + GBR)	3	—

Shift Instructions

Table 2.15 Shift Instructions

Instruction		Instruction Code	Operation	Execution States	T Bit
ROTL	Rn	0100nnnn00000100	T ← Rn ← MSB	1	MSB
ROTR	Rn	0100nnnn00000101	LSB → Rn → T	1	LSB
ROTCL	Rn	0100nnnn00100100	T ← Rn ← T	1	MSB
ROTCR	Rn	0100nnnn00100101	T → Rn → T	1	LSB
SHAL	Rn	0100nnnn00100000	T ← Rn ← 0	1	MSB
SHAR	Rn	0100nnnn00100001	MSB → Rn → T	1	LSB
SHLL	Rn	0100nnnn00000000	T ← Rn ← 0	1	MSB
SHLR	Rn	0100nnnn00000001	0 → Rn → T	1	LSB
SHLL2	Rn	0100nnnn00001000	Rn<<2 → Rn	1	—
SHLR2	Rn	0100nnnn00001001	Rn>>2 → Rn	1	—
SHLL8	Rn	0100nnnn00011000	Rn<<8 → Rn	1	—
SHLR8	Rn	0100nnnn00011001	Rn>>8 → Rn	1	—
SHLL16	Rn	0100nnnn00101000	Rn<<16 → Rn	1	—
SHLR16	Rn	0100nnnn00101001	Rn>>16 → Rn	1	—

Branch Instructions

Table 2.16 Branch Instructions

Instruction		Instruction Code	Operation	Execution States	T Bit
BF	label	10001011dddddddd	If T = 0, disp × 2 + PC → PC; if T = 1, nop	3/1*	—
BF/S	label	10001111dddddddd	Delayed branch, if T = 0, disp × 2 + PC → PC; if T = 1, nop	3/1*	—
BT	label	10001001dddddddd	If T = 1, disp × 2 + PC → PC; if T = 0, nop	3/1*	—
BT/S	label	10001101dddddddd	Delayed branch, if T = 1, disp × 2 + PC → PC; if T = 0, nop	2/1*	—
BRA	label	1010dddddddddddd	Delayed branch, disp × 2 + PC → PC	2	—
BRAF	Rm	0000mmmm00100011	Delayed branch, Rm + PC → PC	2	—
BSR	label	1011dddddddddddd	Delayed branch, PC → PR, disp × 2 + PC → PC	2	—
BSRF	Rm	0000mmmm00000011	Delayed branch, PC → PR, Rm + PC → PC	2	—
JMP	@Rm	0100mmmm00101011	Delayed branch, Rm → PC	2	—
JSR	@Rm	0100mmmm00001011	Delayed branch, PC → PR, Rm → PC	2	—
RTS		0000000000001011	Delayed branch, PR → PC	2	—

Note: * One state when the program does not branch.

System Control Instructions

Table 2.17 System Control Instructions

Instruction		Instruction Code	Operation	Execution States	T Bit
CLRT		0000000000001000	0 → T	1	0
CLRMAC		0000000000101000	0 → MACH, MACL	1	—
LDC	Rm,SR	0100mmmm00001110	Rm → SR	1	LSB
LDC	Rm,GBR	0100mmmm00011110	Rm → GBR	1	—
LDC	Rm,VBR	0100mmmm00101110	Rm → VBR	1	—
LDC.L	@Rm+,SR	0100mmmm00000111	(Rm) → SR, Rm + 4 → Rm	3	LSB
LDC.L	@Rm+,GBR	0100mmmm00010111	(Rm) → GBR, Rm + 4 → Rm	3	—
LDC.L	@Rm+,VBR	0100mmmm00100111	(Rm) → VBR, Rm + 4 → Rm	3	—
LDS	Rm,MACH	0100mmmm00001010	Rm → MACH	1	—
LDS	Rm,MACL	0100mmmm00011010	Rm → MACL	1	—
LDS	Rm,PR	0100mmmm00101010	Rm → PR	1	—
LDS.L	@Rm+,MACH	0100mmmm00000110	(Rm) → MACH, Rm + 4 → Rm	1	—
LDS.L	@Rm+,MACL	0100mmmm00010110	(Rm) → MACL, Rm + 4 → Rm	1	—
LDS.L	@Rm+,PR	0100mmmm00100110	(Rm) → PR, Rm + 4 → Rm	1	—
NOP		0000000000001001	No operation	1	—
RTE		0000000000101011	Delayed branch, stack area → PC/SR	4	—
SETT		0000000000011000	1 → T	1	1
SLEEP		0000000000011011	Sleep	3*	—
STC	SR,Rn	0000nnnn00000010	SR → Rn	1	—
STC	GBR,Rn	0000nnnn00010010	GBR → Rn	1	—
STC	VBR,Rn	0000nnnn00100010	VBR → Rn	1	—
STC.L	SR,@-Rn	0100nnnn00000011	Rn – 4 → Rn, SR → (Rn)	2	—
STC.L	GBR,@-Rn	0100nnnn00010011	Rn – 4 → Rn, GBR → (Rn)	2	—
STC.L	VBR,@-Rn	0100nnnn00100011	Rn – 4 → Rn, VBR → (Rn)	2	—
STS	MACH,Rn	0000nnnn00001010	MACH → Rn	1	—
STS	MACL,Rn	0000nnnn00011010	MACL → Rn	1	—
STS	PR,Rn	0000nnnn00101010	PR → Rn	1	—
STS.L	MACH,@-Rn	0100nnnn00000010	Rn – 4 → Rn, MACH → (Rn)	1	—

Instruction	Instruction Code	Operation	Execution States	T Bit
STS.L MACL,@-Rn	0100nnnn00010010	Rn – 4 → Rn, MACL → (Rn)	1	—
STS.L PR,@-Rn	0100nnnn00100010	Rn – 4 → Rn, PR → (Rn)	1	—
TRAPA #imm	11000011iiiiiiii	PC/SR → stack area, (imm × 4 + VBR) → PC	8	—

Note: * The number of execution states before the chip enters sleep mode: The execution states shown in the table are minimums. The actual number of states may be increased when (1) contention occurs between instruction fetches and data access, or (2) when the destination register of the load instruction (memory → register) equals to the register used by the next instruction.

2.6 Processing States

2.6.1 State Transitions

The CPU has five processing states: reset, exception processing, bus release, program execution, and power-down. Figure 2.4 shows the transitions between the states.

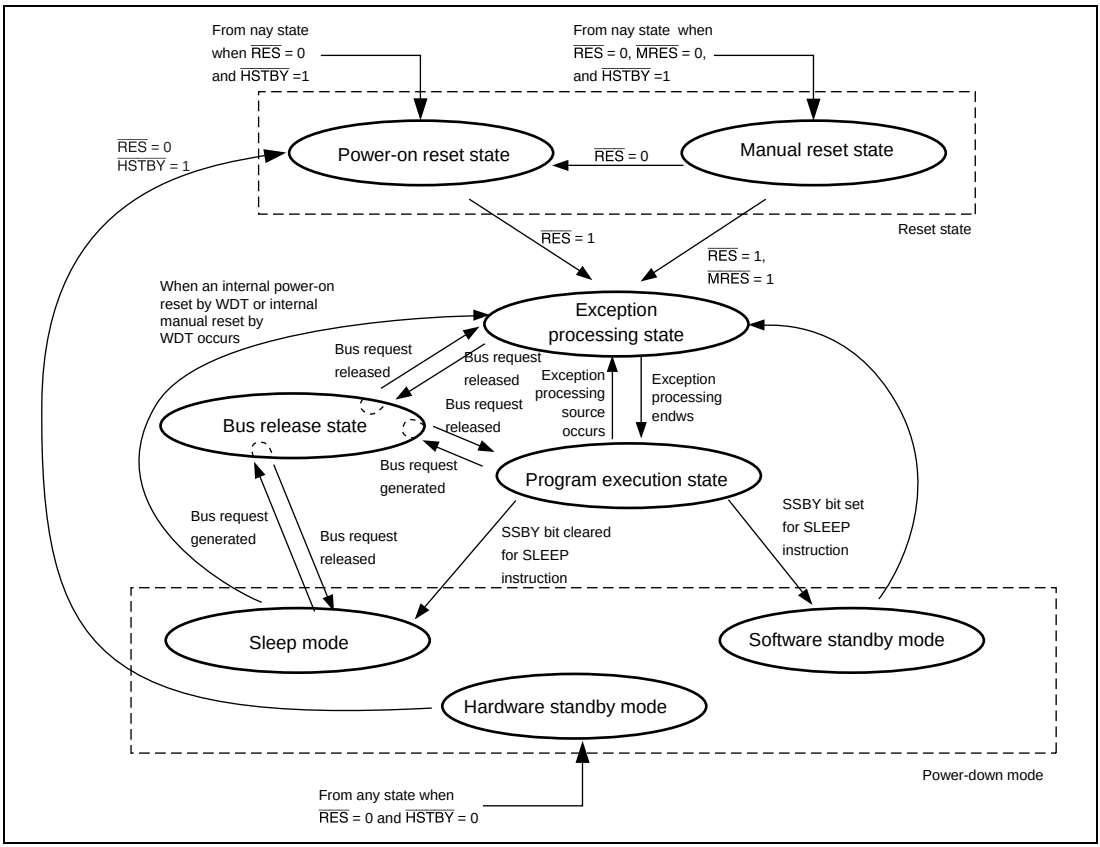


Figure 2.4 Transitions between Processing States

Reset State: The CPU resets in the reset state. When the $\overline{\text{RES}}$ pin level goes low, the power-on reset state is entered. When the $\overline{\text{RES}}$ pin is high and the $\overline{\text{MRES}}$ pin is low, the manual reset state is entered. When the $\overline{\text{HSTBY}}$ pin is driven high and the $\overline{\text{RES}}$ pin level goes low, the power-on reset state is entered.

Exception Processing State: The exception processing state is a transient state that occurs when exception processing sources such as resets or interrupts alter the CPU's processing state flow.

For a reset, the initial values of the program counter (PC) (execution start address) and stack pointer (SP) are fetched from the exception processing vector table and stored; the CPU then branches to the execution start address and execution of the program begins.

For an interrupt, the stack pointer (SP) is accessed and the program counter (PC) and status register (SR) are saved to the stack area. The exception service routine start address is fetched from the exception processing vector table; the CPU then branches to that address and the program starts executing, thereby entering the program execution state.

Program Execution State: In the program execution state, the CPU sequentially executes the program.

Power-Down State: In the power-down state, the CPU operation halts and power consumption declines. The SLEEP instruction places the CPU in the sleep mode or the software standby mode. If the $\overline{\text{HSTBY}}$ pin is driven low when the $\overline{\text{RES}}$ pin is low, the CPU will enter the hardware standby mode.

Bus Release State: In the bus release state, the CPU releases access rights to the bus to the device that has requested them.

Section 3 MCU Operating Modes

3.1 Selection of Operating Modes

This LSI has four operating modes and four clock modes. The operating mode is determined by the settings of MD3 to MD0, and FWP pins. Do not change these pins during LSI operation (while power is on). Do not set these pins in the other way than the combination shown in table 3.1.

Table 3.1 Selection of Operating Modes

	Pin Settings								Product Type	
Mode No.	FWP	MD3	MD2	MD1	MD0	Mode Name	On-Chip ROM	BusWidth of CS0 Space	SH7108 SH7106 SH7104 SH7101	SH7109 SH7107 SH7105
Mode 0	1	x	x	0	0	MCU extended mode 0	Disabled	8 bits	—	Supported
Mode 1*	1	x	x	0	1	MCU extended mode 1	Disabled	—	—	—
Mode 2	1	x	x	1	0	MCU extended mode 2	Enabled	Set by BCR1 in BSC	—	Supported
Mode 3	1	x	x	1	1	Single-chip mode	Enabled	—	Supported	Supported

Notes: The symbol x means “Don’t care”.

* This mode cannot be used for this LSI.

There are two modes as the MCU operating modes: MCU extended mode and single-chip mode.

The clock mode is selected by the input of MD2 and MD3 pins.

Table 3.2 Maximum Operating Clock Frequency for Each Clock Mode

Pin Settings		
MD3	**MD2**	**Maximum Operating Clock Frequency**
0	0	12.5 MHz (Input clock × 1*, maximum of input clock: 12.5 MHz)
0	1	25 MHz (Input clock × 2*, maximum of input clock: 12.5 MHz)
1	0	40 MHz (Input clock × 4*, maximum of input clock: 10 MHz)
1	1	50 MHz (Input clock × 4 for system clock, Input clock × 2 for peripheral clock, maximum of input clock: 12.5 MHz)

Note: * The frequencies for the system and peripheral module clocks are the same.

3.2 Input/Output Pins

Table 3.3 describes the configuration of operating mode related pins.

Table 3.3 Pin Configuration

Pin Name	Input/Output	Function
MD0	Input	Designates operating mode through the level applied to this pin
MD1	Input	Designates operating mode through the level applied to this pin
MD2	Input	Designates clock mode through the level applied to this pin
MD3	Input	Designates clock mode through the level applied to this pin
FWP	Input	Pin for the hardware protection against programming/erasing the on-chip flash memory

3.3 Explanation of Operating Modes

3.3.1 Mode 0 (MCU Extended Mode 0)

The CS0 space becomes an external memory space with 8-bit bus width in mode 0. This mode is not supported in the SH7108/SH7106/SH7104/SH7101.

3.3.2 Mode 1 (MCU Extended Mode 1)

This mode is not supported in this LSI.

3.3.3 Mode 2 (MCU Extended Mode 2)

The on-chip ROM is enabled and the CS0 space can be used in mode 2. This mode is not supported in the SH7108/SH7106/SH7104/SH7101.

3.3.4 Mode 3 (Single-Chip Mode)

All ports can be used in mode 3, however the external address cannot be used. The SH7108/SH7106/SH7104/SH7101 supports only this mode.

3.3.5 Clock Mode

The input waveform frequency can be used as is, doubled, or quadrupled as system clock frequency in mode 0 to mode 3.

3.4 Address Map

The address map for the operating modes are shown in figures 3.1 to 3.6.

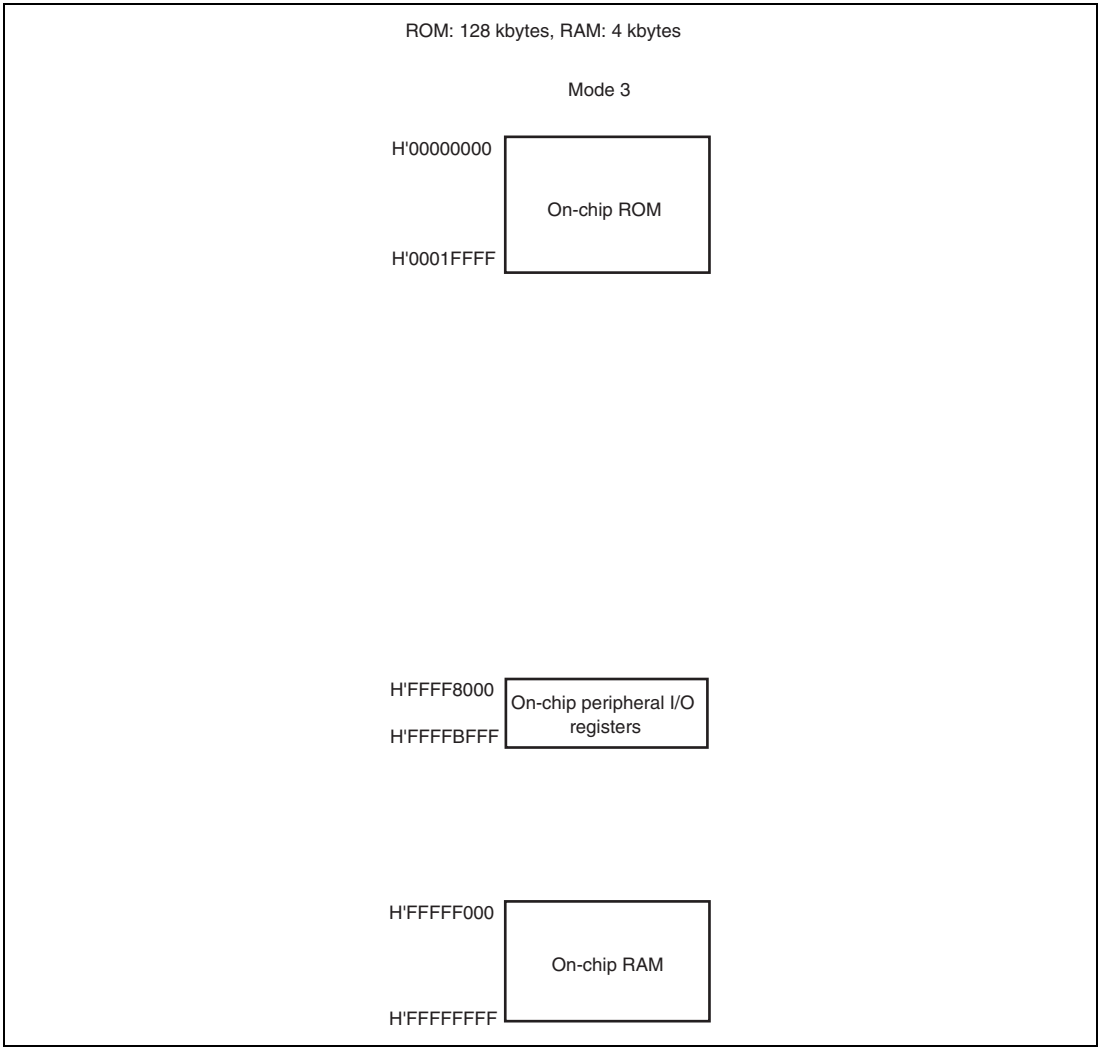


Figure 3.1 Address Map of SH7108

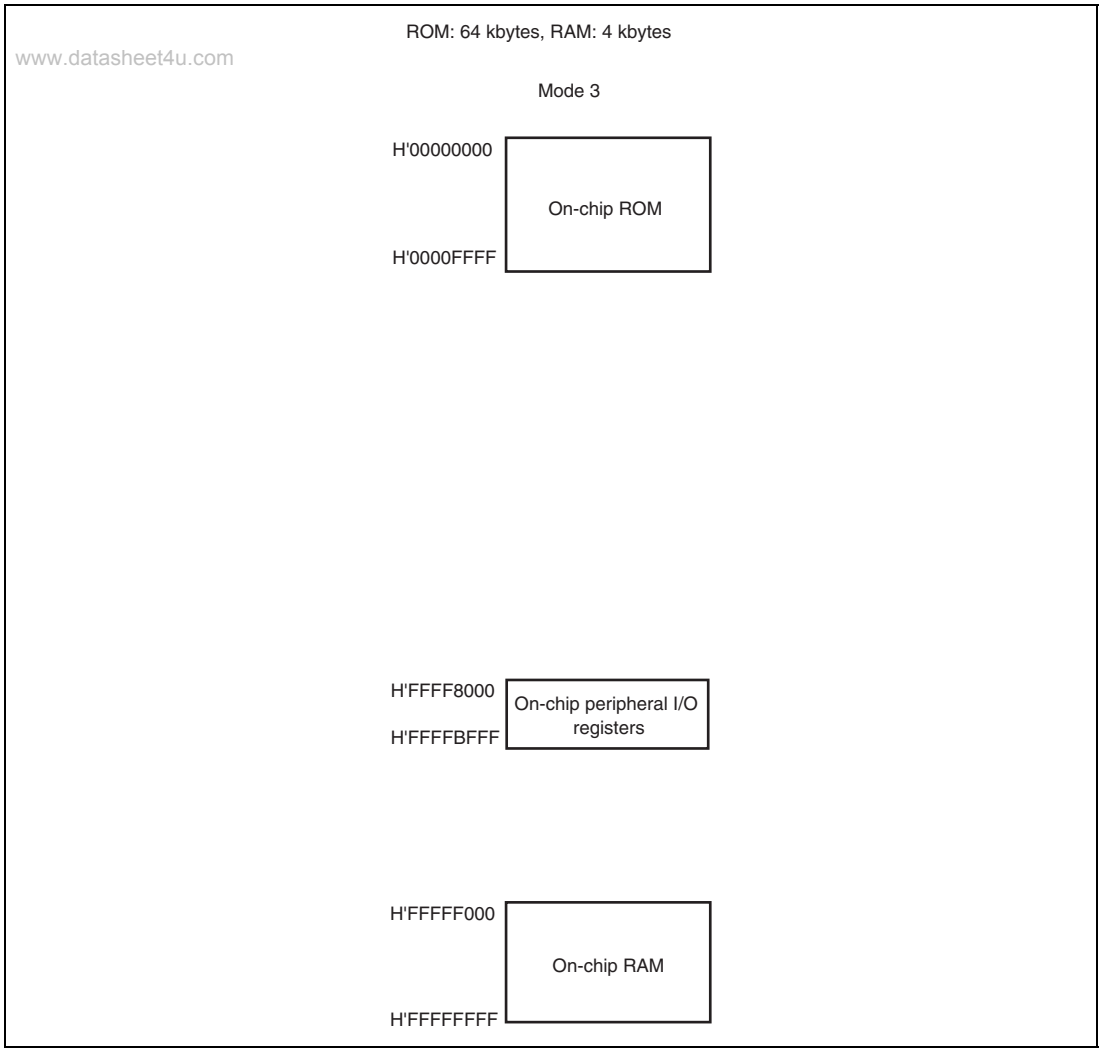


Figure 3.2 Address Map of SH7106

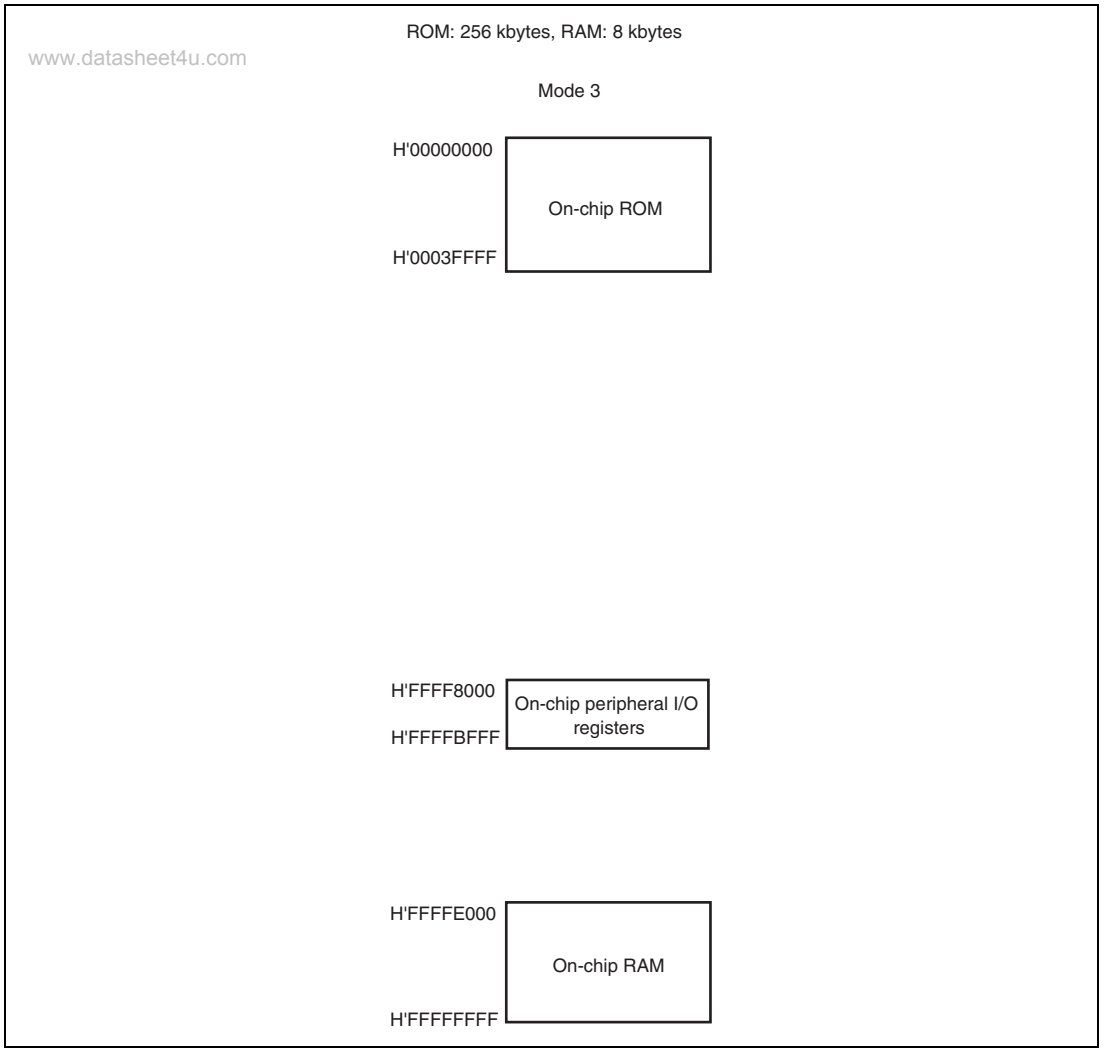


Figure 3.3 Address Map of SH7104

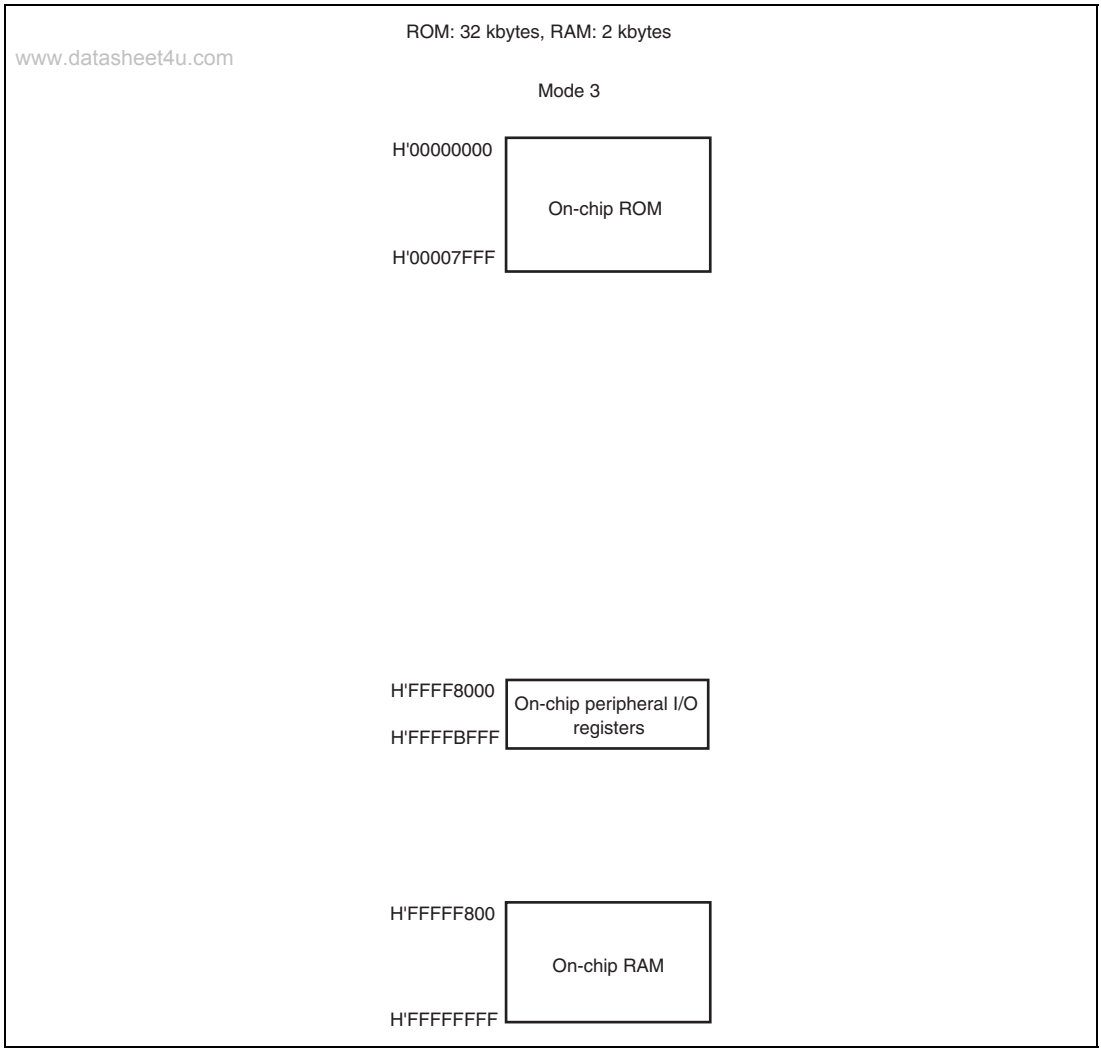


Figure 3.4 Address Map of SH7101

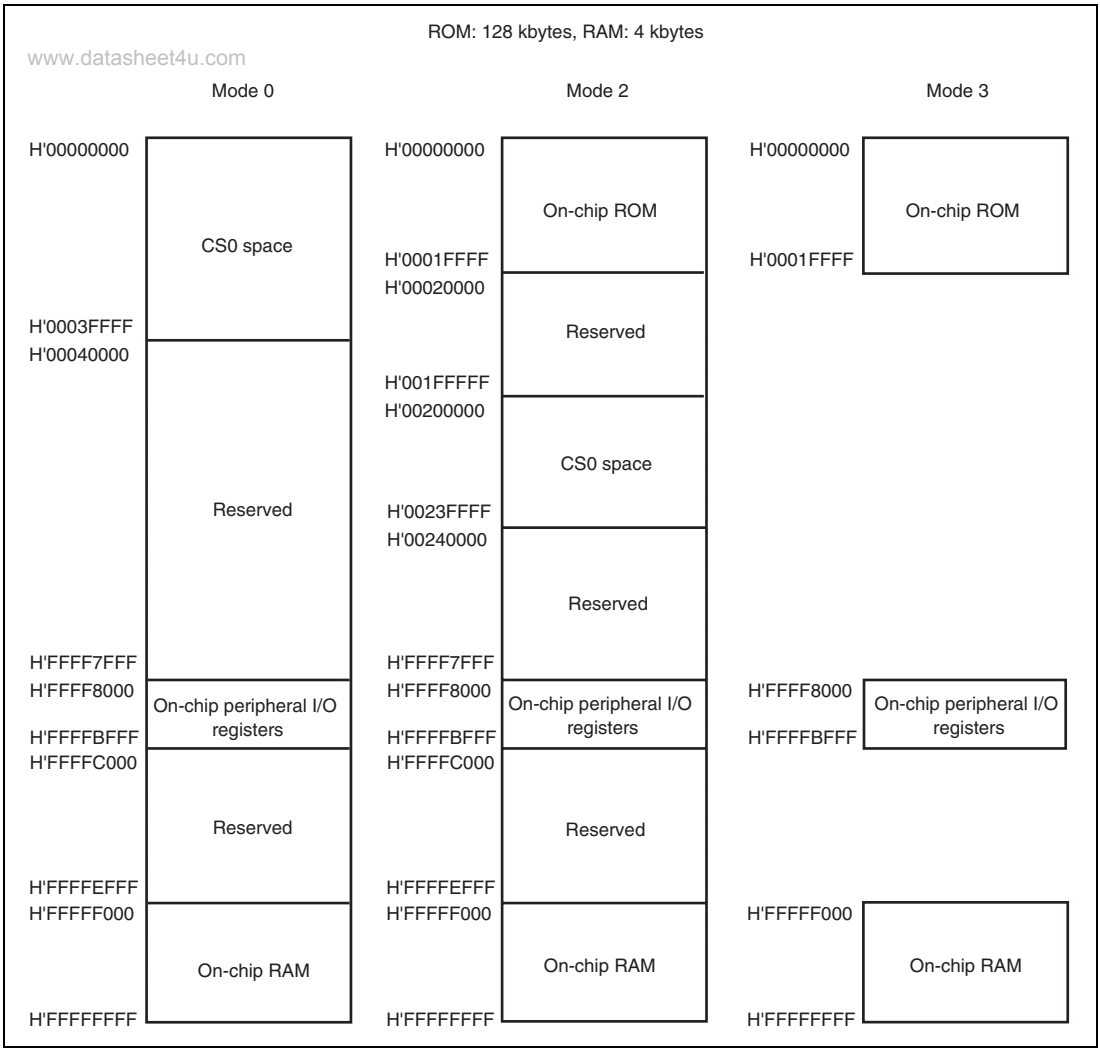


Figure 3.5 Address Map for Operating Modes of SH7109

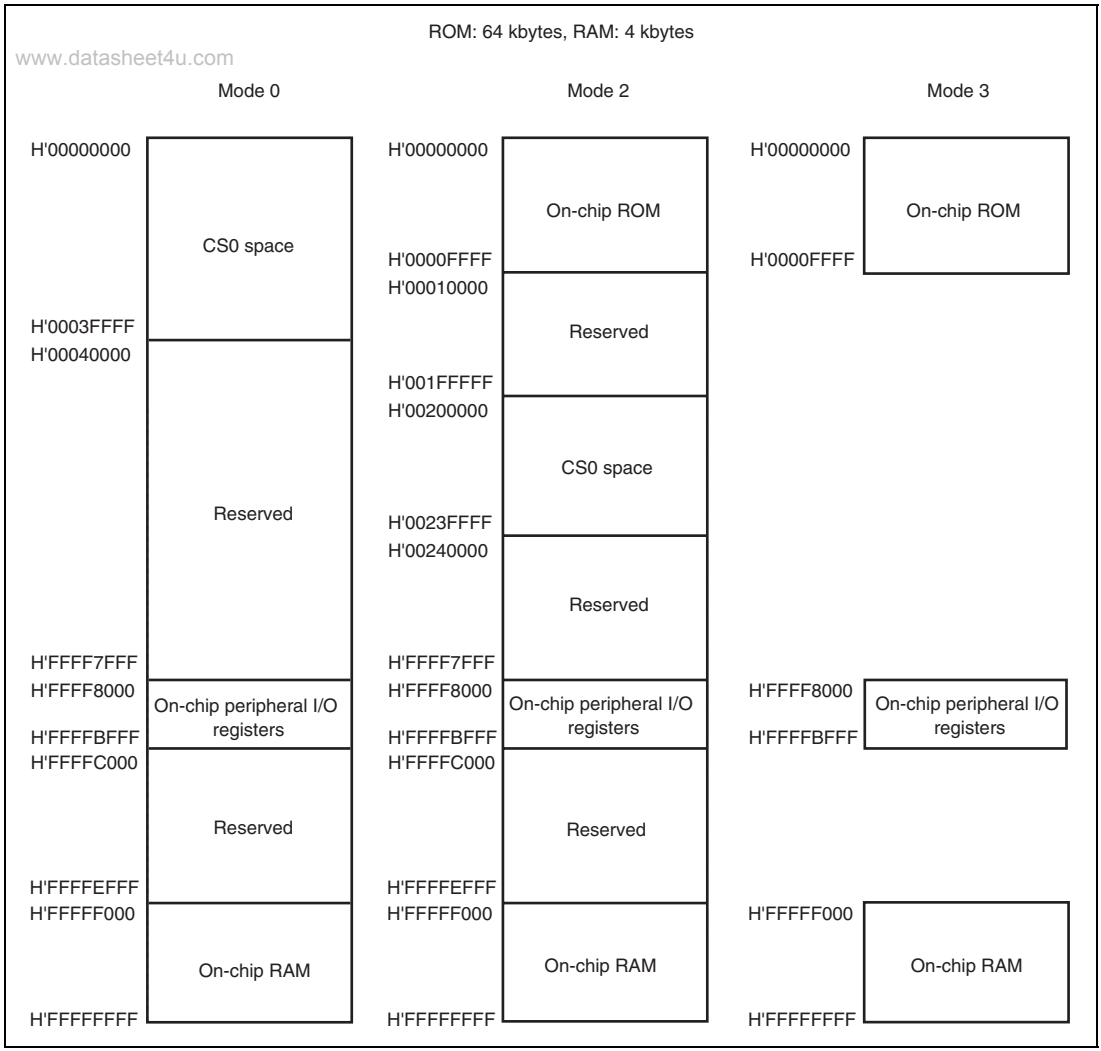


Figure 3.6 Address Map for Operating Modes of SH7107

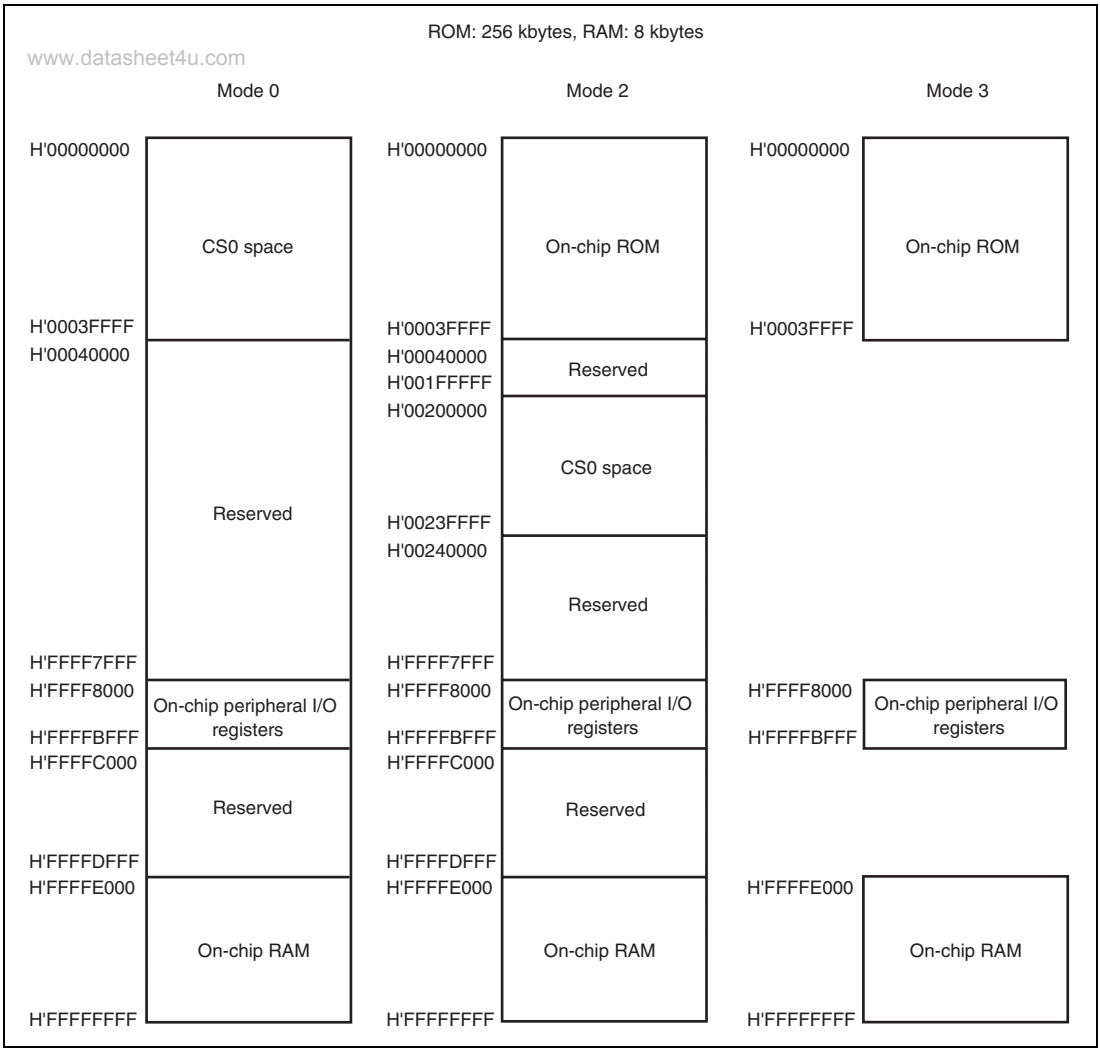


Figure 3.7 Address Map for Operating Modes of SH7105

3.5 Initial State of This LSI

In this LSI, some on-chip modules are set to the module standby state as its initial state for power down.

Therefore, to operate those modules, it is necessary to clear module standby state. For details, refer to section 18, Power-Down Modes.

Section 4 Clock Pulse Generator

This LSI has an on-chip clock pulse generator (CPG) that generates the system clock (ϕ) and peripheral clock (Pϕ) to generate the internal clock (ϕ/2 to ϕ/8192, Pϕ/2 to Pϕ/1024). The CPG consists of an oscillator, PLL circuit, and pre-scaler. A block diagram of the clock pulse generator is shown in figure 4.1. The frequency from the oscillator can be modified by the PLL circuit.

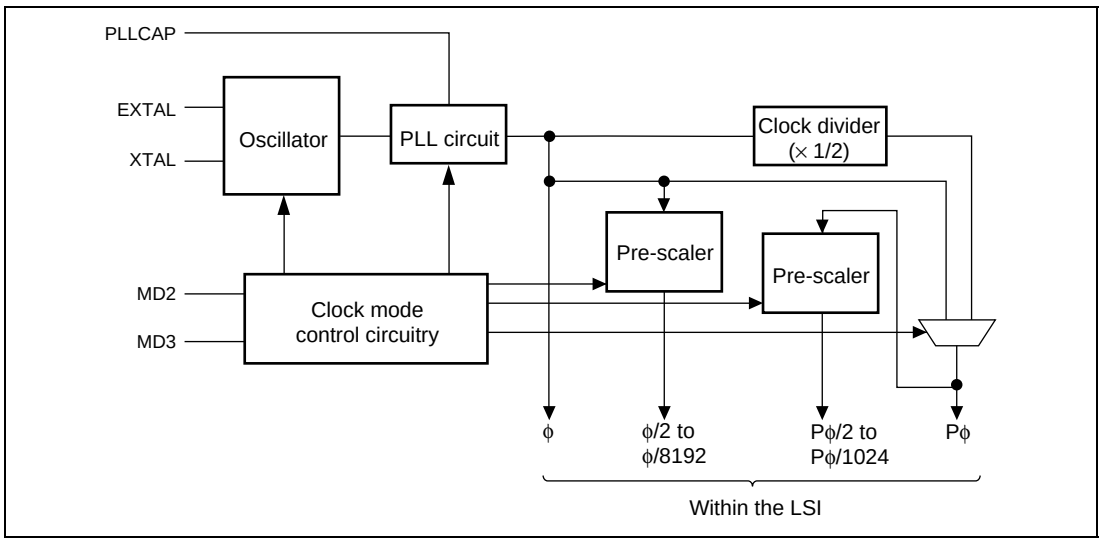


Figure 4.1 Block Diagram of the Clock Pulse Generator

4.1 Oscillator

Clock pulses can be supplied from a connected crystal resonator or an external clock.

4.1.1 Connecting a Crystal Resonator

A crystal resonator can be connected as shown in figure 4.2. Use the damping resistance (Rd) listed in table 4.1. Use an AT-cut parallel-resonance type crystal resonator that has a resonance frequency of 4 to 12.5 MHz. It is recommended to consult crystal dealer concerning the compatibility of the crystal resonator and the LSI.

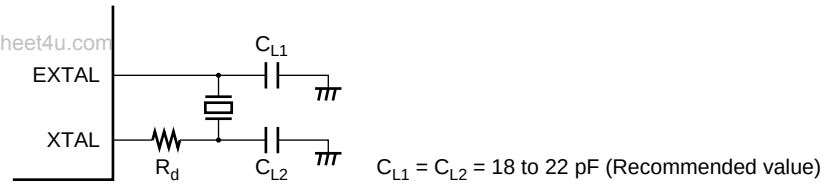


Figure 4.2 Connection of the Crystal Resonator (Example)

Table 4.1 Damping Resistance Values

Frequency (MHz)	4	8	10	12.5
Rd (Ω)	500	200	0	0

Figure 4.3 shows an equivalent circuit of the crystal resonator. Use a crystal resonator with the characteristics listed in table 4.2.

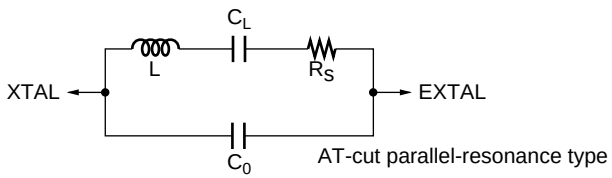


Figure 4.3 Crystal Resonator Equivalent Circuit

Table 4.2 Crystal Resonator Characteristics

Frequency (MHz)	4	8	10	12.5
Rs max (Ω)	120	80	60	50
C_0 max (pF)	7	7	7	7

4.1.2 External Clock Input Method

Figure 4.4 shows an example of an external clock input connection. In this case, make the external clock high level to stop it in standby mode. During operation, make the external input clock frequency 4 to 12.5 MHz.

When leaving the XTAL pin open, make sure the stray capacitance is less than 10 pF.

Even when inputting an external clock, be sure to wait at least the oscillation stabilization time in power-on sequence or in releasing standby mode, in order to ensure the PLL stabilization time.

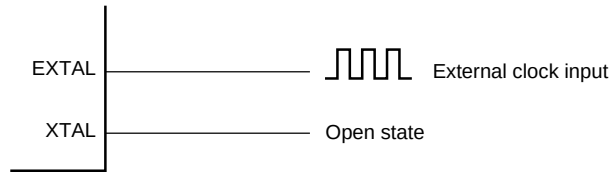


Figure 4.4 Example of External Clock Connection

4.2 Function for Detecting the Oscillator Halt

This CPG can detect a clock halt and automatically cause the timer pins to become high-impedance when any system abnormality causes the oscillator to halt. That is, when a change of EXTAL has not been detected, the high-current 12 pins (PE9/TIOC3B, PE11/TIOC3D, PE12/TIOC4A, PE13/TIOC4B/$\overline{\text{MRES}}$, PE14/TIOC4C, PE15/TIOC4D/$\overline{\text{IRQOUT}}$, PE16/PUOA, PE17/PVOA, PE18/PWOA, PE19/PUOB, PE20/PVOB, PE21/PWOB) are set to high-impedance regardless of PFC setting.

Even in standby mode, these 12 pins become high-impedance regardless of PFC setting. These pins enter the normal state after standby mode is released. When abnormalities that halt the oscillator occur except in standby mode, other LSI operations become undefined. In this case, LSI operations, including these 12 pins, become undefined even when the oscillator operation starts again.

4.3 Usage Notes

4.3.1 Note on Crystal Resonator

A sufficient evaluation at the user's site is necessary to use the LSI, by referring the resonator connection examples shown in this section, because various characteristics related to the crystal resonator are closely linked to the user's board design. Since the resonator circuit component values depend on the resonator itself, floating capacitances in the application circuit, and other factors, we recommend consulting with the resonator manufacturer to determine the circuit component values used. Ensure that a voltage exceeding the maximum rating is not applied to the oscillator pin.

4.3.2 Notes on Board Design

Measures against radiation noise are taken in this LSI. If radiation noise needs to be further reduced, usage of a multi-layer printed circuit board with ground planes is recommended.

When using a crystal resonator, place the crystal resonator and its load capacitors as close as possible to the XTAL and EXTAL pins. Do not route any signal lines near the oscillator circuitry as shown in figure 4.5. Otherwise, correct oscillation can be interfered by induction.

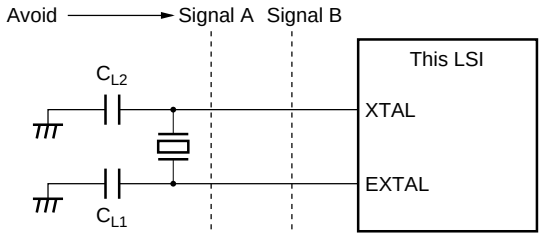
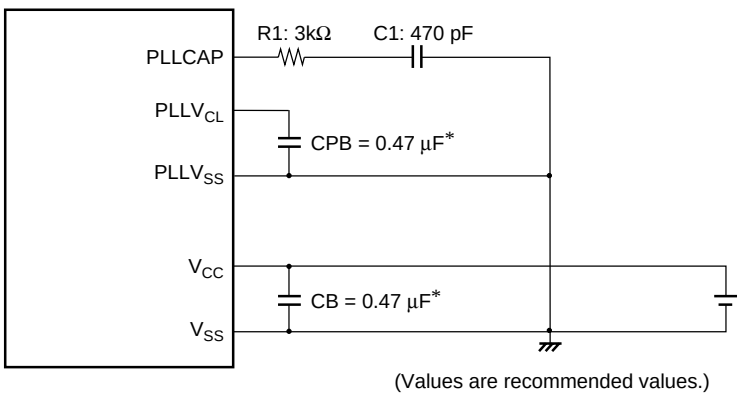


Figure 4.5 Cautions for Oscillator Circuit System Board Design

A circuitry shown in figure 4.6 is recommended as an external circuitry around the PLL. Place oscillation stabilization capacitor C1 close to the PLLCAP pin, and ensure that no other signal lines cross this line. Separate PLLVCL and PLLVSS circuit against VCC and VSS circuit from the board power-supply source, and be sure to insert bypass capacitors CB and CPB close to the pins.



Note: * CB and CPB are laminated ceramic type.

Figure 4.6 Recommended External Circuitry Around the PLL

Electromagnetic waves are radiated from an LSI in operation. This LSI has an electromagnetic peak in the harmonics band whose primary frequency is determined by the lower frequency between the system clock (ϕ) and peripheral clock (Pϕ). For example, when ϕ = 50 MHz and Pϕ = 40 MHz, the primary frequency is 40 MHz. If this LSI is used adjacent to a device sensitive to electromagnetic interference, e.g. FM/VHF band receiver, a printed circuit board of more than four layers with planes exclusively for system ground is recommended.

Section 5 Exception Processing

5.1 Overview

5.1.1 Types of Exception Processing and Priority

Exception processing is started by four sources: resets, address errors, interrupts and instructions and have the priority, as shown in table 5.1. When several exception processing sources occur at once, they are processed according to the priority.

Table 5.1 Types of Exception Processing and Priority

Exception	Source		Priority
Reset	Power-on reset		High
	Manual reset		
Address error	CPU address error		
Interrupt	NMI		
	IRQ		
	On-chip peripheral modules:	• Multifunction timer pulse unit (MTU) • A/D converter 0 and 1 (A/D0, A/D1) • Compare match timer 0 and 1 (CMT0, CMT1) • Watchdog timer (WDT) • Input/output port (I/O) (MTU) • Serial communication interface 2 and 3 (SCI2 and SCI3) • Motor management timer (MMT) • A/D converter 2 (A/D2) • Input/output port (I/O) (MMT)	
Instructions	Trap instruction (TRAPA instruction)		
	General illegal instructions (undefined code)		
	Illegal slot instructions (undefined code placed directly after a delay branch instruction*1 or instructions that rewrite the PC*2)		Low

Notes: 1. Delayed branch instructions: JMP, JSR, BRA, BSR, RTS, RTE, BF/S, BT/S, BSRF, and BRAF.

2. Instructions that rewrite the PC: JMP, JSR, BRA, BSR, RTS, RTE, BT, BF, TRAPA, BF/S, BT/S, BSRF, and BRAF.

5.1.2 Exception Processing Operations

The exception processing sources are detected and the processing starts according to the timing shown in table 5.2.

Table 5.2 Timing for Exception Source Detection and Start of Exception Processing

Exception	Source	Timing of Source Detection and Start of Processing
Reset	Power-on reset	Starts when the $\overline{\text{RES}}$ pin changes from low to high or when WDT overflows.
	Manual reset	Starts when the $\overline{\text{MRES}}$ pin changes from low to high.
Address error		Detected when instruction is decoded and starts when the execution of the previous instruction is completed.
Interrupts		
Instructions	Trap instruction	Starts from the execution of a TRAPA instruction.
	General illegal instructions	Starts from the decoding of undefined code anytime except after a delayed branch instruction (delay slot).
	Illegal slot instructions	Starts from the decoding of undefined code placed in a delayed branch instruction (delay slot) or of instructions that rewrite the PC.

When exception processing starts, the CPU operates as follows:

1. Exception processing triggered by reset:

   The initial values of the program counter (PC) and stack pointer (SP) are fetched from the exception processing vector table (PC and SP are respectively the H'00000000 and H'00000004 addresses for power-on resets and the H'00000008 and H'0000000C addresses for manual resets). See section 5.1.3, Exception Processing Vector Table, for more information. H'00000000 is then written to the vector base register (VBR) , and H'F (B'1111) is written to the interrupt mask bits (I3 to I0) of the status register (SR). The program begins running from the PC address fetched from the exception processing vector table.
2. Exception processing triggered by address errors, interrupts and instructions:

   SR and PC are saved to the stack indicated by R15. For interrupt exception processing, the interrupt priority level is written to the SR's interrupt mask bits (I3 to I0). For address error and instruction exception processing, the I3 to I0 bits are not affected. The start address is then fetched from the exception processing vector table and the program begins running from that address.

5.1.3 Exception Processing Vector Table

Before exception processing begins running, the exception processing vector table must be set in memory. The exception processing vector table stores the start addresses of exception service routines. (The reset exception processing table holds the initial values of PC and SP.)

All exception sources are given different vector numbers and vector table address offsets. The vector table addresses are calculated from these vector numbers and vector table address offsets. During exception processing, the start addresses of the exception service routines are fetched from the exception processing vector table that is indicated by this vector table address.

Table 5.3 shows the vector numbers and vector table address offsets. Table 5.4 shows how vector table addresses are calculated.

Table 5.3 Exception Processing Vector Table

Exception Sources		Vector Numbers	Vector Table Address Offset
Power-on reset	PC	0	H'00000000 to H'00000003
	SP	1	H'00000004 to H'00000007
Manual reset	PC	2	H'00000008 to H'0000000B
	SP	3	H'0000000C to H'0000000F
General illegal instruction		4	H'00000010 to H'00000013
(Reserved by system)		5	H'00000014 to H'00000017
Slot illegal instruction		6	H'00000018 to H'0000001B
(Reserved by system)		7	H'0000001C to H'0000001F
		8	H'00000020 to H'00000023
CPU address error		9	H'00000024 to H'00000027
(Reserved by system)		10	H'00000028 to H'0000002B
Interrupts	NMI	11	H'0000002C to H'0000002F
(Reserved by system)		12	H'00000030 to H'00000033
		13	H'00000034 to H'00000037
		14	H'00000038 to H'0000003B
		15	H'0000003C to H'0000003F
		:	:
		31	H'0000007C to H'0000007F
Trap instruction (user vector)		32	H'00000080 to H'00000083
		:	:
		63	H'000000FC to H'000000FF

Exception Sources		Vector Numbers	Vector Table Address Offset
Interrupts	IRQ0	64	H'00000100 to H'00000103
	IRQ1	65	H'00000104 to H'00000107
	IRQ2	66	H'00000108 to H'0000010B
	IRQ3	67	H'0000010C to H'0000010F
	Reserved by system	68	H'00000110 to H'00000113
		69	H'00000114 to H'00000117
		70	H'00000118 to H'0000011B
		71	H'0000011C to H'0000011F
On-chip peripheral module*		72	H'00000120 to H'00000123
		:	:
		255	H'000003FC to H'000003FF

Note: * The vector numbers and vector table address offsets for each on-chip peripheral module interrupt are given in section 6, Interrupt Controller, and table 6.2, Interrupt Exception Sources, Vector Addresses and Priorities.

Table 5.4 Calculating Exception Processing Vector Table Addresses

Exception Source	Vector Table Address Calculation
Resets	Vector table address = (vector table address offset) = (vector number) × 4
Address errors, interrupts, instructions	Vector table address = VBR + (vector table address offset) = VBR + (vector number) × 4

Notes: 1. VBR: Vector base register
2. Vector table address offset: See table 5.3.
3. Vector number: See table 5.3.

5.2 Resets

5.2.1 Types of Reset

Resets have the highest priority of any exception source. There are two types of resets: manual resets and power-on resets. As table 5.5 shows, both types of resets initialize the internal status of the CPU. In power-on resets, all registers of the on-chip peripheral modules are initialized; in manual resets, they are not.

Table 5.5 Reset Status

	Conditions for Transition to Reset Status			Internal Status		
Type	$\overline{\text{RES}}$	WDT Overflow	$\overline{\text{MRES}}$	CPU/INTC	On-Chip Peripheral Module	PFC, IO Port
Power-on reset	Low	—	—	Initialized	Initialized	Initialized
	High	Overflow	High	Initialized	Initialized	Not initialized
Manual reset	High	—	Low	Initialized	Not initialized	Not initialized

5.2.2 Power-On Reset

Power-On Reset by $\overline{\text{RES}}$ Pin: When the $\overline{\text{RES}}$ pin is driven low, the LSI becomes to be a power-on reset state. To reliably reset the LSI, the $\overline{\text{RES}}$ pin should be kept at low for at least the duration of the oscillation settling time when applying power or when in standby mode (when the clock circuit is halted) or at least 25 tcyc when the clock circuit is running. During power-on reset, CPU internal status and all registers of on-chip peripheral modules are initialized. See appendix A, Pin States, for the status of individual pins during the power-on reset status.

In the power-on reset status, power-on reset exception processing starts when the $\overline{\text{RES}}$ pin is first driven low for a set period of time and then returned to high. The CPU will then operate as follows:

1. The initial value (execution start address) of the program counter (PC) is fetched from the exception processing vector table.
2. The initial value of the stack pointer (SP) is fetched from the exception processing vector table.
3. The vector base register (VBR) is cleared to H'00000000 and the interrupt mask bits (I3 to I0) of the status register (SR) are set to H'F (B'1111).
4. The values fetched from the exception processing vector table are set in PC and SP, then the program begins executing.

Be certain to always perform power-on reset processing when turning the system power on.

Power-On Reset by WDT: When a setting is made for a power-on reset to be generated in the WDT's watchdog timer mode, and the WDT's TCNT overflows, the LSI becomes to be a power-on reset state.

The pin function controller (PFC) registers and I/O port registers are not initialized by the reset signal generated by the WDT (these registers are initialized only by a power-on reset from outside of the chip).

If reset caused by the input signal at the $\overline{\text{RES}}$ pin and a reset caused by WDT overflow occur simultaneously, the $\overline{\text{RES}}$ pin reset has priority, and the WOVF bit in RSTCSR is cleared to 0. When WDT-initiated power-on reset processing is started, the CPU operates as follows:

1. The initial value (execution start address) of the program counter (PC) is fetched from the exception processing vector table.
2. The initial value of the stack pointer (SP) is fetched from the exception processing vector table.
3. The vector base register (VBR) is cleared to H'00000000 and the interrupt mask bits (I3 to I0) of the status register (SR) are set to H'F (B'1111).
4. The values fetched from the exception processing vector table are set in the PC and SP, then the program begins executing.

5.2.3 Manual Reset

When the $\overline{\text{RES}}$ pin is high and the $\overline{\text{MRES}}$ pin is driven low, the LSI enters a manual reset state. To reliably reset the LSI, the $\overline{\text{MRES}}$ pin should be kept at low for at least 25 tcyc. During manual reset, the CPU internal status is initialized. Registers of on-chip peripheral modules are not initialized. When the LSI enters manual reset status in the middle of a bus cycle, manual reset exception processing does not start until the bus cycle has ended. Thus, manual resets do not abort bus cycles. However, once $\overline{\text{MRES}}$ is driven low, hold the low level until the CPU becomes to be a manual reset mode after the bus cycle ends. (Keep at low level for at least the longest bus cycle). See appendix A, Pin States, for the status of individual pins during manual reset mode.

In the manual reset status, manual reset exception processing starts when the $\overline{\text{MRES}}$ pin is first kept low for a set period of time and then returned to high. The CPU will then operate in the same procedures as described for power-on resets.

5.3 Address Errors

5.3.1 The Cause of Address Error Exception

Address errors occur when instructions are fetched or data is read or written, as shown in table 5.6.

Table 5.6 Bus Cycles and Address Errors

	Bus Cycle		
Type	**Bus Master**	**Bus Cycle Description**	**Address Errors**
Instruction fetch	CPU	Instruction fetched from even address	None (normal)
		Instruction fetched from odd address	Address error occurs
		Instruction fetched from other than on-chip peripheral module space*	None (normal)
		Instruction fetched from on-chip peripheral module space*	Address error occurs
		Instruction fetched from external memory space when in single chip mode	Address error occurs
Data read/write	CPU	Word data accessed from even address	None (normal)
		Word data accessed from odd address	Address error occurs
		Longword data accessed from a longword boundary	None (normal)
		Longword data accessed from other than a long-word boundary	Address error occurs
		Byte or word data accessed in on-chip peripheral module space*	None (normal)
		Longword data accessed in 16-bit on-chip peripheral module space*	None (normal)
		Longword data accessed in 8-bit on-chip peripheral module space*	Address error occurs
		External memory space accessed when in single chip mode	Address error occurs

Note: * See section 7, Bus State Controller (BSC) for more information on the on-chip peripheral module space.

5.3.2 Address Error Exception Processing

When an address error occurs, the bus cycle in which the address error occurred ends, the current instruction finishes, and then address error exception processing starts. The CPU operates as follows:

1. The status register (SR) is saved to the stack.
2. The program counter (PC) is saved to the stack. The PC value saved is the start address of the instruction to be executed after the last executed instruction.
3. The start address of the exception service routine is fetched from the exception processing vector table that corresponds to the occurred address error, and the program starts executing from that address. The jump in this case is not a delayed branch.

5.4 Interrupts

5.4.1 Interrupt Sources

Table 5.7 shows the sources that start the interrupt exception processing. They are NMI, IRQ, and on-chip peripheral modules.

Table 5.7 Interrupt Sources

Type	Request Source	Number of Sources
NMI	NMI pin (external input)	1
IRQ	$\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$ pins (external input)	4
On-chip peripheral module	Multifunction timer pulse unit	23
	Compare match timer	2
	A/D converter (A/D0 and A/D1)	2
	A/D converter (A/D2)	1
	Serial communication interface	8
	Watchdog timer	1
	Motor management timer	2
	Input/output port	2

Each interrupt source is allocated a different vector number and vector table offset. See section 6, Interrupt Controller (INTC), and table 6.2, Interrupt Exception Sources, Vector Addresses and Priorities, for more information on vector numbers and vector table address offsets.

5.4.2 Interrupt Priority Level

The interrupt priority is predetermined. When multiple interrupts occur simultaneously (overlapped interruptions), the interrupt controller (INTC) determines their relative priorities and starts the exception processing according to the results.

The priority of interrupts is expressed as priority levels 0 to 16, with priority 0 the lowest and priority 16 the highest. The NMI interrupt has priority 16 and cannot be masked, so it is always accepted. IRQ interrupt and on-chip peripheral module interrupt priority levels can be set freely using the INTC's interrupt priority registers A, D to K (IPRA, IPRD to IPRK) as shown in table 5.8. The priority levels that can be set are 0 to 15. Level 16 cannot be set. See section 6.3.4, Interrupt Priority Registers A, D to K (IPRA, IPRD to IPRK), for more information on IPRA, IPRD to IPRK.

Table 5.8 Interrupt Priority

Type	Priority Level	Comment
NMI	16	Fixed priority level. Cannot be masked.
IRQ	0 to 15	Set with interrupt priority registers A, D to K (IPRA, IPRD to IPRK).
On-chip peripheral module		

5.4.3 Interrupt Exception Processing

When an interrupt occurs, the interrupt controller (INTC) ascertains its priority level. NMI is always accepted, but other interrupts are only accepted if they have a priority level higher than the priority level set in the interrupt mask bits (I3 to I0) in the status register (SR).

When an interrupt is accepted, exception processing begins. In interrupt exception processing, the CPU saves SR and the program counter (PC) to the stack. The priority level value of the accepted interrupt is written to SR bits I3 to I0. For NMI, however, the priority level is 16, but the value set in I3 to I0 is H'F (level 15). Next, the start address of the exception service routine is fetched from the exception processing vector table for the accepted interrupt, that address is jumped to and execution begins. See section 6.6, Interrupt Operation, for more information on the interrupt exception processing.

5.5 Exceptions Triggered by Instructions

5.5.1 Types of Exceptions Triggered by Instructions

Exception processing can be triggered by trap instruction, illegal slot instructions, and general illegal instructions, as shown in table 5.9.

Table 5.9 Types of Exceptions Triggered by Instructions

Type	Source Instruction	Comment
Trap instruction	TRAPA	—
Illegal slot instructions	Undefined code placed immediately after a delayed branch instruction (delay slot) or instructions that rewrite the PC	Delayed branch instructions: JMP, JSR, BRA, BSR, RTS, RTE, BF/S, BT/S, BSRF, BRAF Instructions that rewrite the PC: JMP, JSR, BRA, BSR, RTS, RTE, BT, BF, TRAPA, BF/S, BT/S, BSRF, BRAF
General illegal instructions	Undefined code anywhere besides in a delay slot	—

5.5.2 Trap Instructions

When a TRAPA instruction is executed, trap instruction exception processing starts. The CPU operates as follows:

1. The status register (SR) is saved to the stack.
2. The program counter (PC) is saved to the stack. The PC value saved is the start address of the instruction to be executed after the TRAPA instruction.
3. The CPU reads the start address of the exception service routine from the exception processing vector table that corresponds to the vector number specified in the TRAPA instruction, jumps to that address and starts executing the program. This jump is not a delayed branch.

5.5.3 Illegal Slot Instructions

An instruction placed immediately after a delayed branch instruction is called ″instruction placed in a delay slot″. When the instruction placed in the delay slot is an undefined code, illegal slot exception processing starts after the undefined code is decoded. Illegal slot exception processing also starts when an instruction that rewrites the program counter (PC) is placed in a delay slot and the instruction is decoded. The CPU handles an illegal slot instruction as follows:

1. The status register (SR) is saved to the stack.
2. The program counter (PC) is saved to the stack. The PC value saved is the target address of the delayed branch instruction immediately before the undefined code or the instruction that rewrites the PC.
3. The start address of the exception service routine is fetched from the exception processing vector table that corresponds to the exception that occurred. That address is jumped to and the program starts executing. The jump in this case is not a delayed branch.

5.5.4 General Illegal Instructions

When undefined code placed anywhere other than immediately after a delayed branch instruction (i.e., in a delay slot) is decoded, general illegal instruction exception processing starts. The CPU handles the general illegal instructions in the same procedures as in the illegal slot instructions. Unlike processing of illegal slot instructions, however, the program counter value that is stacked is the start address of the undefined code.

5.6 Cases when Exception Sources Are Not Accepted

When an address error or interrupt is generated directly after a delayed branch instruction or interrupt-disabled instruction, it is sometimes not accepted immediately but stored instead, as shown in table 5.10. In this case, it will be accepted when an instruction that can accept the exception is decoded.

Table 5.10 Generation of Exception Sources Immediately after a Delayed Branch Instruction or Interrupt-Disabled Instruction

	Exception Source	
Point of Occurrence	**Address Error**	**Interrupt**
Immediately after a delayed branch instruction*1	Not accepted	Not accepted
Immediately after an interrupt-disabled instruction*2	Accepted	Not accepted

Notes: 1. Delayed branch instructions: JMP, JSR, BRA, BSR, RTS, RTE, BF/S, BT/S, BSRF, and BRAF
2. Interrupt-disabled instructions: LDC, LDC.L, STC, STC.L, LDS, LDS.L, STS, and STS.L

5.6.1 Immediately after a Delayed Branch Instruction

When an instruction placed immediately after a delayed branch instruction (delay slot) is decoded, neither address errors nor interrupts are accepted. The delayed branch instruction and the instruction placed immediately after it (delay slot) are always executed consecutively, so no exception processing occurs during this period.

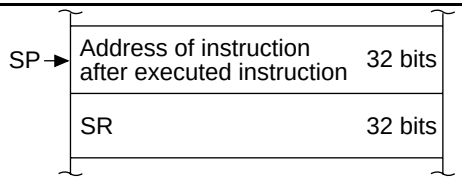
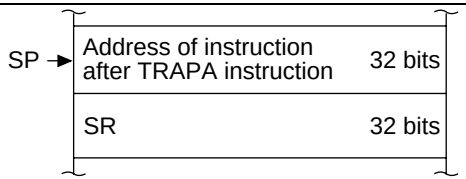
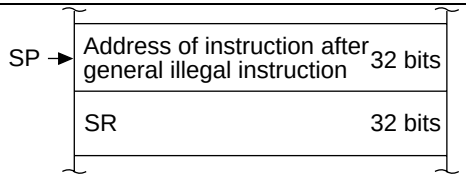
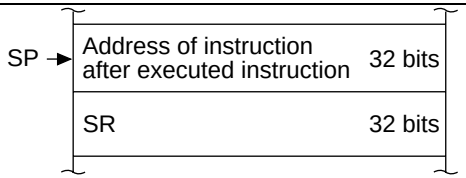
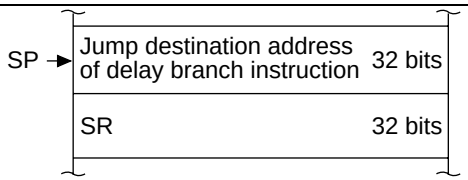
5.6.2 Immediately after an Interrupt-Disabled Instruction

When an instruction placed immediately after an interrupt-disabled instruction is decoded, interrupts are not accepted. Address errors can be accepted.

5.7 Stack Status after Exception Processing Ends

The status of the stack after exception processing ends is shown in table 5.11.

Table 5.11 Stack Status after Exception Processing Ends

Types	Stack Status
Address error	
Trap instruction	
General illegal instruction	
Interrupt	
Illegal slot instruction	

5.8 Usage Notes

5.8.1 Value of Stack Pointer (SP)

The value of the stack pointer must always be a multiple of four. If it is not, an address error will occur when the stack is accessed during exception processing.

5.8.2 Value of Vector Base Register (VBR)

The value of the vector base register must always be a multiple of four. If it is not, an address error will occur when the stack is accessed during exception processing.

5.8.3 Address Errors Caused by Stacking of Address Error Exception Processing

When the value of the stack pointer is not a multiple of four, an address error will occur during stacking of the exception processing (interrupts, etc.) and address error exception processing will start after the first exception processing is ended. Address errors will also occur in the stacking for this address error exception processing. To ensure that address error exception processing does not go into an endless loop, no address errors are accepted at that point. This allows program control to be shifted to the service routine for address error exception and enables error processing.

When an address error occurs during exception processing stacking, the stacking bus cycle (write) is executed. During stacking of the status register (SR) and program counter (PC), the value of SP is reduced by 4 for both of SR and PC, therefore the value of SP is still not a multiple of four after the stacking. The address value output during stacking is the SP value, so the address itself where the error occurred is output. This means that the write data stacked is undefined.

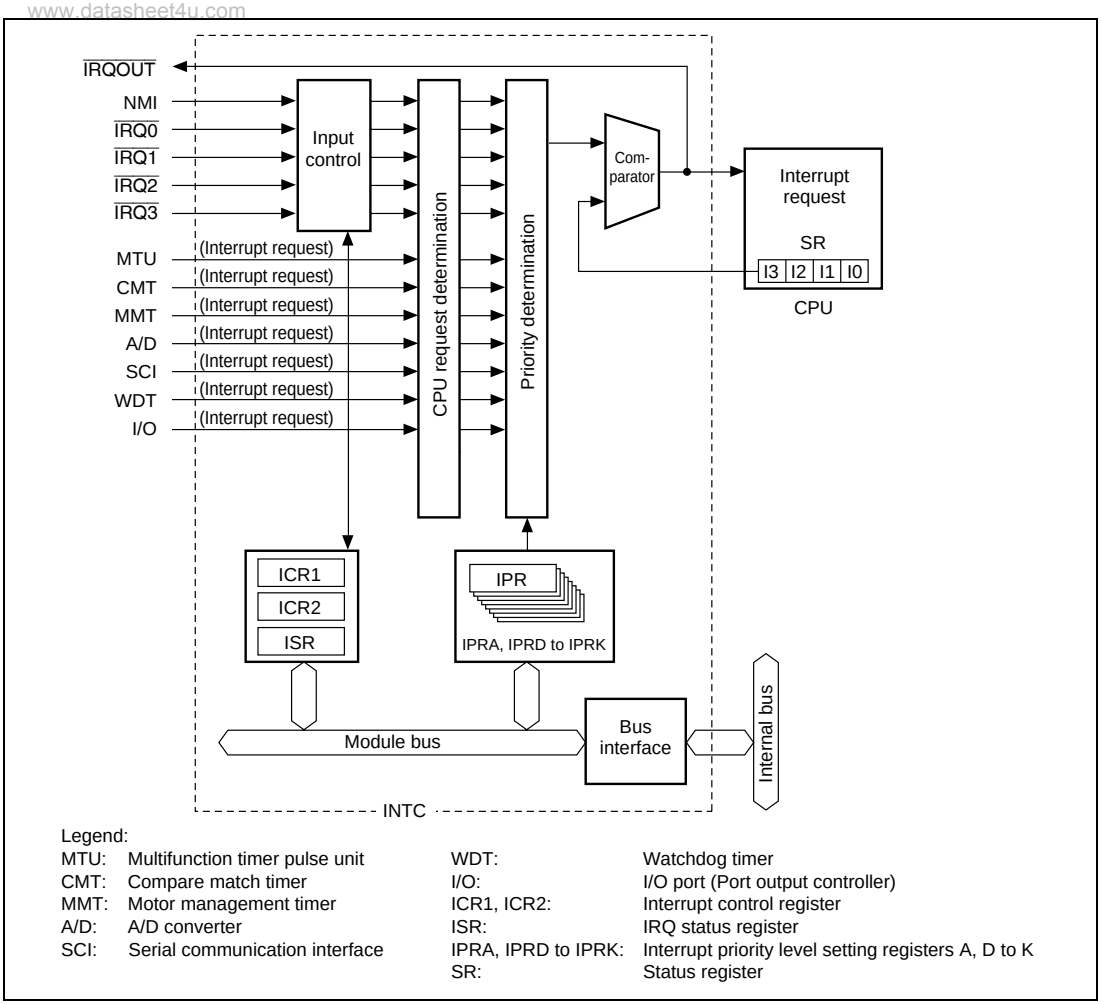
Section 6 Interrupt Controller (INTC)

The interrupt controller (INTC) determines the priority of interrupt sources and controls interrupt requests to the CPU.

6.1 Features

- 16 levels of interrupt priority
- NMI noise canceler function
- Occurrence of interrupt can be reported externally ($\overline{\text{IRQOUT}}$ pin)

Figure 6.1 shows a block diagram of the INTC.



Legend:

MTU:	Multifunction timer pulse unit	WDT:	Watchdog timer
CMT:	Compare match timer	I/O:	I/O port (Port output controller)
MMT:	Motor management timer	ICR1, ICR2:	Interrupt control register
A/D:	A/D converter	ISR:	IRQ status register
SCI:	Serial communication interface	IPRA, IPRD to IPRK:	Interrupt priority level setting registers A, D to K
		SR:	Status register

Figure 6.1 INTC Block Diagram

6.2 Input/Output Pins

Table 6.1 shows the INTC pin configuration.

Table 6.1 Pin Configuration

Name	Abbreviation	I/O	Function
Non-maskable interrupt input pin	NMI	Input	Input of non-maskable interrupt request signal
Interrupt request input pins	$\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$	Input	Input of maskable interrupt request signals
Interrupt request output pin	$\overline{\text{IRQOUT}}$	Output	Output of notification signal when an interrupt has occurred

6.3 Register Descriptions

The interrupt controller has the following registers. For details on register addresses and register states during each processing, refer to section 19, List of Registers.

- Interrupt control register 1 (ICR1)
- Interrupt control register 2 (ICR2)
- IRQ status register (ISR)
- Interrupt priority register A (IPRA)
- Interrupt priority register D (IPRD)
- Interrupt priority register E (IPRE)
- Interrupt priority register F (IPRF)
- Interrupt priority register G (IPRG)
- Interrupt priority register H (IPRH)
- Interrupt priority register I (IPRI)
- Interrupt priority register J (IPRJ)
- Interrupt priority register K (IPRK)

6.3.1 Interrupt Control Register 1 (ICR1)

ICR1 is a 16-bit register that sets the input signal detection mode of the external interrupt input pins NMI and $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$ and indicates the input signal level at the NMI pin.

Bit	Bit Name	Initial Value	R/W	Description
15	NMIL	1/0	R	NMI Input Level Sets the level of the signal input to the NMI pin. This bit can be read to determine the NMI pin level. This bit cannot be modified. 0: NMI input level is low 1: NMI input level is high
14 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	NMIE	0	R/W	NMI Edge Select 0: Interrupt request is detected at falling edge of NMI input 1: Interrupt request is detected at rising edge of NMI input
7	IRQ0S	0	R/W	IRQ0 Sense Select Sets the IRQ0 interrupt request detection mode. 0: Interrupt request is detected at low level of IRQ0 input 1: Interrupt request is detected at edge of IRQ0 input (edge direction is selected by ICR2)
6	IRQ1S	0	R/W	IRQ1 Sense Select Sets the IRQ1 interrupt request detection mode. 0: Interrupt request is detected at low level of IRQ1 input 1: Interrupt request is detected at edge of IRQ1 input (edge direction is selected by ICR2)
5	IRQ2S	0	R/W	IRQ2 Sense Select Sets the IRQ2 interrupt request detection mode. 0: Interrupt request is detected at low level of IRQ2 input 1: Interrupt request is detected at edge of IRQ2 input (edge direction is selected by ICR2)

Bit	Bit Name	Initial Value	R/W	Description
4	IRQ3S	0	R/W	IRQ3 Sense Select Sets the IRQ3 interrupt request detection mode. 0: Interrupt request is detected at low level of IRQ3 input 1: Interrupt request is detected at edge of IRQ3 input (edge direction is selected by ICR2)
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

6.3.2 Interrupt Control Register 2 (ICR2)

ICR2 is a 16-bit register that sets the edge detection mode of the external interrupt input pins $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$. ICR2 is, however, valid only when IRQ interrupt request detection mode is set to the edge detection mode by the sense select bits of IRQ0 to IRQ 3 in the interrupt control register 1 (ICR1). If the IRQ interrupt request detection mode has been set to low level detection mode, the setting of ICR2 is ignored.

Bit	Bit Name	Initial Value	R/W	Description
15 14	IRQ0ES1 IRQ0ES0	0 0	R/W R/W	These bits set the IRQ0 interrupt request edge detection mode. 00: Interrupt request is detected at falling edge of $\overline{\text{IRQ0}}$ input 01: Interrupt request is detected at rising edge of $\overline{\text{IRQ0}}$ input 10: Interrupt request is detected at both falling and rising edges of $\overline{\text{IRQ0}}$ input 11: Setting prohibited
13 12	IRQ1ES1 IRQ1ES0	0 0	R/W R/W	These bits set the IRQ1 interrupt request edge detection mode. 00: Interrupt request is detected at falling edge of $\overline{\text{IRQ1}}$ input 01: Interrupt request is detected at rising edge of $\overline{\text{IRQ1}}$ input 10: Interrupt request is detected at both falling and rising edges of $\overline{\text{IRQ1}}$ input 11: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
11	IRQ2ES1	0	R/W	These bits set the IRQ2 interrupt request edge detection mode.
10	IRQ2ES0	0	R/W	00: Interrupt request is detected at falling edge of $\overline{\text{IRQ2}}$ input 01: Interrupt request is detected at rising edge of $\overline{\text{IRQ2}}$ input 10: Interrupt request is detected at both falling and rising edges of $\overline{\text{IRQ2}}$ input 11: Setting prohibited
9	IRQ3ES1	0	R/W	These bits set the IRQ3 interrupt request edge detection mode.
8	IRQ3ES0	0	R/W	00: Interrupt request is detected at falling edge of $\overline{\text{IRQ3}}$ input 01: Interrupt request is detected at rising edge of $\overline{\text{IRQ3}}$ input 10: Interrupt request is detected at both falling and rising edges of $\overline{\text{IRQ3}}$ input 11: Setting prohibited
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

6.3.3 IRQ Status Register (ISR)

ISR is a 16-bit register that indicates the interrupt request status of the external interrupt input pins $\overline{IRQ0}$ to $\overline{IRQ3}$. When IRQ interrupts are set to edge detection, held interrupt requests can be withdrawn by writing 0 to IRQnF after reading IRQnF = 1.

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	IRQ0F	0	R/W	IRQ0 to IRQ3 Flags These bits display the IRQ0 to IRQ3 interrupt request status. [Setting condition] • When interrupt source that is selected by ICR1 and ICR2 has occurred. [Clearing conditions] • When 0 is written after reading IRQnF = 1 • When interrupt exception processing has been executed at high level of $\overline{IRQn}$ input under the low level detection mode. • When IRQn interrupt exception processing has been executed under the edge detection mode of falling edge, rising edge, or both falling and rising edges.
6	IRQ1F	0	R/W	
5	IRQ2F	0	R/W	
4	IRQ3F	0	R/W	
3 to 0	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.

6.3.4 Interrupt Priority Registers A, D to K (IPRA, IPRD to IPRK)

Interrupt priority registers are nine 16-bit readable/writable registers that set priority levels from 0 to 15 for interrupts except NMI. For the correspondence between interrupt request sources and IPR, refer to table 6.2. Each of the corresponding interrupt priority ranks are established by setting a value from H'0 to H'F in each of the four-bit groups, bits 15 to 12, bits 11 to 8, bits 7 to 4, and bits 3 to 0. Reserved bits that are not assigned should be set H'0 (B'0000.)

Bit	Bit Name	Initial Value	R/W	Description
15	IPR15	0	R/W	These bits set priority levels for the corresponding interrupt source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)
14	IPR14	0	R/W	
13	IPR13	0	R/W	
12	IPR12	0	R/W	
11	IPR11	0	R/W	These bits set priority levels for the corresponding interrupt source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)
10	IPR10	0	R/W	
9	IPR9	0	R/W	
8	IPR8	0	R/W	

Bit	Bit Name	Initial Value	R/W	Description
7	IPR7	0	R/W	These bits set priority levels for the corresponding interrupt source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)
6	IPR6	0	R/W	
5	IPR5	0	R/W	
4	IPR4	0	R/W	
3	IPR3	0	R/W	These bits set priority levels for the corresponding interrupt source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)
2	IPR2	0	R/W	
1	IPR1	0	R/W	
0	IPR0	0	R/W	

Note: Name in the tables above is represented by a general name. Name in the list of register is, on the other hand, represented by a module name.

6.4 Interrupt Sources

6.4.1 External Interrupts

There are four types of interrupt sources: NMI, user breaks, IRQ, and on-chip peripheral modules. Each interrupt has a priority expressed as a priority level (0 to 16, with 0 the lowest and 16 the highest). Giving an interrupt a priority level of 0 masks it.

NMI Interrupts: The NMI interrupt has priority 16 and is always accepted. Input at the NMI pin is detected by edge. Use the NMI edge select bit (NMIE) in the interrupt control register 1 (ICR1) to select either the rising or falling edge. NMI interrupt exception processing sets the interrupt mask level bits (I3 to I0) in the status register (SR) to level 15.

IRQ3 to IRQ0 Interrupts: IRQ interrupts are requested by input from pins $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$. Set the IRQ sense select bits (IRQ0S to IRQ3S) of the interrupt control register 1 (ICR1) and the IRQ edge select bit (IRQ0ES[1:0] to IRQ3ES[1:0]) of the interrupt control register 2 (ICR2) to select low level detection, falling edge detection, or rising edge detection for each pin. The priority level can be set from 0 to 15 for each pin using the interrupt priority registers A (IPRA).

When IRQ interrupts are set to low level detection, an interrupt request signal is sent to the INTC during the period the IRQ pin is low level. Interrupt request signals are not sent to the INTC when the IRQ pin becomes high level. Interrupt request levels can be confirmed by reading the IRQ flags (IRQ0F to IRQ3F) of the IRQ status register (ISR).

When IRQ interrupts are set to falling edge detection, interrupt request signals are sent to the INTC upon detecting a change at the IRQ pin from high to low level. The results of detection for IRQ interrupt request are maintained until the interrupt request is accepted. It is possible to confirm that IRQ interrupt requests have been detected by reading the IRQ flags (IRQ0F to IRQ3F) of the IRQ status register (ISR), and by writing a 0 after reading a 1, IRQ interrupt request detection results can be withdrawn.

In IRQ interrupt exception processing, the interrupt mask bits (I3 to I0) of the status register (SR) are set to the priority level value of the accepted IRQ interrupt. Figure 6.2 shows the block diagram of this IRQ3 to IRQ0 interrupts.

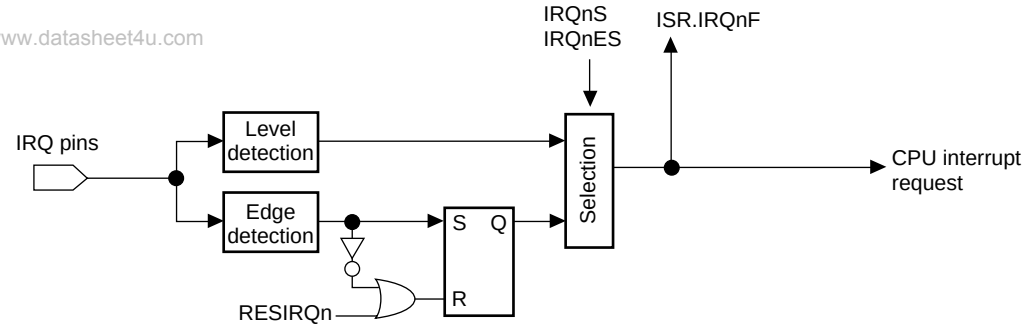


Figure 6.2 Control of IRQ3 to IRQ0 Interrupts

6.4.2 On-Chip Peripheral Module Interrupts

On-chip peripheral module interrupts are interrupts generated by the following on-chip peripheral modules.

As a different interrupt vector is assigned to each interrupt source, the exception service routine does not have to decide which interrupt has occurred. Priority levels between 0 and 15 can be assigned to individual on-chip peripheral modules by setting interrupt priority registers A, D to K (IPRA, IPRD to IPRK). On-chip peripheral module interrupt exception processing sets the interrupt mask level bits (I3 to I0) in the status register (SR) to the priority level value of the on-chip peripheral module interrupt that was accepted.

6.5 Interrupt Exception Processing Vectors Table

Table 6.2 lists interrupt sources and their vector numbers, vector table address offsets, and interrupt priorities.

Each interrupt source is allocated a different vector number and vector table address offset. Vector table addresses are calculated from the vector numbers and address offsets. In interrupt exception processing, the exception service routine start address is fetched from the vector table indicated by the vector table address. For the details of calculation of vector table address, see table 5.4.

IRQ interrupts and on-chip peripheral module interrupt priorities can be set freely between 0 and 15 for each pin or module by setting interrupt priority registers A, D to K (IPRA, IPRD to IPRK). However, the smaller vector number has interrupt source, the higher priority ranking is assigned among two or more interrupt sources specified by the same IPR, and the priority ranking cannot be changed. A power-on reset assigns priority level 0 to IRQ interrupts and on-chip peripheral module interrupts. If the same priority level is assigned to two or more interrupt sources and interrupts from those sources occur simultaneously, they are processed by the default priority order indicated in table 6.2.

Table 6.2 Interrupt Exception Processing Vectors and Priorities

Interrupt Source	Name	Vector No.	Vector Table Starting Address	IPR	Default Priority
External pin	NMI	11	H'0000002C	—	High
—	Reserved by system	14	H'00000038	—	
—	Reserved by system	15	H'0000003C	—	
Interrupts	IRQ0	64	H'00000100	IPRA15 to IPRA12	
	IRQ1	65	H'00000104	IPRA11 to IPRA8	
	IRQ2	66	H'00000108	IPRA7 to IPRA4	
	IRQ3	67	H'0000010C	IPRA3 to IPRA0	
	Reserved by system	68	H'00000110	—	
	Reserved by system	69	H'00000114	—	
	Reserved by system	70	H'00000118	—	
	Reserved by system	71	H'0000011C	—	
—	Reserved by system	72	H'00000120	—	
	Reserved by system	76	H'00000130	—	
	Reserved by system	80	H'00000140	—	
	Reserved by system	84	H'00000150	—	Low

Interrupt Source	Name	Vector No.	Vector Table Starting Address	IPR	Default Priority
MTU channel 0	TGIA_0	88	H'00000160	IPRD15 to IPRD12	High
	TGIB_0	89	H'00000164		
	TGIC_0	90	H'00000168		
	TGID_0	91	H'0000016C		
	TCIV_0	92	H'00000170	IPRD11 to IPRD8	
MTU channel 1	TGIA_1	96	H'00000180	IPRD7 to IPRD4	
	TGIB_1	97	H'00000184		
	TCIV_1	100	H'00000190	IPRD3 to IPRD0	
	TCIU_1	101	H'00000194		
MTU channel 2	TGIA_2	104	H'000001A0	IPRE15 to IPRE12	
	TGIB_2	105	H'000001A4		
	TCIV_2	108	H'000001B0	IPRE11 to IPRE8	
	TCIU_2	109	H'000001B4		
MTU channel 3	TGIA_3	112	H'000001C0	IPRE7 to IPRE4	
	TGIB_3	113	H'000001C4		
	TGIC_3	114	H'000001C8		
	TGID_3	115	H'000001CC		
	TCIV_3	116	H'000001D0	IPRE3 to IPRE0	
MTU channel 4	TGIA_4	120	H'000001E0	IPRF15 to IPRF12	
	TGIB_4	121	H'000001E4		
	TGIC_4	122	H'000001E8		
	TGID_4	123	H'000001EC		
	TCIV_4	124	H'000001F0	IPRF11 to IPRF8	
—	Reserved by system	128 to 135	H'00000200 to H'0000021C	—	
A/D	ADI0	136	H'00000220	IPRG15 to IPRG12	
	ADI1	137	H'00000224		
—	Reserved by system	138 to 143	H'00000228 to H'0000023C	—	Low

Interrupt Source	Name	Vector No.	Vector Table Starting Address	IPR	Default Priority
CMT	CMI0	144	H'00000240	IPRG7 to IPRG4	High
	CMI1	148	H'00000250	IPRG3 to IPRG0	
Watchdog timer	ITI	152	H'00000260	IPRH15 to IPRH12	
—	Reserved by system	153	H'00000264	—	
I/O (MTU)	MTUPOE	156	H'00000270	IPRH11 to IPRH8	
—	Reserved by system	160 to 167	H'00000290 to H'0000029C	—	
SCI channel 2	ERI_2	168	H'000002A0	IPRI15 to IPRI12	
	RXI_2	169	H'000002A4		
	TXI_2	170	H'000002A8		
	TEI_2	171	H'000002AC		
SCI channel 3	ERI_3	172	H'000002B0	IPRI11 to IPRI8	
	RXI_3	173	H'000002B4		
	TXI_3	174	H'000002B8		
	TEI_3	175	H'000002BC		
—	Reserved by system	176 to 179	H'000002C0 to H'000002CC	IPRI7 to IPRI4	
MMT	TGIM	180	H'000002D0	IPRI3 to IPRI0	
	TGIN	181	H'000002D4		
A/D2	ADI2	184	H'000002E0	IPRJ15 to IPRJ12	
—	Reserved by system	188 to 196	H'000002F0 to H'00000310	—	
I/O (MMT)	MMTPOE	200	H'00000320	IPRK15 to IPRK12	
—	Reserved by system	212	H'00000330 to H'000003DC	—	Low

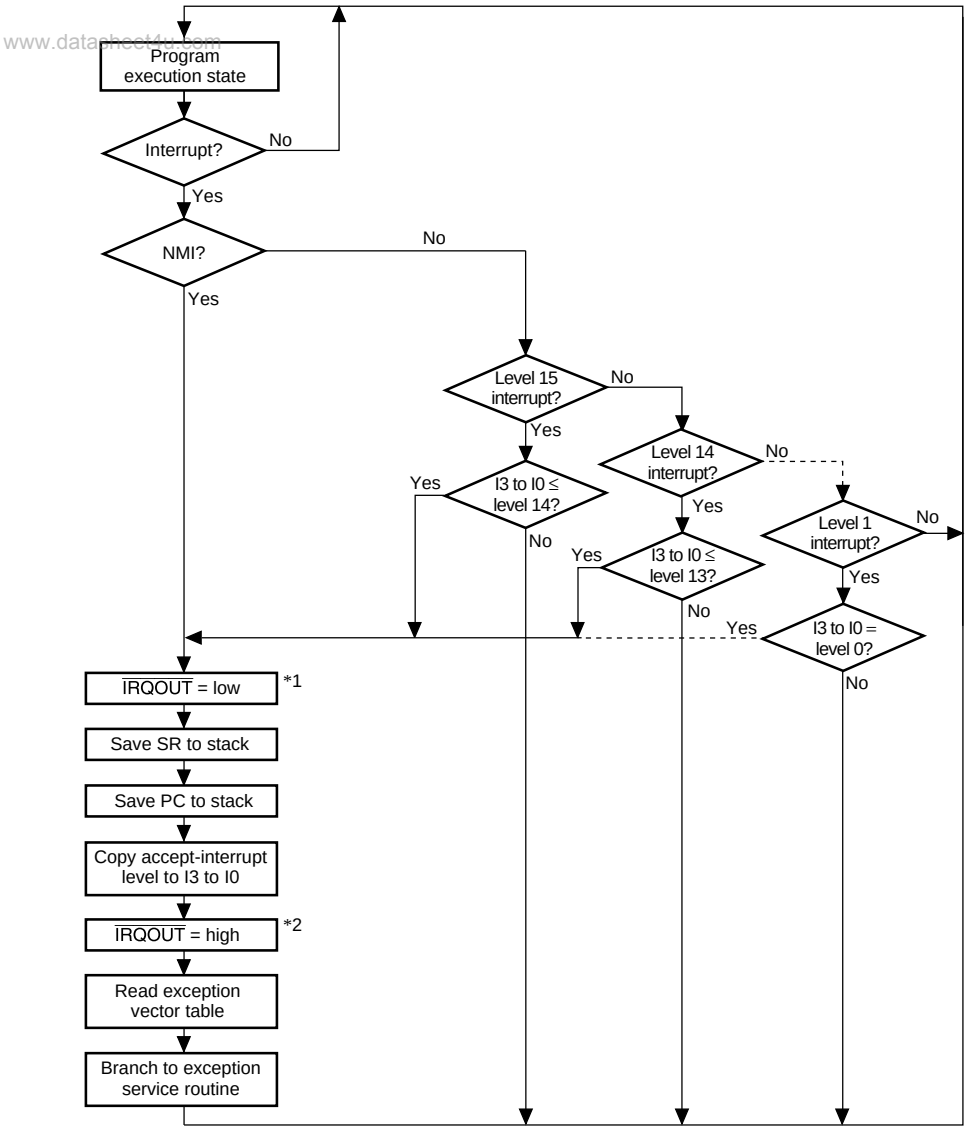
6.6 Interrupt Operation

6.6.1 Interrupt Sequence

The sequence of interrupt operations is explained below. Figure 6.3 is a flowchart of the operations.

1. The interrupt request sources send interrupt request signals to the interrupt controller.
2. The interrupt controller selects the highest priority interrupt in the interrupt requests sent, according to the priority levels set in interrupt priority level setting registers A, D to K (IPRA, IPRD to IPRK). Interrupts that have lower-priority than that of the selected interrupt are ignored.* If interrupts that have the same priority level or interrupts within a same module occur simultaneously, the interrupt with the highest priority is selected according to the default priority order indicated in table 6.2.
3. The interrupt controller compares the priority level of the selected interrupt request with the interrupt mask bits (I3 to I0) in the CPU's status register (SR). If the request priority level is equal to or less than the level set in I3 to I0, the request is ignored. If the request priority level is higher than the level in bits I3 to I0, the interrupt controller accepts the interrupt and sends an interrupt request signal to the CPU.
4. When the interrupt controller accepts an interrupt, a low level is output from the $\overline{\text{IRQOUT}}$ pin.
5. The CPU detects the interrupt request sent from the interrupt controller when CPU decodes the instruction to be executed. Instead of executing the decoded instruction, the CPU starts interrupt exception processing (figure 6.5).
6. SR and PC are saved onto the stack.
7. The priority level of the accepted interrupt is copied to the interrupt mask level bits (I3 to I0) in the status register (SR).
8. When the accepted interrupt is sensed by level or is from an on-chip peripheral module, a high level is output from the $\overline{\text{IRQOUT}}$ pin. When the accepted interrupt is sensed by edge, a high level is output from the $\overline{\text{IRQOUT}}$ pin at the moment when the CPU starts interrupt exception processing instead of instruction execution as noted in (5) above. However, if the interrupt controller accepts an interrupt with a higher priority than the interrupt just to be accepting, the $\overline{\text{IRQOUT}}$ pin holds low level.
9. The CPU reads the start address of the exception service routine from the exception vector table for the accepted interrupt, jumps to that address, and starts executing the program. This jump is not a delay branch.

Note: * Interrupt requests that are designated as edge-detect type are held pending until the interrupt requests are accepted. IRQ interrupts, however, can be cancelled by accessing the IRQ status register (ISR). Interrupts held pending due to edge detection are cleared by a power-on reset or a manual reset.



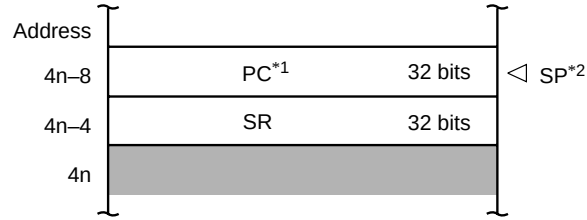
Notes: I3 to I0 are Interrupt mask bits of status register (SR) in the CPU.

1. $\overline{\text{IRQOUT}}$ is the same signal as interrupt request signal to the CPU (see figure 6.1). Therefore, $\overline{\text{IRQOUT}}$ is output when the request priority level is higher than the level in bits I3 to I0 of SR.
2. When the accepted interrupt is sensed by edge, a high level is output from the IRQOUT pin at the moment when the CPU starts interrupt exception processing instead of instruction execution (namely, before saving SR to stack). However, if the interrupt controller accepts an interrupt with a higher priority than the interrupt just to be accepted and has output an interrupt request to the CPU, the $\overline{\text{IRQOUT}}$ pin holds low level.

Figure 6.3 Interrupt Sequence Flowchart

6.6.2 Stack after Interrupt Exception Processing

Figure 6.4 shows the stack after interrupt exception processing.



Notes: 1. PC: Start address of the next instruction (return destination instruction) after the executing instruction
2. Always make sure that SP is a multiple of 4.

Figure 6.4 Stack after Interrupt Exception Processing

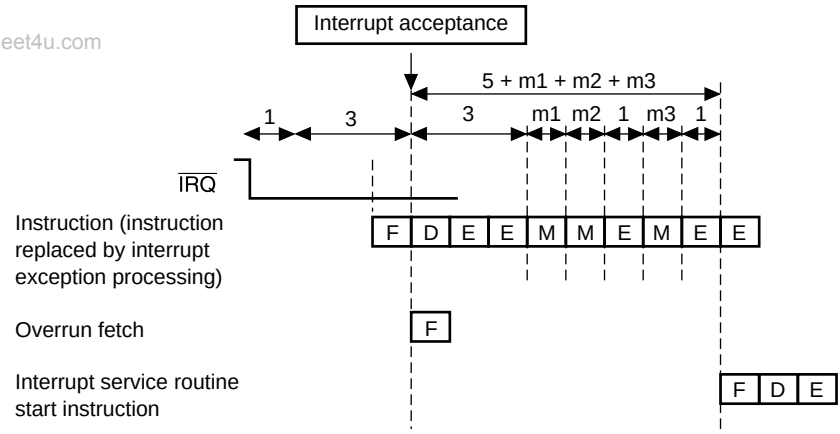
6.7 Interrupt Response Time

Table 6.3 lists the interrupt response time, which is the time from the occurrence of an interrupt request until the interrupt exception processing starts and fetching of the first instruction of the interrupt service routine begins. Figure 6.5 shows an example of the pipeline operation when an IRQ interrupt is accepted.

Table 6.3 Interrupt Response Time

Item		Number of States: NMI, Peripheral Module	Number of States: IRQ	Remarks
Idle cycle		0 or 1	1	
Interrupt priority judgment and comparison with SR mask bits		2	3	
Wait for completion of sequence currently being executed by CPU		X (≥ 0)		The longest sequence is for interrupt or address-error exception processing (X = 4 + m1 + m2 + m3 + m4). If an interrupt-masking instruction follows, however, the time may be even longer.
Time from start of interrupt exception processing until fetch of first instruction of exception service routine starts		5 + m1 + m2 + m3		Performs the saving PC and SR, and vector address fetch.
Interrupt response time	Total:	(7 or 8) + m1 + m2 + m3 + X	9 + m1 + m2 + m3 + X	
	Minimum:	10	12	0.25 to 0.3 µs at 40 MHz
	Maximum:	12 + 2 (m1 + m2 + m3) + m4	13 + 2 (m1 + m2 + m3) + m4	0.48 µs* at 40 MHz

Notes: * 0.48 µs at 40 MHz is the value in the case that m1 = m2 = m3 = m4 = 1.
m1 to m4 are the number of states needed for the following memory accesses.
m1: SR save (longword write)
m2: PC save (longword write)
m3: Vector address read (longword read)
m4: Fetch first instruction of interrupt service routine



F: Instruction fetch (instruction fetched from memory where program is stored).
D: Instruction decoding (fetched instruction is decoded).
E: Instruction execution (data operation and address calculation is performed according to the results of decoding).
M: Memory access (data in memory is accessed).

Figure 6.5 Example of the Pipeline Operation when an IRQ Interrupt Is Accepted

Section 7 Bus State Controller (BSC)

The bus state controller (BSC) divides up the address spaces and outputs control for various types of memory. This enables memories like SRAM and ROM to be linked directly to the chip without external circuitry.

7.1 Features

The BSC has the following features:

- Address space is divided into four spaces (supported only by the SH7109)
  - A maximum linear 2-Mbyte bus width for the on-chip ROM enabled mode and a maximum 4-Mbyte bus width for the on-chip ROM disabled mode, as for the CS0 space (8 bits)
  - Wait states can be inserted by software for each space
  - Wait state insertion with the $\overline{\text{WAIT}}$ pin in external memory space access
  - Outputs control signals for each space according to the type of memory connected
- On-chip ROM and RAM interfaces
  - On-chip ROM and RAM access of 32 bits in 1 state

Figure 7.1 shows the BSC block diagram.

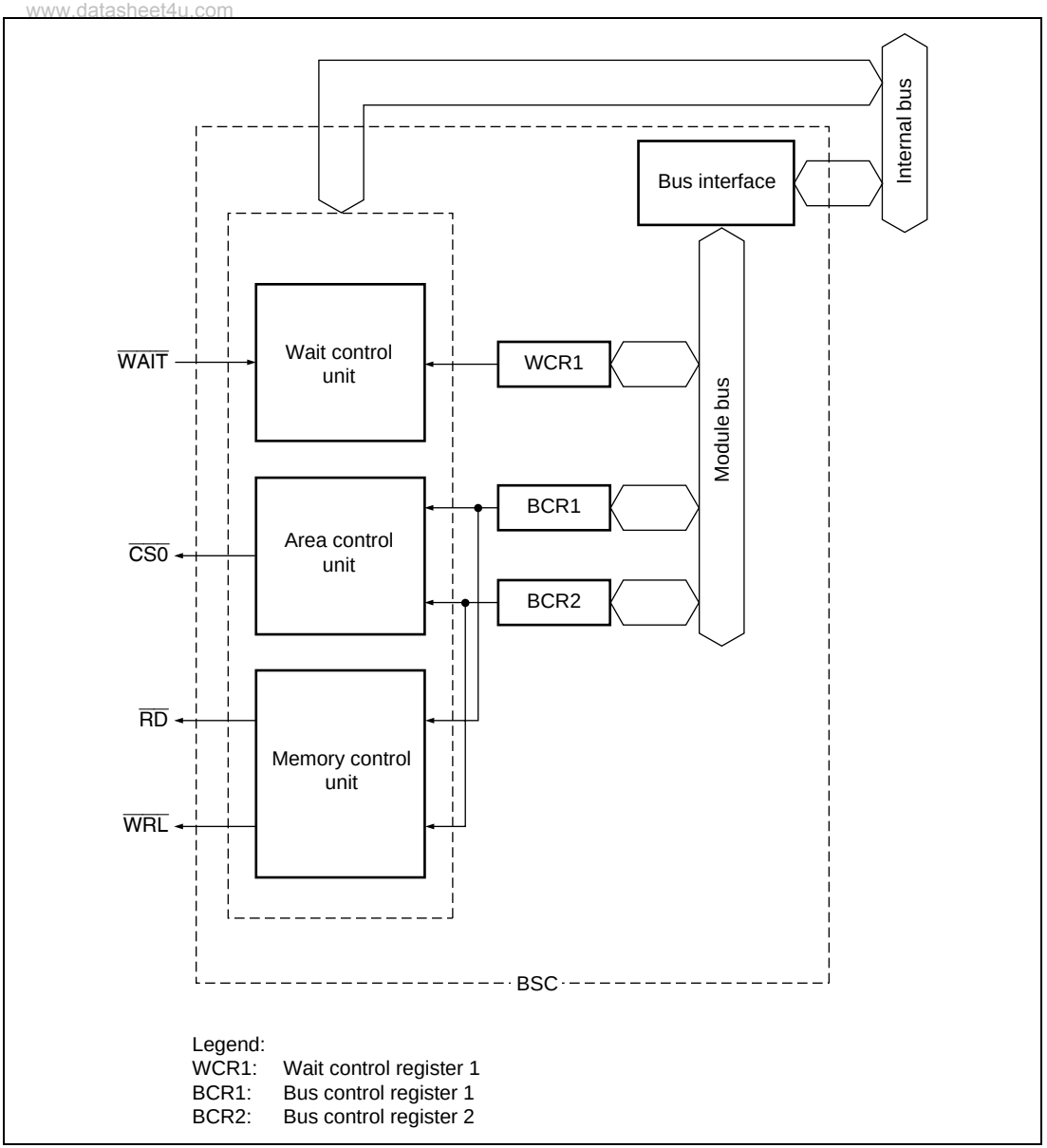


Figure 7.1 BSC Block Diagram

7.2 Input/Output Pins

Table 7.1 lists bus state controller pins of the SH7109. The SH7108 is not equipped with this type of pins.

Table 7.1 Pin Configuration

Name	Abbr.	I/O	Description
Address bus	A17 to A0	Output	Address output
Data bus	D7 to D0	I/O	8-bit data bus
Chip select	$\overline{CS0}$	Output	Chip select signal indicating the area being accessed
Read	$\overline{RD}$	Output	Strobe signal that indicates the read cycle
Lower byte write	$\overline{WRL}$	Output	Strobe signal that indicates a write cycle to the lower 8 bits (D7 to D0)
Wait	$\overline{WAIT}$	Input	Wait state request signal
Bus request	$\overline{BREQ}$	Input	Bus release request input
Bus request acknowledge	$\overline{BACK}$	Output	Bus use enable output

7.3 Register Configuration

The following registers are provided for the bus state controller. For details on addresses and states of these registers in each processing, refer to section 19, List of Registers.

These registers are used to control wait states, bus width, and interfaces with memories like ROM and SRAM. All registers are 16 bits.

- Bus control register 1 (BCR1)
- Bus control register 2 (BCR2)
- Wait control register 1 (WCR1)

7.4 Address Map

Figure 7.2 shows the address format used by this LSI.

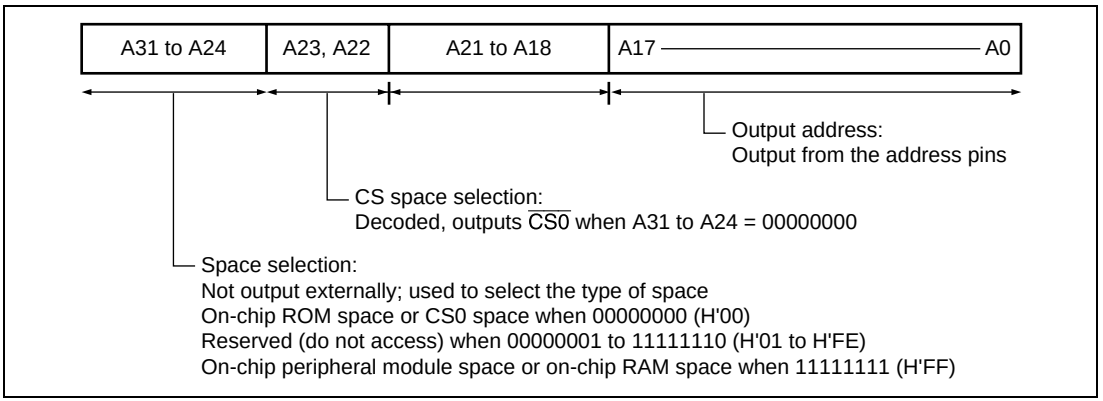


Figure 7.2 Address Format

This chip uses 32-bit addresses:

- Bits A31 to A24 are used to select the type of space and are not output externally.
- Bits A23 and A22 are decoded and output as chip select signals ($\overline{CS0}$) for the corresponding areas when bits A31 to A24 are 00000000.
- A17 to A0 are output externally. A21 to A18 are not output externally.

Table 7.2 shows the address map.

Table 7.2 Address Map

Single Chip Mode

Address	Space	Memory	Size		Bus Width
			SH7105	SH7104	
H'0000 0000 to H'0000 7FFF	On-chip ROM	On-chip ROM	256 kbytes	256 kbytes	32 bits
H'0000 8000 to H'0000 FFFF					
H'0001 0000 to H'0001 FFFF					
H'0002 0000 to H'0002 FFFF					
H'0003 0000 to H'0003 FFFF					
H'0004 0000 to H'001F FFFF	Reserved	Reserved	Reserved	Reserved	
H'0020 0000 to H'0023 FFFF	Reserved	Reserved	Reserved	Reserved	
H'0024 0000 to H'FFFF 7FFF	Reserved	Reserved	Reserved	Reserved	
H'FFFF 8000 to H'FFFF BFFF	On-chip peripheral module	On-chip peripheral module	16 kbytes	16 kbytes	8, 16 bits
H'FFFF C000 to H'FFFF CFFF	Reserved	Reserved	Reserved	Reserved	
H'FFFF D000 to H'FFFF DFFF	On-chip RAM	On-chip RAM	Reserved	Reserved	32 bits
H'FFFF E000 to H'FFFF EFFF			8 kbytes	8 kbytes	
H'FFFF F000 to H'FFFF 7FFF					
H'FFFF F800 to H'FFFF FFFF					

Address	Space	Memory	Size		Bus Width
			SH7109	SH7108	
H'0000 0000 to H'0000 7FFF	On-chip ROM	On-chip ROM	128 kbytes	128 kbytes	32 bits
H'0000 8000 to H'0000 FFFF					
H'0001 0000 to H'0001 FFFF					
H'0002 0000 to H'0002 FFFF			Reserved	Reserved	
H'0003 0000 to H'0003 FFFF					
H'0004 0000 to H'001F FFFF	Reserved	Reserved	Reserved	Reserved	
H'0020 0000 to H'0023 FFFF	Reserved	Reserved	Reserved	Reserved	
H'0024 0000 to H'FFFF 7FFF	Reserved	Reserved	Reserved	Reserved	
H'FFFF 8000 to H'FFFF BFFF	On-chip peripheral module	On-chip peripheral module	16 kbytes	16 kbytes	8, 16 bits
H'FFFF C000 to H'FFFF CFFF	Reserved	Reserved	Reserved	Reserved	
H'FFFF D000 to H'FFFF DFFF	On-chip RAM	On-chip RAM	Reserved	Reserved	32 bits
H'FFFF E000 to H'FFFF EFFF					
H'FFFF F000 to H'FFFF 7FFF			4 kbytes	4 kbytes	
H'FFFF F800 to H'FFFF FFFF					

Address	Space	Memory	Size		Bus Width
			SH7107	SH7106	
H'0000 0000 to H'0000 7FFF	On-chip ROM	On-chip ROM	64 kbytes	64 kbytes	32 bits
H'0000 8000 to H'0000 FFFF					
H'0001 0000 to H'0001 FFFF			Reserved	Reserved	
H'0002 0000 to H'0002 FFFF					
H'0003 0000 to H'0003 FFFF					
H'0004 0000 to H'001F FFFF	Reserved	Reserved	Reserved	Reserved	
H'0020 0000 to H'0023 FFFF	Reserved	Reserved	Reserved	Reserved	
H'0024 0000 to H'FFFF 7FFF	Reserved	Reserved	Reserved	Reserved	
H'FFFF 8000 to H'FFFF BFFF	On-chip peripheral module	On-chip peripheral module	16 kbytes	16 kbytes	8, 16 bits
H'FFFF C000 to H'FFFF CFFF	Reserved	Reserved	Reserved	Reserved	
H'FFFF D000 to H'FFFF DFFF	On-chip RAM	On-chip RAM	Reserved	Reserved	32 bits
H'FFFF E000 to H'FFFF EFFF					
H'FFFF F000 to H'FFFF 7FFF			4 kbytes	4 kbytes	
H'FFFF F800 to H'FFFF FFFF					

Note: Do not access reserved spaces. Operation cannot be guaranteed if they are accessed.

Address	Space	Memory	Size: SH7101	Bus Width
H'0000 0000 to H'0000 7FFF	On-chip ROM	On-chip ROM	32 kbytes	32 bits
H'0000 8000 to H'0000 FFFF			Reserved	
H'0001 0000 to H'0001 FFFF				
H'0002 0000 to H'0002 FFFF				
H'0003 0000 to H'0003 FFFF				
H'0004 0000 to H'001F FFFF	Reserved	Reserved	Reserved	
H'0020 0000 to H'0023 FFFF	Reserved	Reserved	Reserved	
H'0024 0000 to H'FFFF 7FFF	Reserved	Reserved	Reserved	
H'FFFF 8000 to H'FFFF BFFF	On-chip peripheral module	On-chip peripheral module	16 kbytes	8, 16 bits
H'FFFF C000 to H'FFFF CFFF	Reserved	Reserved	Reserved	
H'FFFF D000 to H'FFFF DFFF	On-chip RAM	On-chip RAM	Reserved	32 bits
H'FFFF E000 to H'FFFF EFFF				
H'FFFF F000 to H'FFFF 7FFF				
H'FFFF F800 to H'FFFF FFFF			2 kbytes	

On-Chip ROM Enabled Mode (for SH7109 only)

Address	Space*	Memory	Size			Bus Width
			SH7105	SH7109	SH7107	
H'0000 0000 to H'0000 7FFF	On-chip ROM	On-chip ROM	256 kbytes	128 kbytes	64 kbytes	32 bits
H'0000 8000 to H'0000 FFFF						
H'0001 0000 to H'0001 FFFF					Reserved	
H'0002 0000 to H'0002 FFFF				Reserved		
H'0003 0000 to H'0003 FFFF						
H'0004 0000 to H'001F FFFF	Reserved	Reserved	Reserved	Reserved	Reserved	
H'0020 0000 to H'0023 FFFF	CS0 space	External space	256 kbytes	256 kbytes	256 kbytes	8 bits
H'0024 0000 to H'FFFF 7FFF	Reserved	Reserved	Reserved	Reserved	Reserved	
H'FFFF 8000 to H'FFFF BFFF	On-chip peripheral module	On-chip peripheral module	16 kbytes	16 kbytes	16 kbytes	8, 16 bits
H'FFFF C000 to H'FFFF CFFF	Reserved	Reserved	Reserved	Reserved	Reserved	
H'FFFF D000 to H'FFFF DFFF	On-chip RAM	On-chip RAM	Reserved	Reserved	Reserved	32 bits
H'FFFF E000 to H'FFFF EFFF			8 kbytes			
H'FFFF F000 to H'FFFF 7FFF				4 kbytes	4 kbytes	
H'FFFF F800 to H'FFFF FFFF						

On-Chip ROM Disabled Mode (for SH7109 only)

Address	Space*	Memory	Size SH7105	Size SH7109	Size SH7107	Bus Width
H'0000 0000 to H'0000 7FFF	CS0 space	External space	256 kbytes	256 kbytes	256 kbytes	8 bits
H'0000 8000 to H'0000 FFFF						
H'0001 0000 to H'0001 FFFF						
H'0002 0000 to H'0002 FFFF						
H'0003 0000 to H'0003 FFFF						
H'0004 0000 to H'001F FFFF	Reserved	Reserved	Reserved	Reserved	Reserved	
H'0020 0000 to H'0023 FFFF	Reserved	Reserved	Reserved	Reserved	Reserved	
H'0024 0000 to H'FFFF 7FFF	Reserved	Reserved	Reserved	Reserved	Reserved	
H'FFFF 8000 to H'FFFF BFFF	On-chip peripheral module	On-chip peripheral module	16 kbytes	16 kbytes	16 kbytes	8, 16 bits
H'FFFF C000 to H'FFFF CFFF	Reserved	Reserved	Reserved	Reserved	Reserved	
H'FFFF D000 to H'FFFF DFFF	On-chip RAM	On-chip RAM	Reserved	Reserved	Reserved	32 bits
H'FFFF E000 to H'FFFF EFFF			8 kbytes			
H'FFFF F000 to H'FFFF 7FFF				4 kbytes	4 kbytes	
H'FFFF F800 to H'FFFF FFFF						

Note: * Do not access reserved spaces. Operation cannot be guaranteed if they are accessed. When in single chip mode, spaces other than those for on-chip ROM, on-chip RAM, and internal peripheral module are not available.

7.5 Register Descriptions

7.5.1 Bus Control Register 1 (BCR1)

BCR1 is a 16-bit readable/writable register that enables access to the MMT and MTU control registers and specifies the bus size of the CS0 space.

The AOSZ bit of BCR1 is written to during the initialization stage after a power-on reset. Do not change the values thereafter. In on-chip ROM enabled mode, do not access any of the CS0 space until completion of register initialization.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	MMTRWE	1	R/W	MMT Read/Write Enable This bit enables MMT control register access. For details, refer to section 13, Motor Management Timer (MMT). 0: MMT control register access is disabled 1: MMT control register access is enabled
13	MTURWE	1	R/W	MTU Read/Write Enable This bit enables MTU control register access. For details, refer to section 8, Multifunction Timer Pulse Unit (MTU). 0: MTU control register access is disabled 1: MTU control register access is enabled
12 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 1	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
0	A0SZ	1	R/W	CS0 Space Size Specification Specifies the CS0 space bus size when A0LG is 0. In on-chip ROM enabled mode, 0 should be written to this bit to specify a bus size of 8 bits before the CS0 space is accessed. Note: In on-chip ROM disabled mode, the CS0 space bus size is specified by the mode pin.

7.5.2 Bus Control Register 2 (BCR2)

BCR2 is a 16-bit readable/writable register that specifies the number of idle cycles and $\overline{CS0}$ signal assert extension of each CS0 space.

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
9	IW01	1	R/W	CS0 Space Idle Specification between Cycles
8	IW00	1	R/W	These bits insert idle cycles when a read access is followed immediately by a write access. 00: No CS0 space idle cycle 01: One CS0 space idle cycle 10: Two CS0 space idle cycles 11: Three CS0 space idle cycles
7 to 5	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
4	CW0	1	R/W	CS0 Space Idle Specification for Continuous Access The continuous access idle specification makes insertions to clearly delineate the bus intervals by once negating the $\overline{CS0}$ signal when performing consecutive accesses to the same CS space. 0: No CS0 space continuous access idle cycle 1: One CS0 space continuous access idle cycle When a write immediately follows a read, the number of idle cycles inserted is the larger of the two values specified by IWO1 and IWO0.
3 to 1	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
0	SW0	1	R/W	CS0 Space $\overline{CS}$ Assert Extension Specification The $\overline{CS}$ assert cycle extension specification is for making insertions to prevent extension of the $\overline{RD}$ signal or $\overline{WRL}$ signal assert period beyond the length of the CS0 signal assert period. 0: No CS0 space $\overline{CS}$ assert extension inserted 1: CS0 space $\overline{CS}$ assert extension inserted (one cycle is inserted before and after each bus cycle)

7.5.3 Wait Control Register 1 (WCR1)

WCR1 is a 16-bit readable/writable register that specifies the number of wait cycles for CS0 space.

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 1	R/W	Reserved These bits are always read as 1. The write value should always be 1.
3	W03	1	R/W	CS0 Space Wait Specification
2	W02	1	R/W	These bits specify the number of waits for CS0 space access.
1	W01	1	R/W	
0	W00	1	R/W	0000: No wait (external wait input disabled) 0001: One wait (external wait input enabled) ⋮ 1111: 15 waits (external wait input enabled)

7.6 Accessing External Space

A strobe signal is output in external space accesses to provide primarily for SRAM or ROM direct connections.

7.6.1 Basic Timing

External access bus cycles are performed in 2 states. Figure 7.3 shows the basic timing of external space access.

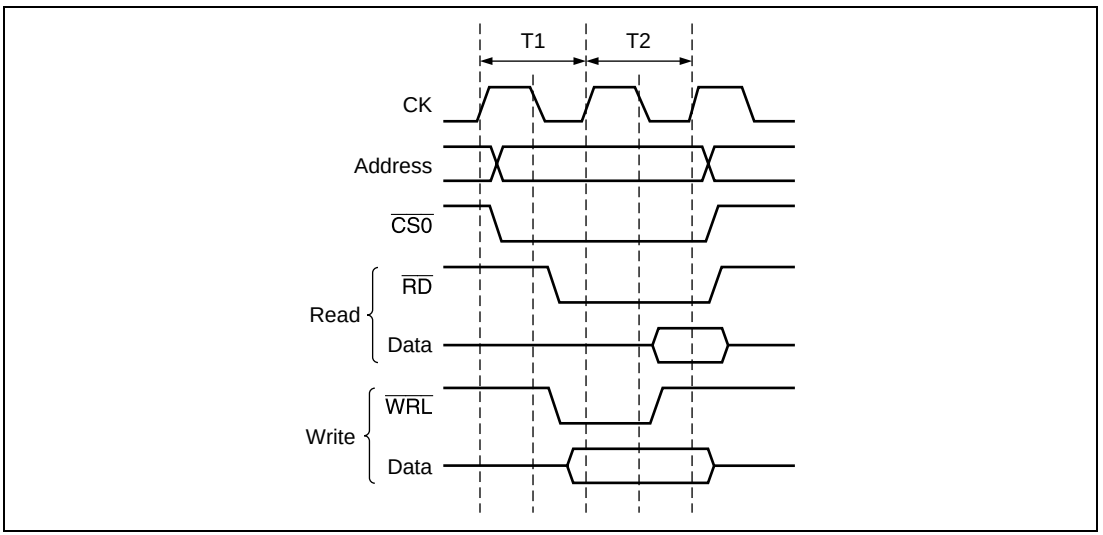


Figure 7.3 Basic Timing of External Space Access

During a read, irrespective of operand size, all bits (8 bits in this LSI) in the data bus width for the access space (address) accessed by $\overline{RD}$ signal are fetched by the LSI.

During a write, the $\overline{WRL}$ (bits 7 to 0) signal indicates the byte location to be written.

7.6.2 Wait State Control

The number of wait states inserted into external space access states can be controlled using the WCR1 settings. The specified number of TW cycles are inserted as software cycles at the timing shown in figure 7.4.

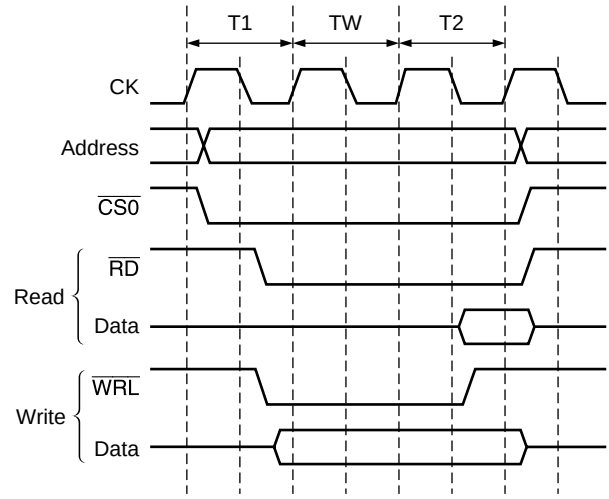


Figure 7.4 Wait State Timing of External Space Access (Software Wait Only)

When the wait is specified by software using WCR1, the wait input $\overline{\text{WAIT}}$ signal from outside is sampled. Figure 7.5 shows the $\overline{\text{WAIT}}$ signal sampling. The $\overline{\text{WAIT}}$ signal is sampled at the clock rise one cycle before the clock rise when the TW state shifts to the T2 state. When using external waits, use a WCR1 setting of 1 state or more in case of extending $\overline{\text{CS}}$ assertion, and 2 states or more otherwise.

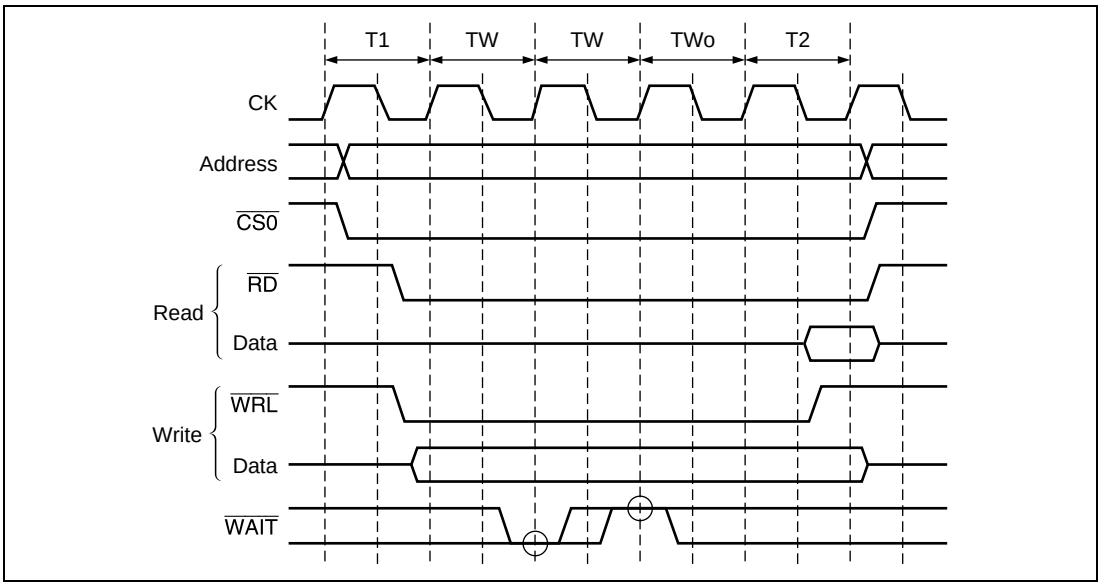


Figure 7.5 Wait State Timing of External Space Access (Two Software Wait States + $\overline{\text{WAIT}}$ Signal Wait State)

7.6.3 $\overline{CS}$ Assert Period Extension

Idle cycles can be inserted to prevent extension of the $\overline{RD}$ or $\overline{WRL}$ signal assert period beyond the length of the $\overline{CS0}$ signal assert period by setting the SW0 bit of BCR2. This allows for flexible interfaces with external circuitry. The timing is shown in figure 7.6. Th and Tf cycles are added respectively before and after the normal cycle. Only $\overline{CS0}$ is asserted in these cycles; $\overline{RD}$ and $\overline{WRL}$ signals are not. Further, data is extended up to the TF cycle, which is effective for gate arrays and the like, which have slower write operations.

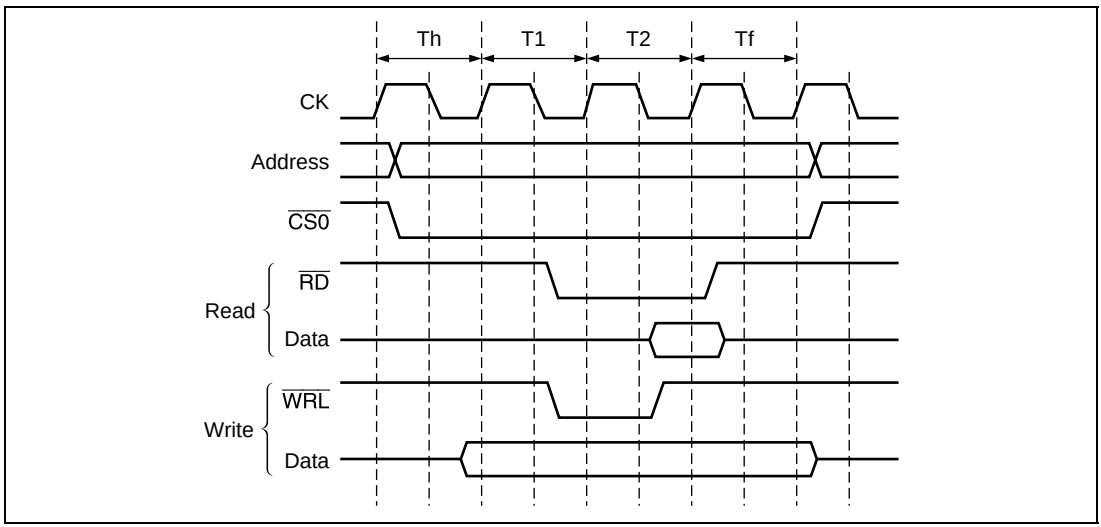


Figure 7.6 $\overline{CS}$ Assert Period Extension Function

7.7 Waits between Access Cycles

When a read from a slow device is completed, data buffers may not go off in time, causing conflict with the next access data. If there is a data conflict during memory access, the problem can be solved by inserting a wait in the access cycle.

To enable detection of the bus cycle start, a wait can be inserted between access cycles during continuous accesses of the same CS0 space by negating the $\overline{CS0}$ signal once.

7.7.1 Prevention of Data Bus Conflicts

Waits are inserted so that the number of write cycles after read cycle and the number of cycles specified by IW01 and IW00 bits of BCR2 can be inserted. When idle cycles already exist between access cycles, only the number of empty cycles remaining beyond the specified number of idle cycles are inserted.

7.7.2 Simplification of Bus Cycle Start Detection

For consecutive accesses to the same CS0 space, waits are inserted to provide the number of idle cycles designated by bit CW0 in BCR2. However, in the case of a write cycle after a read, the number of idle cycles inserted will be the larger of the two values designated by the IW and CW bits. When idle cycles already exist between access cycles, waits are not inserted.

Figure 7.7 shows an example. A continuous access idle is specified for CS0 space, and CS0 space is consecutively write-accessed.

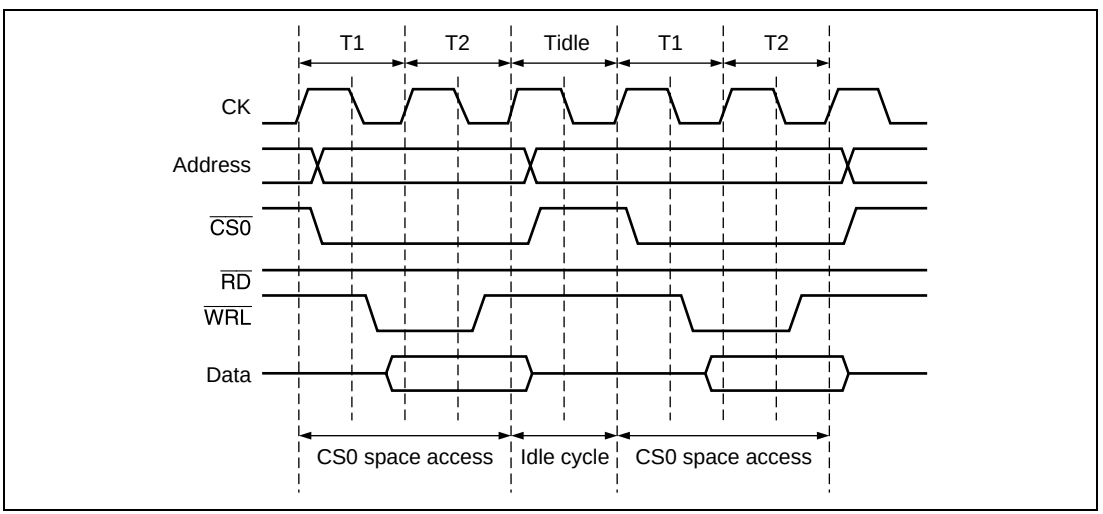


Figure 7.7 Example of Idle Cycle Insertion at Same Space Consecutive Access

7.8 Bus Arbitration

This LSI has a bus arbitration function that, when a bus release request is received from an external device, releases the bus to that device. It also has an internal bus master, the CPU. The priority for arbitrate the bus mastership between these bus masters is:

Bus request from external device > CPU

A bus request by an external device should be input to the $\overline{\text{BREQ}}$ pin. When the $\overline{\text{BREQ}}$ pin is asserted, this LSI releases the bus immediately after the bus cycle being executed is completed. The signal indicating that the bus has been released is output from the $\overline{\text{BACK}}$ pin.

However, the bus is not released between the read and write cycles during TAS instruction execution. Bus arbitration is not executed between multiple bus cycles that occur due to the data bus width smaller than access size, for instance, bus cycles in which 8-bit memory is accessed by a longword.

The bus may be returned when this LSI is releasing the bus. That is, when interrupt request occurs to be processed. This LSI incorporates the $\overline{\text{IRQOUT}}$ pin for the bus request signal. When the bus must be returned to this LSI, the $\overline{\text{IRQOUT}}$ signal can be asserted. The device that is asserting an external bus-release request negates the $\overline{\text{BREQ}}$ signal to release the bus when the $\overline{\text{IRQOUT}}$ signal is asserted. As a result, the bus is returned to and processed by this LSI. The asserting condition of the $\overline{\text{IRQOUT}}$ pin is that an interrupt source occurs and the interrupt request level is higher than that of interrupt mask bits I3 to I0 in the status register (SR).

Figure 7.8 shows the bus mastership release procedure.

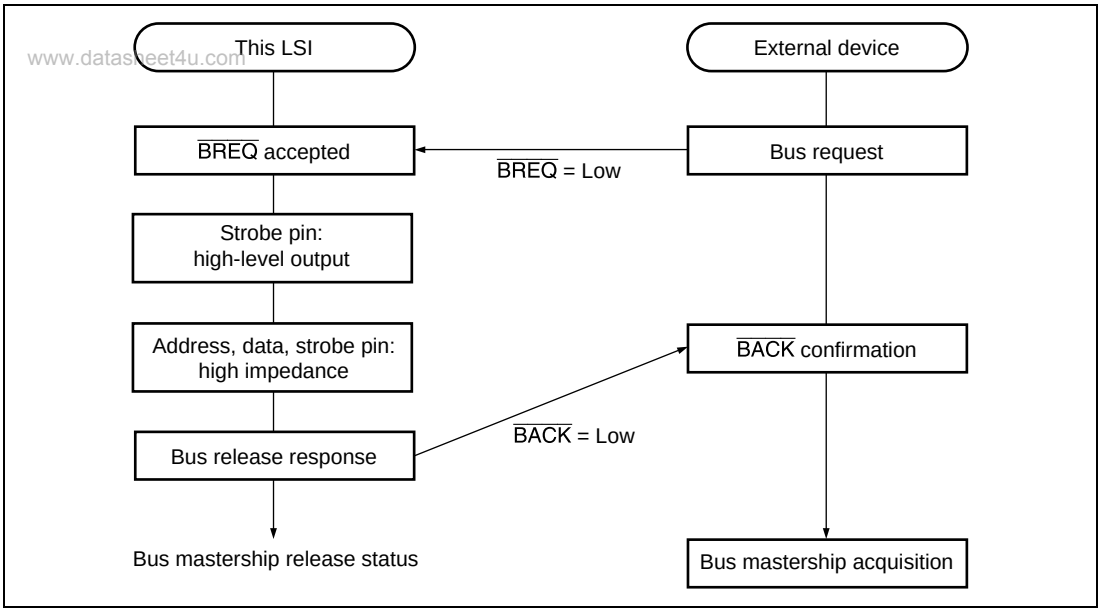


Figure 7.8 Bus Mastership Release Procedure

7.9 Memory Connection Example

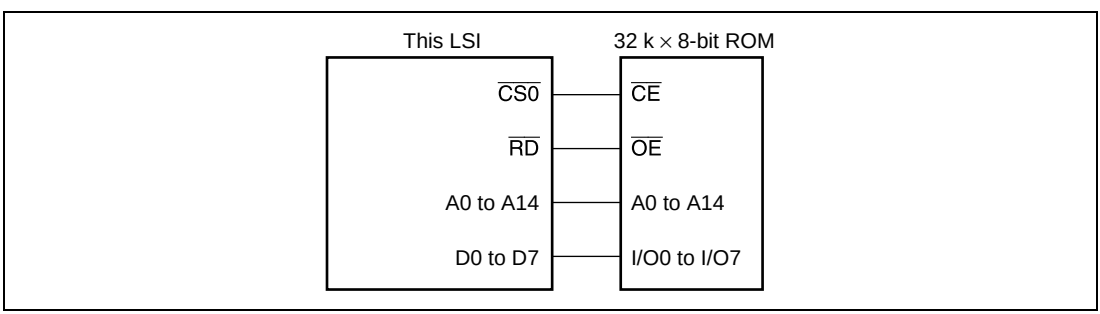


Figure 7.9 Example of 8-Bit Data Bus Width ROM Connection

7.10 On-chip Peripheral I/O Register Access

Internal I/O registers are accessed from the bus state controller, as shown in table 7.3.

Table 7.3 Access to Internal I/O Registers

Internal Module	SCI	MTU, POE	INTC	PFC, PORT	CMT	A/D	WDT	MMT
Connected bus width	8 bits	16 bits	16 bits	16 bits	16 bits	8 bits	16 bits	16 bits
Access cycles	2 cyc*1	2 cyc*1	2 cyc*2	2 cyc*1	2 cyc*1	3 cyc*1	3 cyc*2	2 cyc*1

Notes: 1. Converted to the peripheral clock.
2. Converted to the system clock.

7.11 Cycles in which Bus Is not Released

One Bus Cycle: The bus is never released during a single bus cycle. For example, in the case of a longword read (or write) in 8-bit normal space, four memory accesses to the 8-bit normal space constitute a single bus cycle, and the bus is never released during this period. Assuming that one memory access requires two states, the bus is not released during an 8-state period.

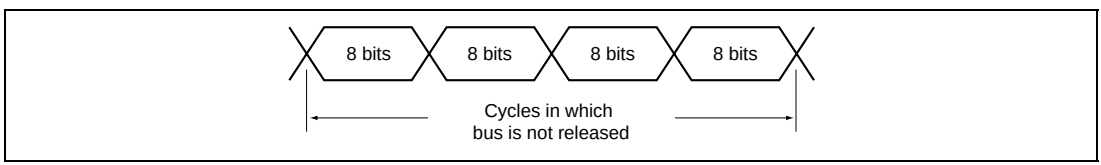


Figure 7.10 One Bus Cycle

7.12 CPU Operation when Program Is in External Memory

In this LSI, two words (equivalent to two instructions) are normally fetched in a single instruction fetch. This is also true when the program is located in external memory, irrespective of whether the external memory bus width is 8 or 16 bits.

If the program counter value immediately after the program branched is an odd-word (2n+1) address, or if the program counter value immediately before the program branches is an even-word (2n) address, the CPU will always fetch 32 bits (equivalent to two instructions) that include the respective word instruction.

Section 8 Multifunction Timer Pulse Unit (MTU)

This LSI has an on-chip multifunction timer pulse unit (MTU) that comprises five 16-bit timer channels.

The block diagram is shown in figure 8.1.

8.1 Features

- Maximum 16-pulse input/output
- Selection of 8 counter input clocks for each channel
- The following operations can be set for each channel:
  - — Waveform output at compare match
  - — Input capture function
  - — Counter clear operation

    Multiple timer counters (TCNT) can be written to simultaneously

    Simultaneous clearing by compare match and input capture is possible

    Register simultaneous input/output is possible by synchronous counter operation
  - — A maximum 12-phase PWM output is possible in combination with synchronous operation
- Buffer operation settable for channels 0, 3, and 4
- Phase counting mode settable independently for each of channels 1 and 2
- Cascade connection operation
- Fast access via internal 16-bit bus
- 23 interrupt sources
- Automatic transfer of register data
- A/D converter conversion start trigger can be generated
- Module standby mode can be set
- Positive and negative 3-phase waveforms (6-phase waveforms in total) can be output in complementary or reset synchronous PWM mode by combining channels 3 and 4.
- AC synchronous motor (brushless DC motor) can be driven in complementary or reset synchronous PWM mode by combining channels 0, 3, and 4. Chopping or level output can be selected as drive waveform output.

Table 8.1 MTU Functions

Item		Channel 0	Channel 1	Channel 2	Channel 3	Channel 4
Count clock		Pϕ/1 Pϕ/4 Pϕ/16 Pϕ/64 TCLKA TCLKB TCLKC TCLKD	Pϕ/1 Pϕ/4 Pϕ/16 Pϕ/64 Pϕ/256 TCLKA TCLKB	Pϕ/1 Pϕ/4 Pϕ/16 Pϕ/64 Pϕ/1024 TCLKA TCLKB TCLKC	Pϕ/1 Pϕ/4 Pϕ/16 Pϕ/64 Pϕ/256 Pϕ/1024 TCLKA TCLKB	Pϕ/1 Pϕ/4 Pϕ/16 Pϕ/64 Pϕ/256 Pϕ/1024 TCLKA TCLKB
General registers		TGRA_0 TGRB_0	TGRA_1 TGRB_1	TGRA_2 TGRB_2	TGRA_3 TGRB_3	TGRA_4 TGRB_4
General registers/ buffer registers		TGRC_0 TGRD_0	—	—	TGRC_3 TGRD_3	TGRC_4 TGRD_4
I/O pins		TIOC0A TIOC0B TIOC0C TIOC0D	TIOC1A TIOC1B	TIOC2A TIOC2B	TIOC3A TIOC3B TIOC3C TIOC3D	TIOC4A TIOC4B TIOC4C TIOC4D
Counter clear function		TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture
Compare match output	0 output	○	○	○	○	○
	1 output	○	○	○	○	○
	Toggle output	○	○	○	○	○
Input capture function		○	○	○	○	○
Synchronous operation		○	○	○	○	○
PWM mode 1		○	○	○	○	○
PWM mode 2		○	○	○	—	—
Complementary PWM mode		—	—	—	○	○
Reset synchronous PWM mode		—	—	—	○	○
AC synchronous motor drive mode		○	—	—	○	○
Phase counting mode		—	○	○	—	—

Item	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4
Buffer operation	○	—	—	○	○
A/D converter start trigger	TGRA_0 compare match or input capture	TGRA_1 compare match or input capture	TGRA_2 compare match or input capture	TGRA_3 compare match or input capture	TGRA_4 compare match or input capture
Interrupt sources	5 sources • Compare match or input capture 0A • Compare match or input capture 0B • Compare match or input capture 0C • Compare match or input capture 0D • Overflow	4 sources • Compare match or input capture 1A • Compare match or input capture 1B • Overflow • Underflow	4 sources • Compare match or input capture 2A • Compare match or input capture 2B • Overflow • Underflow	5 sources • Compare match or input capture 3A • Compare match or input capture 3B • Compare match or input capture 3C • Compare match or input capture 3D • Overflow	5 sources • Compare match or input capture 4A • Compare match or input capture 4B • Compare match or input capture 4C • Compare match or input capture 4D • Overflow • Underflow

Legend:

○ : Possible

— : Not possible

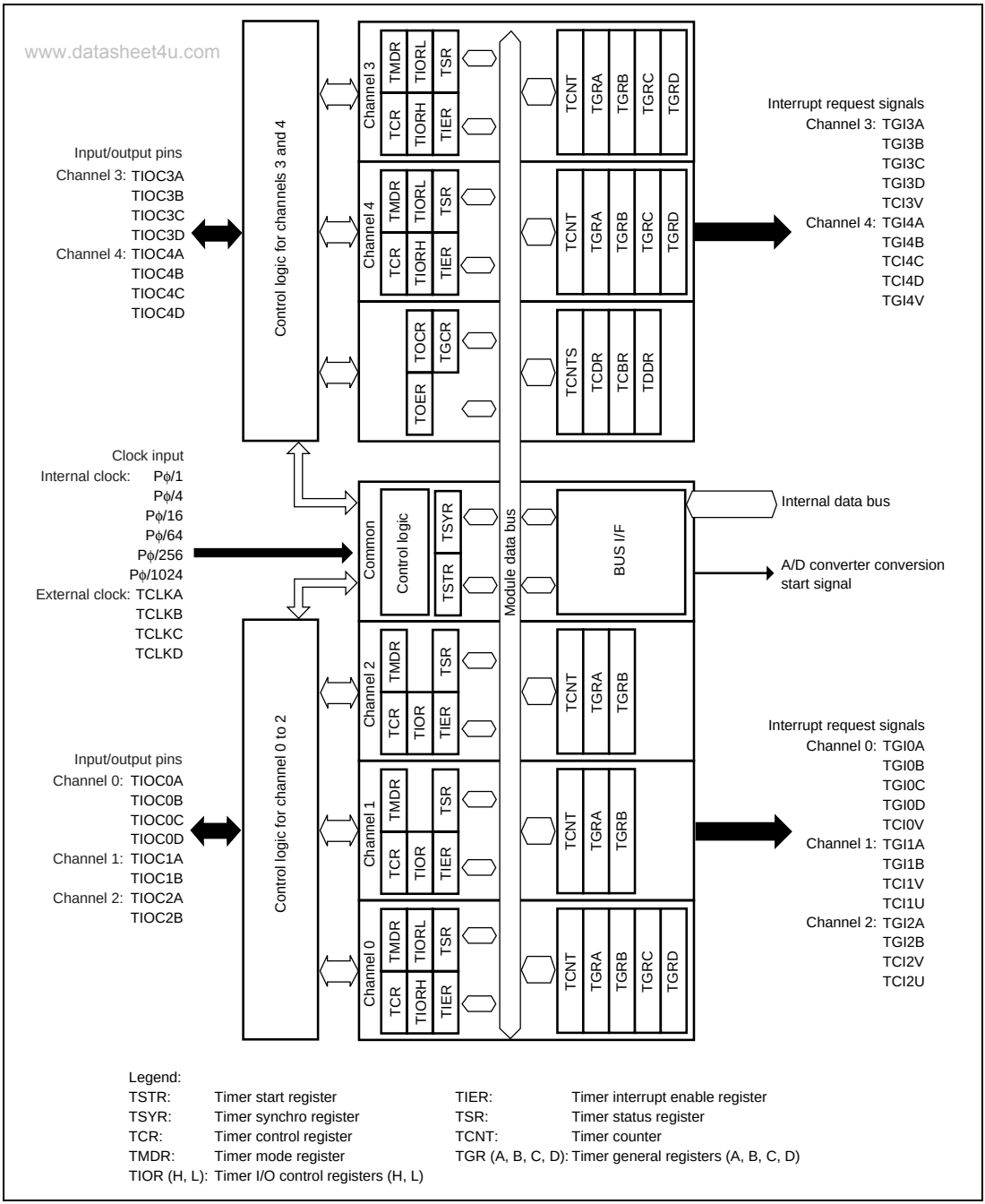


Figure 8.1 Block Diagram of TPU

8.2 Input/Output Pins

Table 8.2 Pin Configuration

Channel	Symbol	I/O	Function
Common	TCLKA	Input	External clock A input pin (Channel 1 phase counting mode A phase input)
	TCLKB	Input	External clock B input pin (Channel 1 phase counting mode B phase input)
	TCLKC	Input	External clock C input pin (Channel 2 phase counting mode A phase input)
	TCLKD	Input	External clock D input pin (Channel 2 phase counting mode B phase input)
0	TIOC0A	I/O	TGRA_0 input capture input/output compare output/PWM output pin
	TIOC0B	I/O	TGRB_0 input capture input/output compare output/PWM output pin
	TIOC0C	I/O	TGRC_0 input capture input/output compare output/PWM output pin
	TIOC0D	I/O	TGRD_0 input capture input/output compare output/PWM output pin
1	TIOC1A	I/O	TGRA_1 input capture input/output compare output/PWM output pin
	TIOC1B	I/O	TGRB_1 input capture input/output compare output/PWM output pin
2	TIOC2A	I/O	TGRA_2 input capture input/output compare output/PWM output pin
	TIOC2B	I/O	TGRB_2 input capture input/output compare output/PWM output pin
3	TIOC3A	I/O	TGRA_3 input capture input/output compare output/PWM output pin
	TIOC3B	I/O	TGRB_3 input capture input/output compare output/PWM output pin
	TIOC3C	I/O	TGRC_3 input capture input/output compare output/PWM output pin
	TIOC3D	I/O	TGRD_3 input capture input/output compare output/PWM output pin
4	TIOC4A	I/O	TGRA_4 input capture input/output compare output/PWM output pin
	TIOC4B	I/O	TGRB_4 input capture input/output compare output/PWM output pin
	TIOC4C	I/O	TGRC_4 input capture input/output compare output/PWM output pin
	TIOC4D	I/O	TGRD_4 input capture input/output compare output/PWM output pin

8.3 Register Descriptions

The MTU has the following registers. For details on register addresses and register states during each process, refer to section 19, List of Registers. To distinguish registers in each channel, an underscore and the channel number are added as a suffix to the register name; TCR for channel 0 is expressed as TCR_0.

Channel 0

- Timer control register_0 (TCR_0)
- Timer mode register_0 (TMDR_0)
- Timer I/O control register H_0 (TIORH_0)
- Timer I/O control register L_0 (TIORL_0)
- Timer interrupt enable register_0 (TIER_0)
- Timer status register_0 (TSR_0)
- Timer counter_0 (TCNT_0)
- Timer general register A_0 (TGRA_0)
- Timer general register B_0 (TGRB_0)
- Timer general register C_0 (TGRC_0)
- Timer general register D_0 (TGRD_0)

Channel 1

- Timer control register_1 (TCR_1)
- Timer mode register_1 (TMDR_1)
- Timer I/O control register _1 (TIOR_1)
- Timer interrupt enable register_1 (TIER_1)
- Timer status register_1 (TSR_1)
- Timer counter_1 (TCNT_1)
- Timer general register A_1 (TGRA_1)
- Timer general register B_1 (TGRB_1)

Channel 2

- Timer control register_2 (TCR_2)
- Timer mode register_2 (TMDR_2)
- Timer I/O control register_2 (TIOR_2)
- Timer interrupt enable register_2 (TIER_2)
- Timer status register_2 (TSR_2)
- Timer counter_2 (TCNT_2)

- Timer general register A_2 (TGRA_2)
- Timer general register B_2 (TGRB_2)

Channel 3

- Timer control register_3 (TCR_3)
- Timer mode register_3 (TMDR_3)
- Timer I/O control register H_3 (TIORH_3)
- Timer I/O control register L_3 (TIORL_3)
- Timer interrupt enable register_3 (TIER_3)
- Timer status register_3 (TSR_3)
- Timer counter_3 (TCNT_3)
- Timer general register A_3 (TGRA_3)
- Timer general register B_3 (TGRB_3)
- Timer general register C_3 (TGRC_3)
- Timer general register D_3 (TGRD_3)

Channel 4

- Timer control register_4 (TCR_4)
- Timer mode register_4 (TMDR_4)
- Timer I/O control register H_4 (TIORH_4)
- Timer I/O control register L_4 (TIORL_4)
- Timer interrupt enable register_4 (TIER_4)
- Timer status register_4 (TSR_4)
- Timer counter_4 (TCNT_4)
- Timer general register A_4 (TGRA_4)
- Timer general register B_4 (TGRB_4)
- Timer general register C_4 (TGRC_4)
- Timer general register D_4 (TGRD_4)

Common registers

- Timer start register (TSTR)
- Timer synchro register (TSYR)

Common registers for timers 3 and 4

- Timer output master enable register (TOER)
- Timer output control enable register (TOCR)

- Timer gate control register (TGCR)
- Timer cycle data register (TCDR)
- Timer dead time data register (TDDR)
- Timer subcounter (TCNTS)
- Timer cycle buffer register (TCBR)

8.3.1 Timer Control Register (TCR)

The TCR registers are 8-bit readable/writable registers that control the TCNT operation for each channel. The MTU has a total of five TCR registers, one for each channel (channel 0 to 4). TCR register settings should be conducted only when TCNT operation is stopped.

Bit	Bit Name	Initial value	R/W	Description
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0	R/W	These bits select the TCNT counter clearing source. See tables 8.3 and 8.4 for details.
5	CCLR0	0	R/W	
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge. When the input clock is counted using both edges, the input clock period is halved (e.g. Pϕ/4 both edges = ϕ/2 rising edge). If phase counting mode is used on channels 1 and 2, this setting is ignored and the phase counting mode setting has priority. Internal clock edge selection is valid when the input clock is Pϕ/4 or slower. When Pϕ/1, or the overflow/underflow of another channel is selected for the input clock, although values can be written, counter operation compiles with the initial value. 00: Count at rising edge 01: Count at falling edge 1x: Count at both edges Legend: x: Don't care
2	TPSC2	0	R/W	Time Prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the TCNT counter clock. The clock source can be selected independently for each channel. See tables 8.5 to 8.8 for details.
0	TPSC0	0	R/W	

Table 8.3 CCLR0 to CCLR2 (Channels 0, 3, and 4)

Channel	Bit 7 CCLR2	Bit 6 CCLR1	Bit 5 CCLR0	Description
0, 3, 4	0	0	0	TCNT clearing disabled
			1	TCNT cleared by TGRA compare match/input capture
		1	0	TCNT cleared by TGRB compare match/input capture
			1	TCNT cleared by counter clearing for another channel performing synchronous clearing/ synchronous operation*[1]
	1	0	0	TCNT clearing disabled
			1	TCNT cleared by TGRC compare match/input capture*[2]
		1	0	TCNT cleared by TGRD compare match/input capture*[2]
			1	TCNT cleared by counter clearing for another channel performing synchronous clearing/ synchronous operation*[1]

Notes: 1. Synchronous operation is set by setting the SYNC bit in TSYR to 1.
2. When TGRC or TGRD is used as a buffer register, TCNT is not cleared because the buffer register setting has priority, and compare match/input capture does not occur.

Table 8.4 CCLR0 to CCLR2 (Channels 1 and 2)

Channel	Bit 7 Reserved*[2]	Bit 6 CCLR1	Bit 5 CCLR0	Description
1, 2	0	0	0	TCNT clearing disabled
			1	TCNT cleared by TGRA compare match/input capture
		1	0	TCNT cleared by TGRB compare match/input capture
			1	TCNT cleared by counter clearing for another channel performing synchronous clearing/ synchronous operation*[1]

Notes: 1. Synchronous operation is selected by setting the SYNC bit in TSYR to 1.
2. Bit 7 is reserved in channels 1 and 2. It is always read as 0. Writing is ignored.

Table 8.5 TPSC0 to TPSC2 (Channel 0)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
0	0	0	0	Internal clock: counts on Pϕ/1
			1	Internal clock: counts on Pϕ/4
		1	0	Internal clock: counts on Pϕ/16
			1	Internal clock: counts on Pϕ/64
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKB pin input
		1	0	External clock: counts on TCLKC pin input
			1	External clock: counts on TCLKD pin input

Table 8.6 TPSC0 to TPSC2 (Channel 1)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
1	0	0	0	Internal clock: counts on Pϕ/1
			1	Internal clock: counts on Pϕ/4
		1	0	Internal clock: counts on Pϕ/16
			1	Internal clock: counts on Pϕ/64
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKB pin input
		1	0	Internal clock: counts on Pϕ/256
			1	Counts on TCNT_2 overflow/underflow

Note: This setting is ignored when channel 1 is in phase counting mode.

Table 8.7 TPSC0 to TPSC2 (Channel 2)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
2	0	0	0	Internal clock: counts on Pϕ/1
			1	Internal clock: counts on Pϕ/4
		1	0	Internal clock: counts on Pϕ/16
			1	Internal clock: counts on Pϕ/64
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKB pin input
		1	0	External clock: counts on TCLKC pin input
			1	Internal clock: counts on Pϕ/1024

Note: This setting is ignored when channel 2 is in phase counting mode.

Table 8.8 TPSC0 to TPSC2 (Channels 3 and 4)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
3, 4	0	0	0	Internal clock: counts on Pϕ/1
			1	Internal clock: counts on Pϕ/4
		1	0	Internal clock: counts on Pϕ/16
			1	Internal clock: counts on Pϕ/64
	1	0	0	Internal clock: counts on Pϕ/256
			1	Internal clock: counts on Pϕ/1024
		1	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKB pin input

8.3.2 Timer Mode Register (TMDR)

The TMDR registers are 8-bit readable/writable registers that are used to set the operating mode of each channel. The MTU has five TMDR registers, one for each channel. TMDR register settings should be changed only when TCNT operation is stopped.

Bit	Bit Name	Initial value	R/W	Description
7, 6	—	All 1	—	Reserved These bits are always read as 1. The write value should always be 1.
5	BFB	0	R/W	Buffer Operation B Specifies whether TGRB is to operate in the normal way, or TGRB and TGRD are to be used together for buffer operation. When TGRD is used as a buffer register, TGRD input capture/output compare is not generated. In channels 1 and 2, which have no TGRD, bit 5 is reserved. It is always read as 0, and the write value should always be 0. 0: TGRB and TGRD operate normally 1: TGRB and TGRD used together for buffer operation
4	BFA	0	R/W	Buffer Operation A Specifies whether TGRA is to operate in the normal way, or TGRA and TGRC are to be used together for buffer operation. When TGRC is used as a buffer register, TGRC input capture/output compare is not generated. In channels 1 and 2, which have no TGRC, bit 4 is reserved. It is always read as 0, and the write value should always be 0. 0: TGRA and TGRD operate normally 1: TGRA and TGRC used together for buffer operation
3	MD3	0	R/W	Modes 3 to 0 These bits are used to set the timer operating mode. See table 8.9 for details.
2	MD2	0	R/W	
1	MD1	0	R/W	
0	MD0	0	R/W	

Table 8.9 MD0 to MD3

Bit 3 MD3	Bit 2 MD2	Bit 1 MD1	Bit 0 MD0	Description
0	0	0	0	Normal operation
			1	Reserved (setting prohibited)
		1	0	PWM mode 1
			1	PWM mode 2*[1]
	1	0	0	Phase counting mode 1*[2]
			1	Phase counting mode 2*[2]
		1	0	Phase counting mode 3*[2]
			1	Phase counting mode 4*[2]
1	0	0	0	Reset synchronous PWM mode*[3]
			1	Reserved (setting prohibited)
		1	x	Reserved (setting prohibited)
	1	0	0	Reserved (setting prohibited)
			1	Complementary PWM mode 1 (transmit at peak)*[3]
		1	0	Complementary PWM mode 2 (transmit at trough)*[3]
			1	Complementary PWM mode 2 (transmit at peak and trough)*[3]

Legend: x: Don't care

Notes: 1. PWM mode 2 can not be set for channels 3 and 4.

2. Phase counting mode can not be set for channels 0, 3, and 4.

3. Reset synchronous PWM mode, complementary PWM mode can only be set for channel 3. When channel 3 is set to reset synchronous PWM mode or complementary PWM mode, the channel 4 settings become ineffective and automatically conform to the channel 3 settings. However, do not set channel 4 to reset synchronous PWM mode or complementary PWM mode. Reset synchronous PWM mode and complementary PWM mode can not be set for channels 0, 1, and 2.

8.3.3 Timer I/O Control Register (TIOR)

The TIOR registers are 8-bit readable/writable registers that control the TGR registers. The MTU has eight TIOR registers, two each for channels 0, 3, and 4, and one each for channels 1 and 2.

Care is required as TIOR is affected by the TMDR setting. The initial output specified by TIOR is valid when the counter is stopped (the CST bit in TSTR is cleared to 0). Note also that, in PWM mode 2, the output at the point at which the counter is cleared to 0 is specified.

When TGRC or TGRD is designated for buffer operation, this setting is invalid and the register operates as a buffer register.

TIORH_0, TIOR_1, TIOR_2, TIORH_3, TIORH_4

Bit	Bit Name	Initial value	R/W	Description
7	IOB3	0	R/W	I/O Control B3 to B0
6	IOB2	0	R/W	Specify the function of TGRB.
5	IOB1	0	R/W	See the following tables.
4	IOB0	0	R/W	TIORH_0: Table 8.10 TIOR_1: Table 8.14 TIOR_2: Table 8.16 TIORH_3: Table 8.18 TIORH_4: Table 8.22
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	Specify the function of TGRA.
1	IOA1	0	R/W	See the following tables.
0	IOA0	0	R/W	TIORH_0: Table 8.11 TIOR_1: Table 8.15 TIOR_2: Table 8.17 TIORH_3: Table 8.19 TIORH_4: Table 8.23

TIORL_0, TIORL_3, TIORL_4

Bit	Bit Name	Initial value	R/W	Description
7	IOD3	0	R/W	I/O Control D3 to D0
6	IOD2	0	R/W	Specify the function of TGRD.
5	IOD1	0	R/W	When the TGRD is used as a buffer register of the TGRB, this setting is invalid and input capture/output compare is not generated. See the following tables. TIORL_0: Table 8.12 TIORL_3: Table 8.20 TIORL_4: Table 8.24
4	IOD0	0	R/W	
3	IOC3	0	R/W	I/O Control C3 to C0
2	IOC2	0	R/W	Specify the function of TGRC.
1	IOC1	0	R/W	When the TGRC is used as a buffer register of the TGRA, this setting is invalid and input capture/output compare is not generated. See the following tables. TIORL_0: Table 8.13 TIORL_3: Table 8.21 TIORL_4: Table 8.25
0	IOC0	0	R/W	

Table 8.10 TIORH_0 (Channel 0)

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_0 Function**	**TIOC0B Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Capture input source is channel 1/count clock Input capture at TCNT_1 count- up/count-down

Legend: x: Don’t care

Table 8.11 TIORH_0 (Channel 0)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_0 Function**	**TIOC0A Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Capture input source is channel 1/count clock Input capture at TCNT_1 count-up/count-down

Legend: x: Don't care

Table 8.12 TIORL_0 (Channel 0)

				Description	
Bit 7 IOD3	**Bit 6 IOD2**	**Bit 5 IOD1**	**Bit 4 IOD0**	**TGRD_0 Function**	**TIOC0D Pin Function**
0	0	0	0	Output compare register*	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register*	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Capture input source is channel 1/count clock Input capture at TCNT_1 count-up/count-down

Legend: x: Don't care

Note: * When the BFB bit in TMDR_0 is set to 1 and TGRD_0 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 8.13 TIORL_0 (Channel 0)

				Description	
Bit 3 IOC3	**Bit 2 IOC2**	**Bit 1 IOC1**	**Bit 0 IOC0**	**TGRC_0 Function**	**TIOC0C Pin Function**
0	0	0	0	Output compare register*	Output hold*[1]
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register*	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Capture input source is channel 1/count clock Input capture at TCNT_1 count-up/count-down

Legend: x: Don't care

Note: * When the BFA bit in TMDR_0 is set to 1 and TGRC_0 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 8.14 TIOR_1 (Channel 1)

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_1 Function**	**TIOC1B Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Input capture at generation of TGRC_0 compare match/input capture

Legend: x: Don't care

Table 8.15 TIOR_1 (Channel 1)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_1 Function**	**TIOC1A Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Input capture at generation of channel 0/TGRA_0 compare match/input capture

Legend: x: Don't care

Table 8.16 TIOR_2 (Channel 2)

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_2 Function**	**TIOC2B Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges

Legend: x: Don't care

Table 8.17 TIOR_2 (channel 2)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_2 Function**	**TIOC2A Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

Legend: x: Don't care

Table 8.18 TIORH_3 (Channel 3)

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_3 Function**	**TIOC3B Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

Legend: x: Don't care

Table 8.19 TIORH_3 (Channel 3)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_3 Function**	**TIOC3A Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

Legend: x: Don't care

Table 8.20 TIORL_3 (Channel 3)

				Description	
Bit 7 IOD3	**Bit 6 IOD2**	**Bit 5 IOD1**	**Bit 4 IOD0**	**TGRD_3 Function**	**TIOC3D Pin Function**
0	0	0	0	Output compare register*	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register*[2]	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

Legend: x: Don't care

Note: * When the BFB bit in TMDR_3 is set to 1 and TGRD_3 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 8.21 TIORL_3 (Channel 3)

				Description	
Bit 3 IOC3	**Bit 2 IOC2**	**Bit 1 IOC1**	**Bit 0 IOC0**	**TGRC_3 Function**	**TIOC3C Pin Function**
0	0	0	0	Output compare register*	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register*	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

Legend: x: Don't care

Note: * When the BFA bit in TMDR_3 is set to 1 and TGRC_3 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 8.22 TIORH_4 (Channel 4)

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_4 Function**	**TIOC4B Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

Legend: x: Don't care

Table 8.23 TIORH_4 (Channel 4)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_4 Function**	**TIOC4A Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

Legend: x: Don't care

Table 8.24 TIORL_4 (Channel 4)

				Description	
Bit 7 IOD3	**Bit 6 IOD2**	**Bit 5 IOD1**	**Bit 4 IOD0**	**TGRD_4 Function**	**TIOC4B Pin Function**
0	0	0	0	Output compare register*	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

Legend: x: Don't care

Note: * When the BFB bit in TMDR_4 is set to 1 and TGRD_4 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 8.25 TIORL_4 (Channel 4)

				Description	
Bit 3 IOC3	**Bit 2 IOC2**	**Bit 1 IOC1**	**Bit 0 IOC0**	**TGRC_4 Function**	**TIOC4C Pin Function**
0	0	0	0	Output compare register*	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output value retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

Legend: x: Don't care

Note: * When the BFA bit in TMDR_4 is set to 1 and TGRC_4 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

8.3.4 Timer Interrupt Enable Register (TIER)

The TIER registers are 8-bit readable/writable registers that control enabling or disabling of interrupt requests for each channel. The MTU has five TIER registers, one for each channel.

Bit	Bit Name	Initial value	R/W	Description
7	TTGE	0	R/W	A/D Conversion Start Request Enable Enables or disables generation of A/D conversion start requests by TGRA input capture/compare match. 0: A/D conversion start request generation disabled 1: A/D conversion start request generation enabled
6	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
5	TCIEU	0	R/W	Underflow Interrupt Enable Enables or disables interrupt requests (TCIU) by the TCFU flag when the TCFU flag in TSR is set to 1 in channels 1 and 2. In channels 0, 3, and 4, bit 5 is reserved. It is always read as 0, and the write value should always be 0. 0: Interrupt requests (TCIU) by TCFU disabled 1: Interrupt requests (TCIU) by TCFU enabled
4	TCIEV	0	R/W	Overflow Interrupt Enable Enables or disables interrupt requests (TCIV) by the TCFV flag when the TCFV flag in TSR is set to 1. 0: Interrupt requests (TCIV) by TCFV disabled 1: Interrupt requests (TCIV) by TCFV enabled
3	TGIED	0	R/W	TGR Interrupt Enable D Enables or disables interrupt requests (TGID) by the TGFD bit when the TGFD bit in TSR is set to 1 in channels 0, 3, and 4. In channels 1 and 2, bit 3 is reserved. It is always read as 0, and the write value should always be 0. 0: Interrupt requests (TGID) by TGFD bit disabled 1: Interrupt requests (TGID) by TGFD bit enabled

Bit	Bit Name	Initial value	R/W	Description
2	TGIEC	0	R/W	TGR Interrupt Enable C Enables or disables interrupt requests (TGIC) by the TGFC bit when the TGFC bit in TSR is set to 1 in channels 0, 3, and 4. In channels 1 and 2, bit 2 is reserved. It is always read as 0, and the write value should always be 0. 0: Interrupt requests (TGIC) by TGFC bit disabled 1: Interrupt requests (TGIC) by TGFC bit enabled
1	TGIEB	0	R/W	TGR Interrupt Enable B Enables or disables interrupt requests (TGIB) by the TGFB bit when the TGFB bit in TSR is set to 1. 0: Interrupt requests (TGIB) by TGFB bit disabled 1: Interrupt requests (TGIB) by TGFB bit enabled
0	TGIEA	0	R/W	TGR Interrupt Enable A Enables or disables interrupt requests (TGIA) by the TGFA bit when the TGFA bit in TSR is set to 1. 0: Interrupt requests (TGIA) by TGFA bit disabled 1: Interrupt requests (TGIA) by TGFA bit enabled

8.3.5 Timer Status Register (TSR)

The TSR registers are 8-bit readable/writable registers that indicate the status of each channel. The MTU has five TSR registers, one for each channel.

Bit	Bit Name	Initial value	R/W	Description
7	TCFD	1	R	Count Direction Flag Status flag that shows the direction in which TCNT counts in channels 1, 2, 3, and 4. In channel 0, bit 7 is reserved. It is always read as 1, and should only be written with 1. 0: TCNT counts down 1: TCNT counts up
6	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
5	TCFU	0	R/(W)	Underflow Flag Status flag that indicates that TCNT underflow has occurred when channels 1 and 2 are set to phase counting mode. Only 0 can be written, for flag clearing. In channels 0, 3, and 4, bit 5 is reserved. It is always read as 0, and the write value should always be 0. [Setting condition] • When the TCNT value underflows (changes from H'0000 to H'FFFF) [Clearing condition] • When 0 is written to TCFU after reading TCFU = 1
4	TCFV	0	R/(W)	Overflow Flag Status flag that indicates that TCNT overflow has occurred. Only 0 can be written, for flag clearing. [Setting condition] • When the TCNT value overflows (changes from H'FFFF to H'0000) In channel 4, when TCNT-4 is underflowed (H'0001 → H'0000) in complementary PWM mode. [Clearing condition] • When 0 is written to TCFV after reading TCFV = 1

Bit	Bit Name	Initial value	R/W	Description
3	TGFD	0	R/(W)	Input Capture/Output Compare Flag D Status flag that indicates the occurrence of TGRD input capture or compare match in channels 0, 3, and 4. Only 0 can be written, for flag clearing. In channels 1 and 2, bit 3 is reserved. It is always read as 0, and the write value should always be 0. [Setting conditions] • When TCNT = TGRD and TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal and TGRD is functioning as input capture register [Clearing condition] • When 0 is written to TGFD after reading TGFD = 1
2	TGFC	0	R/(W)	Input Capture/Output Compare Flag C Status flag that indicates the occurrence of TGRC input capture or compare match in channels 0, 3, and 4. Only 0 can be written, for flag clearing. In channels 1 and 2, bit 2 is reserved. It is always read as 0, and the write value should always be 0. [Setting conditions] • When TCNT = TGRC and TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal and TGRC is functioning as input capture register [Clearing condition] • When 0 is written to TGFC after reading TGFC = 1

Bit	Bit Name	Initial value	R/W	Description
1	TGFB	0	R/(W)	Input Capture/Output Compare Flag B Status flag that indicates the occurrence of TGRB input capture or compare match. Only 0 can be written, for flag clearing. [Setting conditions] • When TCNT = TGRB and TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal and TGRB is functioning as input capture register [Clearing condition] • When 0 is written to TGFB after reading TGFB = 1
0	TGFA	0	R/(W)	Input Capture/Output Compare Flag A Status flag that indicates the occurrence of TGRA input capture or compare match. Only 0 can be written, for flag clearing. [Setting conditions] • When TCNT = TGRA and TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal and TGRA is functioning as input capture register [Clearing condition] • When 0 is written to TGFA after reading TGFA = 1

8.3.6 Timer Counter (TCNT)

The TCNT registers are 16-bit readable/writable counters. The MTU has five TCNT counters, one for each channel. The initial value is H'0000.

Access to TCNT in 8-bit units is not allowed. Applications must always access TCNT in 16-bit units. Note that TCNT is initialized to H'0000 by a reset.

8.3.7 Timer General Register (TGR)

The TGR registers are dual function 16-bit readable/writable registers, functioning as either output compare or input capture registers. The MTU has 16 TGR registers, four each for channels 0, 3, and 4 and two each for channels 1 and 2. TGRC and TGRD for channels 0, 3, and 4 can also be designated for operation as buffer registers. The TGR registers cannot be accessed in 8-bit units; they must always be accessed as a 16-bit unit. TGR buffer register combinations are TGRA—TGRC and TGRB—TGRD. The initial value is H'FFFF.

8.3.8 Timer Start Register (TSTR)

TSTR is an 8-bit readable/writable register that selects operation/stoppage for channels 0 to 4. When setting the operating mode in TMDR or setting the count clock in TCR, first stop the TCNT counter.

Bit	Bit Name	Initial value	R/W	Description
7	CST4	0	R/W	Counter Start 4 and 3
6	CST3	0	R/W	These bits select operation or stoppage for TCNT. If 0 is written to the CST bit during operation with the TIOC pin designated for output, the counter stops but the TIOC pin output compare output level is retained. If TIOR is written to when the CST bit is cleared to 0, the pin output level will be changed to the set initial output value. 0: TCNT_4 and TCNT_3 count operation is stopped 1: TCNT_4 and TCNT_3 performs count operation
5 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	CST2	0	R/W	Counter Start 2 to 0
1	CST1	0	R/W	These bits select operation or stoppage for TCNT. If 0 is written to the CST bit during operation with the TIOC pin designated for output, the counter stops but the TIOC pin output compare output level is retained. If TIOR is written to when the CST bit is cleared to 0, the pin output level will be changed to the set initial output value. 0: TCNT_2 and TCNT_0 count operation is stopped 1: TCNT_2 and TCNT_0 performs count operation
0	CST0	0	R/W	

8.3.9 Timer Synchro Register (TSYR)

TSYR is an 8-bit readable/writable register that selects independent operation or synchronous operation for the channel 0 to 4 TCNT counters. A channel performs synchronous operation when the corresponding bit in TSYR is set to 1.

Bit	Bit Name	Initial value	R/W	Description
7	SYNC4	0	R/W	Timer Synchro 4 and 3
6	SYNC3	0	R/W	These bits are used to select whether operation is independent of or synchronized with other channels. When synchronous operation is selected, the TCNT synchronous presetting of multiple channels, and synchronous clearing by counter clearing on another channel, are possible. To set synchronous operation, the SYNC bits for at least two channels must be set to 1. To set synchronous clearing, in addition to the SYNC bit, the TCNT clearing source must also be set by means of bits CCLR0 to CCLR2 in TCR. 0: TCNT_4 and TCNT_3 operate independently (TCNT presetting/clearing is unrelated to other channels) 1: TCNT_4 and TCNT_3 performs synchronous operation TCNT synchronous presetting/synchronous clearing is possible
5 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial value	R/W	Description
2	SYNC2	0	R/W	Timer Synchro 2 to 0
1	SYNC1	0	R/W	These bits are used to select whether operation is independent of or synchronized with other channels.
0	SYNC0	0	R/W	When synchronous operation is selected, the TCNT synchronous presetting of multiple channels, and synchronous clearing by counter clearing on another channel, are possible. To set synchronous operation, the SYNC bits for at least two channels must be set to 1. To set synchronous clearing, in addition to the SYNC bit, the TCNT clearing source must also be set by means of bits CCLR0 to CCLR2 in TCR. 0: TCNT_2 to TCNT_0 operates independently. TCNT presetting /clearing is unrelated to other channels. 1: TCNT_2 to TCNT_0 performs synchronous operation. TCNT synchronous presetting/synchronous clearing is possible.

8.3.10 Timer Output Master Enable Register (TOER)

TOER is an 8-bit readable/writable register that enables/disables output settings for output pins TIOC4D, TIOC4C, TIOC3D, TIOC4B, TIOC4A, and TIOC3B. These pins do not output correctly if the TOER bits have not been set. Set TOER of CH3 and CH4 prior to setting TIOR of CH3 and CH4.

Bit	Bit Name	Initial value	R/W	Description
7, 6	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
5	OE4D	0	R/W	Master Enable TIOC4D This bit enables/disables the TIOC4D pin MTU output. 0: MTU output is disabled 1: MTU output is enabled
4	OE4C	0	R/W	Master Enable TIOC4C This bit enables/disables the TIOC4C pin MTU output. 0: MTU output is disabled 1: MTU output is enabled
3	OE3D	0	R/W	Master Enable TIOC3D This bit enables/disables the TIOC3D pin MTU output. 0: MTU output is disabled 1: MTU output is enabled
2	OE4B	0	R/W	Master Enable TIOC4B This bit enables/disables the TIOC4B pin MTU output. 0: MTU output is disabled 1: MTU output is enabled
1	OE4A	0	R/W	Master Enable TIOC4A This bit enables/disables the TIOC4A pin MTU output. 0: MTU output is disabled 1: MTU output is enabled
0	OE3B	0	R/W	Master Enable TIOC3B This bit enables/disables the TIOC3B pin MTU output. 0: MTU output is disabled 1: MTU output is enabled

8.3.11 Timer Output Control Register (TOCR)

TOCR is an 8-bit readable/writable register that enables/disables PWM synchronized toggle output in complementary PWM mode/reset synchronized PWM mode, and controls output level inversion of PWM output.

Bit	Bit Name	Initial value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PSYE	0	R/W	PWM Synchronous Output Enable This bit selects the enable/disable of toggle output synchronized with the PWM period. 0: Toggle output is disabled 1: Toggle output is enabled
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	OLSN	0	R/W	Output Level Select N This bit selects the reverse phase output level in reset-synchronized PWM mode/complementary PWM mode. See table 8.26
0	OLSP	0	R/W	Output Level Select P This bit selects the positive phase output level in reset-synchronized PWM mode/complementary PWM mode. See table 8.27

Table 8.26 Output Level Select Function

Bit 1	Function			
			Compare Match Output	
OLSN	Initial Output	Active Level	Increment Count	Decrement Count
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

Note: The reverse phase waveform initial output value changes to active level after elapse of the dead time after count start.

Table 8.27 Output Level Select Function

Bit 1	Function			
			Compare Match Output	
OLSP	Initial Output	Active Level	Increment Count	Decrement Count
0	High level	Low level	Low level	High level
1	Low level	High level	High level	Low level

Figure 8.2 shows an example of complementary PWM mode output (1 phase) when OLSN = 1, OLSP = 1.

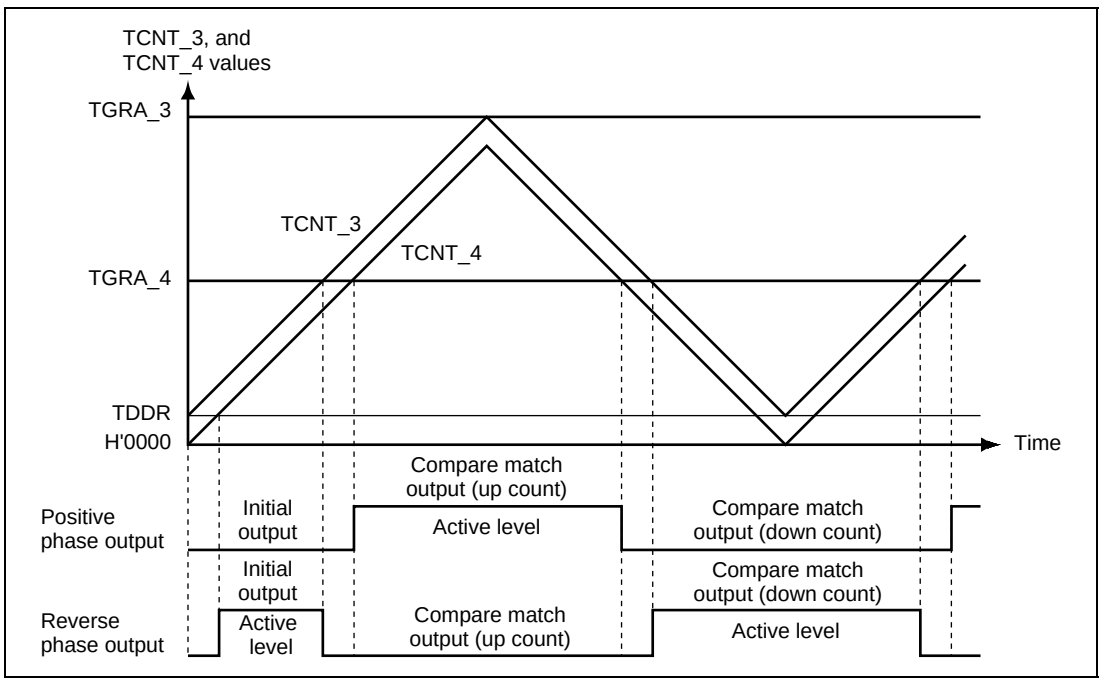


Figure 8.2 Complementary PWM Mode Output Level Example

8.3.12 Timer Gate Control Register (TGCR)

TGCR is an 8-bit readable/writable register that controls the waveform output necessary for brushless DC motor control in reset-synchronized PWM mode/complementary PWM mode. These register settings are ineffective for anything other than complementary PWM mode/reset-synchronized PWM mode.

Bit	Bit Name	Initial value	R/W	Description
7	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
6	BDC	0	R/W	Brushless DC Motor This bit selects whether to make the functions of this register (TGCR) effective or ineffective. 0: Ordinary output 1: Functions of this register are made effective
5	N	0	R/W	Reverse Phase Output (N) Control This bit selects whether the level output or the reset-synchronized PWM/complementary PWM output while the reverse pins (TIOC3D, TIOC4C, and TIOC4D) are on-output. 0: Level output 1: Reset synchronized PWM/complementary PWM output
4	P	0	R/W	Positive Phase Output (P) Control This bit selects whether the level output or the reset-synchronized PWM/complementary PWM output while the positive pin (TIOC3B, TIOC4A, and TIOC4B) are on-output. 0: Level output 1: Reset synchronized PWM/complementary PWM output
3	FB	0	R/W	External Feedback Signal Enable This bit selects whether the switching of the output of the positive/reverse phase is carried out automatically with the MTU/channel 0 TGRA, TGRB, TGRC input capture signals or by writing 0 or 1 to bits 2 to 0 in TGCR. 0: Output switching is carried out by external input (Input sources are channel 0 TGRA, TGRB, TGRC input capture signal) 1: Output switching is carried out by software (TGCR's UF, VF, WF settings).
2	WF	0	R/W	Output Phase Switch 2 to 0 These bits set the positive phase/negative phase output phase on or off state. The setting of these bits is valid only when the FB bit in this register is set to 1. In this case, the setting of bits 2 to 0 is a substitute for external input. See table 8.28.
1	VF	0	R/W	
0	UF	0	R/W	

Table 8.28 Output Level Select Function

			Function					
Bit 2	Bit 1	Bit 0	TIOC3B	TIOC4A	TIOC4B	TIOC3D	TIOC4C	TIOC4D
WF	VF	UF	U Phase	V Phase	W Phase	U Phase	V Phase	W Phase
0	0	0	OFF	OFF	OFF	OFF	OFF	OFF
		1	ON	OFF	OFF	OFF	OFF	ON
	1	0	OFF	ON	OFF	ON	OFF	OFF
		1	OFF	ON	OFF	OFF	OFF	ON
1	0	0	OFF	OFF	ON	OFF	ON	OFF
		1	ON	OFF	OFF	OFF	ON	OFF
	1	0	OFF	OFF	ON	ON	OFF	OFF
		1	OFF	OFF	OFF	OFF	OFF	OFF

8.3.13 Timer Subcounter (TCNTS)

TCNTS is a 16-bit read-only counter that is used only in complementary PWM mode. The initial value is H'0000.

Note: Accessing the TCNTS in 8-bit units is prohibited. Always access in 16-bit units.

8.3.14 Timer Dead Time Data Register (TDDR)

TDDR is a 16-bit register, used only in complementary PWM mode, that specifies the TCNT_3 and TCNT_4 counter offset values. In complementary PWM mode, when the TCNT_3 and TCNT_4 counters are cleared and then restarted, the TDDR register value is loaded into the TCNT_3 counter and the count operation starts. The initial value is H'FFFF.

Note: Accessing the TDDR in 8-bit units is prohibited. Always access in 16-bit units.

8.3.15 Timer Period Data Register (TCDR)

TCDR is a 16-bit register used only in complementary PWM mode. Set half the PWM carrier sync value as the TCDR register value. This register is constantly compared with the TCNTS counter in complementary PWM mode, and when a match occurs, the TCNTS counter switches direction (decrement to increment). The initial value is H'FFFF.

Note: Accessing the TCDR in 8-bit units is prohibited. Always access in 16-bit units.

8.3.16 Timer Period Buffer Register (TCBR)

The timer period buffer register (TCBR) is a 16-bit register used only in complementary PWM mode. It functions as a buffer register for the TCDR register. The TCBR register values are transferred to the TCDR register with the transfer timing set in the TMDR register. The initial value is H'FFFF.

Note: Accessing the TCBR in 8-bit units is prohibited. Always access in 16-bit units.

8.3.17 Bus Master Interface

The timer counters (TCNT), general registers (TGR), timer subcounter (TCNTS), timer period buffer register (TCBR), and timer dead time data register (TDDR), and timer period data register (TCDR) are 16-bit registers. A 16-bit data bus to the bus master enables 16-bit read/writes. 8-bit read/write is not possible. Always access in 16-bit units.

All registers other than the above registers are 8-bit registers. These are connected to the CPU by a 16-bit data bus, so 16-bit read/writes and 8-bit read/writes are both possible.

8.4 Operation

8.4.1 Basic Functions

Each channel has a TCNT and TGR register. TCNT performs up-counting, and is also capable of free-running operation, synchronous counting, and external event counting.

Each TGR can be used as an input capture register or output compare register.

Always set the MTU external pins function using the pin function controller (PFC).

Counter Operation

When one of bits CST0 to CST4 is set to 1 in TSTR, the TCNT counter for the corresponding channel begins counting. TCNT can operate as a free-running counter, periodic counter, for example.

Example of Count Operation Setting Procedure: Figure 8.3 shows an example of the count operation setting procedure.

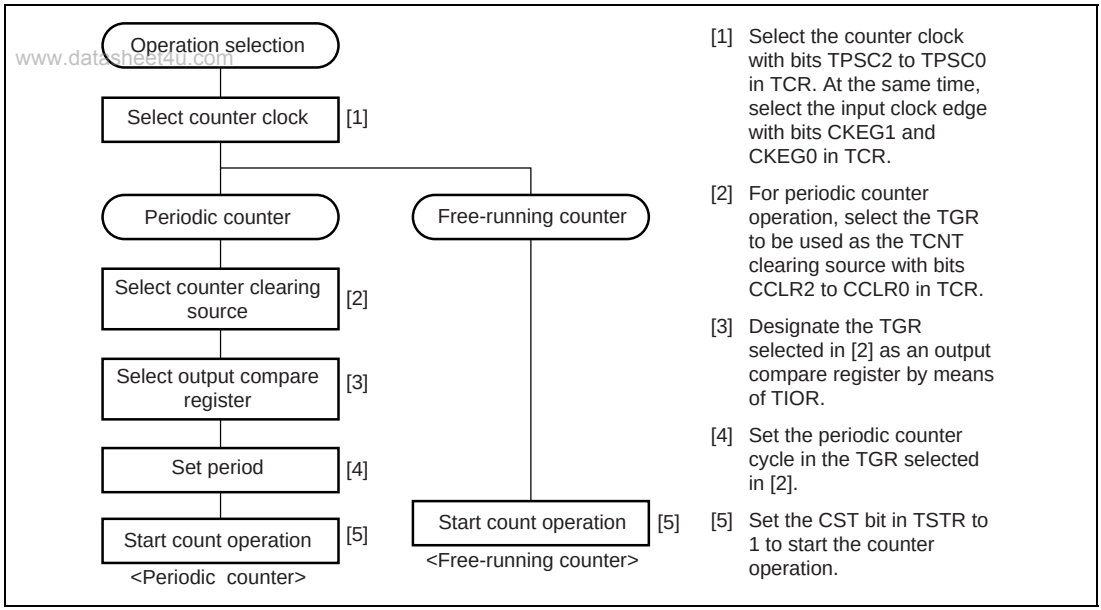


Figure 8.3 Example of Counter Operation Setting Procedure

Free-Running Count Operation and Periodic Count Operation: Immediately after a reset, the MTU's TCNT counters are all designated as free-running counters. When the relevant bit in TSTR is set to 1 the corresponding TCNT counter starts up-count operation as a free-running counter. When TCNT overflows (from H'FFFF to H'0000), the TCFV bit in TSR is set to 1. If the value of the corresponding TCIEV bit in TIER is 1 at this point, the MTU requests an interrupt. After overflow, TCNT starts counting up again from H'0000.

Figure 8.4 illustrates free-running counter operation.

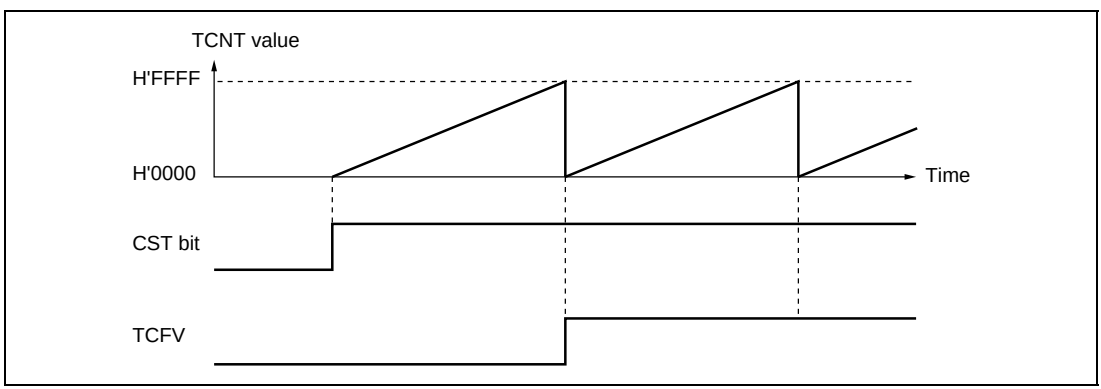


Figure 8.4 Free-Running Counter Operation

When compare match is selected as the TCNT clearing source, the TCNT counter for the relevant channel performs periodic count operation. The TGR register for setting the period is designated as an output compare register, and counter clearing by compare match is selected by means of bits CCLR0 to CCLR2 in TCR. After the settings have been made, TCNT starts up-count operation as a periodic counter when the corresponding bit in TSTR is set to 1. When the count value matches the value in TGR, the TGF bit in TSR is set to 1 and TCNT is cleared to H'0000.

If the value of the corresponding TGIE bit in TIER is 1 at this point, the TPU requests an interrupt. After a compare match, TCNT starts counting up again from H'0000.

Figure 8.5 illustrates periodic counter operation.

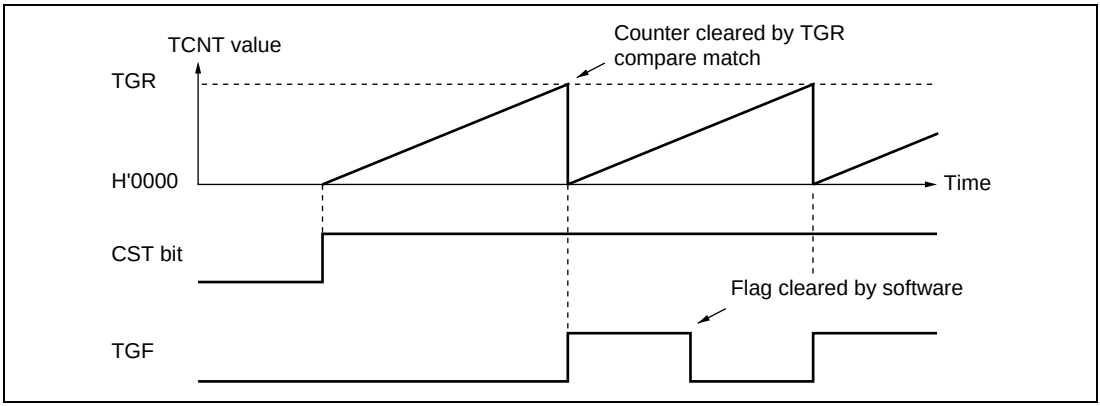


Figure 8.5 Periodic Counter Operation

Waveform Output by Compare Match

The MTU can perform 0, 1, or toggle output from the corresponding output pin using compare match.

Example of Setting Procedure for Waveform Output by Compare Match: Figure 8.6 shows an example of the setting procedure for waveform output by compare match

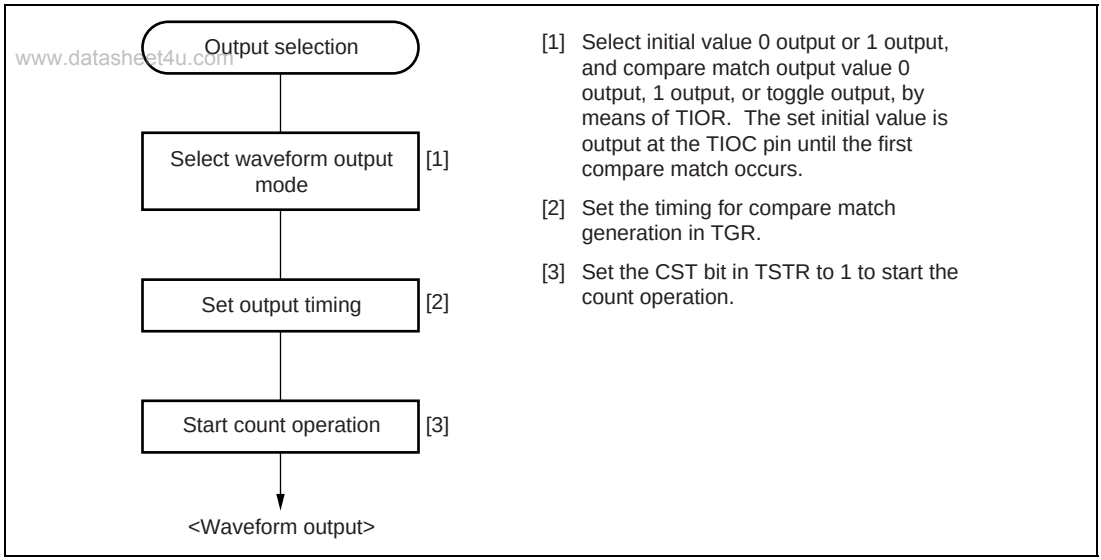


Figure 8.6 Example of Setting Procedure for Waveform Output by Compare Match

Examples of Waveform Output Operation: Figure 8.7 shows an example of 0 output/1 output.

In this example TCNT has been designated as a free-running counter, and settings have been made such that 1 is output by compare match A, and 0 is output by compare match B. When the set level and the pin level coincide, the pin level does not change.

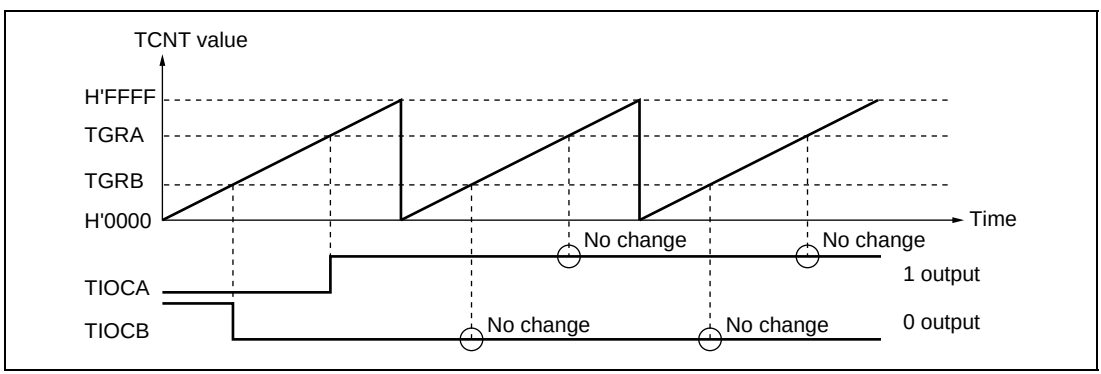


Figure 8.7 Example of 0 Output/1 Output Operation

Figure 8.8 shows an example of toggle output.

In this example, TCNT has been designated as a periodic counter (with counter clearing on compare match B), and settings have been made such that the output is toggled by both compare match A and compare match B.

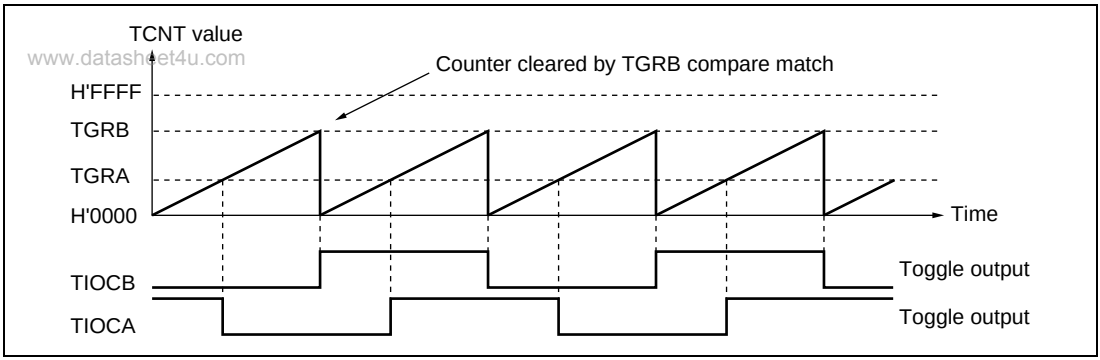


Figure 8.8 Example of Toggle Output Operation

Input Capture Function

The TCNT value can be transferred to TGR on detection of the TIOC pin input edge.

Rising edge, falling edge, or both edges can be selected as the detected edge. For channels 0 and 1, it is also possible to specify another channel's counter input clock or compare match signal as the input capture source.

Note: When another channel's counter input clock is used as the input capture input for channels 0 and 1, ϕ/1 should not be selected as the counter input clock used for input capture input. Input capture will not be generated if ϕ/1 is selected.

Example of Input Capture Operation Setting Procedure: Figure 8.9 shows an example of the input capture operation setting procedure.

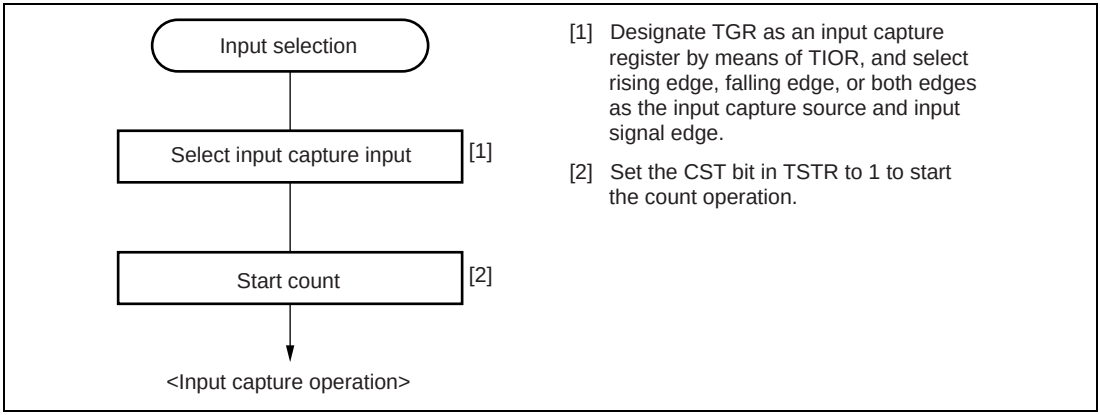


Figure 8.9 Example of Input Capture Operation Setting Procedure

Example of Input Capture Operation: Figure 8.10 shows an example of input capture operation.

In this example both rising and falling edges have been selected as the TIOCA pin input capture input edge, the falling edge has been selected as the TIOCB pin input capture input edge, and counter clearing by TGRB input capture has been designated for TCNT.

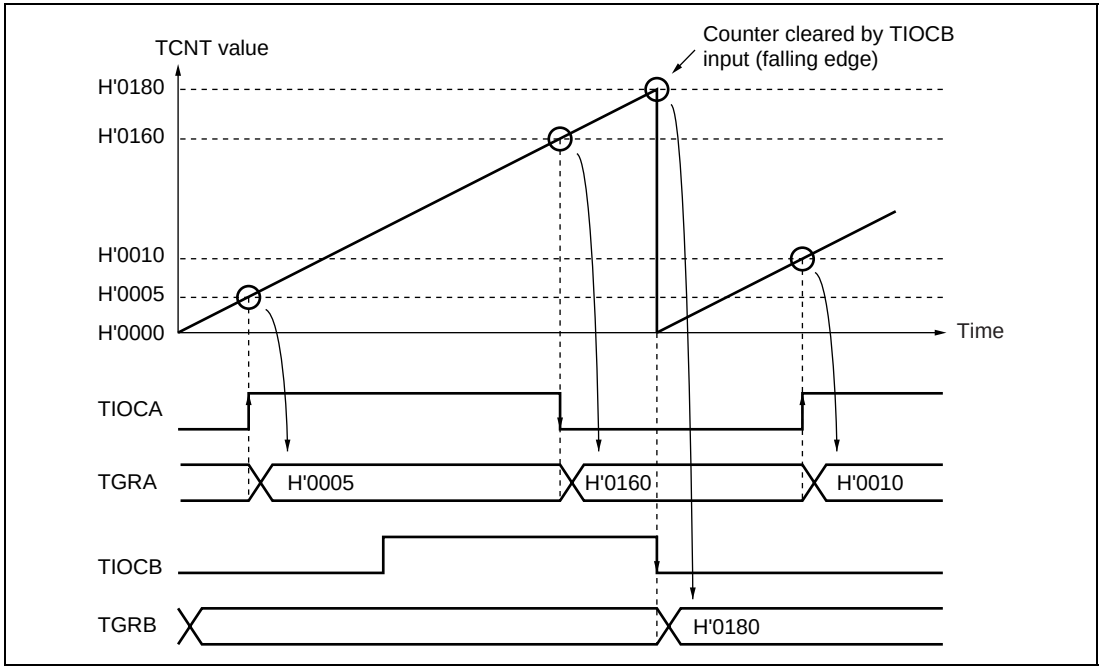


Figure 8.10 Example of Input Capture Operation

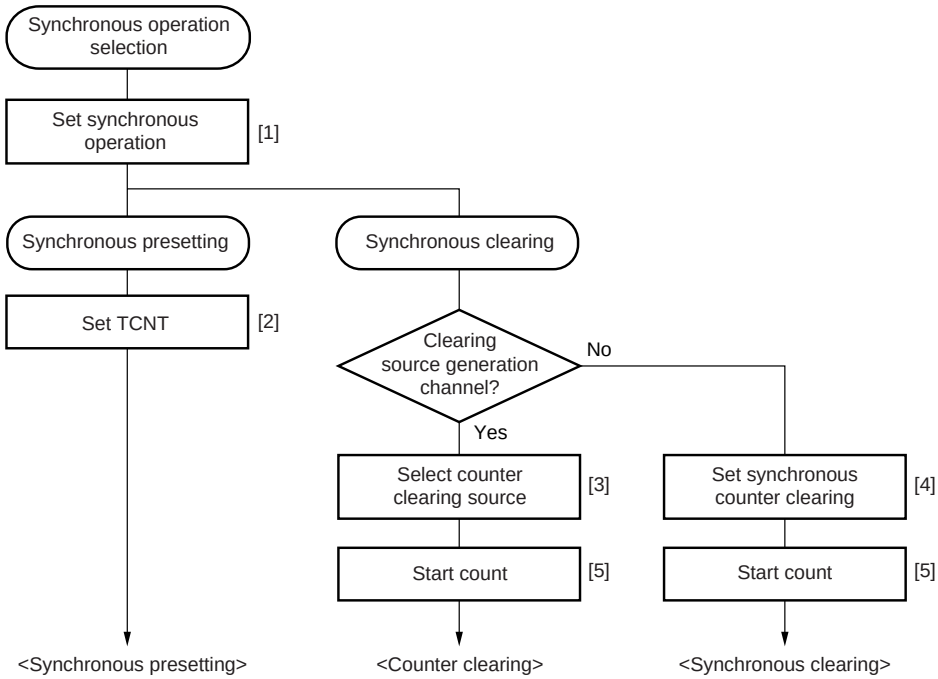
8.4.2 Synchronous Operation

In synchronous operation, the values in a number of TCNT counters can be rewritten simultaneously (synchronous presetting). Also, a number of TCNT counters can be cleared simultaneously by making the appropriate setting in TCR (synchronous clearing).

Synchronous operation enables TGR to be incremented with respect to a single time base.

Channels 0 to 4 can all be designated for synchronous operation.

Example of Synchronous Operation Setting Procedure: Figure 8.11 shows an example of the synchronous operation setting procedure.



[1] Set to 1 the SYNC bits in TSYR corresponding to the channels to be designated for synchronous operation.
[2] When the TCNT counter of any of the channels designated for synchronous operation is written to, the same value is simultaneously written to the other TCNT counters.
[3] Use bits CCLR2 to CCLR0 in TCR to specify TCNT clearing by input capture/output compare, etc.
[4] Use bits CCLR2 to CCLR0 in TCR to designate synchronous clearing for the counter clearing source.
[5] Set to 1 the CST bits in TSTR for the relevant channels, to start the count operation.

Figure 8.11 Example of Synchronous Operation Setting Procedure

Example of Synchronous Operation: Figure 8.12 shows an example of synchronous operation.

In this example, synchronous operation and PWM mode 1 have been designated for channels 0 to 2, TGRB_0 compare match has been set as the channel 0 counter clearing source, and synchronous clearing has been set for the channel 1 and 2 counter clearing source.

Three-phase PWM waveforms are output from pins TIOC0A, TIOC1A, and TIOC2A. At this time, synchronous presetting, and synchronous clearing by TGRB_0 compare match, are performed for channel 0 to 2 TCNT counters, and the data set in TGRB_0 is used as the PWM cycle.

For details of PWM modes, see section 8.4.5, PWM Modes.

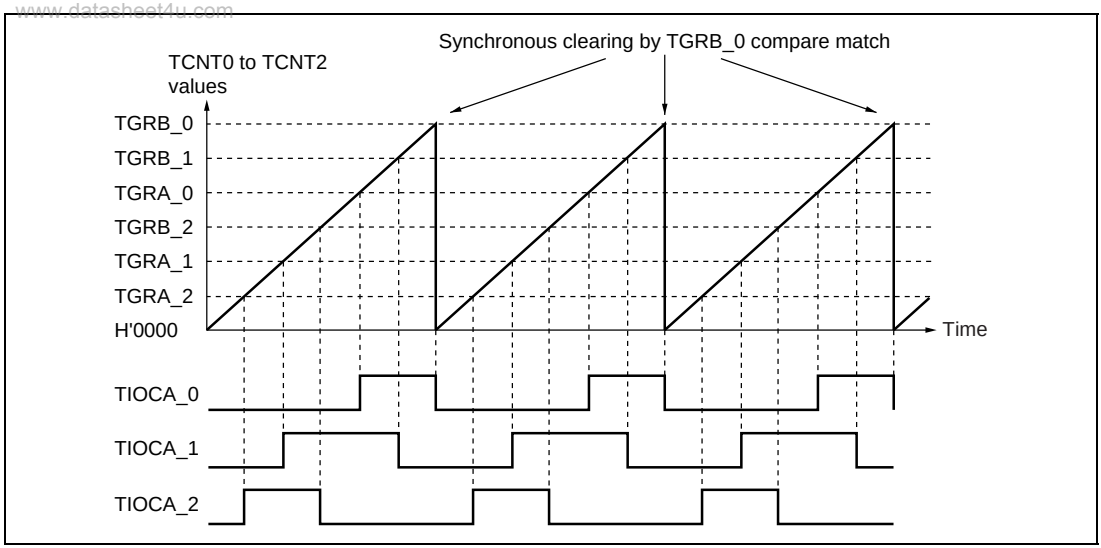


Figure 8.12 Example of Synchronous Operation

8.4.3 Buffer Operation

Buffer operation, provided for channels 0, 3, and 4, enables TGRC and TGRD to be used as buffer registers.

Buffer operation differs depending on whether TGR has been designated as an input capture register or as a compare match register.

Table 8.29 shows the register combinations used in buffer operation.

Table 8.29 Register Combinations in Buffer Operation

Channel	Timer General Register	Buffer Register
0	TGRA_0	TGRC_0
	TGRB_0	TGRD_0
3	TGRA_3	TGRC_3
	TGRB_3	TGRD_3
4	TGRA_4	TGRC_4
	TGRB_4	TGRD_4

- When TGR is an output compare register

  When a compare match occurs, the value in the buffer register for the corresponding channel is transferred to the timer general register.

  This operation is illustrated in figure 8.13.

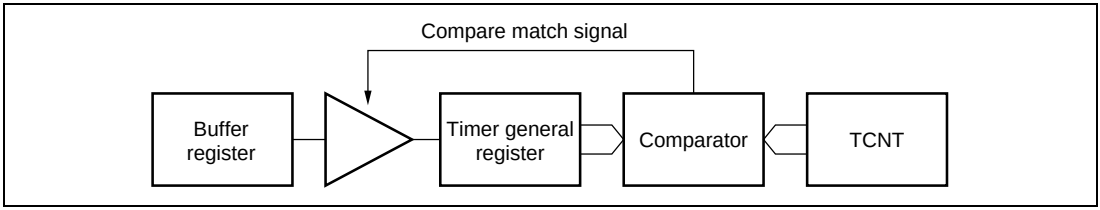


Figure 8.13 Compare Match Buffer Operation

- When TGR is an input capture register

  When input capture occurs, the value in TCNT is transferred to TGR and the value previously held in the timer general register is transferred to the buffer register.

  This operation is illustrated in figure 8.14.

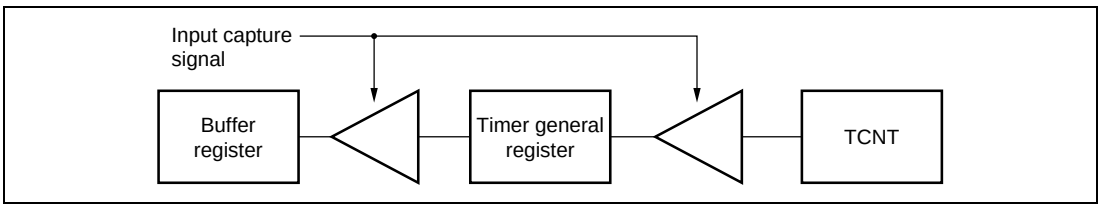


Figure 8.14 Input Capture Buffer Operation

Example of Buffer Operation Setting Procedure: Figure 8.15 shows an example of the buffer operation setting procedure.

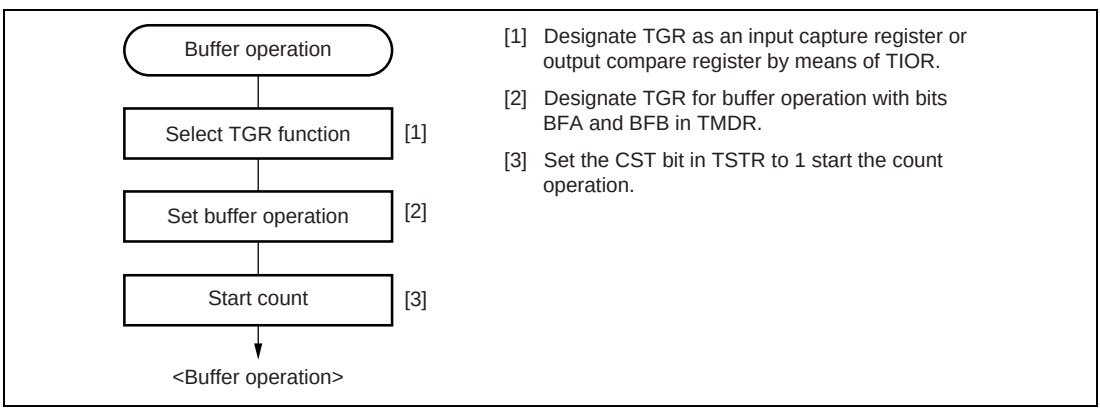


Figure 8.15 Example of Buffer Operation Setting Procedure

Examples of Buffer Operation:

- When TGR is an output compare register

  Figure 8.16 shows an operation example in which PWM mode 1 has been designated for channel 0, and buffer operation has been designated for TGRA and TGRC. The settings used in this example are TCNT clearing by compare match B, 1 output at compare match A, and 0 output at compare match B.

  As buffer operation has been set, when compare match A occurs the output changes and the value in buffer register TGRC is simultaneously transferred to timer general register TGRA. This operation is repeated each time that compare match A occurs.

  For details of PWM modes, see section 8.4.5, PWM Modes.

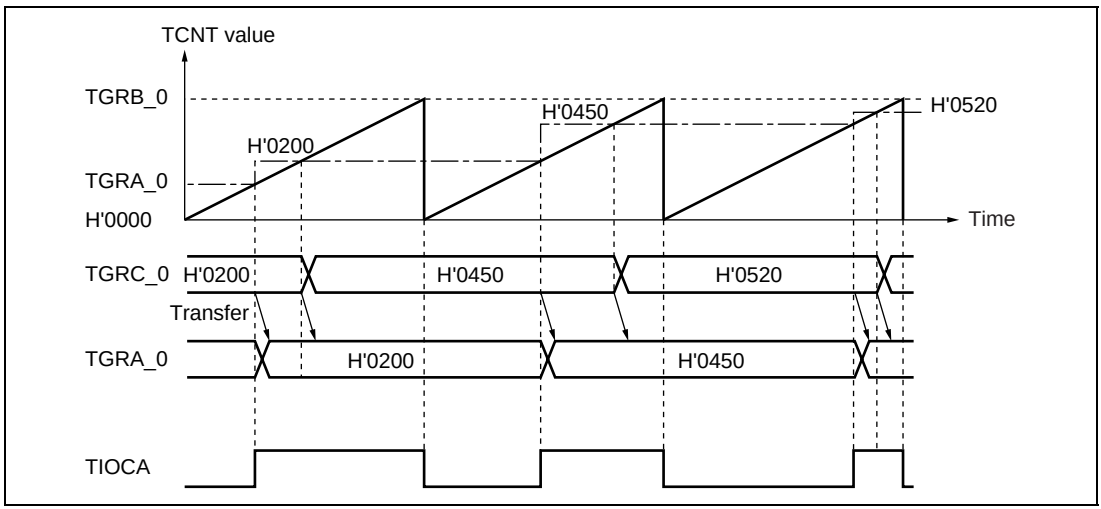


Figure 8.16 Example of Buffer Operation (1)

- When TGR is an input capture register

  Figure 8.17 shows an operation example in which TGRA has been designated as an input capture register, and buffer operation has been designated for TGRA and TGRC.

  Counter clearing by TGRA input capture has been set for TCNT, and both rising and falling edges have been selected as the TIOCA pin input capture input edge.

  As buffer operation has been set, when the TCNT value is stored in TGRA upon the occurrence of input capture A, the value previously stored in TGRA is simultaneously transferred to TGRC.

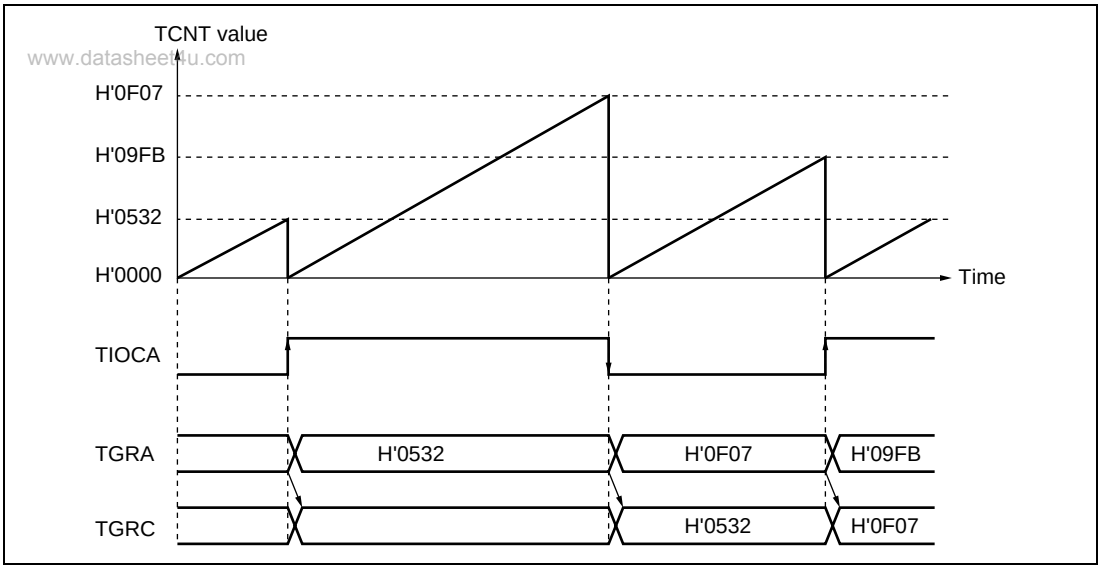


Figure 8.17 Example of Buffer Operation (2)

8.4.4 Cascaded Operation

In cascaded operation, two 16-bit counters for different channels are used together as a 32-bit counter.

This function works by counting the channel 1 counter clock upon overflow/underflow of TCNT_2 as set in bits TPSC0 to TPSC2 in TCR.

Underflow occurs only when the lower 16-bit TCNT is in phase-counting mode.

Table 8.30 shows the register combinations used in cascaded operation.

Note: When phase counting mode is set for channel 1, the counter clock setting is invalid and the counter operates independently in phase counting mode.

Table 8.30 Cascaded Combinations

Combination	Upper 16 Bits	Lower 16 Bits
Channels 1 and 2	TCNT_1	TCNT_2

Example of Cascaded Operation Setting Procedure: Figure 8.18 shows an example of the setting procedure for cascaded operation.

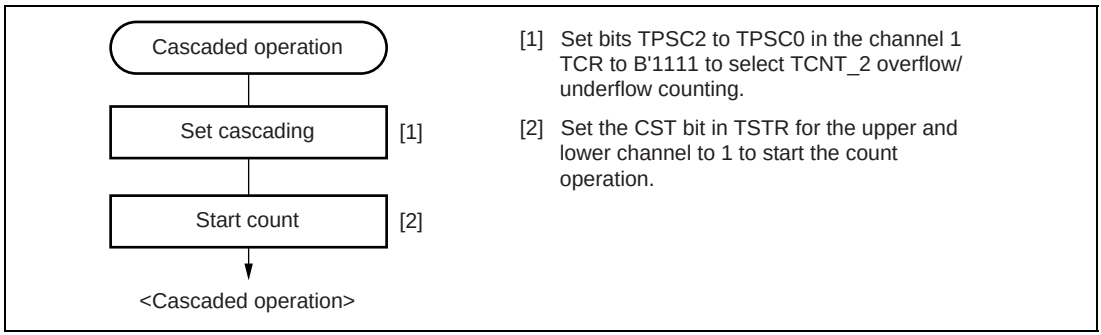


Figure 8.18 Cascaded Operation Setting Procedure

Examples of Cascaded Operation: Figure 8.19 illustrates the operation when TCNT_2 overflow/underflow counting has been set for TCNT_1 and phase counting mode has been designated for channel 2.

TCNT_1 is incremented by TCNT_2 overflow and decremented by TCNT_2 underflow.

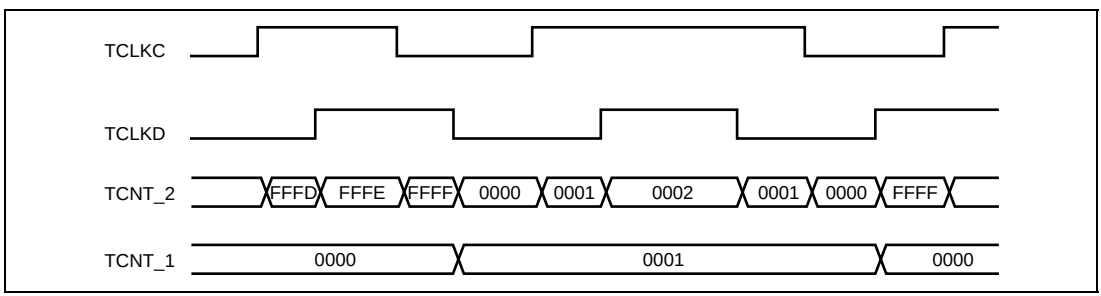


Figure 8.19 Example of Cascaded Operation (2)

8.4.5 PWM Modes

In PWM mode, PWM waveforms are output from the output pins. The output level can be selected as 0, 1, or toggle output in response to a compare match of each TGR.

TGR registers settings can be used to output a PWM waveform in the range of 0% to 100% duty cycle.

Designating TGR compare match as the counter clearing source enables the period to be set in that register. All channels can be designated for PWM mode independently. Synchronous operation is also possible.

There are two PWM modes, as described below.

- PWM mode 1

  PWM output is generated from the TIOCA and TIOCC pins by pairing TGRA with TGRB and TGRC with TGRD. The output specified by bits IOA0 to IOA3 and IOC0 to IOC3 in TIOR is output from the TIOCA and TIOCC pins at compare matches A and C, and the output specified by bits IOB0 to IOB3 and IOD0 to IOD3 in TIOR is output at compare matches B and D. The initial output value is the value set in TGRA or TGRC. If the set values of paired TGRs are identical, the output value does not change when a compare match occurs.

  In PWM mode 1, a maximum 8-phase PWM output is possible.

- PWM mode 2

  PWM output is generated using one TGR as the cycle register and the others as duty cycle registers. The output specified in TIOR is performed by means of compare matches. Upon counter clearing by a synchronization register compare match, the output value of each pin is the initial value set in TIOR. If the set values of the cycle and duty cycle registers are identical, the output value does not change when a compare match occurs.

  In PWM mode 2, a maximum 8-phase PWM output is possible in combination use with synchronous operation.

The correspondence between PWM output pins and registers is shown in table 8.31.

Table 8.31 PWM Output Registers and Output Pins

Channel	Registers	Output Pins	
		PWM Mode 1	PWM Mode 2
0	TGRA_0	TIOC0A	TIOC0A
	TGRB_0		TIOC0B
	TGRC_0	TIOC0C	TIOC0C
	TGRD_0		TIOC0D
1	TGRA_1	TIOC1A	TIOC1A
	TGRB_1		TIOC1B
2	TGRA_2	TIOC2A	TIOC2A
	TGRB_2		TIOC2B
3	TGRA_3	TIOC3A	Cannot be set
	TGRB_3		Cannot be set
	TGRC_3	TIOC3C	Cannot be set
	TGRD_3		Cannot be set
4	TGRA_4	TIOC4A	Cannot be set
	TGRB_4		Cannot be set
	TGRC_4	TIOC4C	Cannot be set
	TGRD_4		Cannot be set

Note: In PWM mode 2, PWM output is not possible for the TGR register in which the period is set.

Example of PWM Mode Setting Procedure: Figure 8.20 shows an example of the PWM mode setting procedure.

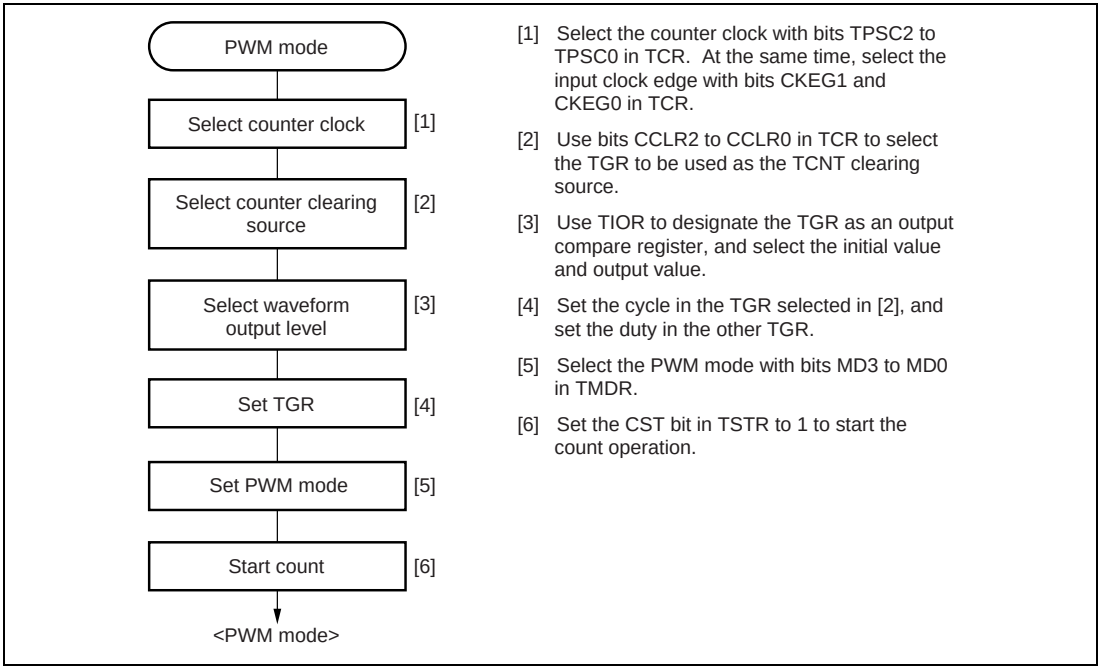


Figure 8.20 Example of PWM Mode Setting Procedure

Examples of PWM Mode Operation: Figure 8.21 shows an example of PWM mode 1 operation.

In this example, TGRA compare match is set as the TCNT clearing source, 0 is set for the TGRA initial output value and output value, and 1 is set as the TGRB output value.

In this case, the value set in TGRA is used as the period, and the values set in the TGRB registers are used as the duty cycle.

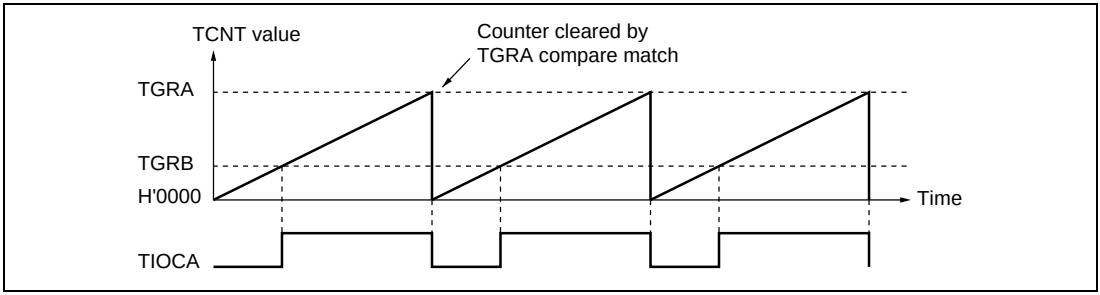


Figure 8.21 Example of PWM Mode Operation (1)

Figure 8.22 shows an example of PWM mode 2 operation.

In this example, synchronous operation is designated for channels 0 and 1, TGRB_1 compare match is set as the TCNT clearing source, and 0 is set for the initial output value and 1 for the output value of the other TGR registers (TGRA_0 to TGRD_0, TGRA_1), outputting a 5-phase PWM waveform.

In this case, the value set in TGRB_1 is used as the cycle, and the values set in the other TGRs are used as the duty cycle levels.

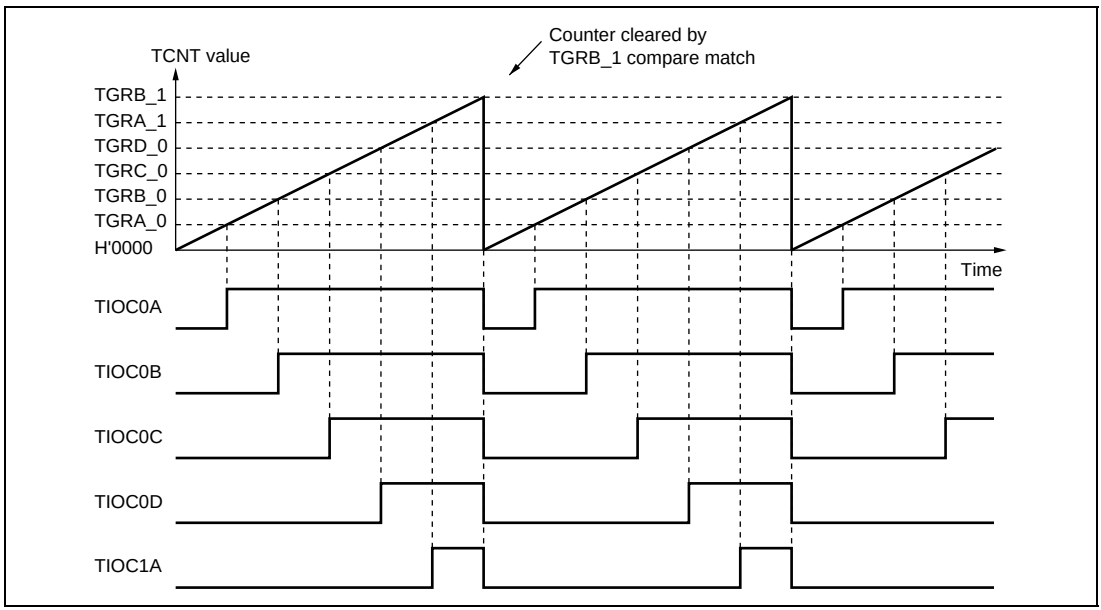


Figure 8.22 Example of PWM Mode Operation (2)

Figure 8.23 shows examples of PWM waveform output with 0% duty cycle and 100% duty cycle in PWM mode.

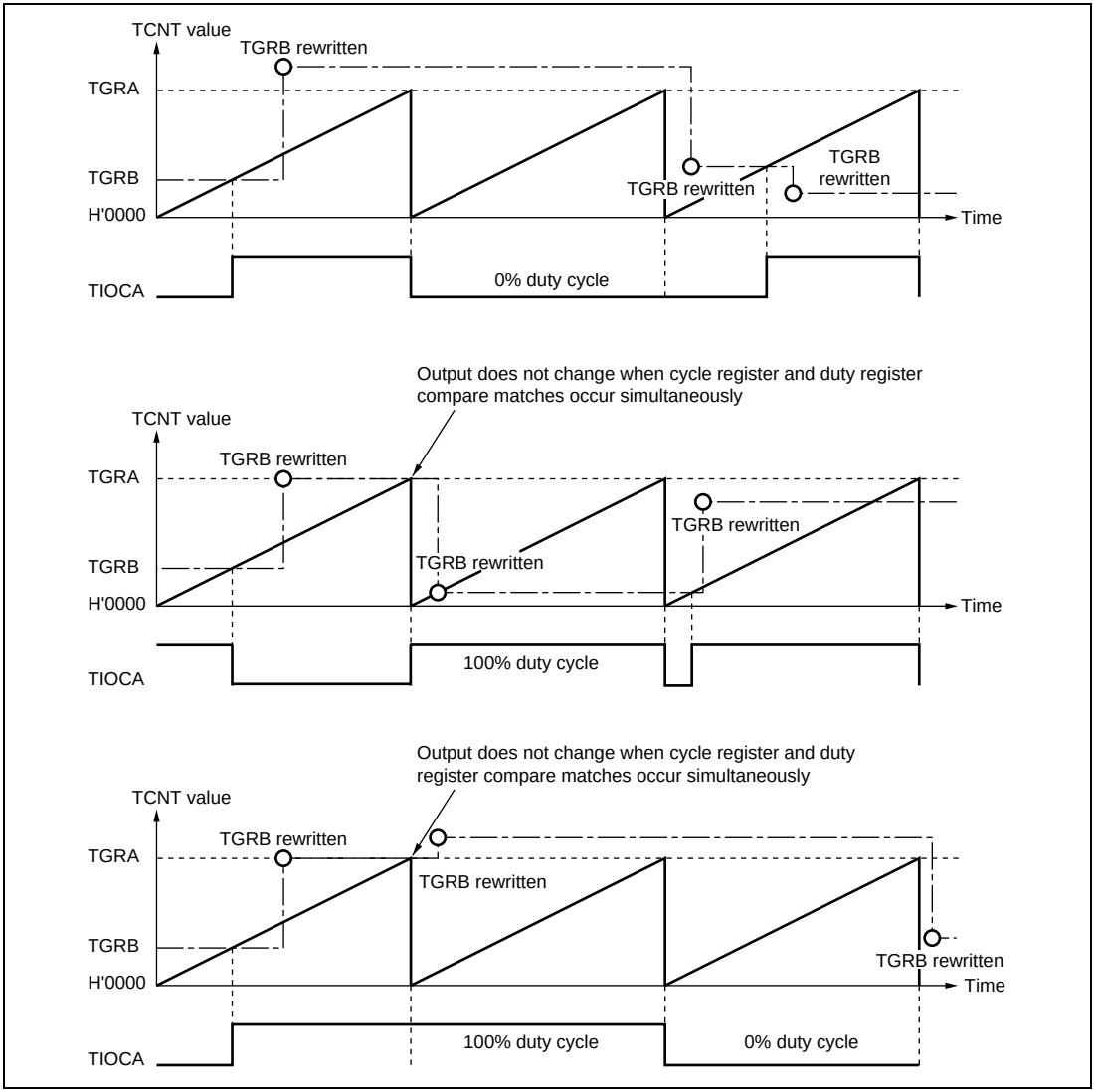


Figure 8.23 Example of PWM Mode Operation (3)

8.4.6 Phase Counting Mode

In phase counting mode, the phase difference between two external clock inputs is detected and TCNT counts up or down accordingly. This mode can be set for channels 1 and 2.

When phase counting mode is set, an external clock is selected as the counter input clock and TCNT operates as an up/down-counter regardless of the setting of bits TPSC0 to TPSC2 and bits CKEG0 and CKEG1 in TCR. However, the functions of bits CCLR0 and CCLR1 in TCR, and of TIOR, TIER, and TGR, are valid, and input capture/compare match and interrupt functions can be used.

This can be used for two-phase encoder pulse input.

If overflow occurs when TCNT is counting up, the TCFV flag in TSR is set; if underflow occurs when TCNT is counting down, the TCFU flag is set.

The TCFD bit in TSR is the count direction flag. Reading the TCFD flag reveals whether TCNT is counting up or down.

Table 8.32 shows the correspondence between external clock pins and channels.

Table 8.32 Phase Counting Mode Clock Input Pins

	External Clock Pins	
Channels	**A-Phase**	**B-Phase**
When channel 1 is set to phase counting mode	TCLKA	TCLKB
When channel 2 is set to phase counting mode	TCLKC	TCLKD

Example of Phase Counting Mode Setting Procedure: Figure 8.24 shows an example of the phase counting mode setting procedure.

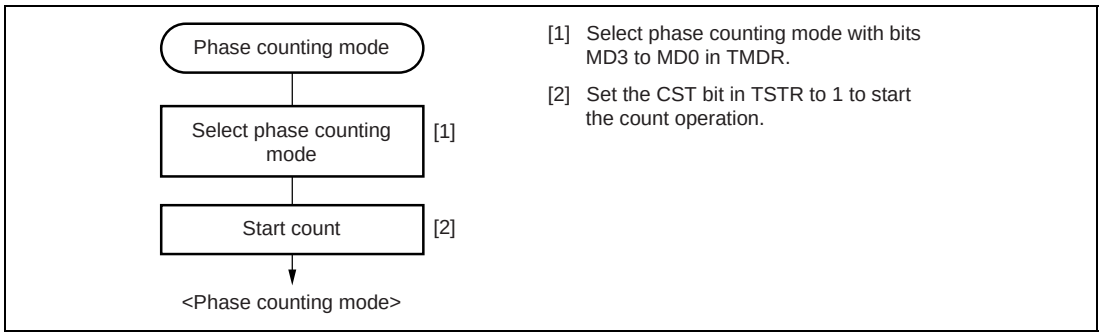


Figure 8.24 Example of Phase Counting Mode Setting Procedure

Examples of Phase Counting Mode Operation: In phase counting mode, TCNT counts up or down according to the phase difference between two external clocks. There are four modes, according to the count conditions.

- Phase counting mode 1

  Figure 8.25 shows an example of phase counting mode 1 operation, and table 8.33 summarizes the TCNT up/down-count conditions.

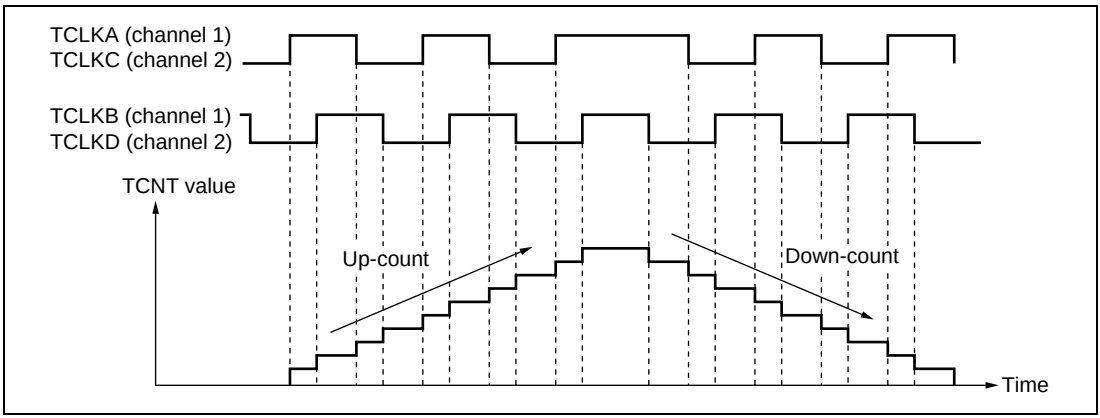


Figure 8.25 Example of Phase Counting Mode 1 Operation

Table 8.33 Up/Down-Count Conditions in Phase Counting Mode 1

TCLKA (Channel 1) TCLKC (Channel 2)	TCLKB (Channel 1) TCLKD (Channel 2)	Operation
High level	↑	Up-count
Low level	↓	
↑	Low level	
↓	High level	
High level	↓	Down-count
Low level	↑	
↑	High level	
↓	Low level	

Legend:

↑ : Rising edge

↓ : Falling edge

- Phase counting mode 2

Figure 8.26 shows an example of phase counting mode 2 operation, and table 8.34 summarizes the TCNT up/down-count conditions.

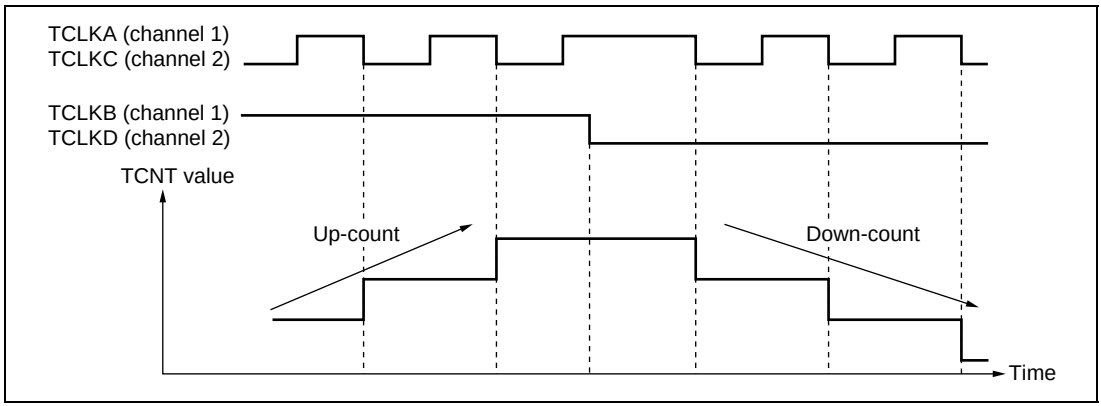


Figure 8.26 Example of Phase Counting Mode 2 Operation

Table 8.34 Up/Down-Count Conditions in Phase Counting Mode 2

TCLKA (Channel 1) TCLKC (Channel 2)	TCLKB (Channel 1) TCLKD (Channel 2)	Operation
High level	↑	Don't care
Low level	↓	Don't care
↑	Low level	Don't care
↓	High level	Up-count
High level	↓	Don't care
Low level	↑	Don't care
↑	High level	Don't care
↓	Low level	Down-count

Legend:
↑ : Rising edge
↓ : Falling edge

- Phase counting mode 3

Figure 8.27 shows an example of phase counting mode 3 operation, and table 8.35 summarizes the TCNT up/down-count conditions.

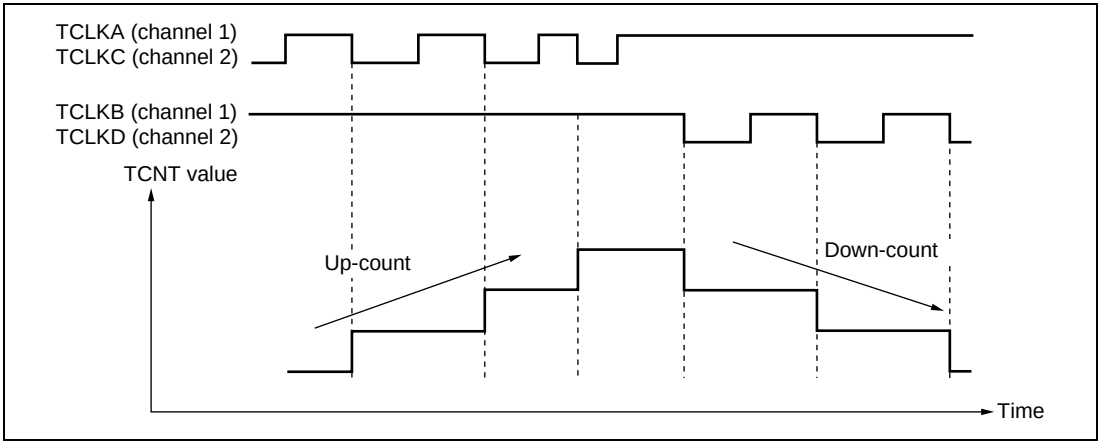


Figure 8.27 Example of Phase Counting Mode 3 Operation

Table 8.35 Up/Down-Count Conditions in Phase Counting Mode 3

TCLKA (Channel 1) TCLKC (Channel 2)	TCLKB (Channel 1) TCLKD (Channel 2)	Operation
High level	↑	Don't care
Low level	↓	Don't care
↑	Low level	Don't care
↓	High level	Up-count
High level	↓	Down-count
Low level	↑	Don't care
↑	High level	Don't care
↓	Low level	Don't care

Legend:

↑ : Rising edge

↓ : Falling edge

- Phase counting mode 4

Figure 8.28 shows an example of phase counting mode 4 operation, and table 8.36 summarizes the TCNT up/down-count conditions.

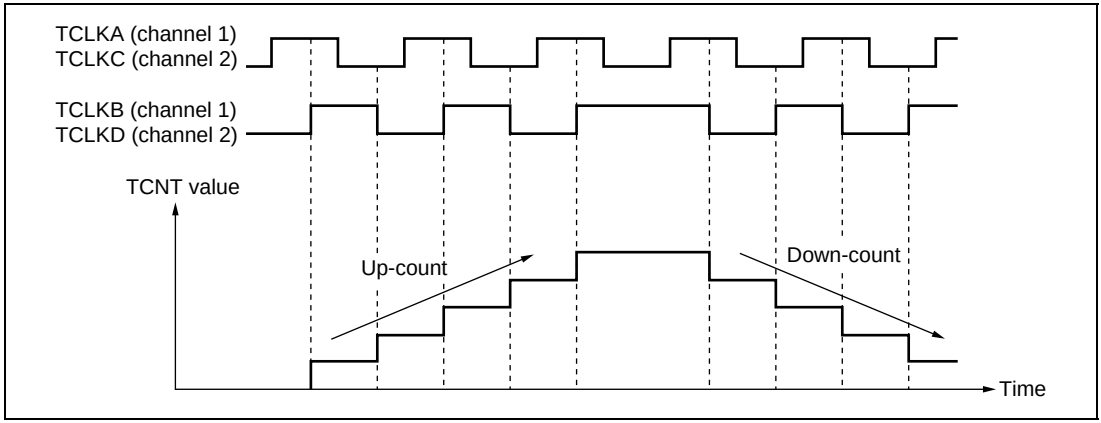


Figure 8.28 Example of Phase Counting Mode 4 Operation

Table 8.36 Up/Down-Count Conditions in Phase Counting Mode 4

TCLKA (Channel 1) TCLKC (Channel 2)	TCLKB (Channel 1) TCLKD (Channel 2)	Operation
High level	↑	Up-count
Low level	↓	
↑	Low level	Don't care
↓	High level	
High level	↓	Down-count
Low level	↑	
↑	High level	Don't care
↓	Low level	

Legend:
↑ : Rising edge
↓ : Falling edge

Phase Counting Mode Application Example: Figure 8.29 shows an example in which channel 1 is in phase counting mode, and channel 1 is coupled with channel 0 to input servo motor 2-phase encoder pulses in order to detect position or speed.

Channel 1 is set to phase counting mode 1, and the encoder pulse A-phase and B-phase are input to TCLKA and TCLKB.

Channel 0 operates with TCNT counter clearing by TGRC_0 compare match; TGRA_0 and TGRC_0 are used for the compare match function and are set with the speed control period and position control period. TGRB_0 is used for input capture, with TGRB_0 and TGRD_0 operating in buffer mode. The channel 1 counter input clock is designated as the TGRB_0 input capture source, and the pulse widths of 2-phase encoder 4-multiplication pulses are detected.

TGRA_1 and TGRB_1 for channel 1 are designated for input capture, and channel 0 TGRA_0 and TGRC_0 compare matches are selected as the input capture source and store the up/down-counter values for the control periods.

This procedure enables the accurate detection of position and speed.

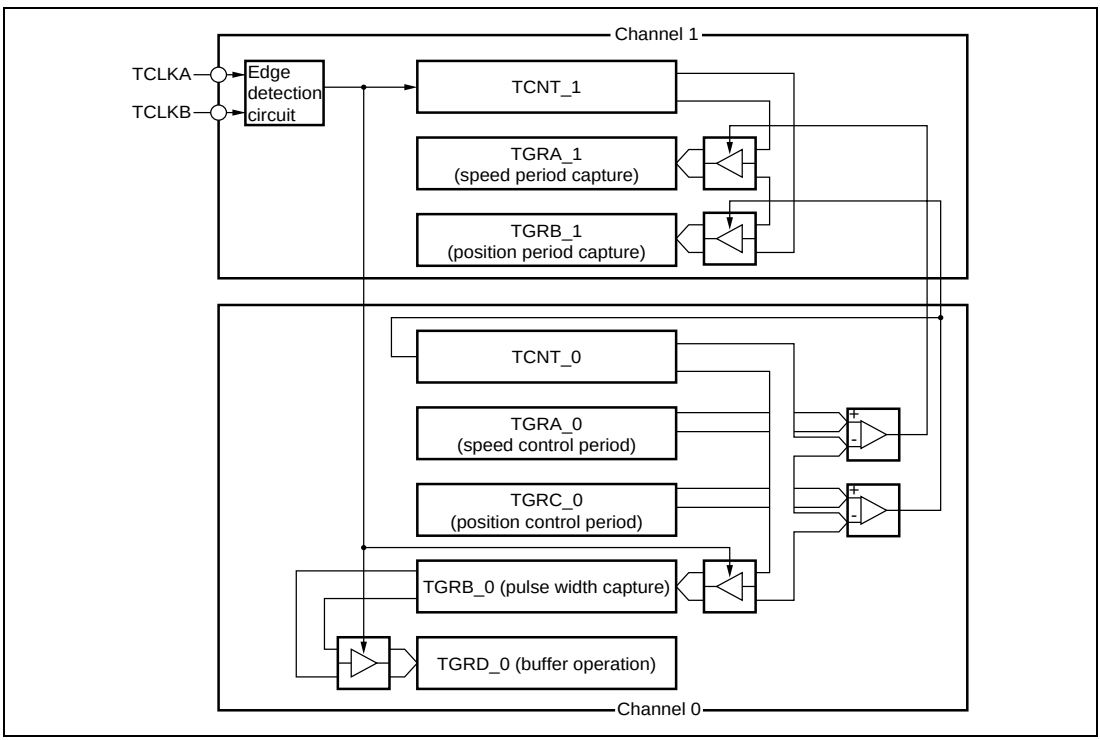


Figure 8.29 Phase Counting Mode Application Example

8.4.7 Reset-Synchronized PWM Mode

In the reset-synchronized PWM mode, three-phase output of positive and negative PWM waveforms that share a common wave transition point can be obtained by combining channels 3 and 4.

When set for reset-synchronized PWM mode, the TIOC3B, TIOC3D, TIOC4A, TIOC4C, TIOC4B, and TIOC4D pins function as PWM output pins and TCNT3 functions as an upcounter.

Table 8.37 shows the PWM output pins used. Table 8.38 shows the settings of the registers.

Table 8.37 Output Pins for Reset-Synchronized PWM Mode

Channel	Output Pin	Description
3	TIOC3B	PWM output pin 1
	TIOC3D	PWM output pin 1' (negative-phase waveform of PWM output 1)
4	TIOC4A	PWM output pin 2
	TIOC4C	PWM output pin 2' (negative-phase waveform of PWM output 2)
	TIOC4B	PWM output pin 3
	TIOC4D	PWM output pin 3' (negative-phase waveform of PWM output 3)

Table 8.38 Register Settings for Reset-Synchronized PWM Mode

Register	Description of Setting
TCNT_3	Initial setting of H'0000
TCNT_4	Initial setting of H'0000
TGRA_3	Set count cycle for TCNT_3
TGRB_3	Sets the turning point for PWM waveform output by the TIOC3B and TIOC3D pins
TGRA_4	Sets the turning point for PWM waveform output by the TIOC4A and TIOC4C pins
TGRB_4	Sets the turning point for PWM waveform output by the TIOC4B and TIOC4D pins

Procedure for Selecting the Reset-Synchronized PWM Mode: Figure 8.30 shows an example of procedure for selecting the reset-synchronized PWM mode.

1. Clear the CST3 and CST4 bits in the TSTR to 0 to halt the counting of TCNT. The reset-synchronized PWM mode must be set up while TCNT_3 and TCNT_4 are halted.
2. Set bits TPSC2 to TPSC0 and CKEG1 and CKEG0 in the TCR_3 to select the counter clock and clock edge for channel 3. Set bits CCLR2 to CCLR0 in the TCR_3 to select TGRA compare-match as a counter clear source.
3. When performing brushless DC motor control, set bit BDC in the timer gate control register (TGCR) and set the feedback signal input source and output chopping or gate signal direct output.
4. Reset TCNT_3 and TCNT_4 to H'0000.
5. TGRA_3 is the period register. Set the waveform period value in TGRA_3. Set the transition timing of the PWM output waveforms in TGRB_3, TGRA_4, and TGRB_4. Set times within the compare-match range of TCNT_3.

   $x \leq$ TGRA_3 (x: set value).
6. Select enabling/disabling of toggle output synchronized with the PMW cycle using bit PSYE in the timer output control register (TOCR), and set the PWM output level with bits OLSP and OLSN.
7. Set bits MD3 to MD0 in TMDR_3 to B'1000 to select the reset-synchronized PWM mode. TIOC3A, TIOC3B, TIOC3D, TIOC4A, TIOC4B, TIOC4C and TIOC4D function as PWM output pins*. Do not set to TMDR_4.
8. Set the enabling/disabling of the PWM waveform output pin in TOER.
9. Set the CST3 bit in the TSTR to 1 to start the count operation.

Note: The output waveform starts to toggle operation at the point of TCNT_3 = TGRA_3 = x by setting x = TGRA, i.e., cycle = duty cycle.

* PFC registers should be specified before this procedure.

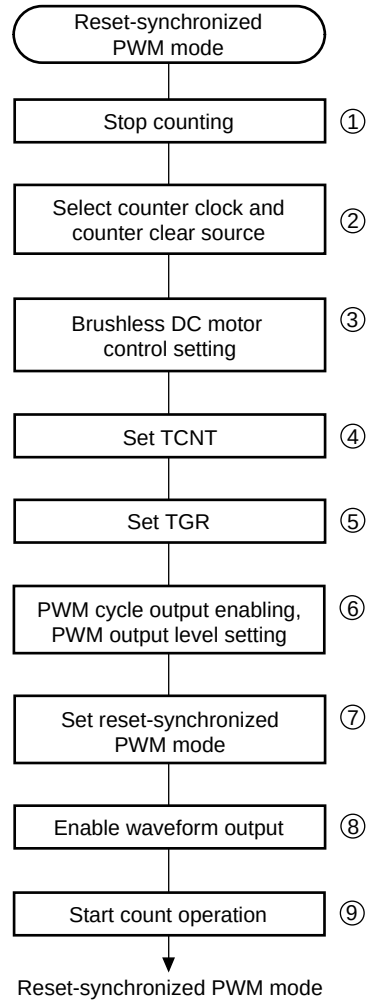


Figure 8.30 Procedure for Selecting the Reset-Synchronized PWM Mode

Reset-Synchronized PWM Mode Operation: Figure 8.31 shows an example of operation in the reset-synchronized PWM mode. TCNT_3 and TCNT_4 operate as upcounters. The counter is cleared when a TCNT_3 and TGRA_3 compare-match occurs, and then begins counting up from H'0000. The PWM output pin output toggles with each occurrence of a TGRB_3, TGRA_4, TGRB_4 compare-match, and upon counter clears.

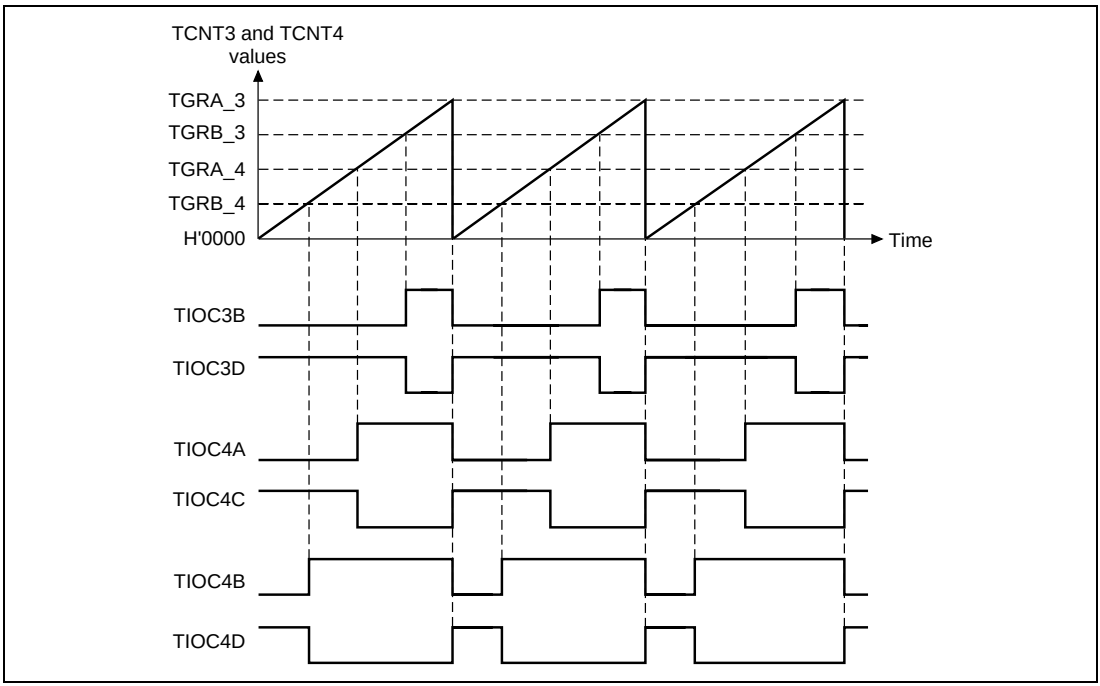


Figure 8.31 Reset-Synchronized PWM Mode Operation Example (When the TOCR's OLSN = 1 and OLSP = 1)

8.4.8 Complementary PWM Mode

In the complementary PWM mode, three-phase output of non-overlapping positive and negative PWM waveforms can be obtained by combining channels 3 and 4.

In complementary PWM mode, TIOC3B, TIOC3D, TIOC4A, TIOC4B, TIOC4C, and TIOC4D pins function as PWM output pins, the TIOC3A pin can be set for toggle output synchronized with the PWM period. TCNT_3 and TCNT_4 function as increment/decrement counters.

Table 8.39 shows the PWM output pins used. Table 8.40 shows the settings of the registers used.

A function to directly cut off the PWM output by using an external signal is supported as a port function.

Table 8.39 Output Pins for Complementary PWM Mode

Channel	Output Pin	Description
3	TIOC3A	Toggle output synchronized with PWM period (or I/O port)
	TIOC3B	PWM output pin 1
	TIOC3C	I/O port*
	TIOC3D	PWM output pin 1' (non-overlapping negative-phase waveform of PWM output 1)
4	TIOC4A	PWM output pin 2
	TIOC4B	PWM output pin 3
	TIOC4C	PWM output pin 2' (non-overlapping negative-phase waveform of PWM output 2)
	TIOC4D	PWM output pin 3' (non-overlapping negative-phase waveform of PWM output 3)

Note: * Avoid setting the TIOC3C pin as a timer I/O pin in the complementary PWM mode.

Table 8.40 Register Settings for Complementary PWM Mode

Channel	Counter/Register	Description	Read/Write from CPU
3	TCNT_3	Start of up-count from value set in dead time register	Maskable by BSC/BCR1 setting*
	TGRA_3	Set TCNT_3 upper limit value (1/2 carrier cycle + dead time)	Maskable by BSC/BCR1 setting*
	TGRB_3	PWM output 1 compare register	Maskable by BSC/BCR1 setting*
	TGRC_3	TGRA_3 buffer register	Always readable/writable
	TGRD_3	PWM output 1/TGRB_3 buffer register	Always readable/writable
4	TCNT_4	Up-count start, initialized to H'0000	Maskable by BSC/BCR1 setting*
	TGRA_4	PWM output 2 compare register	Maskable by BSC/BCR1 setting*
	TGRB_4	PWM output 3 compare register	Maskable by BSC/BCR1 setting*
	TGRC_4	PWM output 2/TGRA_4 buffer register	Always readable/writable
	TGRD_4	PWM output 3/TGRB_4 buffer register	Always readable/writable
Timer dead time data register (TDDR)		Set TCNT_4 and TCNT_3 offset value (dead time value)	Maskable by BSC/BCR1 setting*
Timer cycle data register (TCDR)		Set TCNT_4 upper limit value (1/2 carrier cycle)	Maskable by BSC/BCR1 setting*
Timer cycle buffer register (TCBR)		TCDR buffer register	Always readable/writable
Subcounter (TCNTS)		Subcounter for dead time generation	Read-only
Temporary register 1 (TEMP1)		PWM output 1/TGRB_3 temporary register	Not readable/writable
Temporary register 2 (TEMP2)		PWM output 2/TGRA_4 temporary register	Not readable/writable
Temporary register 3 (TEMP3)		PWM output 3/TGRB_4 temporary register	Not readable/writable

Note: * Access can be enabled or disabled according to the setting of bit 13 (MTURWE) in BSC/BCR1 (bus controller/bus control register 1).

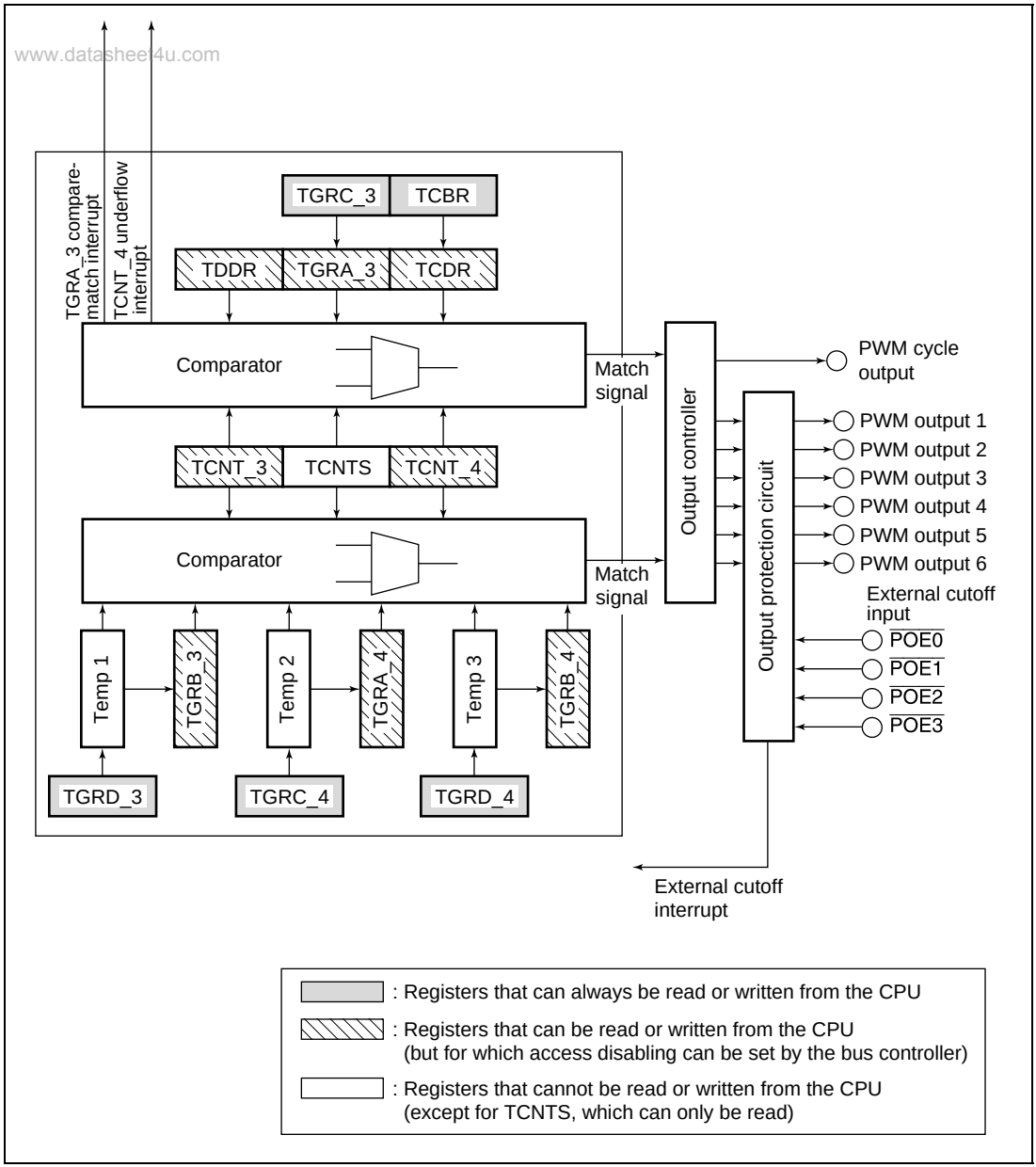


Figure 8.32 Block Diagram of Channels 3 and 4 in Complementary PWM Mode

Example of Complementary PWM Mode Setting Procedure: An example of the complementary PWM mode setting procedure is shown in figure 8.33.

1. Clear bits CST3 and CST4 in the timer start register (TSTR) to 0, and halt timer counter (TCNT) operation. Perform complementary PWM mode setting when TCNT_3 and TCNT_4 are stopped.
2. Set the same counter clock and clock edge for channels 3 and 4 with bits TPSC2 to TPSC0 and bits CKEG1 and CKEG0 in the timer control register (TCR). Use bits CCLR2 to CCLR0 to set synchronous clearing only when restarting by a synchronous clear from another channel during complementary PWM mode operation.
3. When performing brushless DC motor control, set bit BDC in the timer gate control register (TGCR) and set the feedback signal input source and output chopping or gate signal direct output.
4. Set the dead time in TCNT_3. Set TCNT_4 to H'0000.
5. Set only when restarting by a synchronous clear from another channel during complementary PWM mode operation. In this case, synchronize the channel generating the synchronous clear with channels 3 and 4 using the timer synchro register (TSYR).
6. Set the output PWM duty cycle in the duty cycle registers (TGRB_3, TGRA_4, TGRB_4) and buffer registers (TGRD_3, TGRC_4, TGRD_4). Set the same initial value in each corresponding TGR.
7. Set the dead time in the dead time register (TDDR), 1/2 the carrier cycle in the carrier cycle data register (TCDR) and carrier cycle buffer register (TCBR), and 1/2 the carrier cycle plus the dead time in TGRA_3 and TGRC_3.
8. Select enabling/disabling of toggle output synchronized with the PWM cycle using bit PSYE in the timer output control register (TOCR), and set the PWM output level with bits OLSP and OLSN.
9. Select complementary PWM mode in timer mode register 3 (TMDR_3). Pins TIOC3A, TIOC3B, TIOC3D, TIOC4A, TIOC4B, TIOC4C, and TIOC4D function as output pins*. Do not set in TMDR_4.
10. Set enabling/disabling of PWM waveform output pin output in the timer output master enable register (TOER).
11. Set bits CST3 and CST4 in TSTR to 1 simultaneously to start the count operation.

Note: * PFC registers should be specified before this procedure.

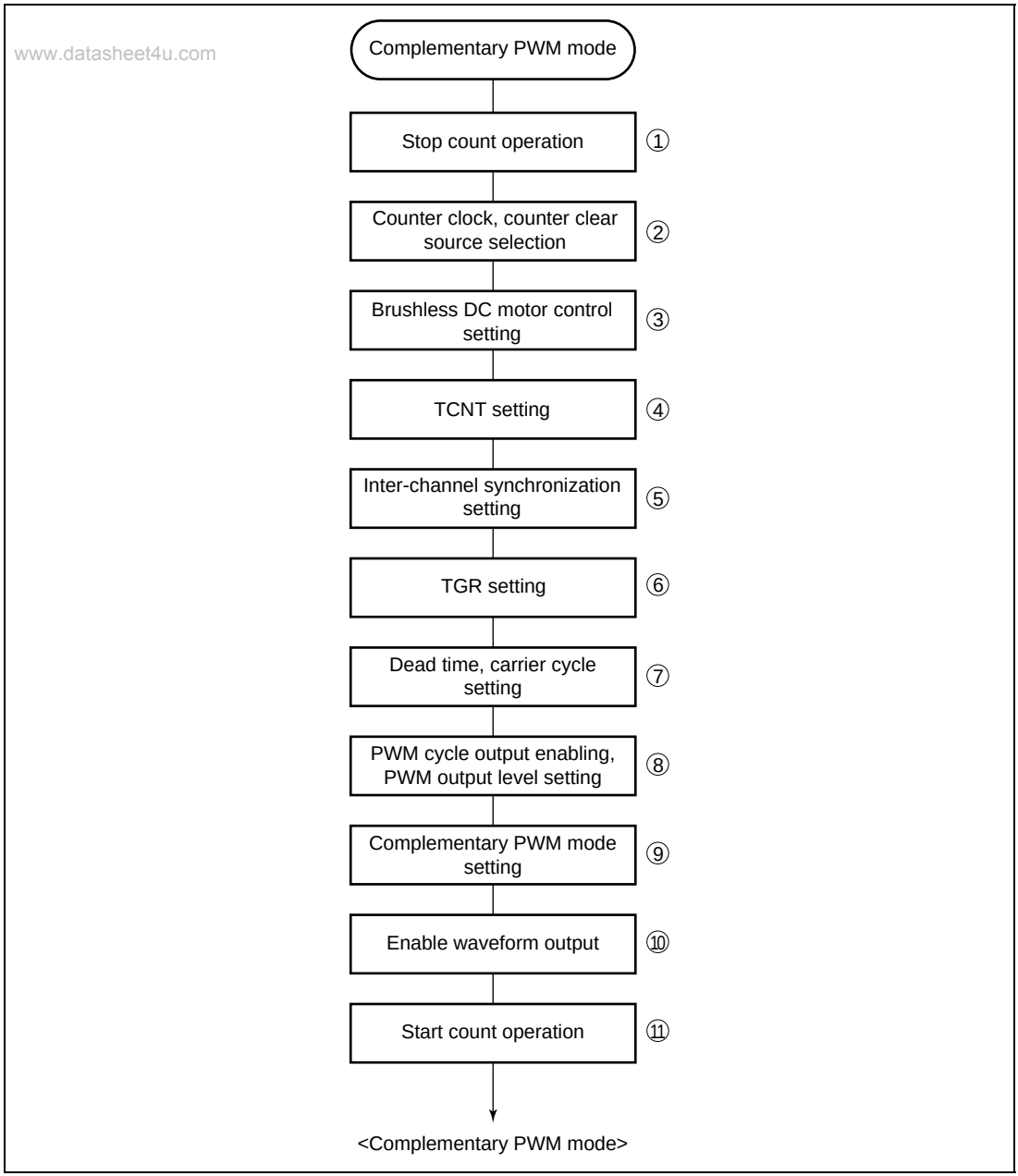


Figure 8.33 Example of Complementary PWM Mode Setting Procedure

Outline of Complementary PWM Mode Operation

In complementary PWM mode, 6-phase PWM output is possible. Figure 8.34 illustrates counter operation in complementary PWM mode, and figure 8.35 shows an example of complementary PWM mode operation.

Counter Operation: In complementary PWM mode, three counters—TCNT_3, TCNT_4, and TCNTS—perform up/down-count operations.

TCNT_3 is automatically initialized to the value set in TDDR when complementary PWM mode is selected and the CST bit in TSTR is 0.

When the CST bit is set to 1, TCNT_3 counts up to the value set in TGRA_3, then switches to down-counting when it matches TGRA_3. When the TCNT_3 value matches TDDR, the counter switches to up-counting, and the operation is repeated in this way.

TCNT_4 is initialized to H'0000.

When the CST bit is set to 1, TCNT_4 counts up in synchronization with TCNT_3, and switches to down-counting when it matches TCDR. On reaching H'0000, TCNT_4 switches to up-counting, and the operation is repeated in this way.

TCNTS is a read-only counter. It need not be initialized.

When TCNT_3 matches TCDR during TCNT_3 and TCNT_4 up/down-counting, down-counting is started, and when TCNTS matches TCDR, the operation switches to up-counting. When TCNTS matches TGRA_3, it is cleared to H'0000.

When TCNT_4 matches TDDR during TCNT_3 and TCNT_4 down-counting, up-counting is started, and when TCNTS matches TDDR, the operation switches to down-counting. When TCNTS reaches H'0000, it is set with the value in TGRA_3.

TCNTS is compared with the compare register and temporary register in which the PWM duty cycle is set during the count operation only.

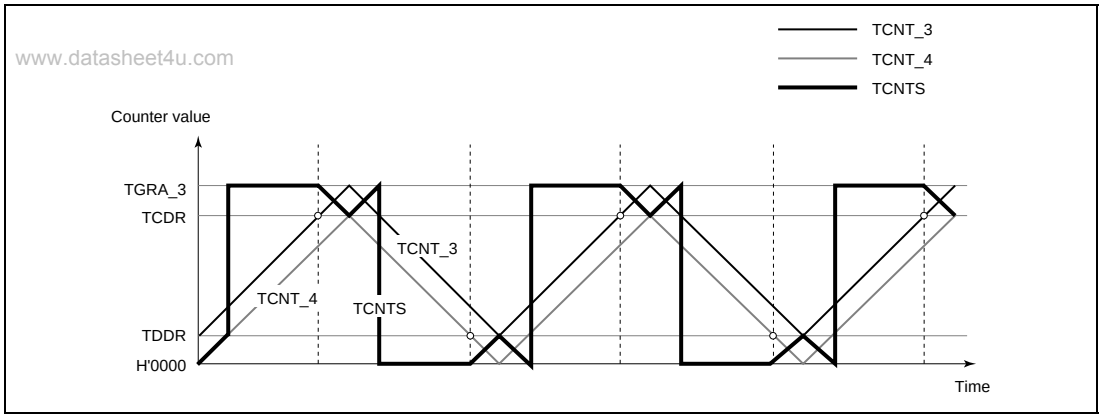


Figure 8.34 Complementary PWM Mode Counter Operation

Register Operation: In complementary PWM mode, nine registers are used, comprising compare registers, buffer registers, and temporary registers. Figure 8.35 shows an example of complementary PWM mode operation.

The registers which are constantly compared with the counters to perform PWM output are TGRB_3, TGRA_4, and TGRB_4. When these registers match the counter, the value set in bits OLSN and OLSP in the timer output control register (TOCR) is output.

The buffer registers for these compare registers are TGRD_3, TGRC_4, and TGRD_4.

Between a buffer register and compare register there is a temporary register. The temporary registers cannot be accessed by the CPU.

Data in a compare register is changed by writing the new data to the corresponding buffer register. The buffer registers can be read or written at any time.

The data written to a buffer register is constantly transferred to the temporary register in the Ta interval. Data is not transferred to the temporary register in the Tb interval. Data written to a buffer register in this interval is transferred to the temporary register at the end of the Tb interval.

The value transferred to a temporary register is transferred to the compare register when TCNTS for which the Tb interval ends matches TGRA_3 when counting up, or H'0000 when counting down. The timing for transfer from the temporary register to the compare register can be selected with bits MD3 to MD0 in the timer mode register (TMDR). Figure 8.35 shows an example in which the mode is selected in which the change is made in the trough.

In the Tb interval (Tb1 in figure 8.35) in which data transfer to the temporary register is not performed, the temporary register has the same function as the compare register, and is compared

with the counter. In this interval, therefore, there are two compare match registers for one-phase output, with the compare register containing the pre-change data, and the temporary register containing the new data. In this interval, the three counters—TCNT_3, TCNT_4, and TCNTS—and two registers—compare register and temporary register—are compared, and PWM output controlled accordingly.

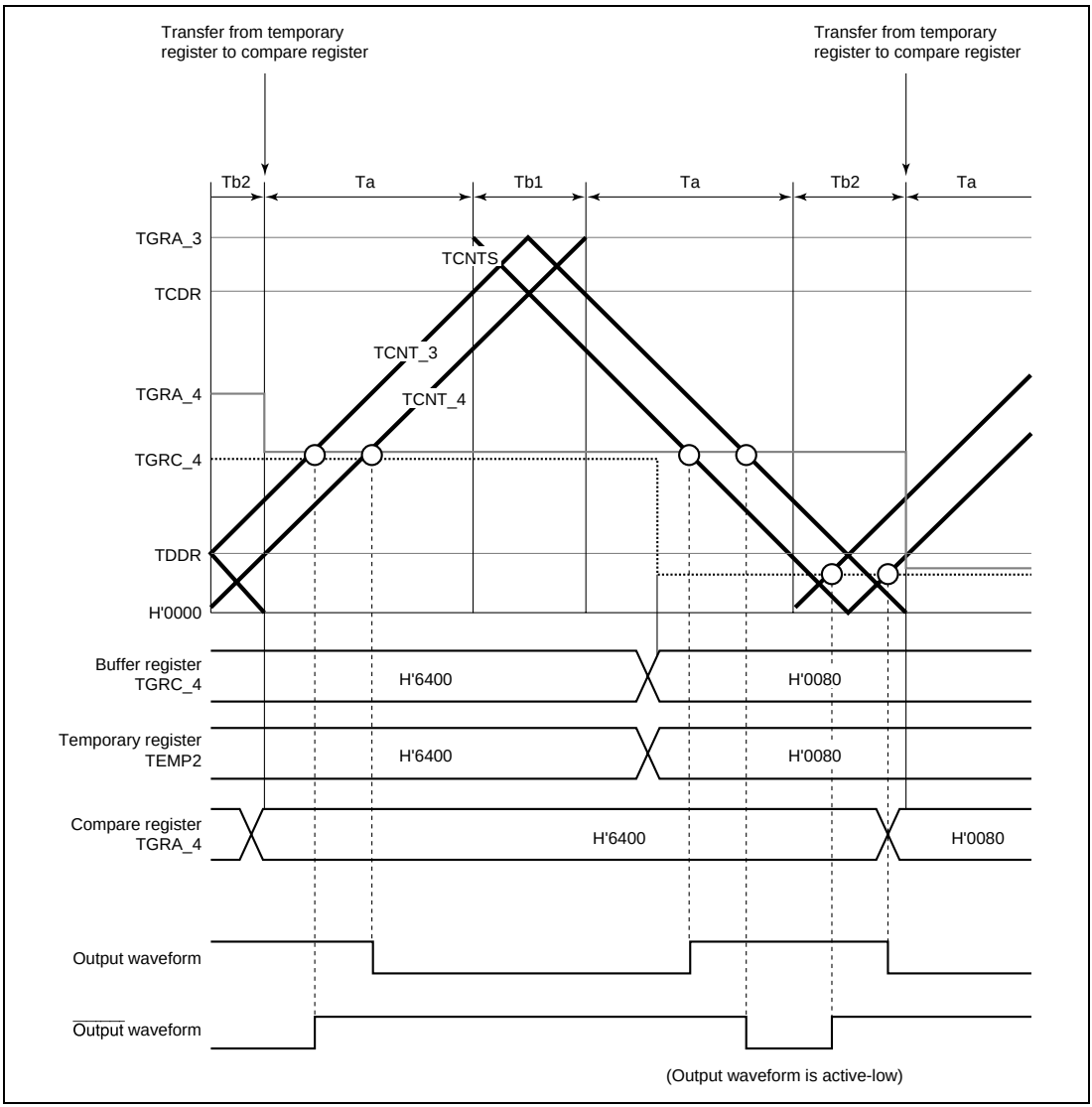


Figure 8.35 Example of Complementary PWM Mode Operation

Initialization: In complementary PWM mode, there are six registers that must be initialized.

Before setting complementary PWM mode with bits MD3 to MD0 in the timer mode register (TMDR), the following initial register values must be set.

TGRC_3 operates as the buffer register for TGRA_3, and should be set with 1/2 the PWM carrier cycle + dead time Td. The timer cycle buffer register (TCBR) operates as the buffer register for the timer cycle data register (TCDR), and should be set with 1/2 the PWM carrier cycle. Set dead time Td in the timer dead time data register (TDDR).

Set the respective initial PWM duty cycle values in buffer registers TGRD_3, TGRC_4, and TGRD_4.

The values set in the five buffer registers excluding TDDR are transferred simultaneously to the corresponding compare registers when complementary PWM mode is set.

Set TCNT_4 to H'0000 before setting complementary PWM mode.

Table 8.41 Registers and Counters Requiring Initialization

Register/Counter	Set Value
TGRC_3	1/2 PWM carrier cycle + dead time Td
TDDR	Dead time Td
TCBR	1/2 PWM carrier cycle
TGRD_3, TGRC_4, TGRD_4	Initial PWM duty cycle value for each phase
TCNT_4	H'0000

Note: The TGRC_3 set value must be the sum of 1/2 the PWM carrier cycle set in TCBR and dead time Td set in TDDR.

PWM Output Level Setting: In complementary PWM mode, the PWM pulse output level is set with bits OLSN and OLSP in the timer output control register (TOCR).

The output level can be set for each of the three positive phases and three negative phases of 6-phase output.

Complementary PWM mode should be cleared before setting or changing output levels.

Dead Time Setting: In complementary PWM mode, PWM pulses are output with a non-overlapping relationship between the positive and negative phases. This non-overlap time is called the dead time.

The non-overlap time is set in the timer dead time data register (TDDR). The value set in TDDR is used as the TCNT_3 counter start value, and creates non-overlap between TCNT_3 and TCNT_4. Complementary PWM mode should be cleared before changing the contents of TDDR.

PWM Cycle Setting: In complementary PWM mode, the PWM pulse cycle is set in two registers—TGRA_3, in which the TCNT_3 upper limit value is set, and TCDR, in which the TCNT_4 upper limit value is set. The settings should be made so as to achieve the following relationship between these two registers:

TGRA_3 set value = TCDR set value + TDDR set value

The TGRA_3 and TCDR settings are made by setting the values in buffer registers TGRC_3 and TCBR. The values set in TGRC_3 and TCBR are transferred simultaneously to TGRA_3 and TCDR in accordance with the transfer timing selected with bits MD3 to MD0 in the timer mode register (TMDR).

The updated PWM cycle is reflected from the next cycle when the data update is performed at the peak, and from the current cycle when performed in the trough. Figure 8.36 illustrates the operation when the PWM cycle is updated at the peak.

See the following section, Register data updating, for the method of updating the data in each buffer register.

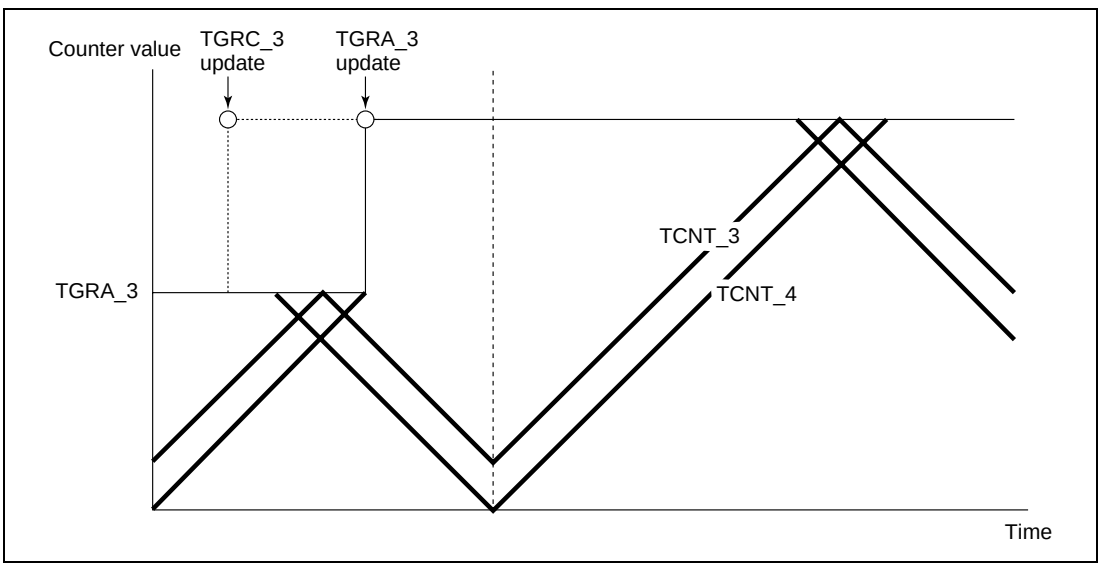


Figure 8.36 Example of PWM Cycle Updating

Register Data Updating: In complementary PWM mode, the buffer register is used to update the data in a compare register. The update data can be written to the buffer register at any time. There are five PWM duty cycle and carrier cycle registers that have buffer registers and can be updated during operation.

There is a temporary register between each of these registers and its buffer register. When subcounter TCNTS is not counting, if buffer register data is updated, the temporary register value is also rewritten. Transfer is not performed from buffer registers to temporary registers when TCNTS is counting; in this case, the value written to a buffer register is transferred after TCNTS halts.

The temporary register value is transferred to the compare register at the data update timing set with bits MD3 to MD0 in the timer mode register (TMDR). Figure 8.37 shows an example of data updating in complementary PWM mode. This example shows the mode in which data updating is performed at both the counter peak and trough.

When rewriting buffer register data, a write to TGRD_4 must be performed at the end of the update. Data transfer from the buffer registers to the temporary registers is performed simultaneously for all five registers after the write to TGRD_4.

A write to TGRD_4 must be performed after writing data to the registers to be updated, even when not updating all five registers, or when updating the TGRD_4 data. In this case, the data written to TGRD_4 should be the same as the data prior to the write operation.

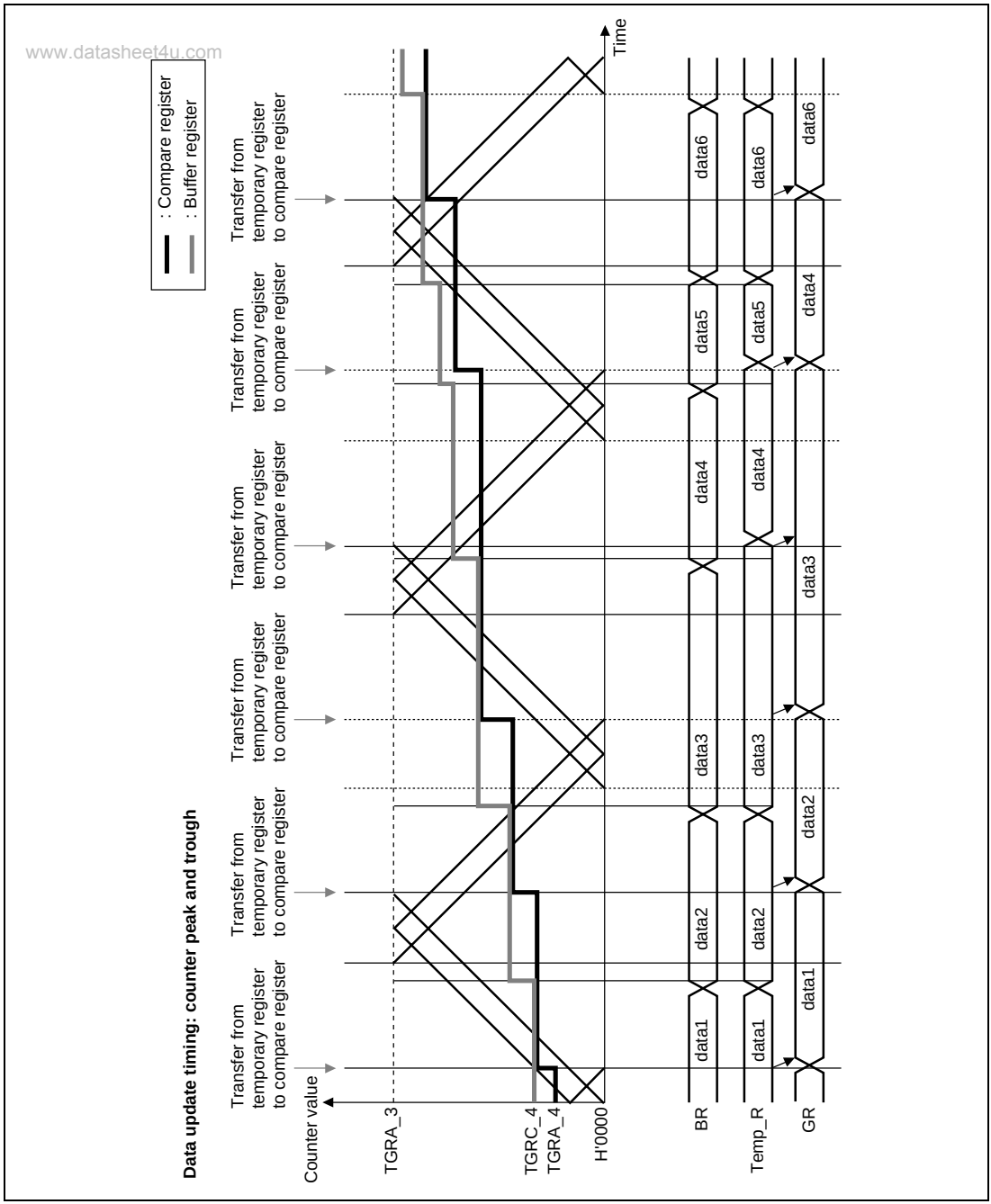


Figure 8.37 Example of Data Update in Complementary PWM Mode

Initial Output in Complementary PWM Mode: In complementary PWM mode, the initial output is determined by the setting of bits OLSN and OLSP in the timer output control register (TOCR).

This initial output is the PWM pulse non-active level, and is output from when complementary PWM mode is set with the timer mode register (TMDR) until TCNT_4 exceeds the value set in the dead time register (TDDR). Figure 8.38 shows an example of the initial output in complementary PWM mode.

An example of the waveform when the initial PWM duty cycle value is smaller than the TDDR value is shown in figure 8.39.

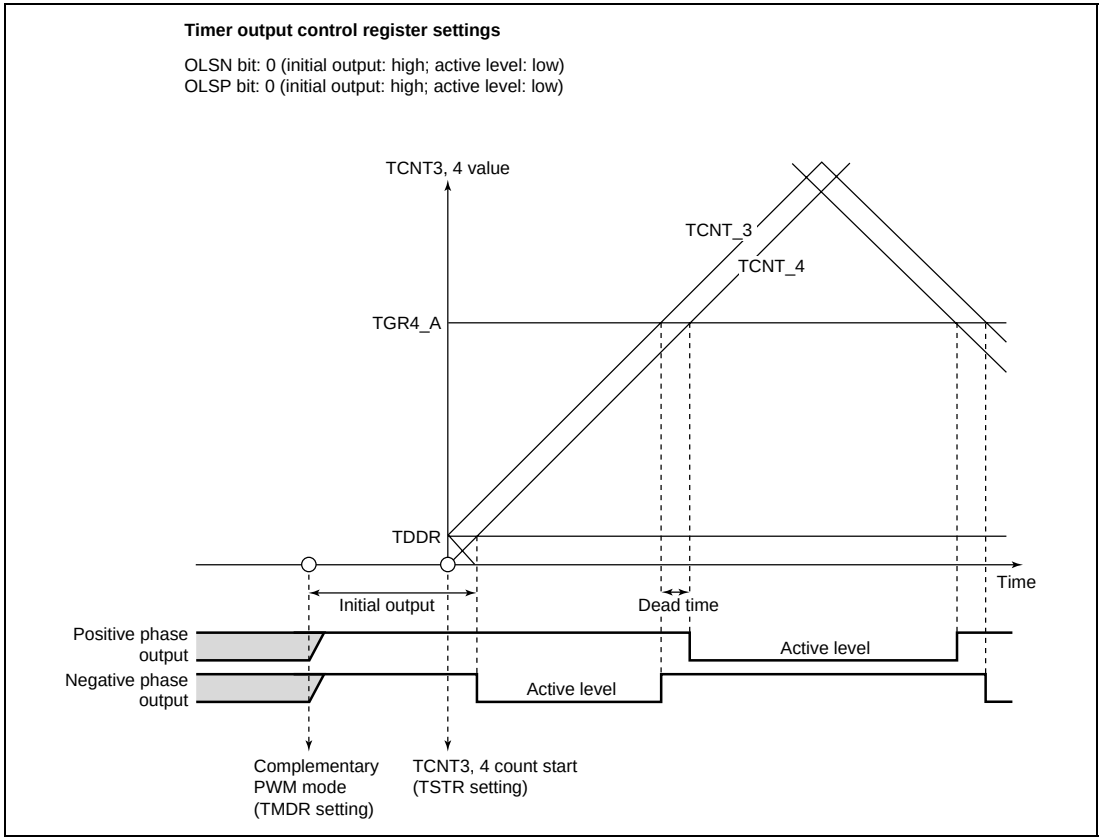


Figure 8.38 Example of Initial Output in Complementary PWM Mode (1)

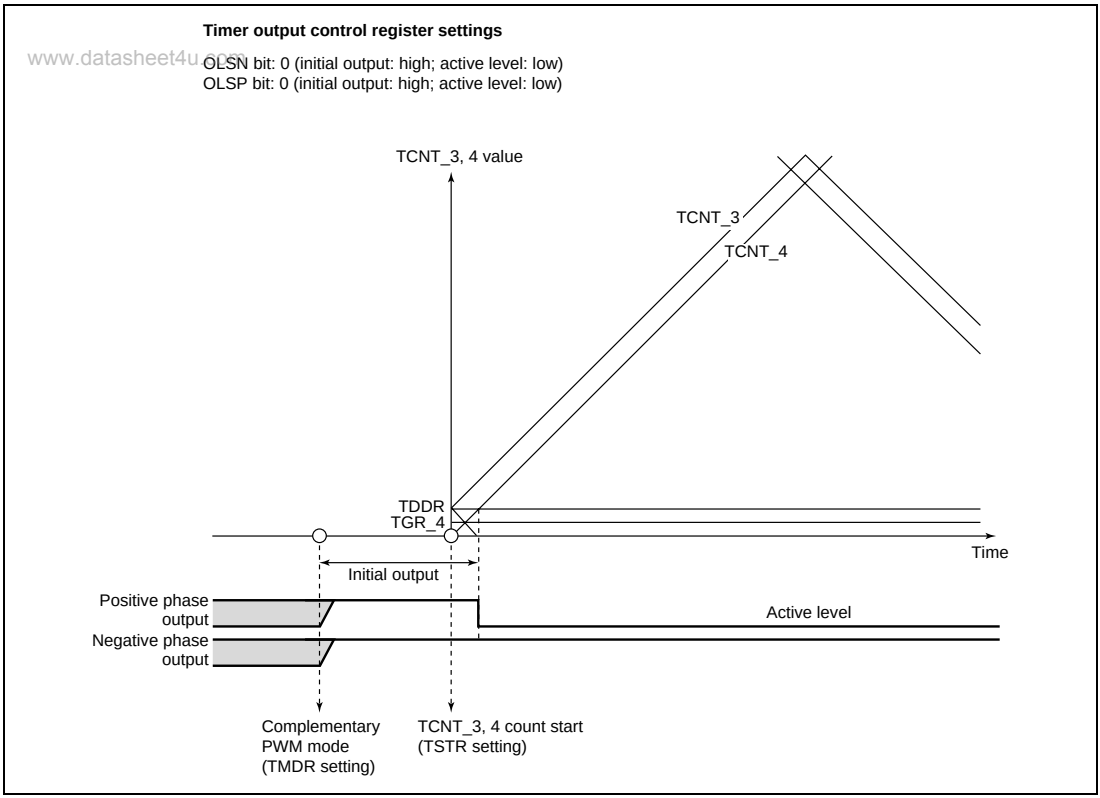


Figure 8.39 Example of Initial Output in Complementary PWM Mode (2)

Complementary PWM Mode PWM Output Generation Method: In complementary PWM mode, 3-phase output is performed of PWM waveforms with a non-overlap time between the positive and negative phases. This non-overlap time is called the dead time.

A PWM waveform is generated by output of the output level selected in the timer output control register in the event of a compare-match between a counter and data register. While TCNTS is counting, data register and temporary register values are simultaneously compared to create consecutive PWM pulses from 0 to 100%. The relative timing of on and off compare-match occurrence may vary, but the compare-match that turns off each phase takes precedence to secure the dead time and ensure that the positive phase and negative phase on times do not overlap. Figures 8.40 to 8.42 show examples of waveform generation in complementary PWM mode.

The positive phase/negative phase off timing is generated by a compare-match with the solid-line counter, and the on timing by a compare-match with the dotted-line counter operating with a delay of the dead time behind the solid-line counter. In the T1 period, compare-match **a** that turns off the negative phase has the highest priority, and compare-matches occurring prior to **a** are ignored. In

the T2 period, compare-match **c** that turns off the positive phase has the highest priority, and compare-matches occurring prior to **c** are ignored.

In normal cases, compare-matches occur in the order **a** → **b** → **c** → **d** (or **c** → **d** → **a'** → **b'**), as shown in figure 8.40.

If compare-matches deviate from the **a** → **b** → **c** → **d** order, since the time for which the negative phase is off is less than twice the dead time, the figure shows the positive phase is not being turned on. If compare-matches deviate from the **c** → **d** → **a'** → **b'** order, since the time for which the positive phase is off is less than twice the dead time, the figure shows the negative phase is not being turned on.

If compare-match **c** occurs first following compare-match **a**, as shown in figure 8.41, compare-match **b** is ignored, and the negative phase is turned off by compare-match **d**. This is because turning off of the positive phase has priority due to the occurrence of compare-match **c** (positive phase off timing) before compare-match **b** (positive phase on timing) (consequently, the waveform does not change since the positive phase goes from off to off).

Similarly, in the example in figure 8.42, compare-match **a'** with the new data in the temporary register occurs before compare-match **c**, but other compare-matches occurring up to **c**, which turns off the positive phase, are ignored. As a result, the positive phase is not turned on.

Thus, in complementary PWM mode, compare-matches at turn-off timings take precedence, and turn-on timing compare-matches that occur before a turn-off timing compare-match are ignored.

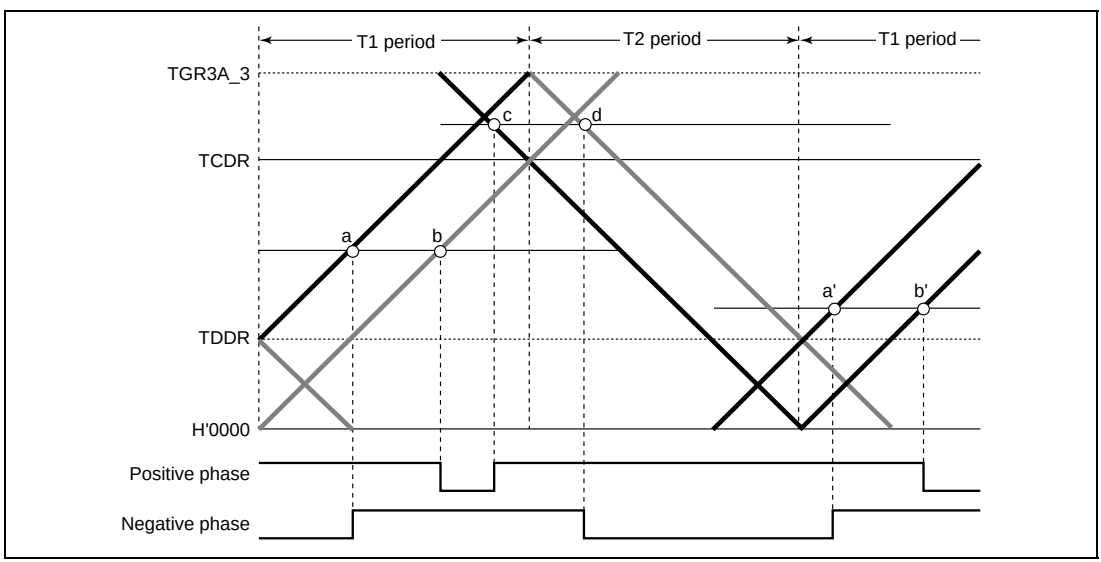


Figure 8.40 Example of Complementary PWM Mode Waveform Output (1)

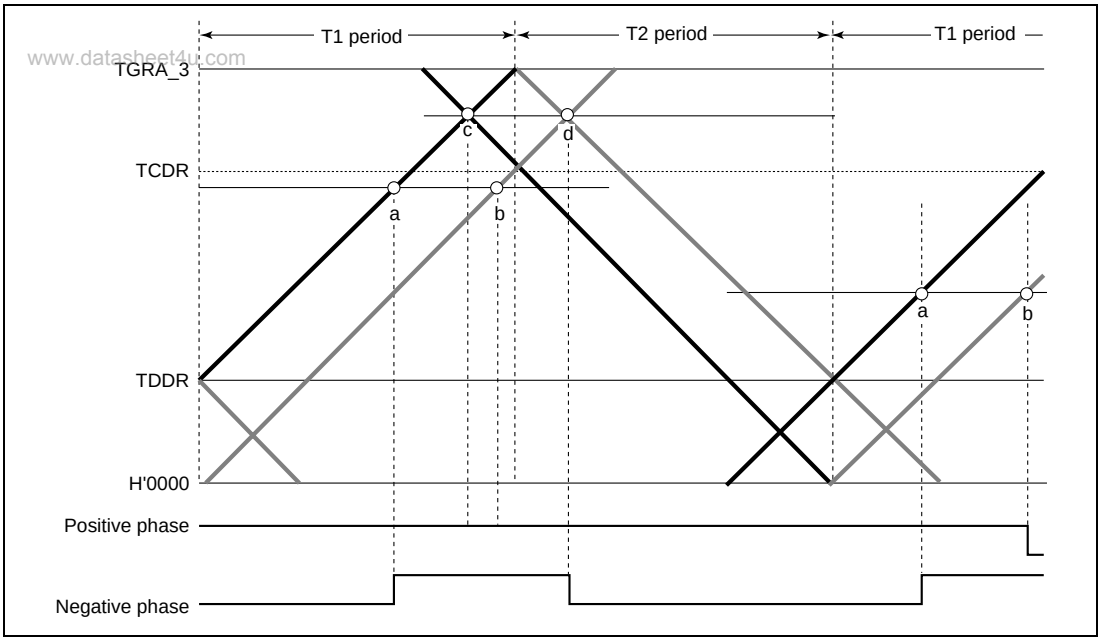


Figure 8.41 Example of Complementary PWM Mode Waveform Output (2)

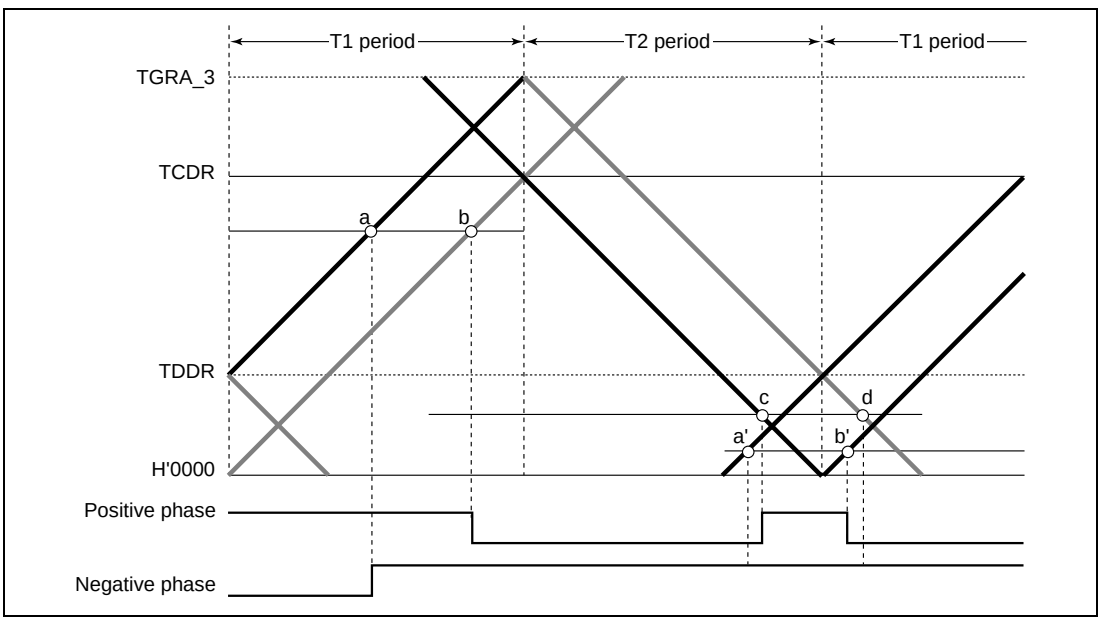


Figure 8.42 Example of Complementary PWM Mode Waveform Output (3)

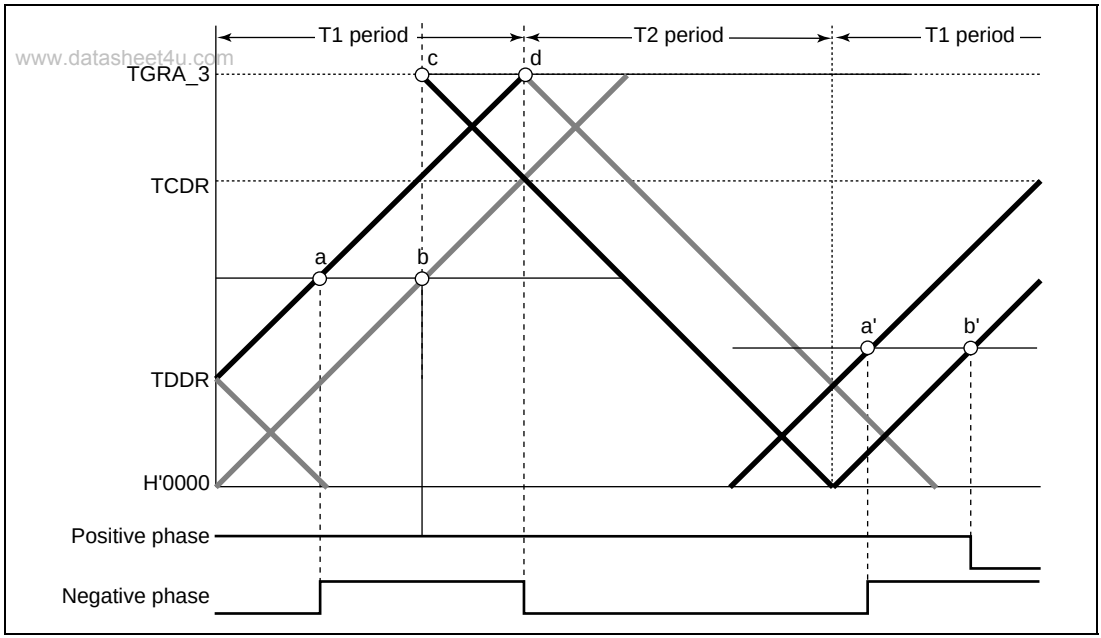


Figure 8.43 Example of Complementary PWM Mode 0% and 100% Waveform Output (1)

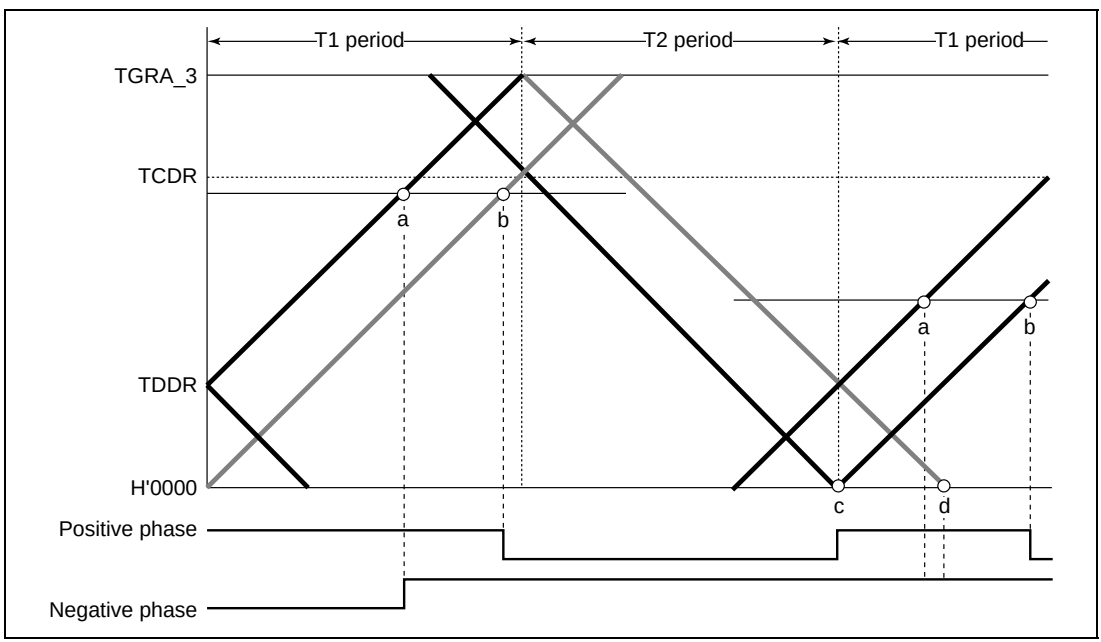


Figure 8.44 Example of Complementary PWM Mode 0% and 100% Waveform Output (2)

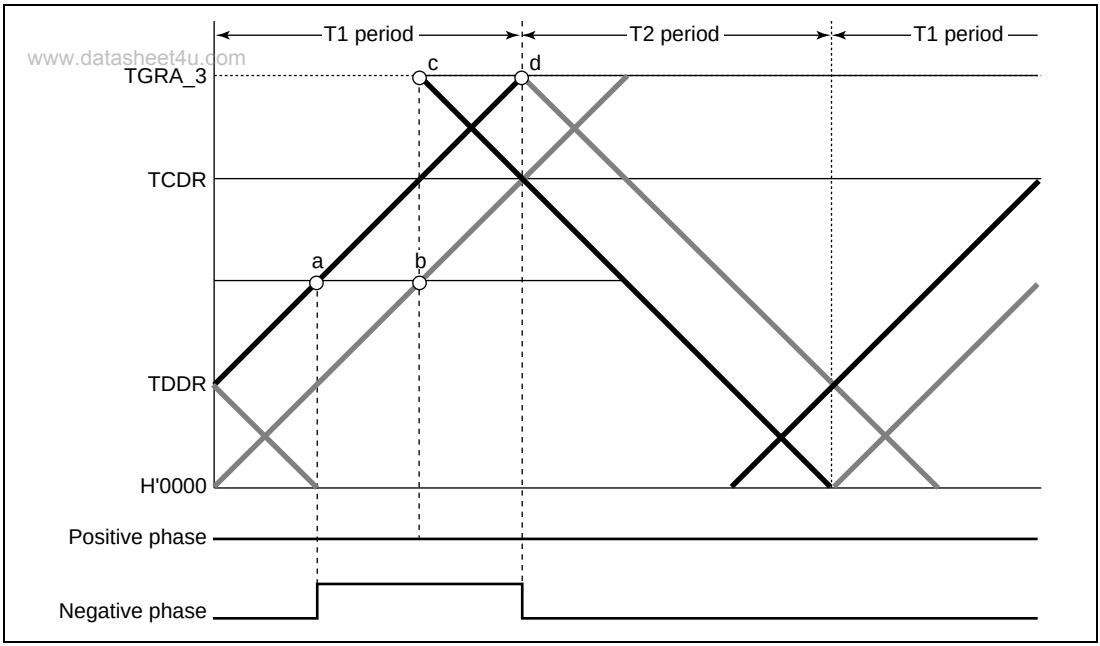


Figure 8.45 Example of Complementary PWM Mode 0% and 100% Waveform Output (3)

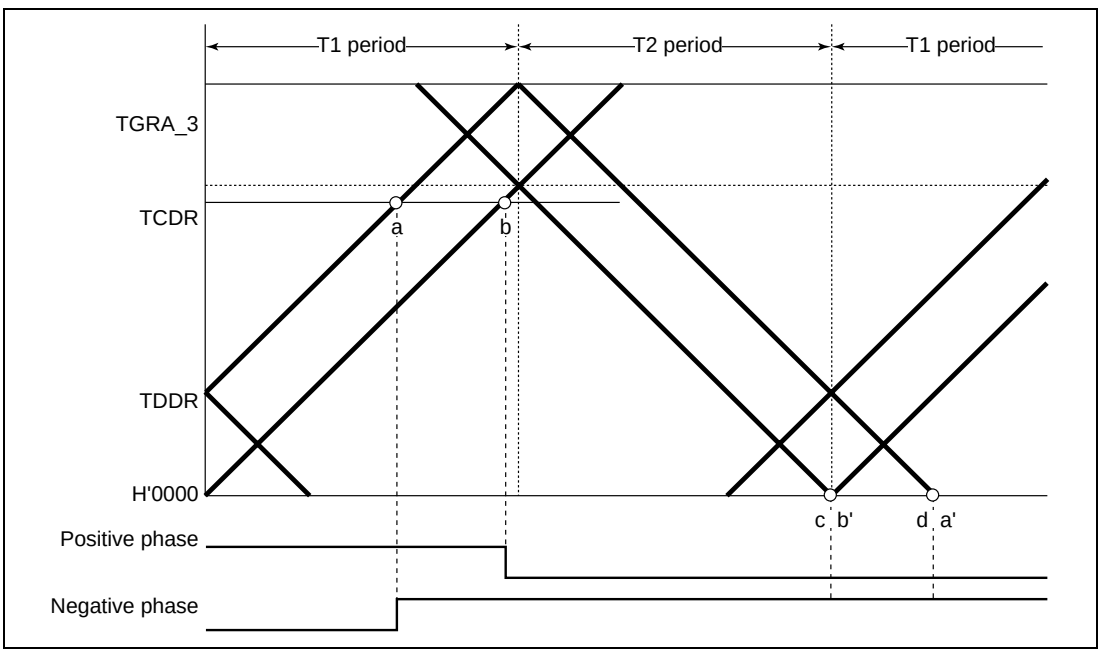


Figure 8.46 Example of Complementary PWM Mode 0% and 100% Waveform Output (4)

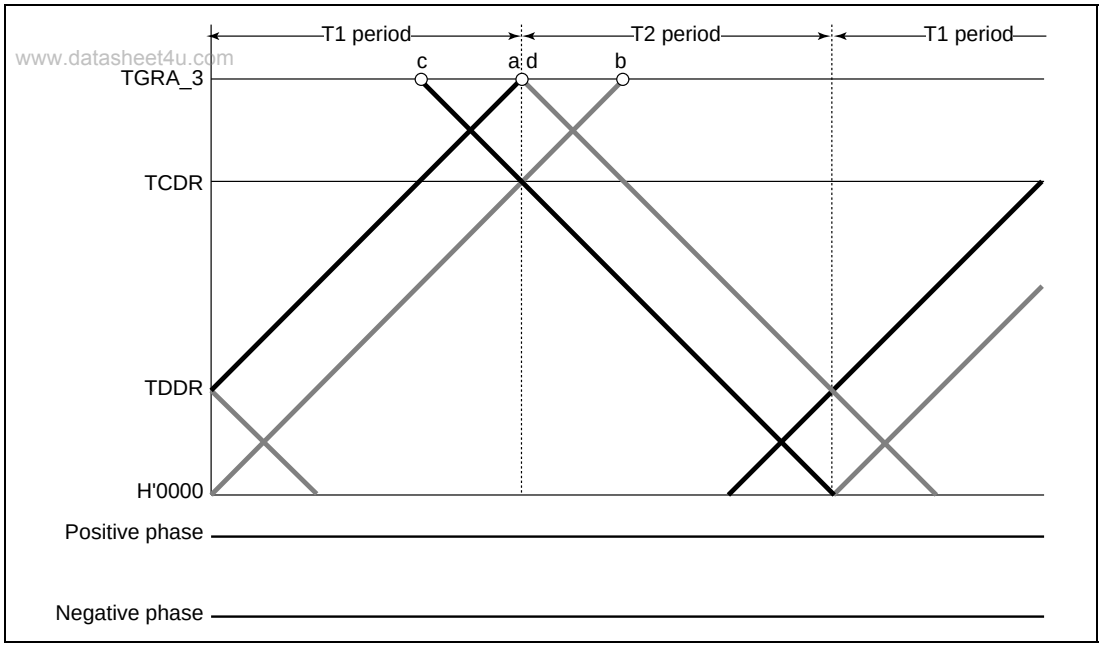


Figure 8.47 Example of Complementary PWM Mode 0% and 100% Waveform Output (5)

Complementary PWM Mode 0% and 100% Duty Cycle Output: In complementary PWM mode, 0% and 100% duty cycles can be output as required. Figures 8.43 to 8.47 show output examples.

100% duty cycle output is performed when the data register value is set to H'0000. The waveform in this case has a positive phase with a 100% on-state. 0% duty cycle output is performed when the data register value is set to the same value as TGRA_3. The waveform in this case has a positive phase with a 100% off-state.

On and off compare-matches occur simultaneously, but if a turn-on compare-match and turn-off compare-match for the same phase occur simultaneously, both compare-matches are ignored and the waveform does not change.

Toggle Output Synchronized with PWM Cycle: In complementary PWM mode, toggle output can be performed in synchronization with the PWM carrier cycle by setting the PSYE bit to 1 in the timer output control register (TOCR). An example of a toggle output waveform is shown in figure 8.48.

This output is toggled by a compare-match between TCNT_3 and TGRA_3 and a compare-match between TCNT4 and H'0000.

The output pin for this toggle output is the TIOC3A pin. The initial output is 1.

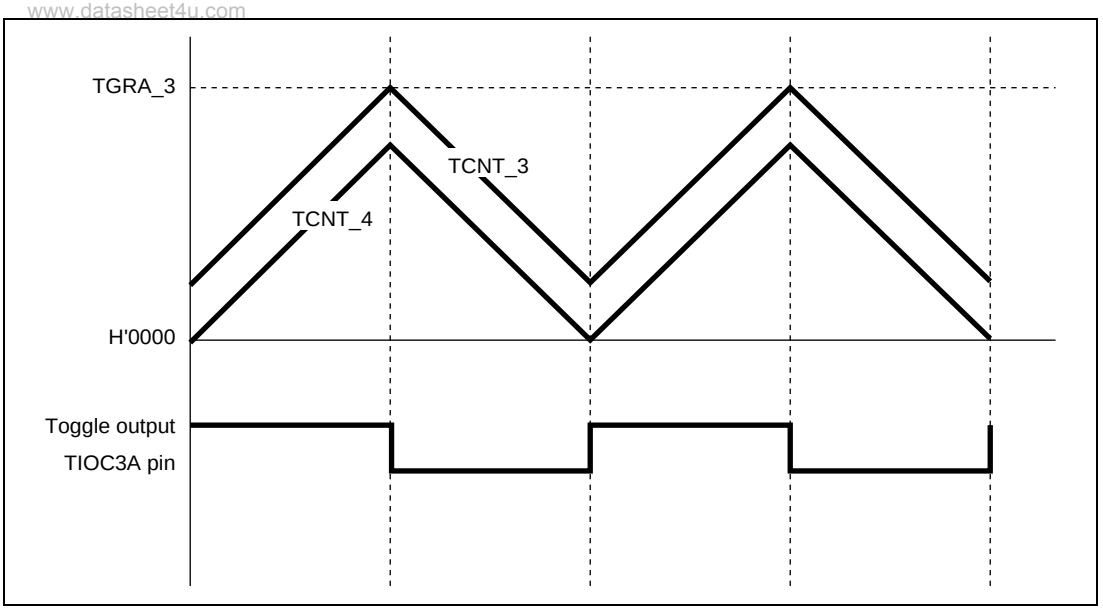


Figure 8.48 Example of Toggle Output Waveform Synchronized with PWM Output

Counter Clearing by another Channel: In complementary PWM mode, by setting a mode for synchronization with another channel by means of the timer synchro register (TSYR), and selecting synchronous clearing with bits CCLR2 to CCLR0 in the timer control register (TCR), it is possible to have TCNT_3, TCNT_4, and TCNTS cleared by another channel.

Figure 8.49 illustrates the operation.

Use of this function enables counter clearing and restarting to be performed by means of an external signal.

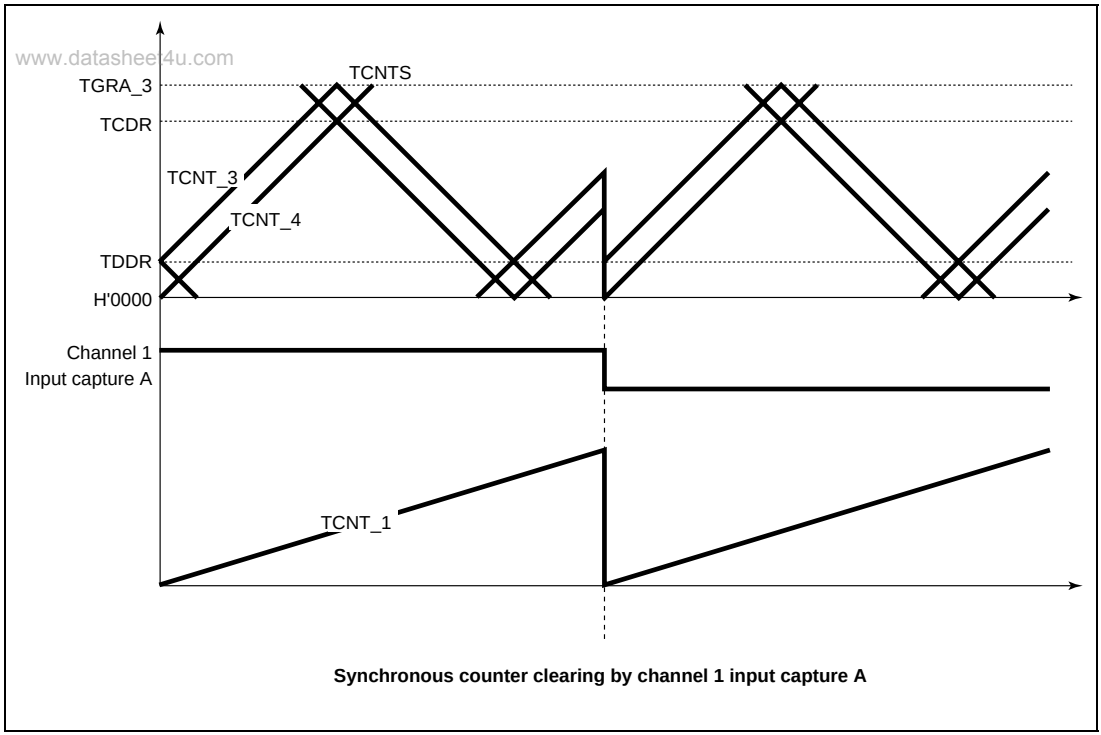


Figure 8.49 Counter Clearing Synchronized with Another Channel

Example of AC Synchronous Motor (Brushless DC Motor) Drive Waveform Output: In complementary PWM mode, a brushless DC motor can easily be controlled using the timer gate control register (TGCR). Figures 8.50 to 8.53 show examples of brushless DC motor drive waveforms created using TGCR.

When output phase switching for a 3-phase brushless DC motor is performed by means of external signals detected with a Hall element, etc., clear the FB bit in TGCR to 0. In this case, the external signals indicating the polarity position are input to channel 0 timer input pins TIOC0A, TIOC0B, and TIOC0C (set with PFC). When an edge is detected at pin TIOC0A, TIOC0B, or TIOC0C, the output on/off state is switched automatically.

When the FB bit is 1, the output on/off state is switched when the UF, VF, or WF bit in TGCR is cleared to 0 or set to 1.

The drive waveforms are output from the complementary PWM mode 6-phase output pins. With this 6-phase output, in the case of on output, it is possible to use complementary PWM mode output and perform chopping output by setting the N bit or P bit to 1. When the N bit or P bit is 0, level output is selected.

The 6-phase output active level (on output level) can be set with the OLSN and OLSP bits in the timer output control register (TOCR) regardless of the setting of the N and P bits.

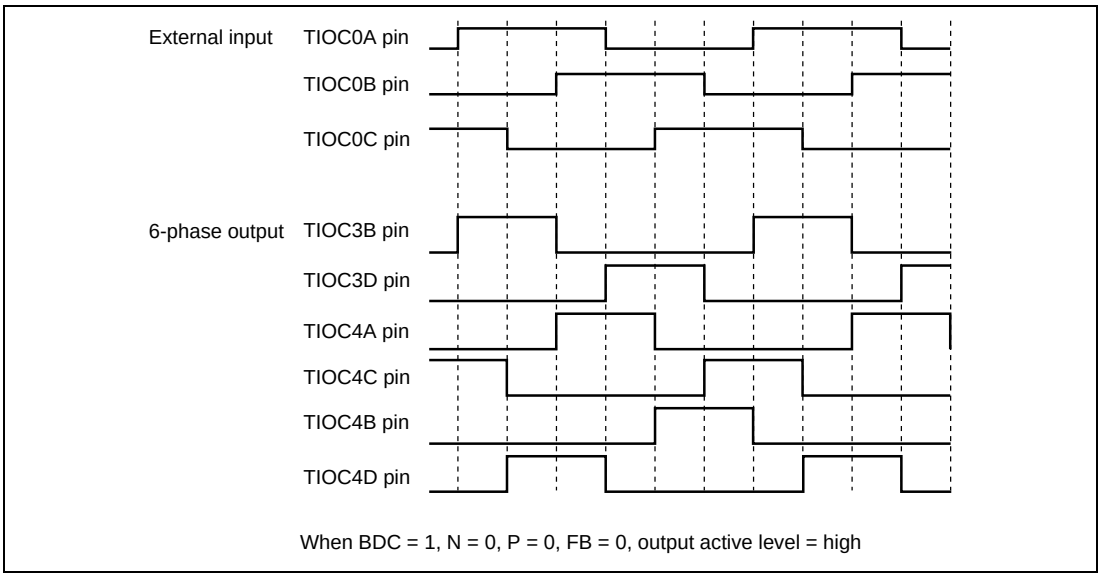


Figure 8.50 Example of Output Phase Switching by External Input (1)

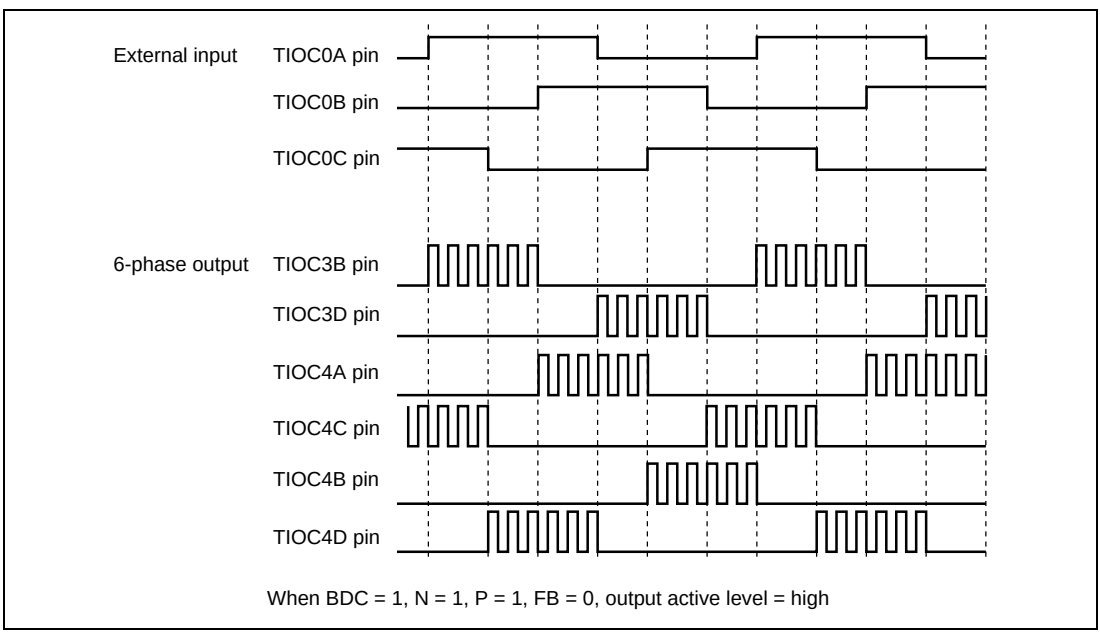


Figure 8.51 Example of Output Phase Switching by External Input (2)

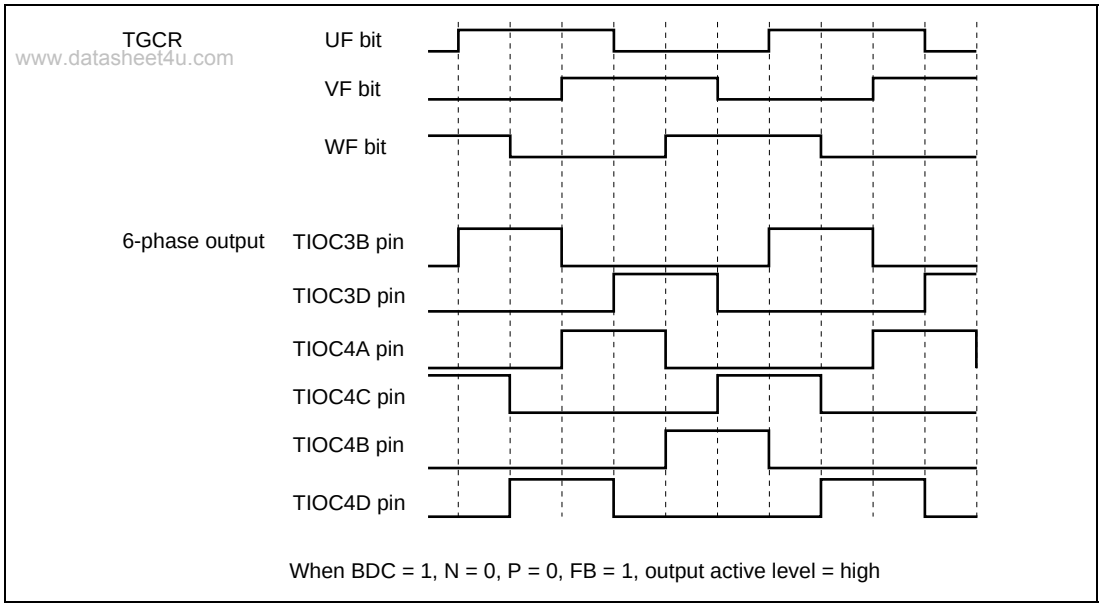


Figure 8.52 Example of Output Phase Switching by Means of UF, VF, WF Bit Settings (1)

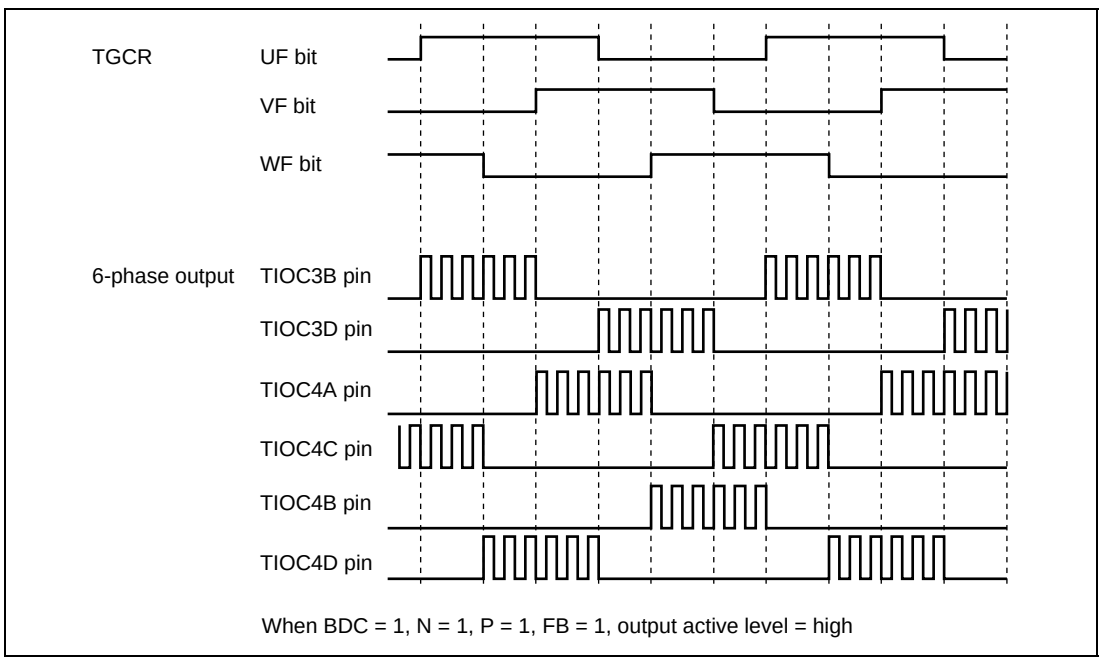


Figure 8.53 Example of Output Phase Switching by Means of UF, VF, WF Bit Settings (2)

A/D Conversion Start Request Setting: In complementary PWM mode, an A/D conversion start request can be set using a TGRA_3 compare-match or a compare-match on a channel other than channels 3 and 4.

When start requests using a TGRA_3 compare-match are set, A/D conversion can be started at the center of the PWM pulse.

A/D conversion start requests can be set by setting the TTGE bit to 1 in the timer interrupt enable register (TIER).

Complementary PWM Mode Output Protection Function

Complementary PWM mode output has the following protection functions.

- Register and counter miswrite prevention function

  With the exception of the buffer registers, which can be rewritten at any time, access by the CPU can be enabled or disabled for the mode registers, control registers, compare registers, and counters used in complementary PWM mode by means of bit 13 in the bus controller's bus control register 1 (BCR1). The registers and counters concerned are listed in table 8.3.

  This function enables the CPU to prevent miswriting due to CPU runaway by disabling CPU access to the mode registers, control registers, and counters.

- Halting of PWM output by external signal

  The 6-phase PWM output pins can be set automatically to the high-impedance state by inputting specified external signals. There are four external signal input pins.

  See section 8.9, Port Output Enable (POE), for details.

- Halting of PWM output when oscillator is stopped

  If it is detected that the clock input to this LSI has stopped, the 6-phase PWM output pins automatically go to the high-impedance state. The pin states are not guaranteed when the clock is restarted.

  For details, see section 4.2, Function for Detecting the Oscillator Halt.

8.5 Interrupt Sources

8.5.1 Interrupts and Priorities

There are three kinds of MTU interrupt source; TGR input capture/compare match, TCNT overflow, and TCNT underflow. Each interrupt source has its own status flag and enable/disabled bit, allowing the generation of interrupt request signals to be enabled or disabled individually.

When an interrupt request is generated, the corresponding status flag in TSR is set to 1. If the corresponding enable/disable bit in TIER is set to 1 at this time, an interrupt is requested. The interrupt request is cleared by clearing the status flag to 0.

Relative channel priorities can be changed by the interrupt controller, however the priority order within a channel is fixed. For details, see section 6, Interrupt Controller (INTC).

Table 8.42 lists the MTU interrupt sources.

Table 8.42 MTU Interrupts

Channel	Name	Interrupt Source	Interrupt Flag	Priority
0	TGI0A	TGRA_0 input capture/compare match	TGFA_0	High
	TGI0B	TGRB_0 input capture/compare match	TGFB_0	
	TGI0C	TGRC_0 input capture/compare match	TGFC_0	
	TGI0D	TGRD_0 input capture/compare match	TGFD_0	
	TCI0V	TCNT_0 overflow	TCFV_0	
1	TGI1A	TGRA_1 input capture/compare match	TGFA_1	
	TGI1B	TGRB_1 input capture/compare match	TGFB_1	
	TCI1V	TCNT_1 overflow	TCFV_1	
	TCI1U	TCNT_1 underflow	TCFU_1	
2	TGI2A	TGRA_2 input capture/compare match	TGFA_2	
	TGI2B	TGRB_2 input capture/compare match	TGFB_2	
	TCI2V	TCNT_2 overflow	TCFV_2	
	TCI2U	TCNT_2 underflow	TCFU_2	
3	TGI3A	TGRA_3 input capture/compare match	TGFA_3	
	TGI3B	TGRB_3 input capture/compare match	TGFB_3	
	TGI3C	TGRC_3 input capture/compare match	TGFC_3	
	TGI3D	TGRD_3 input capture/compare match	TGFD_3	
	TCI3V	TCNT_3 overflow	TCFV_3	
4	TGI4A	TGRA_4 input capture/compare match	TGFA_4	
	TGI4B	TGRB_4 input capture/compare match	TGFB_4	
	TGI4C	TGRC_4 input capture/compare match	TGFC_4	
	TGI4D	TGRD_4 input capture/compare match	TGFD_4	
	TCI4V	TCNT_4 overflow	TCFV_4	Low

Note: This table shows the initial state immediately after a reset. The relative channel priorities can be changed by the interrupt controller.

Input Capture/Compare Match Interrupt: An interrupt is requested if the TGIE bit in TIER is set to 1 when the TGF flag in TSR is set to 1 by the occurrence of a TGR input capture/compare match on a particular channel. The interrupt request is cleared by clearing the TGF flag to 0. The MTU has 16 input capture/compare match interrupts, four each for channels 0, 3, and 4, and two each for channels 1 and 2.

Overflow Interrupt: An interrupt is requested if the TCIEV bit in TIER is set to 1 when the TCFV flag in TSR is set to 1 by the occurrence of TCNT overflow on a channel. The interrupt request is cleared by clearing the TCFV flag to 0. The MTU has five overflow interrupts, one for each channel.

Underflow Interrupt: An interrupt is requested if the TCIEU bit in TIER is set to 1 when the TCFU flag in TSR is set to 1 by the occurrence of TCNT underflow on a channel. The interrupt request is cleared by clearing the TCFU flag to 0. The MTU has four underflow interrupts, one each for channels 1 and 2.

8.5.2 A/D Converter Activation

The A/D converter can be activated by the TGRA input capture/compare match in each channel.

If the TTGE bit in TIER is set to 1 when the TGFA flag in TSR is set to 1 by the occurrence of a TGRA input capture/compare match on a particular channel, a request to start A/D conversion is sent to the A/D converter. If the MTU conversion start trigger has been selected on the A/D converter at this time, A/D conversion starts.

In the MTU, a total of five TGRA input capture/compare match interrupts can be used as A/D converter conversion start sources, one for each channel.

8.6 Operation Timing

8.6.1 Input/Output Timing

TCNT Count Timing: Figure 8.54 shows TCNT count timing in internal clock operation, and Figure 8.55 shows TCNT count timing in external clock operation (normal mode), and figure 8.56 shows TCNT count timing in external clock operation (phase counting mode).

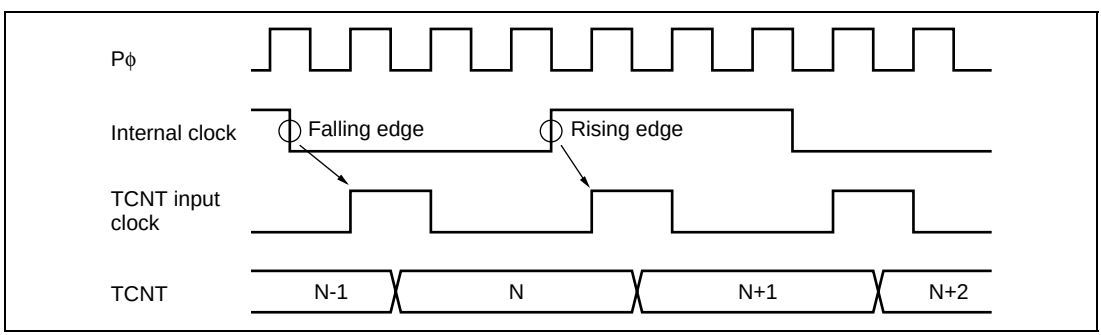


Figure 8.54 Count Timing in Internal Clock Operation

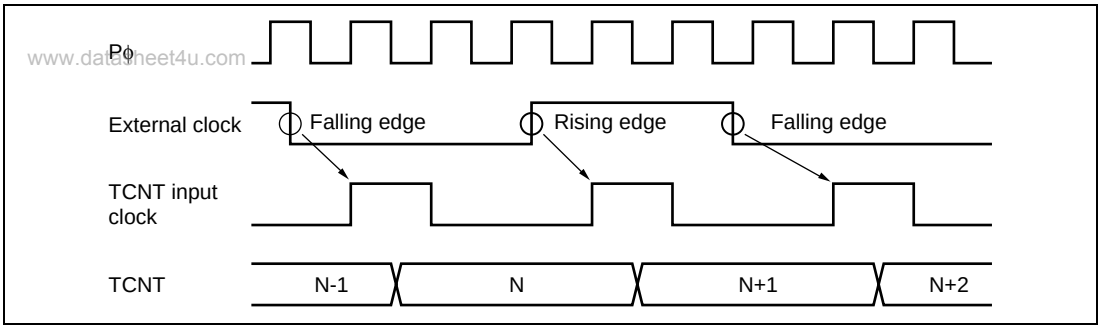


Figure 8.55 Count Timing in External Clock Operation

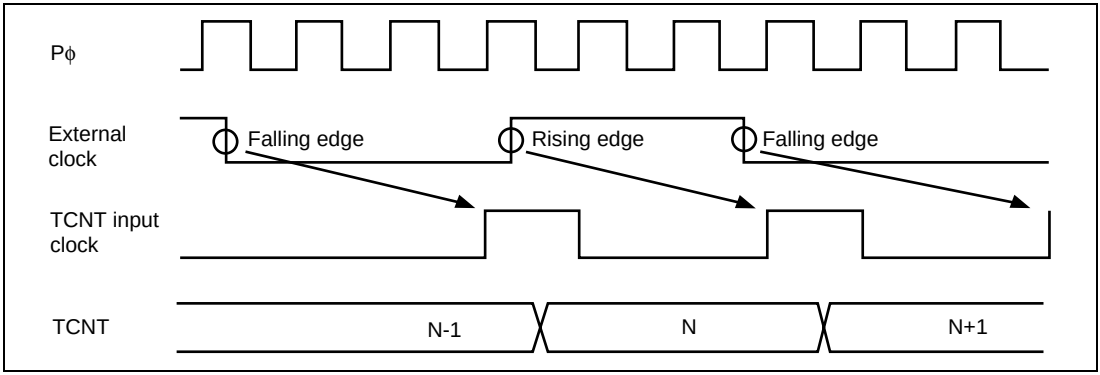


Figure 8.56 Count Timing in External Clock Operation (Phase Counting Mode)

Output Compare Output Timing: A compare match signal is generated in the final state in which TCNT and TGR match (the point at which the count value matched by TCNT is updated). When a compare match signal is generated, the output value set in TIOR is output at the output compare output pin (TIOC pin). After a match between TCNT and TGR, the compare match signal is not generated until the TCNT input clock is generated.

Figure 8.57 shows output compare output timing (normal mode and PWM mode) and figure 8.58 shows output compare output timing (complementary PWM mode and reset synchronous PWM mode).

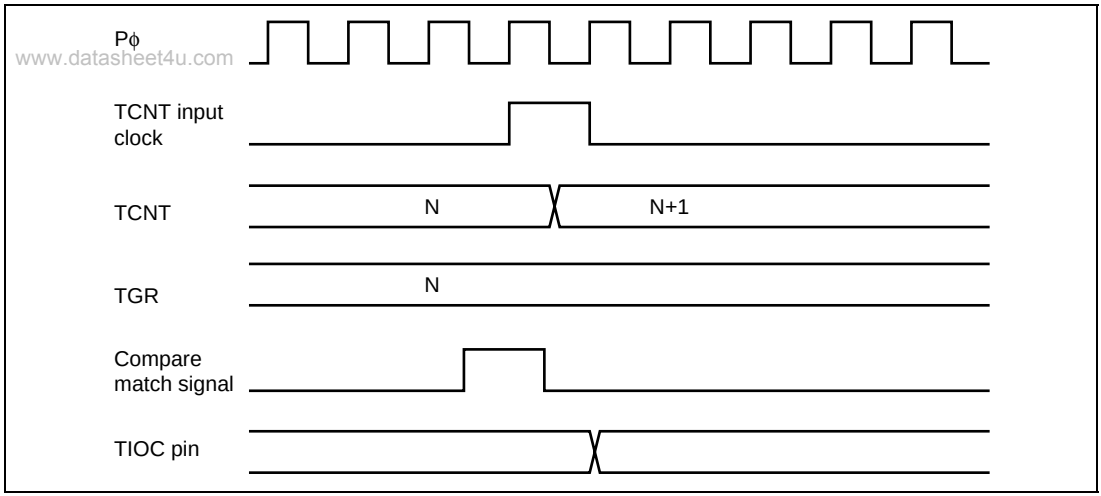


Figure 8.57 Output Compare Output Timing (Normal Mode/PWM Mode)

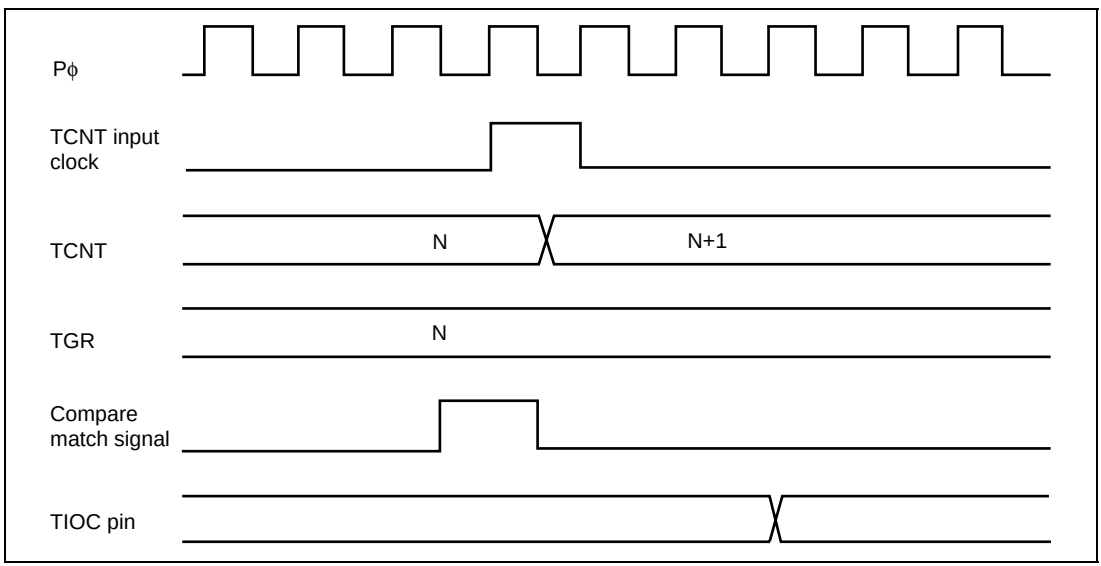


Figure 8.58 Output Compare Output Timing (Complementary PWM Mode/Reset Synchronous PWM Mode)

Input Capture Signal Timing: Figure 8.59 shows input capture signal timing.

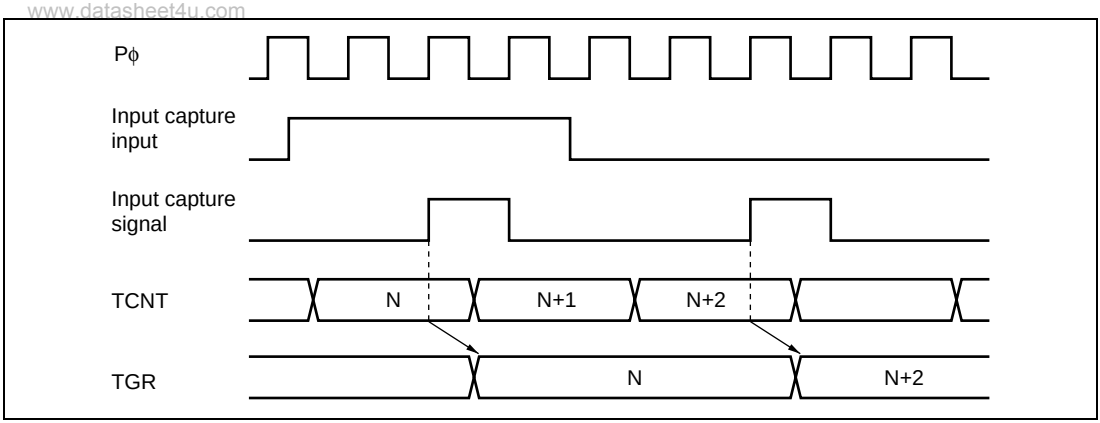


Figure 8.59 Input Capture Input Signal Timing

Timing for Counter Clearing by Compare Match/Input Capture: Figure 8.60 shows the timing when counter clearing on compare match is specified, and figure 8.61 shows the timing when counter clearing on input capture is specified.

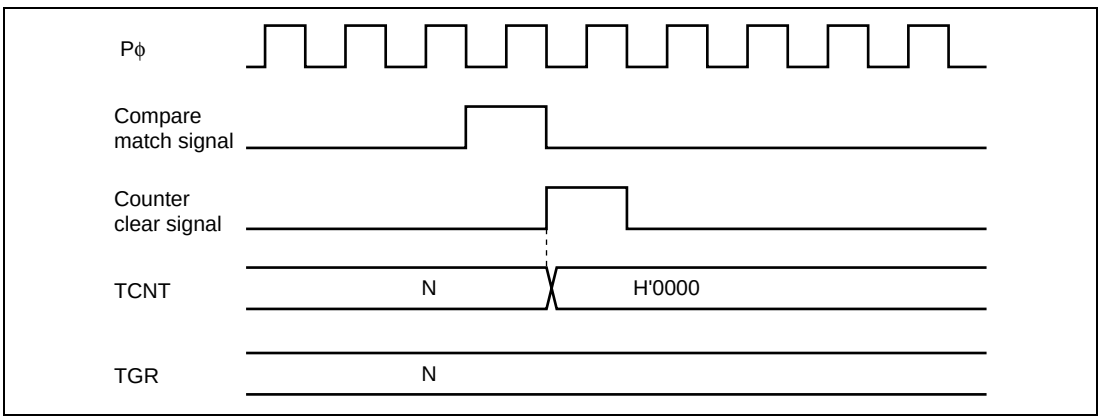


Figure 8.60 Counter Clear Timing (Compare Match)

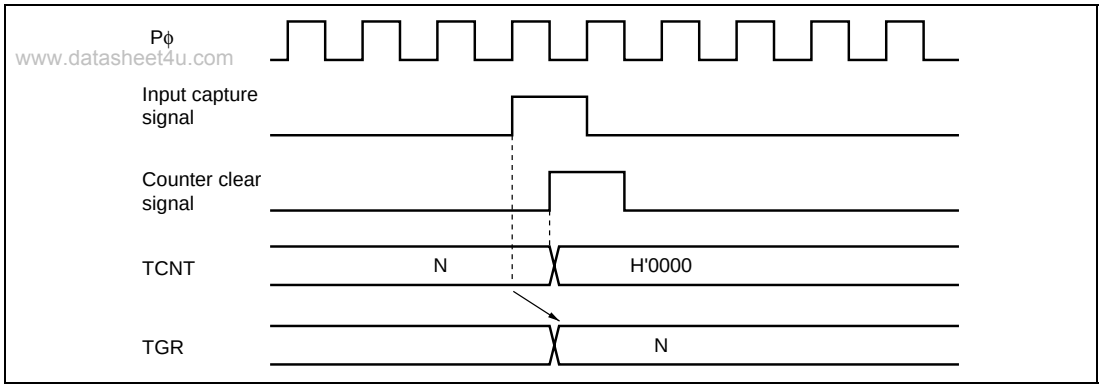


Figure 8.61 Counter Clear Timing (Input Capture)

Buffer Operation Timing: Figures 8.62 and 8.63 show the timing in buffer operation.

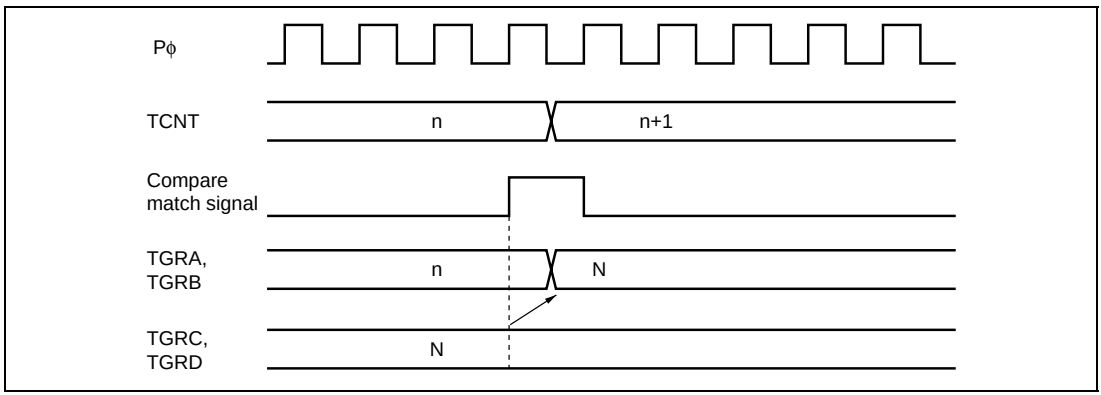


Figure 8.62 Buffer Operation Timing (Compare Match)

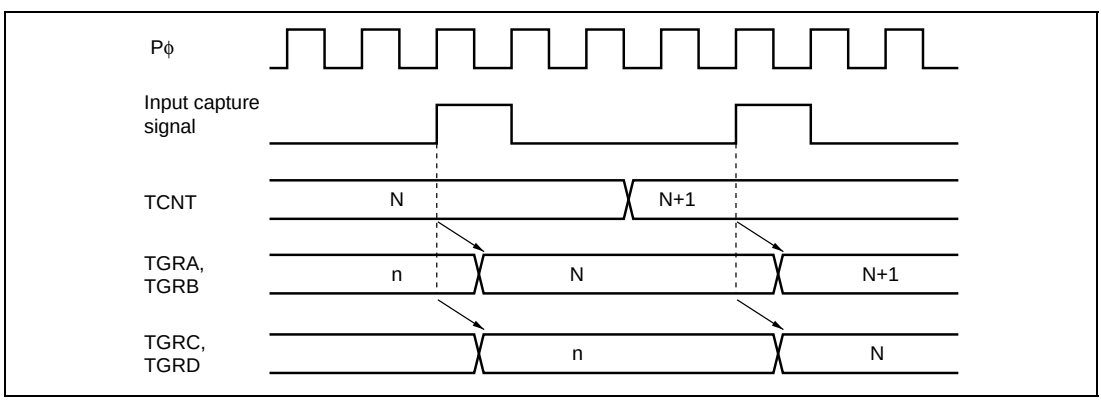


Figure 8.63 Buffer Operation Timing (Input Capture)

8.6.2 Interrupt Signal Timing

TGF Flag Setting Timing in Case of Compare Match: Figure 8.64 shows the timing for setting of the TGF flag in TSR on compare match, and TGI interrupt request signal timing.

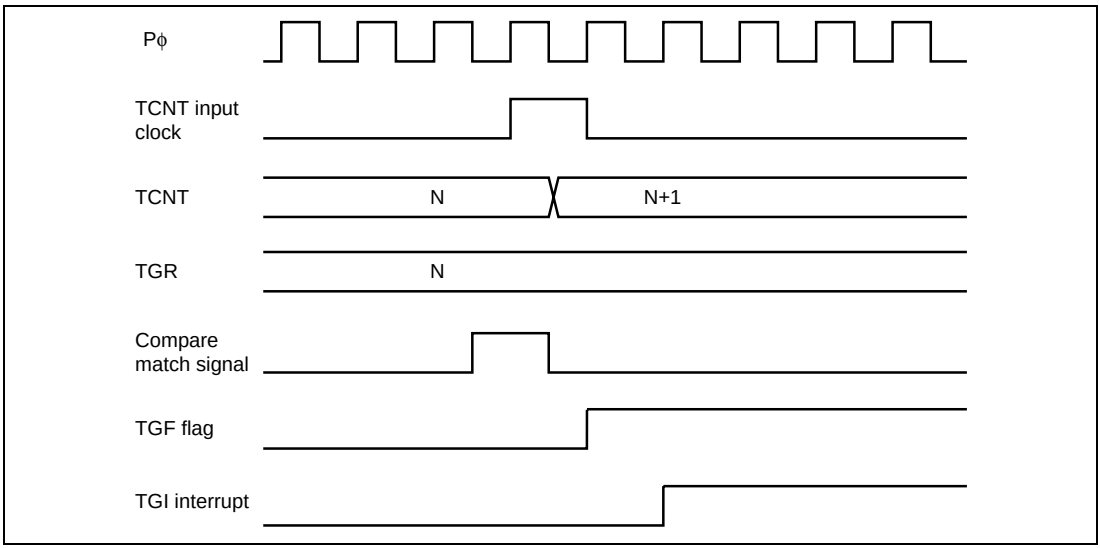


Figure 8.64 TGI Interrupt Timing (Compare Match)

TGF Flag Setting Timing in Case of Input Capture: Figure 8.65 shows the timing for setting of the TGF flag in TSR on input capture, and TGI interrupt request signal timing.

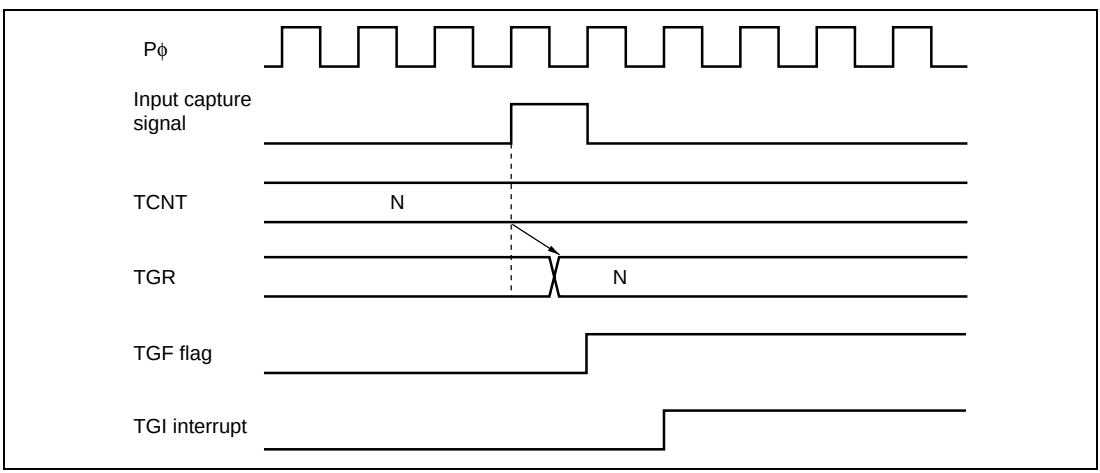


Figure 8.65 TGI Interrupt Timing (Input Capture)

TCFV Flag/TCFU Flag Setting Timing: Figure 8.66 shows the timing for setting of the TCFV flag in TSR on overflow, and TCIV interrupt request signal timing.

Figure 8.67 shows the timing for setting of the TCFU flag in TSR on underflow, and TCIU interrupt request signal timing.

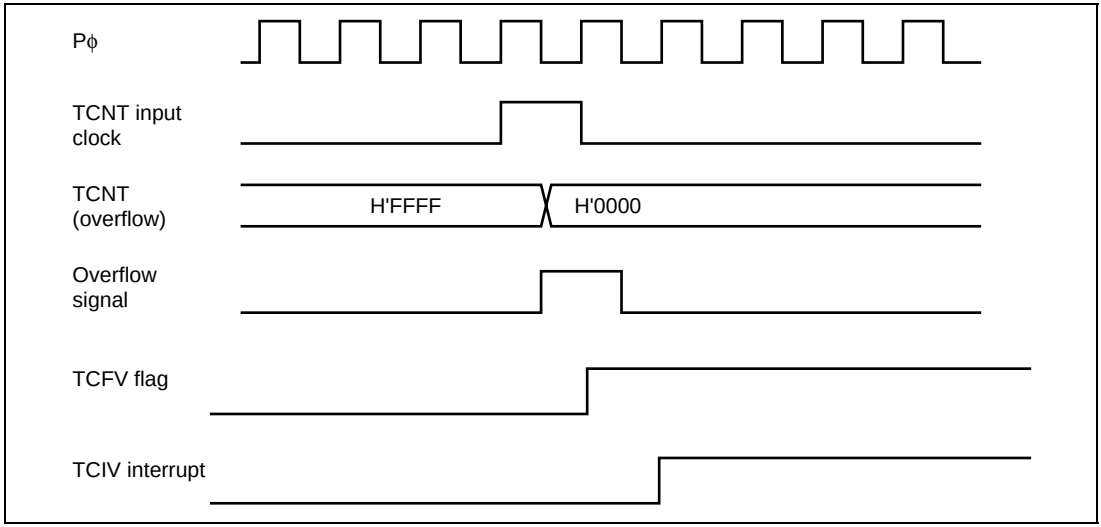


Figure 8.66 TCIV Interrupt Setting Timing

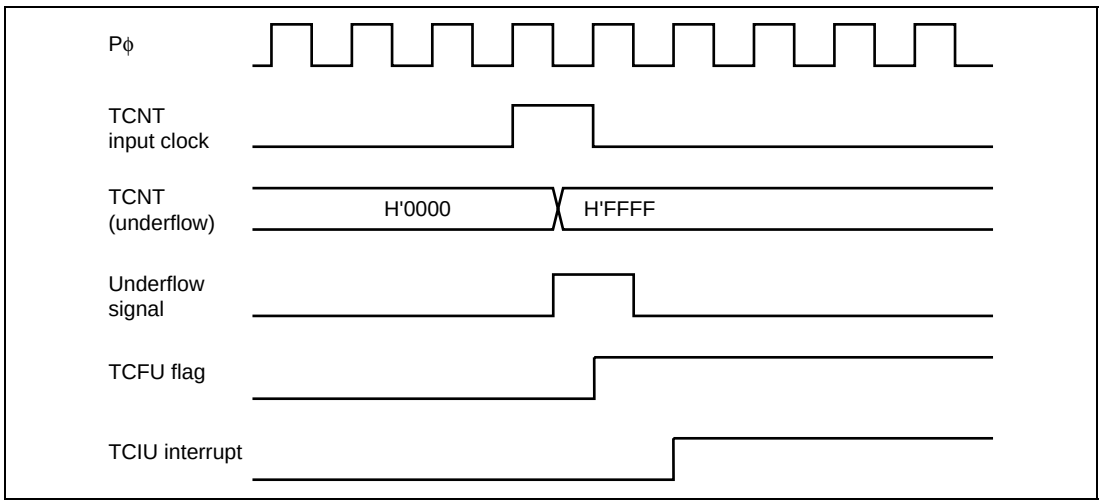


Figure 8.67 TCIU Interrupt Setting Timing

Status Flag Clearing Timing: After a status flag is read as 1 by the CPU, it is cleared by writing 0 to it. When the DTC is activated, the flag is cleared automatically. Figure 8.68 shows the timing for status flag clearing by the CPU.

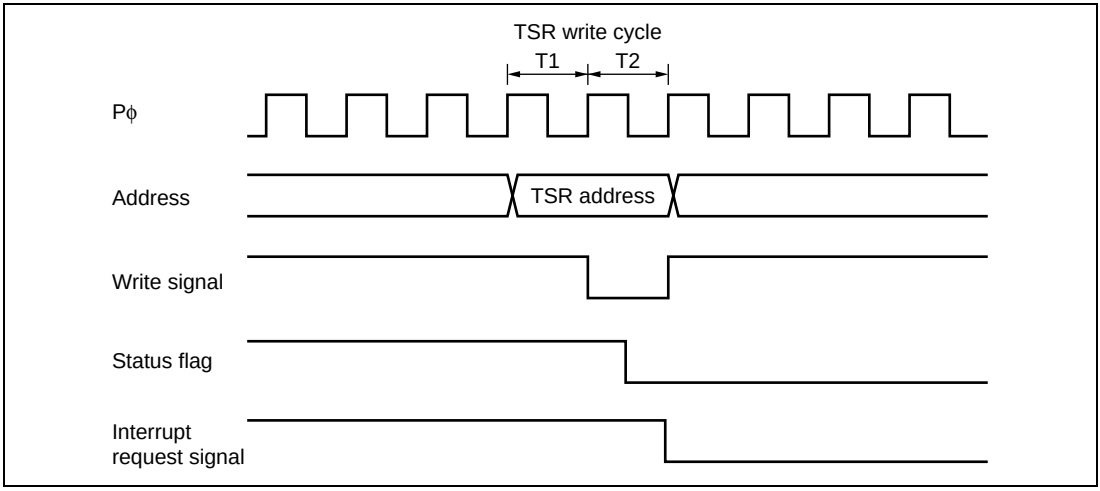


Figure 8.68 Timing for Status Flag Clearing by the CPU

8.7 Usage Notes

8.7.1 Module Standby Mode Setting

MTU operation can be disabled or enabled using the module standby register. The initial setting is for MTU operation to be halted. Register access is enabled by clearing module standby mode. For details, refer to section 18, Power-Down Modes.

8.7.2 Input Clock Restrictions

The input clock pulse width must be at least 1.5 states in the case of single-edge detection, and at least 2.5 states in the case of both-edge detection. The TPU will not operate properly at narrower pulse widths.

In phase counting mode, the phase difference and overlap between the two input clocks must be at least 1.5 states, and the pulse width must be at least 2.5 states. Figure 8.69 shows the input clock conditions in phase counting mode.

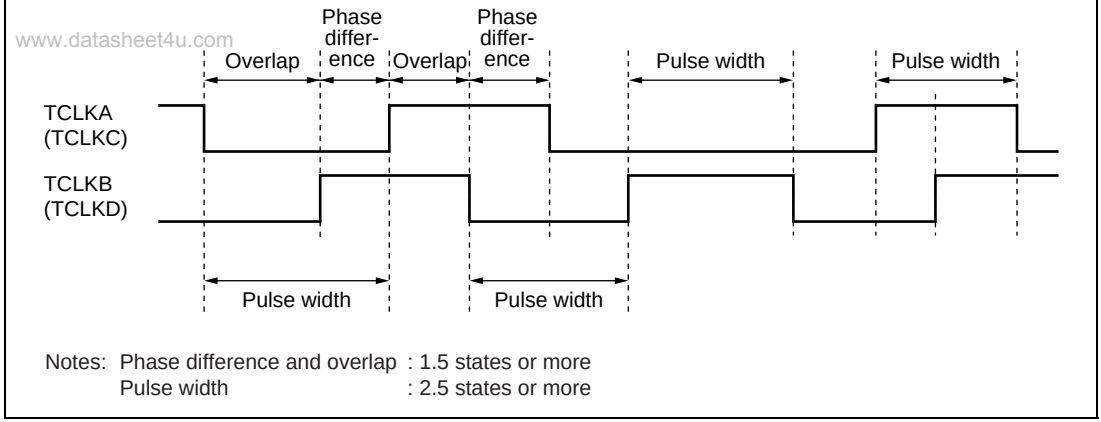


Figure 8.69 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

8.7.3 Caution on Period Setting

When counter clearing on compare match is set, TCNT is cleared in the final state in which it matches the TGR value (the point at which the count value matched by TCNT is updated). Consequently, the actual counter frequency is given by the following formula:

$$f = \frac{P\phi}{(N + 1)}$$

Where f : Counter frequency
Pϕ : Peripheral clock operating frequency
N : TGR set value

8.7.4 Contention between TCNT Write and Clear Operations

If the counter clear signal is generated in the T2 state of a TCNT write cycle, TCNT clearing takes precedence and the TCNT write is not performed.

Figure 8.70 shows the timing in this case.

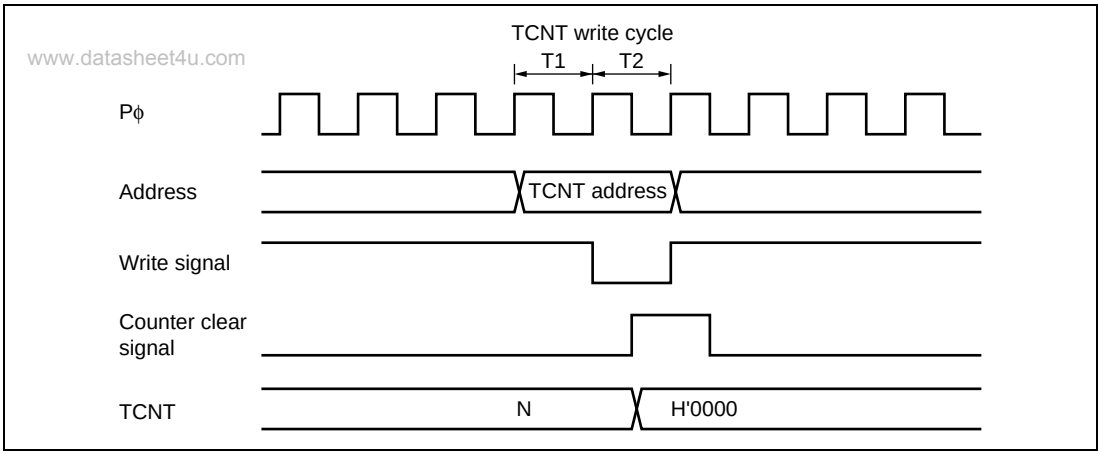


Figure 8.70 Contention between TCNT Write and Clear Operations

8.7.5 Contention between TCNT Write and Increment Operations

If incrementing occurs in the T2 state of a TCNT write cycle, the TCNT write takes precedence and TCNT is not incremented.

Figure 8.71 shows the timing in this case.

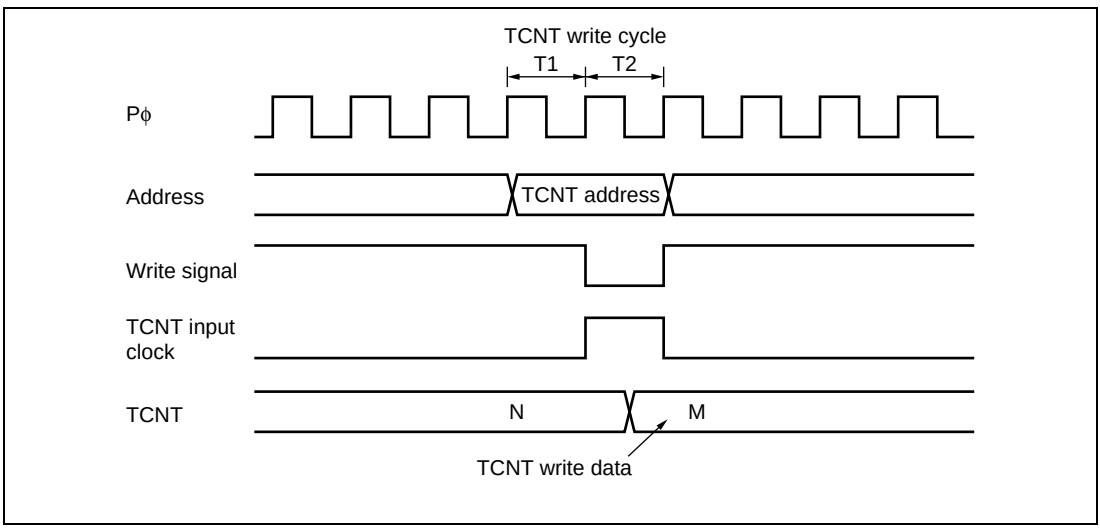


Figure 8.71 Contention between TCNT Write and Increment Operations

8.7.6 Contention between TGR Write and Compare Match

When a compare match occurs in the T2 state of a TGR write cycle, the TGR write is executed and the compare match signal is generated.

Figure 8.72 shows the timing in this case.

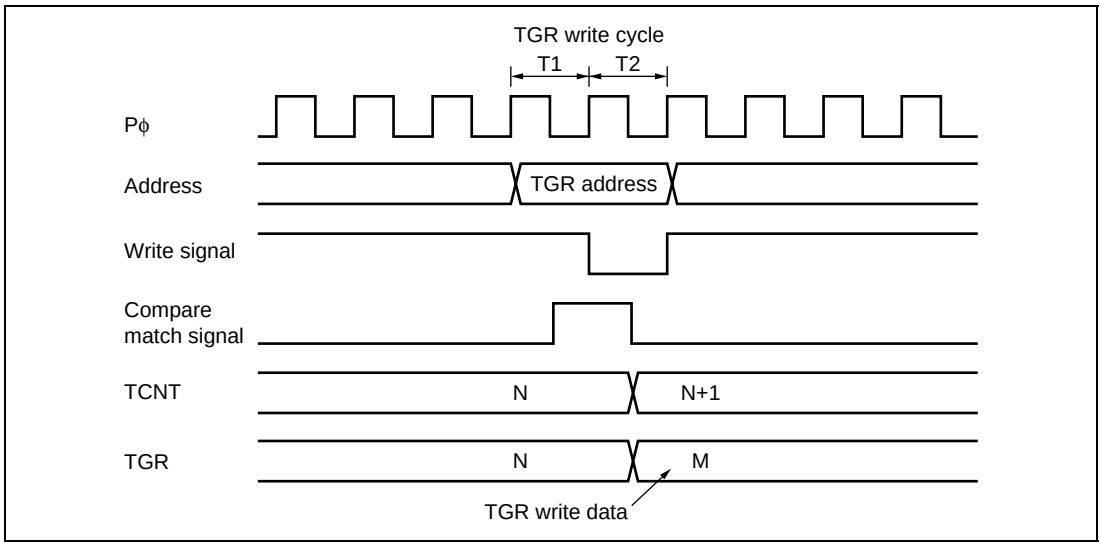


Figure 8.72 Contention between TGR Write and Compare Match

8.7.7 Contention between Buffer Register Write and Compare Match

If a compare match occurs in the T2 state of a TGR write cycle, the data that is transferred to TGR by the buffer operation differs depending on channel 0 and channels 3 and 4: data on channel 0 is that after write, and on channels 3 and 4, before write.

Figures 8.73 and 8.74 show the timing in this case.

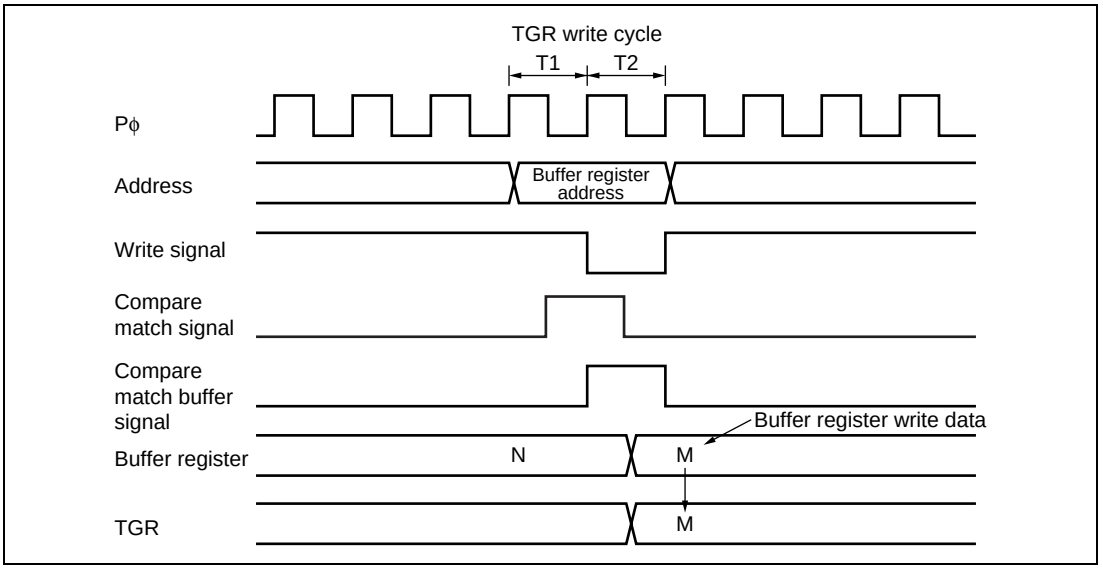


Figure 8.73 Contention between Buffer Register Write and Compare Match (Channel 0)

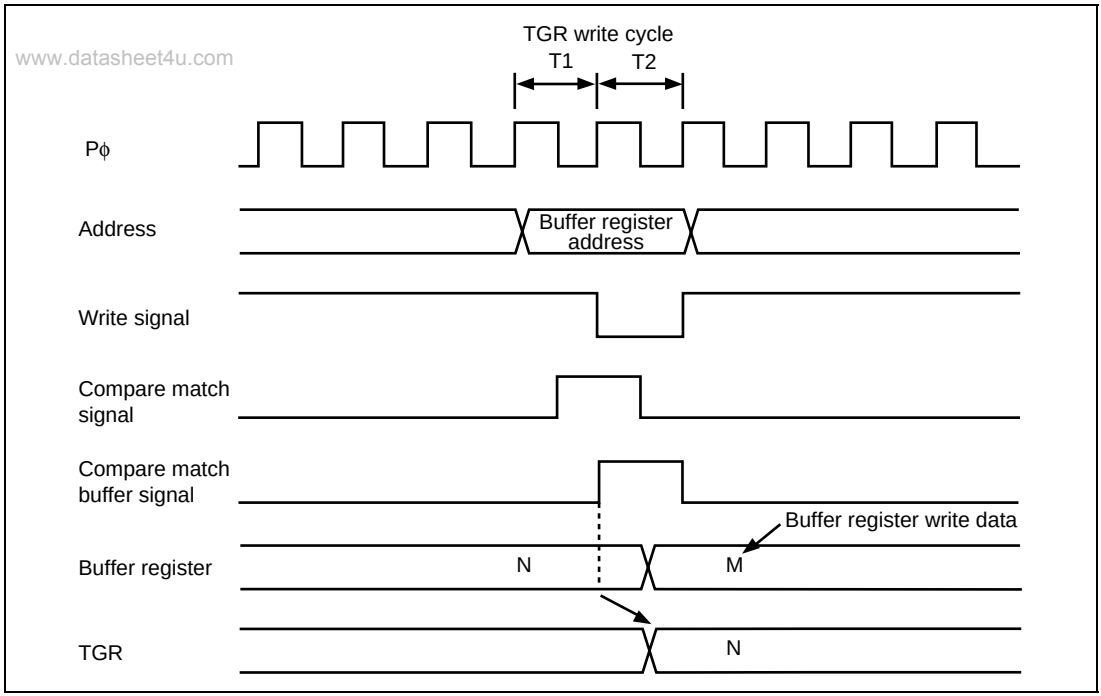


Figure 8.74 Contention between Buffer Register Write and Compare Match (Channels 3 and 4)

8.7.8 Contention between TGR Read and Input Capture

If an input capture signal is generated in the T1 state of a TGR read cycle, the data that is read will be that in the buffer after input capture transfer.

Figure 8.75 shows the timing in this case.

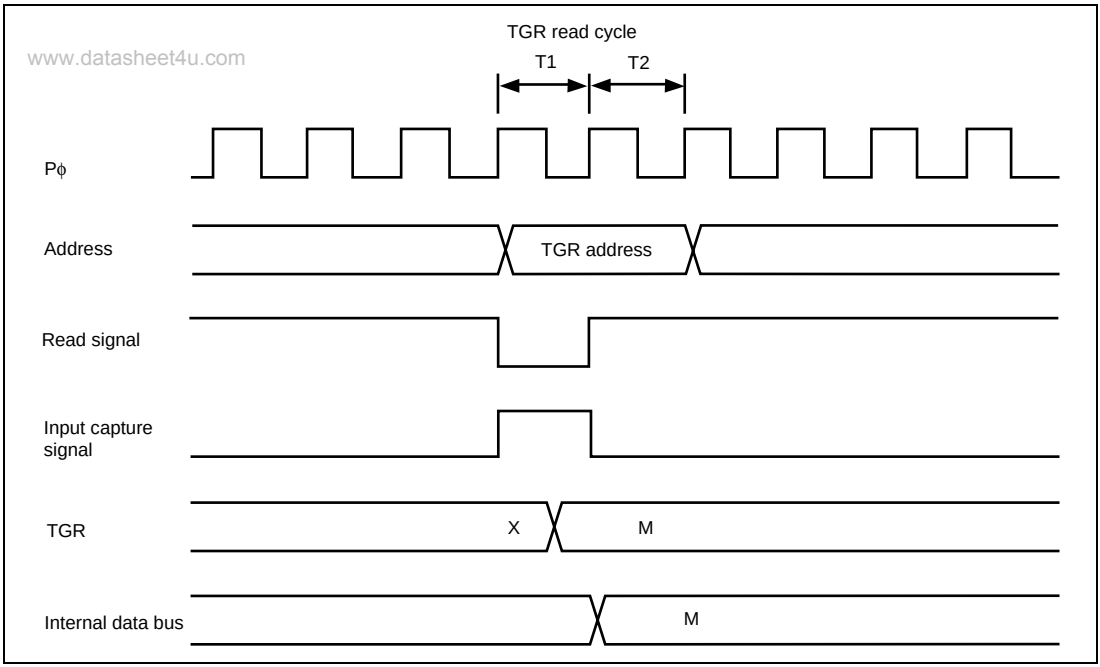


Figure 8.75 Contention between TGR Read and Input Capture

8.7.9 Contention between TGR Write and Input Capture

If an input capture signal is generated in the T2 state of a TGR write cycle, the input capture operation takes precedence and the write to TGR is not performed.

Figure 8.76 shows the timing in this case.

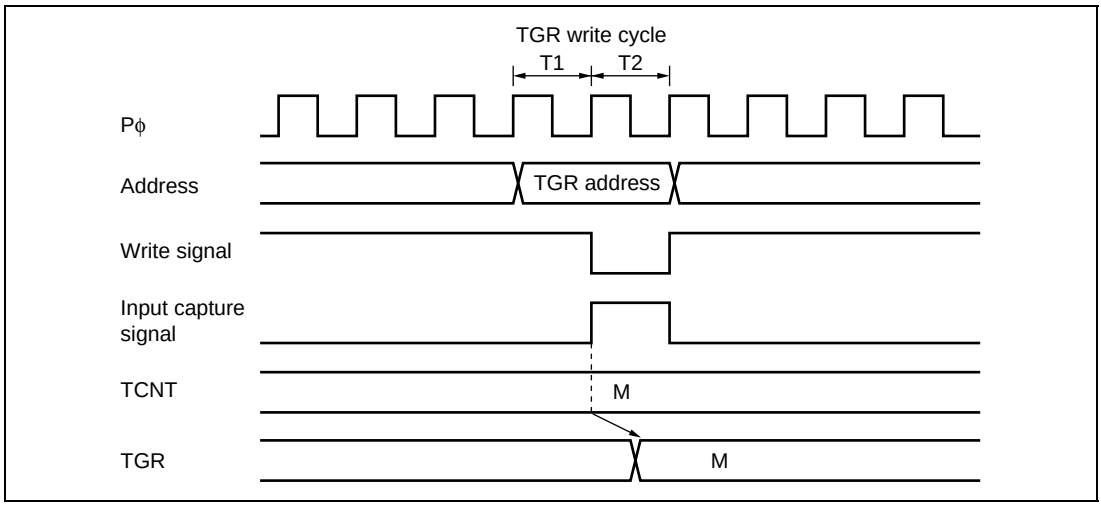


Figure 8.76 Contention between TGR Write and Input Capture

8.7.10 Contention between Buffer Register Write and Input Capture

If an input capture signal is generated in the T2 state of a buffer register write cycle, the buffer operation takes precedence and the write to the buffer register is not performed.

Figure 8.77 shows the timing in this case.

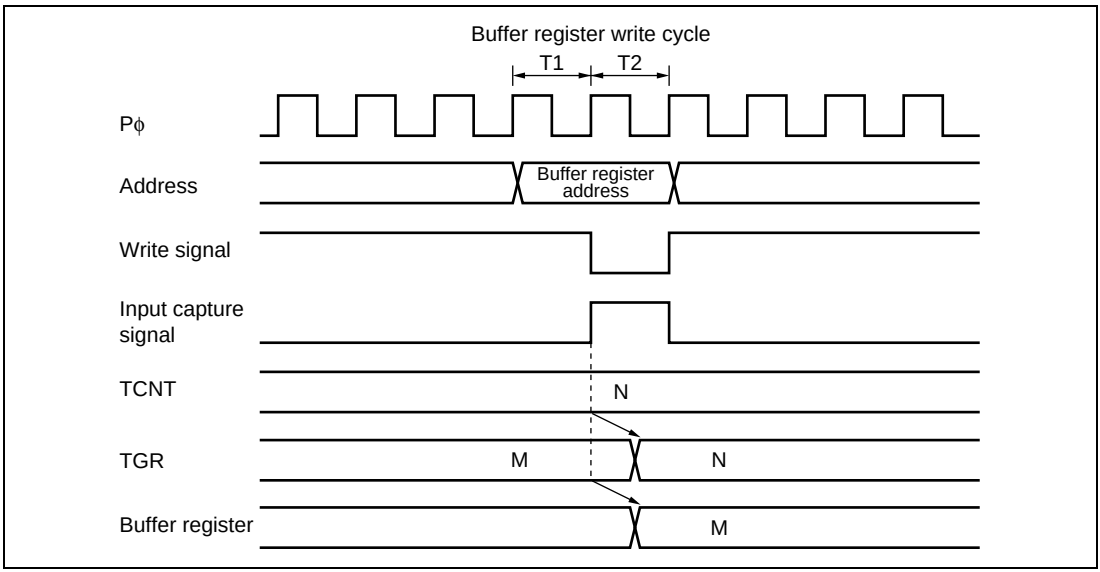


Figure 8.77 Contention between Buffer Register Write and Input Capture

8.7.11 TCNT2 Write and Overflow/Underflow Contention in Cascade Connection

With timer counters TCNT1 and TCNT2 in a cascade connection, when a contention occurs during TCNT_1 count (during a TCNT_2 overflow/underflow) in the T2 state of the TCNT_2 write cycle, the write to TCNT_2 is conducted, and the TCNT_1 count signal is disabled. At this point, if there is match with TGRA_1 and the TCNT_1 value, a compare signal is issued. Furthermore, when the TCNT_1 count clock is selected as the input capture source of channel 0, TGRA_0 to D_0 carry out the input capture operation. In addition, when the compare match/input capture is selected as the input capture source of TGRB_1, TGRB_1 carries out input capture operation. The timing is shown in figure 8.78.

For cascade connections, be sure to synchronize settings for channels 1 and 2 when setting TCNT clearing.

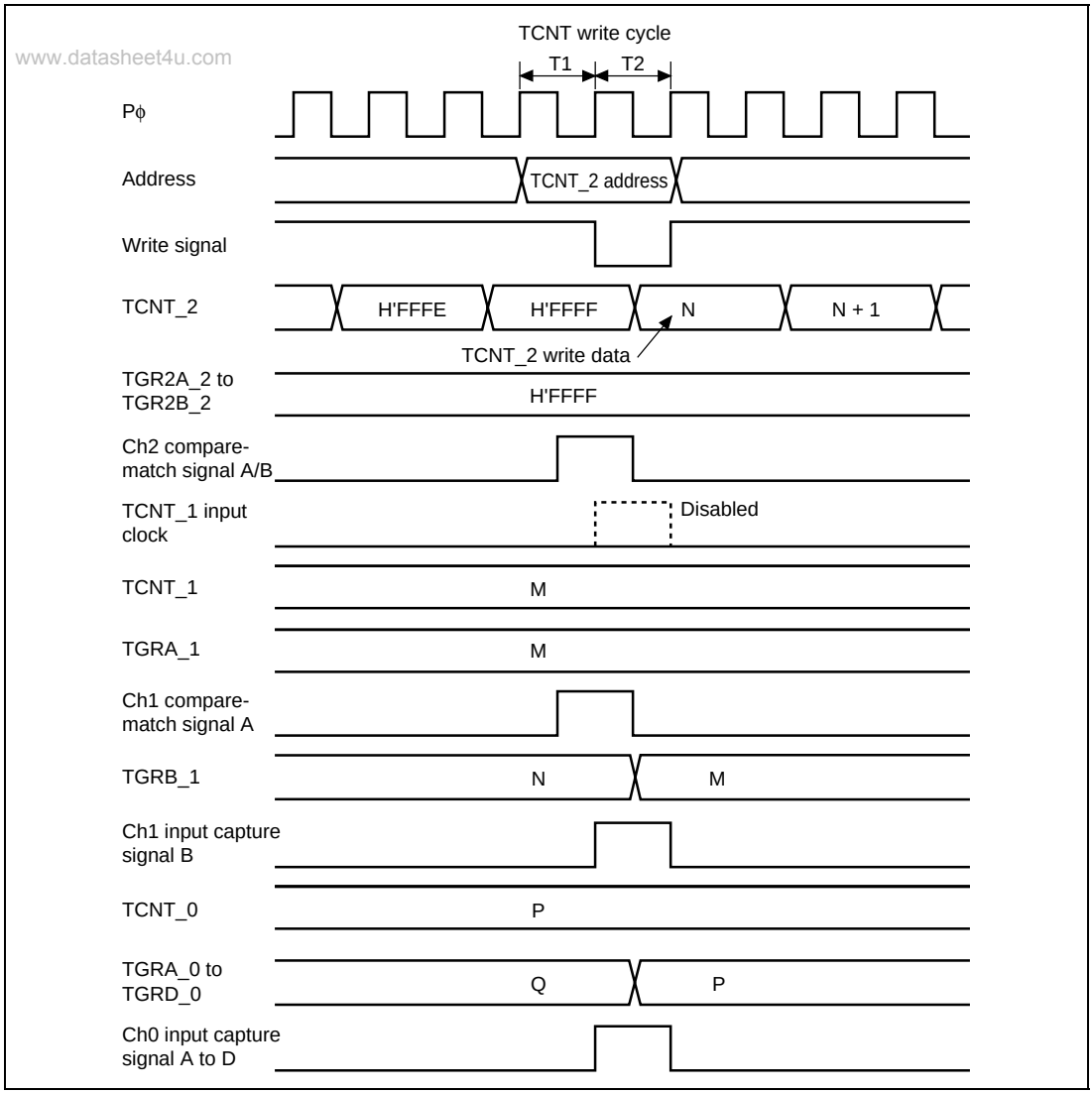


Figure 8.78 TCNT_2 Write and Overflow/Underflow Contention with Cascade Connection

8.7.12 Counter Value during Complementary PWM Mode Stop

When counting operation is stopped with TCNT_3 and TCNT_4 in complementary PWM mode, TCNT_3 has the timer dead time register (TDDR) value, and TCNT_4 is set to H'0000.

When restarting complementary PWM mode, counting begins automatically from the initialized state. This explanatory diagram is shown in figure 8.79.

When counting begins in another operating mode, be sure that TCNT_3 and TCNT_4 are set to the initial values.

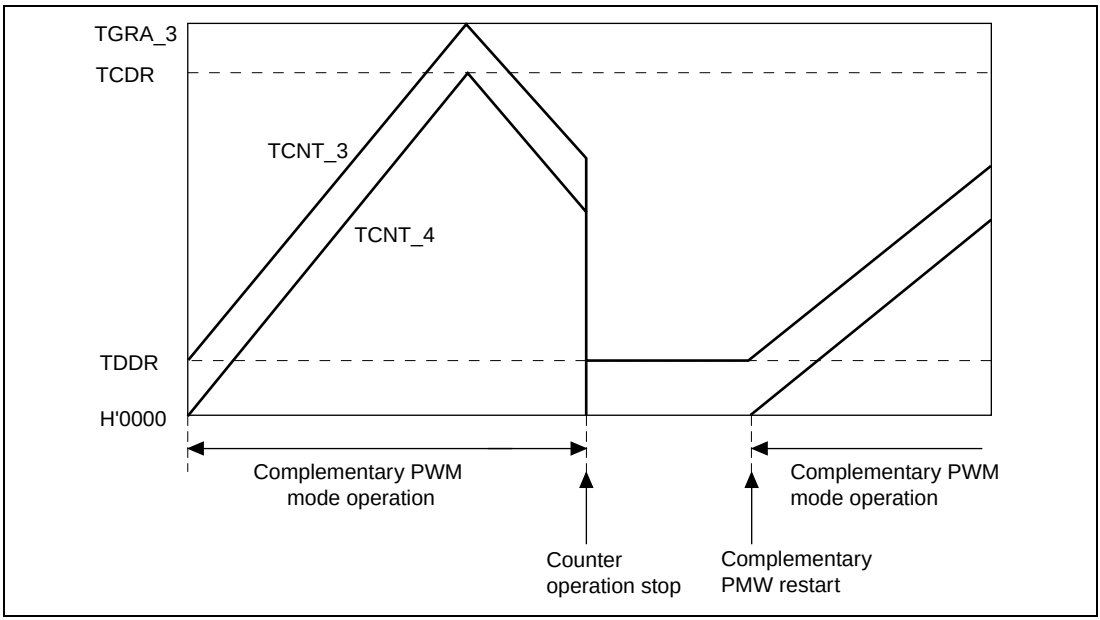


Figure 8.79 Counter Value during Complementary PWM Mode Stop

8.7.13 Buffer Operation Setting in Complementary PWM Mode

In complementary PWM mode, conduct rewrites by buffer operation for the PWM cycle setting register (TGRA_3), timer cycle data register (TCDR), and duty cycle setting registers (TGRB_3, TRGA_4, and TGRB_4).

In complementary PWM mode, channel 3 and channel 4 buffers operate in accordance with bit settings BFA and BFB of TMDR_3. When TMDR_3's BFA bit is set to 1, TGRC_3 functions as a buffer register for TGRA_3. At the same time, TGRC_4 functions as the buffer register for TRGA_4, while the TCBR functions as the TCDR's buffer register.

8.7.14 Reset Sync PWM Mode Buffer Operation and Compare Match Flag

When setting buffer operation for reset sync PWM mode, set the BFA and BFB bits of TMDR_4 to 0. The TIOC4C pin will be unable to produce its waveform output if the BFA bit of TMDR_4 is set to 1.

In reset sync PWM mode, the channel 3 and channel 4 buffers operate in accordance with the BFA and BFB bit settings of TMDR_3. For example, if the BFA bit of TMDR_3 is set to 1, TGRC_3

functions as the buffer register for TGRA_3. At the same time, TGRC_4 functions as the buffer register for TRGA_4.

The TGFC bit and TGFD bit of TSR_3 and TSR_4 are not set when TGRC_3 and TGRD_3 are operating as buffer registers.

Figure 8.80 shows an example of operations for TGR_3, TGR_4, TIOC3, and TIOC4, with TMDR_3's BFA and BFB bits set to 1, and TMDR_4's BFA and BFB bits set to 0.

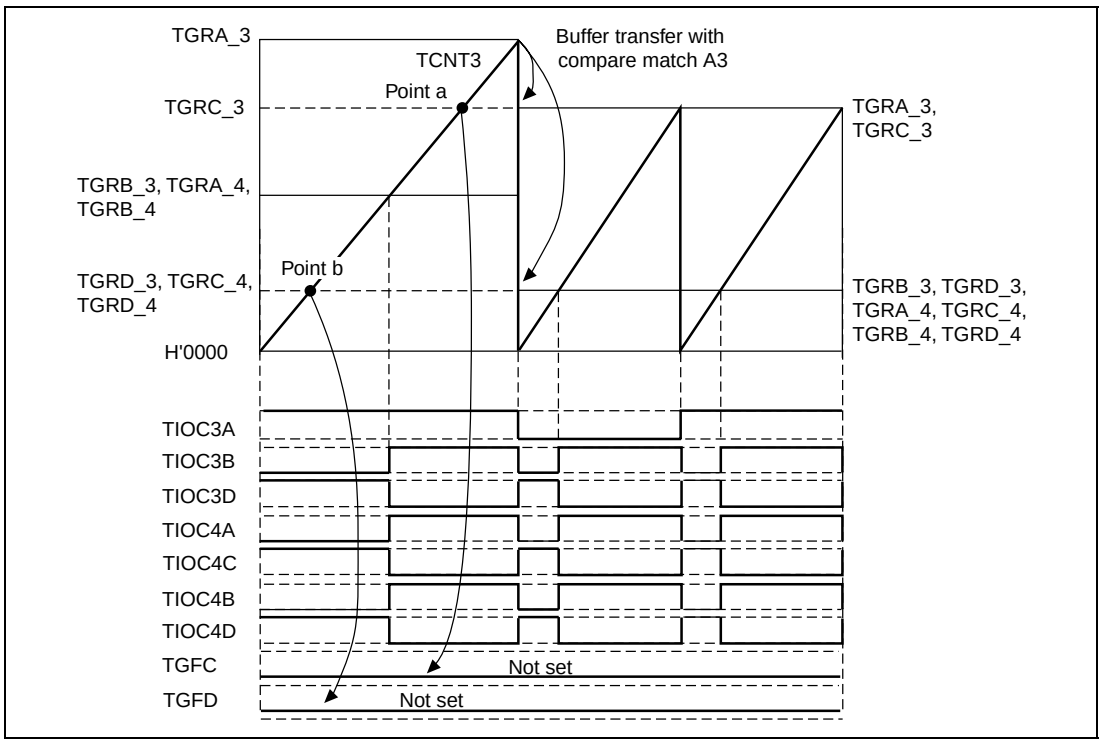


Figure 8.80 Buffer Operation and Compare-Match Flags in Reset Sync PWM Mode

8.7.15 Overflow Flags in Reset Sync PWM Mode

When set to reset sync PWM mode, TCNT_3 and TCNT_4 start counting when the CST3 bit of TSTR is set to 1. At this point, TCNT_4's count clock source and count edge obey the TCR_3 setting.

In reset sync PWM mode, with cycle register TGRA_3's set value at H'FFFF, when specifying TGR3A compare-match for the counter clear source, TCNT_3 and TCNT_4 count up to H'FFFF,

then a compare-match occurs with TGRA_3, and TCNT_3 and TCNT_4 are both cleared. At this point, TSR's overflow flag TCFV bit is not set.

Figure 8.81 shows a TCFV bit operation example in reset sync PWM mode with a set value for cycle register TGRA_3 of H'FFFF, when a TGRA_3 compare-match has been specified without synchronous setting for the counter clear source.

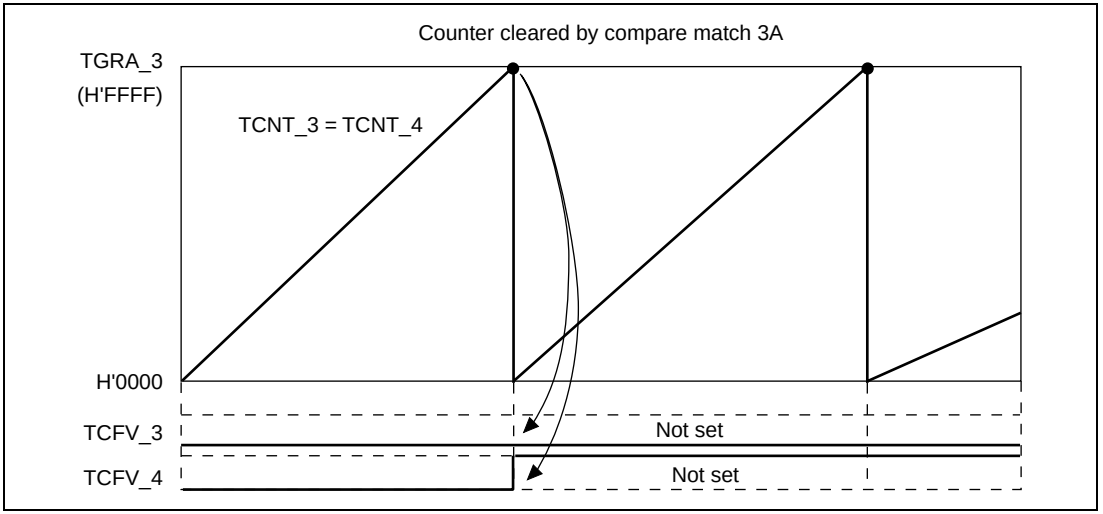


Figure 8.81 Reset Sync PWM Mode Overflow Flag

8.7.16 Contention between Overflow/Underflow and Counter Clearing

If overflow/underflow and counter clearing occur simultaneously, the TCFV/TCFU flag in TSR is not set and TCNT clearing takes precedence.

Figure 8.82 shows the operation timing when a TGR compare match is specified as the clearing source, and when H'FFFF is set in TGR.

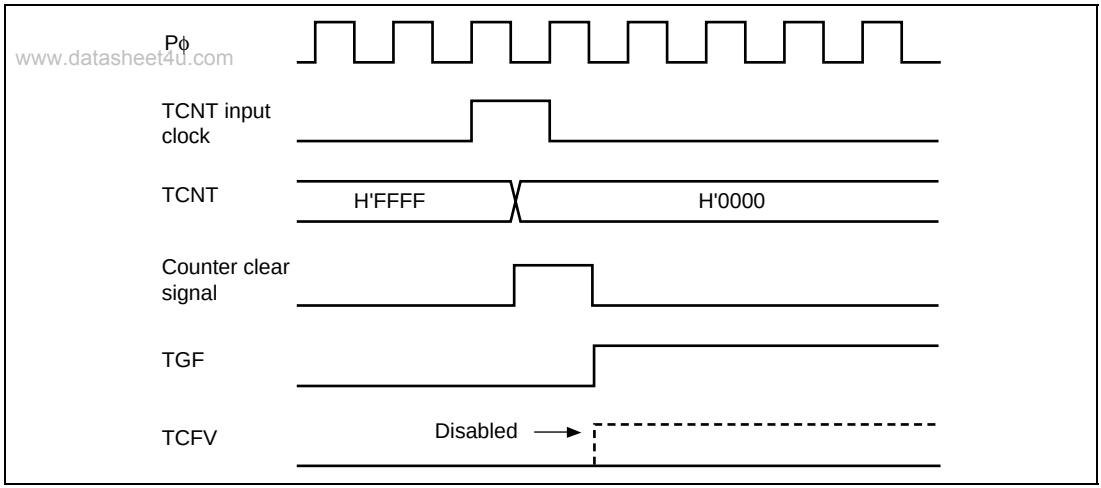


Figure 8.82 Contention between Overflow and Counter Clearing

8.7.17 Contention between TCNT Write and Overflow/Underflow

If there is an up-count or down-count in the T2 state of a TCNT write cycle, and overflow/underflow occurs, the TCNT write takes precedence and the TCFV/TCFU flag in TSR is not set.

Figure 8.83 shows the operation timing when there is contention between TCNT write and overflow.

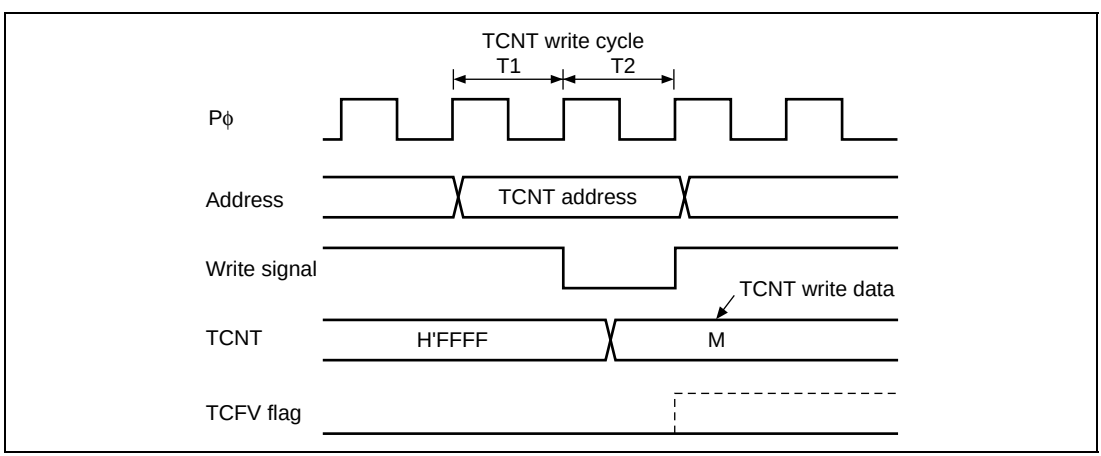


Figure 8.83 Contention between TCNT Write and Overflow

8.7.18 Cautions on Transition from Normal Operation or PWM Mode 1 to Reset-Synchronous PWM Mode

When making a transition from channel 3 or 4 normal operation or PWM mode 1 to reset-synchronous PWM mode, if the counter is halted with the output pins (TIOC3B, TIOC3D, TIOC4A, TIOC4C, TIOC4B, TIOC4D) in the high-impedance state, followed by the transition to reset-synchronous PWM mode and operation in that mode, the initial pin output will not be correct.

When making a transition from normal operation to reset-synchronous PWM mode, write H'11 to registers TIOR3H, TIOR3L, TIOR4H, and TIOR4L to initialize the output pins to low level output, then set an initial register value of H'00 before making the mode transition.

When making a transition from PWM mode 1 to reset-synchronous PWM mode, first switch to normal operation, then initialize the output pins to low level output and set an initial register value of H'00 before making the transition to reset-synchronous PWM mode.

8.7.19 Output Level in Complementary PWM Mode and Reset-Synchronous PWM Mode

When channels 3 and 4 are in complementary PWM mode or reset-synchronous PWM mode, the PWM waveform output level is set with the OLSP and OLSN bits in the timer output control register (TOCR). In the case of complementary PWM mode or reset-synchronous PWM mode, TIOR should be set to H'00.

8.7.20 Interrupts in Module Standby Mode

If module standby mode is entered when an interrupt has been requested, it will not be possible to clear the CPU interrupt source. Interrupts should therefore be disabled before entering module standby mode.

8.7.21 Simultaneous Input Capture of TCNT-1 and TCNT-2 in Cascade Connection

When cascade-connected timer counters (TCNT-1 and TCNT-2) are operated, cascade values cannot be captured even if input capture is executed simultaneously with TIOC1A or TIOC1B and TIOC2A or TIOC2B.

8.8 MTU Output Pin Initialization

8.8.1 Operating Modes

The MTU has the following six operating modes. Waveform output is possible in all of these modes.

- Normal mode (channels 0 to 4)
- PWM mode 1 (channels 0 to 4)
- PWM mode 2 (channels 0 to 2)
- Phase counting modes 1 to 4 (channels 1 and 2)
- Complementary PWM mode (channels 3 and 4)
- Reset-synchronous PWM mode (channels 3 and 4)

The MTU output pin initialization method for each of these modes is described in this section.

8.8.2 Reset Start Operation

The MTU output pins (TIOC*) are initialized low by a reset or in standby mode. Since MTU pin function selection is performed by the pin function controller (PFC), when the PFC is set, the MTU pin states at that point are output to the ports. When MTU output is selected by the PFC immediately after a reset, the MTU output initial level, low, is output directly at the port. When the active level is low, the system will operate at this point, and therefore the PFC setting should be made after initialization of the MTU output pins is completed.

Note: Channel number and port notation are substituted for *.

8.8.3 Operation in Case of Re-Setting Due to Error During Operation, Etc.

If an error occurs during MTU operation, MTU output should be cut by the system. Cutoff is performed by switching the pin output to port output with the PFC and outputting the inverse of the active level. For large-current pins, output can also be cut by hardware, using port output enable (POE). The pin initialization procedures for re-setting due to an error during operation, etc., and the procedures for restarting in a different mode after re-setting, are shown below.

The MTU has six operating modes, as stated above. There are thus 36 mode transition combinations, but some transitions are not available with certain channel and mode combinations. Possible mode transition combinations are shown in table 8.43.

Table 8.43 Mode Transition Combinations

	After					
Before	**Normal**	**PWM1**	**PWM2**	**PCM**	**CPWM**	**RPWM**
Normal	(1)	(2)	(3)	(4)	(5)	(6)
PWM1	(7)	(8)	(9)	(10)	(11)	(12)
PWM2	(13)	(14)	(15)	(16)	None	None
PCM	(17)	(18)	(19)	(20)	None	None
CPWM	(21)	(22)	None	None	(23) (24)	(25)
RPWM	(26)	(27)	None	None	(28)	(29)

Legend:
Normal: Normal mode
PWM1: PWM mode 1
PWM2: PWM mode 2
PCM: Phase counting modes 1 to 4
CPWM: Complementary PWM mode
RPWM: Reset-synchronous PWM mode

The above abbreviations are used in some places in following descriptions.

8.8.4 Overview of Initialization Procedures and Mode Transitions in Case of Error during Operation, etc.

- When making a transition to a mode (Normal, PWM1, PWM2, PCM) in which the pin output level is selected by the timer I/O control register (TIOR) setting, initialize the pins by means of a TIOR setting.
- In PWM mode 1, since a waveform is not output to the TIOC*B (TIOC *D) pin, setting TIOR will not initialize the pins. If initialization is required, carry it out in normal mode, then switch to PWM mode 1.
- In PWM mode 2, since a waveform is not output to the cycle register pin, setting TIOR will not initialize the pins. If initialization is required, carry it out in normal mode, then switch to PWM mode 2.
- In normal mode or PWM mode 2, if TGRC and TGRD operate as buffer registers, setting TIOR will not initialize the buffer register pins. If initialization is required, clear buffer mode, carry out initialization, and then set buffer mode again.
- In PWM mode 1, if either TGRC or TGRD operates as a buffer register, setting TIOR will not initialize the TGRC pin. To initialize the TGRC pin, clear buffer mode, carry out initialization, then set buffer mode again.
- When making a transition to a mode (CPWM, RPWM) in which the pin output level is selected by the timer output control register (TOCR) setting, switch to normal mode and perform initialization with TIOR, then restore TIOR to its initial value, and temporarily disable channel 3 and 4 output with the timer output master enable register (TOER). Then operate the unit in accordance with the mode setting procedure (TOCR setting, TMDR setting, TOER setting).

Pin initialization procedures are described below for the numbered combinations in table 8.43. The active level is assumed to be low.

Note: Channel number is substituted for * indicated in this article.

(1) Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in Normal Mode

Figure 8.84 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in normal mode after re-setting.

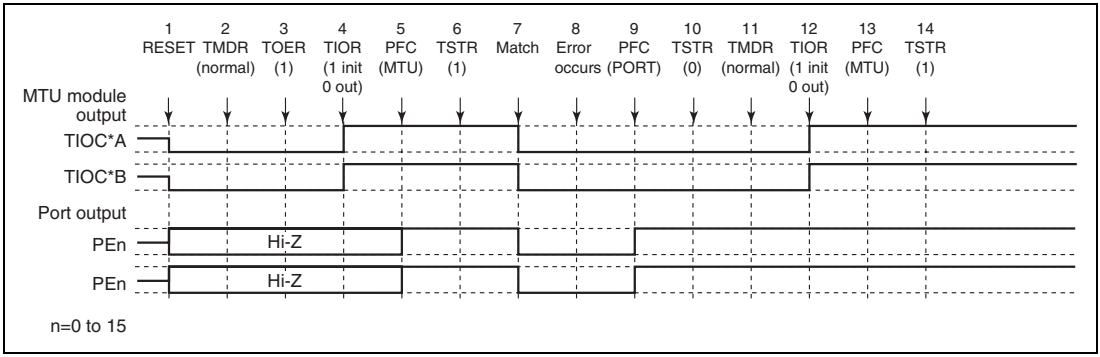


Figure 8.84 Error Occurrence in Normal Mode, Recovery in Normal Mode

1. After a reset, MTU output is low and ports are in the high-impedance state.
2. After a reset, the TMDR setting is for normal mode.
3. For channels 3 and 4, enable output with TOER before initializing the pins with TIOR.
4. Initialize the pins with TIOR. (The example shows initial high output, with low output on compare-match occurrence.)
5. Set MTU output with the PFC.
6. The count operation is started by TSTR.
7. Output goes low on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR.
11. Not necessary when restarting in normal mode.
12. Initialize the pins with TIOR.
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

(2) Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in PWM Mode 1

Figure 8.85 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in PWM mode 1 after re-setting.

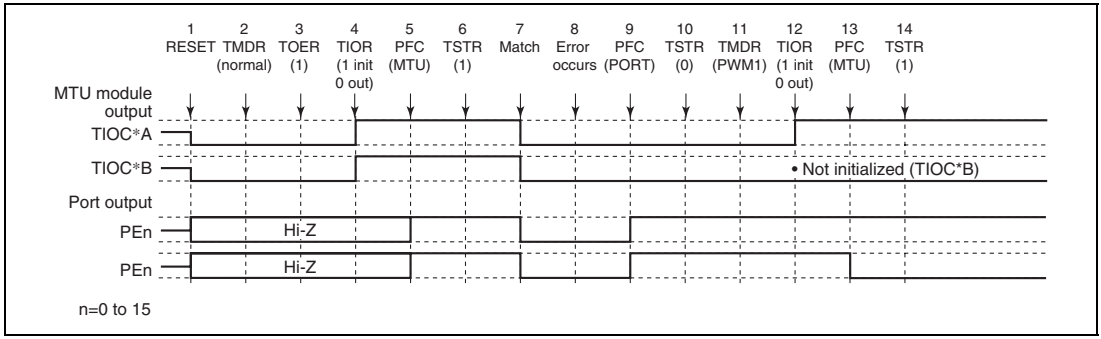


Figure 8.85 Error Occurrence in Normal Mode, Recovery in PWM Mode 1

1 to 10 are the same as in figure 8.84.

11. Set PWM mode 1.
12. Initialize the pins with TIOR. (In PWM mode 1, the TIOC*B side is not initialized. If initialization is required, initialize in normal mode, then switch to PWM mode 1.)
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

(3) Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in PWM Mode 2

Figure 8.86 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in PWM mode 2 after re-setting.

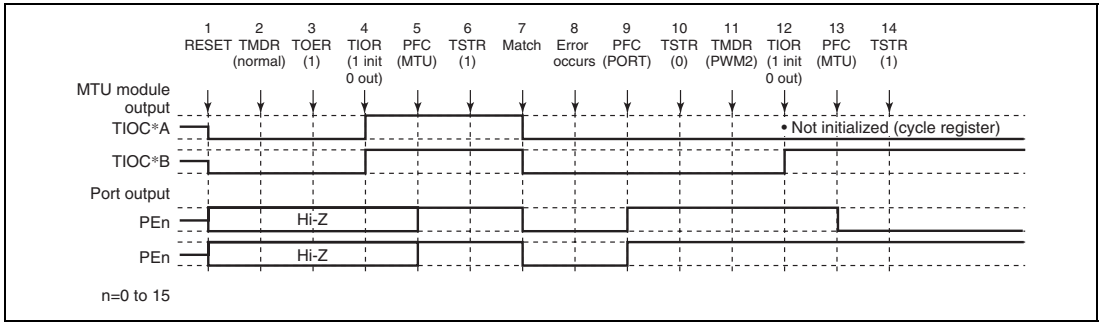


Figure 8.86 Error Occurrence in Normal Mode, Recovery in PWM Mode 2

1 to 10 are the same as in figure 8.84.

11. Set PWM mode 2.
12. Initialize the pins with TIOR. (In PWM mode 2, the cycle register pins are not initialized. If initialization is required, initialize in normal mode, then switch to PWM mode 2.)
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

Note: PWM mode 2 can only be set for channels 0 to 2, and therefore TOER setting is not necessary.

(4) Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in Phase Counting Mode

Figure 8.87 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in phase counting mode after re-setting.

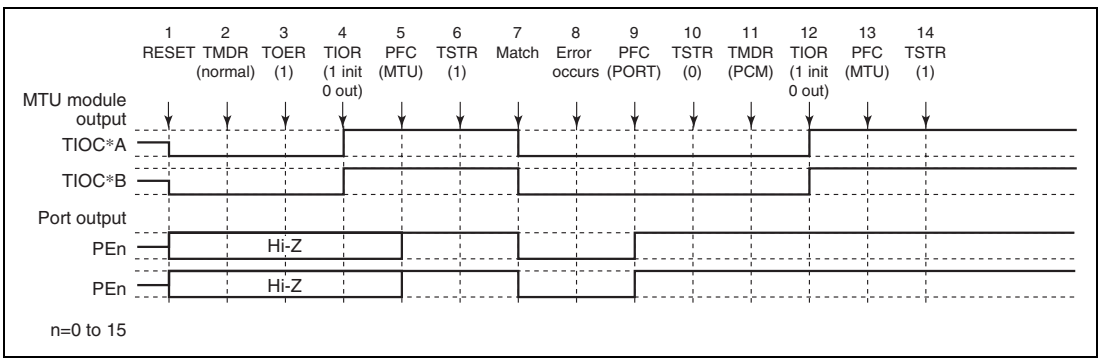


Figure 8.87 Error Occurrence in Normal Mode, Recovery in Phase Counting Mode

1 to 10 are the same as in figure 8.84.

11. Set phase counting mode.
12. Initialize the pins with TIOR.
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

Note: Phase counting mode can only be set for channels 1 and 2, and therefore TOER setting is not necessary.

(5) Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in Complementary PWM Mode

Figure 8.88 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in complementary PWM mode after re-setting.

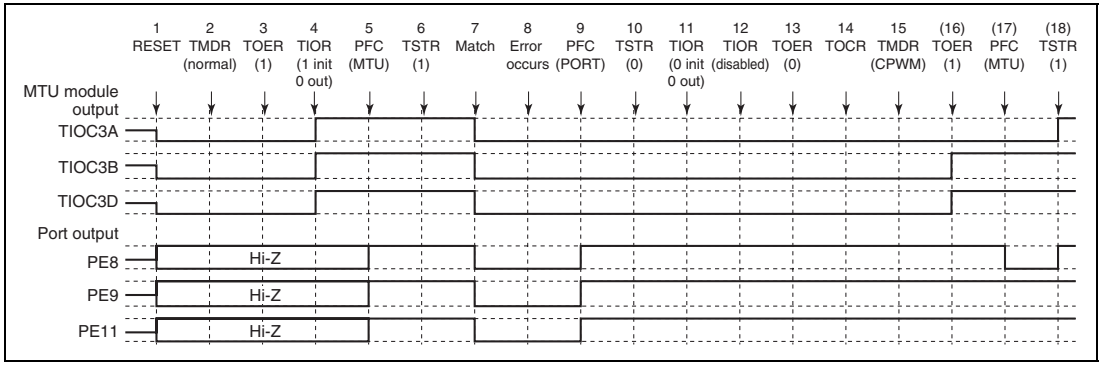


Figure 8.88 Error Occurrence in Normal Mode, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 8.84.

11. Initialize the normal mode waveform generation section with TIOR.
12. Disable operation of the normal mode waveform generation section with TIOR.
13. Disable channel 3 and 4 output with TOER.
14. Select the complementary PWM output level and cyclic output enabling/disabling with TOCR.
15. Set complementary PWM.
16. Enable channel 3 and 4 output with TOER.
17. Set MTU output with the PFC.
18. Operation is restarted by TSTR.

(6) Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in Reset-Synchronous PWM Mode

Figure 8.89 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in reset-synchronous PWM mode after re-setting.

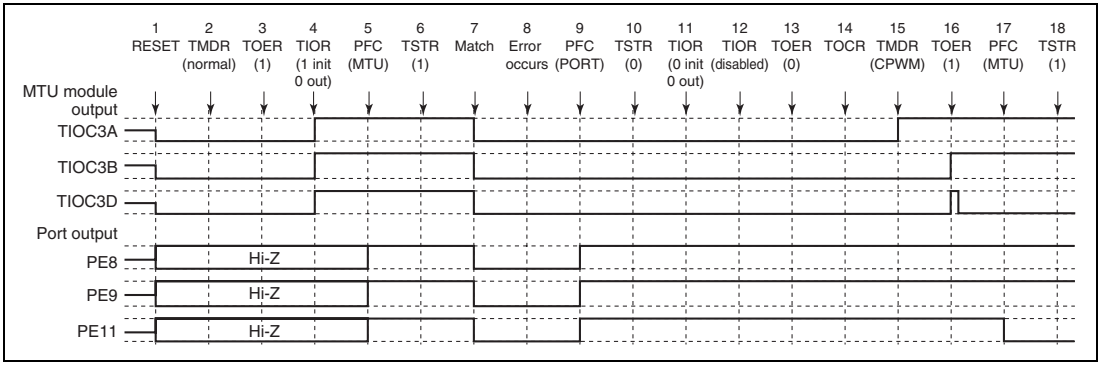


Figure 8.89 Error Occurrence in Normal Mode, Recovery in Reset-Synchronous PWM Mode

1 to 13 are the same as in figure 8.88.

14. Select the reset-synchronous PWM output level and cyclic output enabling/disabling with TOCR.
15. Set reset-synchronous PWM.
16. Enable channel 3 and 4 output with TOER.
17. Set MTU output with the PFC.
18. Operation is restarted by TSTR.

(7) Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in Normal Mode

Figure 8.90 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in normal mode after re-setting.

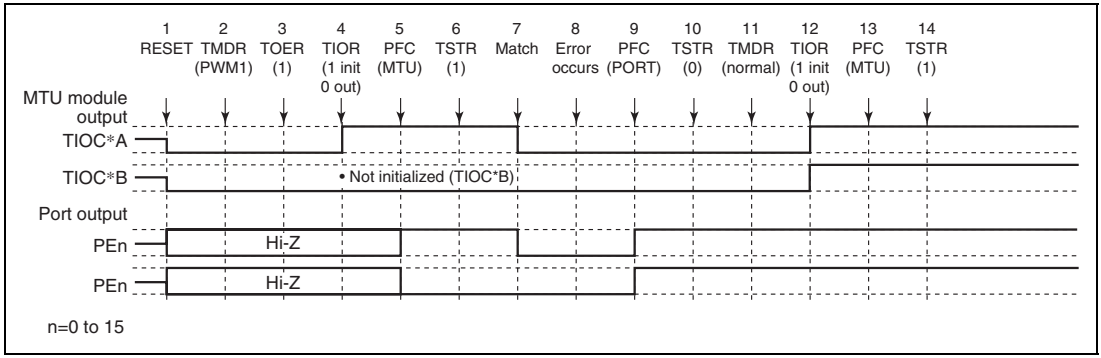


Figure 8.90 Error Occurrence in PWM Mode 1, Recovery in Normal Mode

1. After a reset, MTU output is low and ports are in the high-impedance state.
2. Set PWM mode 1.
3. For channels 3 and 4, enable output with TOER before initializing the pins with TIOR.
4. Initialize the pins with TIOR. (The example shows initial high output, with low output on compare-match occurrence. In PWM mode 1, the TIOC*B side is not initialized.)
5. Set MTU output with the PFC.
6. The count operation is started by TSTR.
7. Output goes low on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR.
11. Set normal mode.
12. Initialize the pins with TIOR.
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

(8) Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in PWM Mode 1

Figure 8.91 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in PWM mode 1 after re-setting.

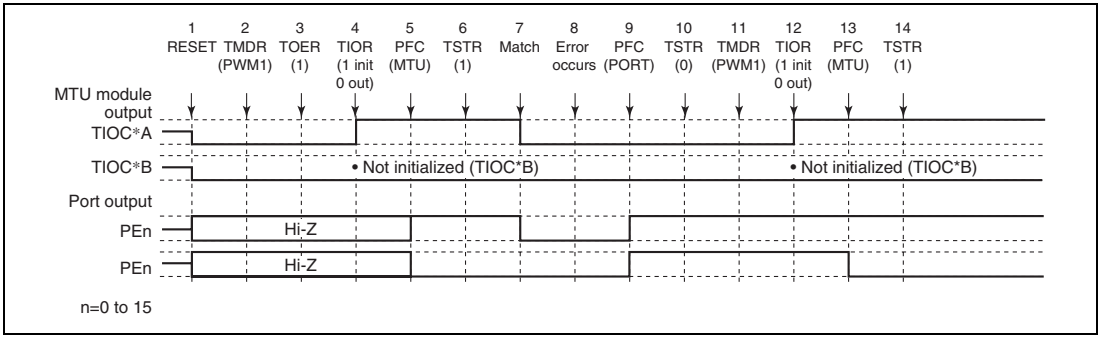


Figure 8.91 Error Occurrence in PWM Mode 1, Recovery in PWM Mode 1

1 to 10 are the same as in figure 8.90.

11. Not necessary when restarting in PWM mode 1.
12. Initialize the pins with TIOR. (In PWM mode 1, the TIOC*B side is not initialized.)
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

(9) Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in PWM Mode 2

Figure 8.92 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in PWM mode 2 after re-setting.

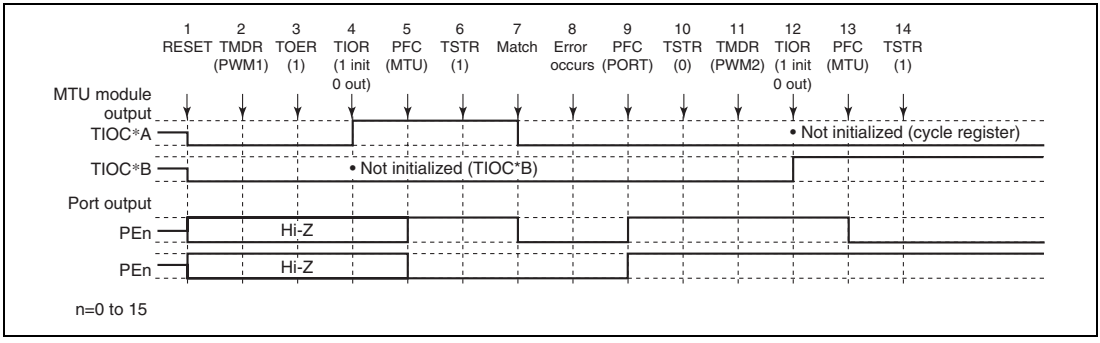


Figure 8.92 Error Occurrence in PWM Mode 1, Recovery in PWM Mode 2

1 to 10 are the same as in figure 8.90.

11. Set PWM mode 2.
12. Initialize the pins with TIOR. (In PWM mode 2, the cycle register pins are not initialized.)
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

Note: PWM mode 2 can only be set for channels 0 to 2, and therefore TOER setting is not necessary.

(10) Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in Phase Counting Mode

Figure 8.93 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in phase counting mode after re-setting.

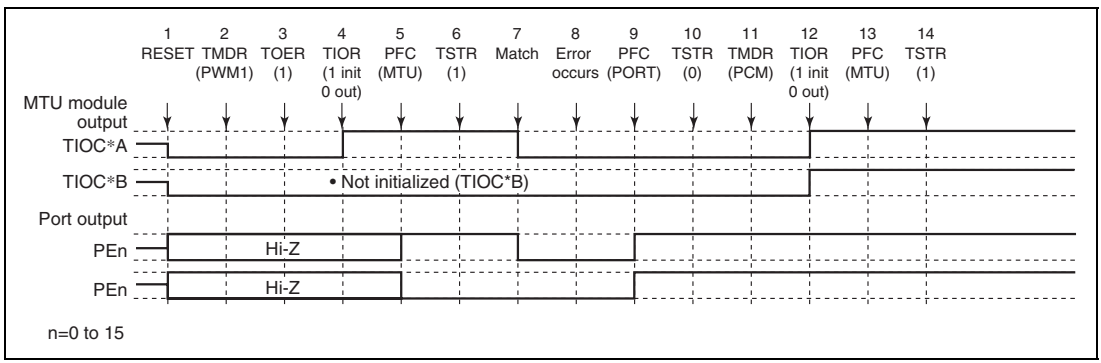


Figure 8.93 Error Occurrence in PWM Mode 1, Recovery in Phase Counting Mode

1 to 10 are the same as in figure 8.90.

11. Set phase counting mode.
12. Initialize the pins with TIOR.
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

Note: Phase counting mode can only be set for channels 1 and 2, and therefore TOER setting is not necessary.

(11) Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in Complementary PWM Mode

Figure 8.94 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in complementary PWM mode after re-setting.

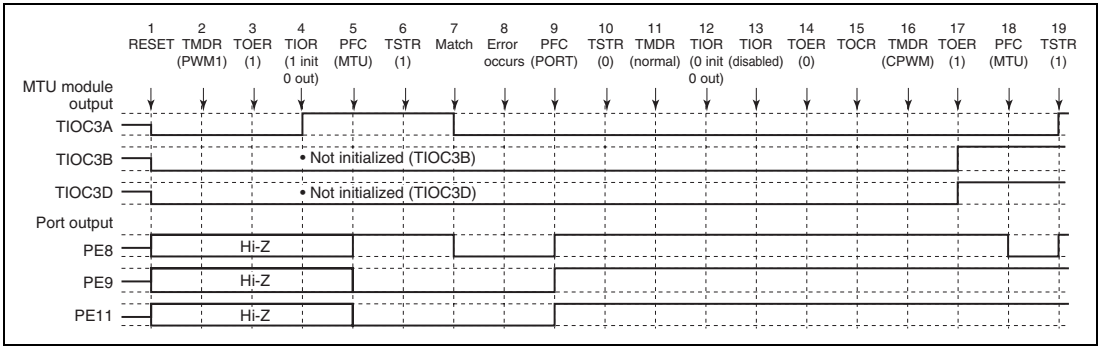


Figure 8.94 Error Occurrence in PWM Mode 1, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 8.90.

11. Set normal mode for initialization of the normal mode waveform generation section.
12. Initialize the PWM mode 1 waveform generation section with TIOR.
13. Disable operation of the PWM mode 1 waveform generation section with TIOR.
14. Disable channel 3 and 4 output with TOER.
15. Select the complementary PWM output level and cyclic output enabling/disabling with TOCR.
16. Set complementary PWM.
17. Enable channel 3 and 4 output with TOER.
18. Set MTU output with the PFC.
19. Operation is restarted by TSTR.

(12) Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in Reset-Synchronous PWM Mode

Figure 8.95 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in reset-synchronous PWM mode after re-setting.

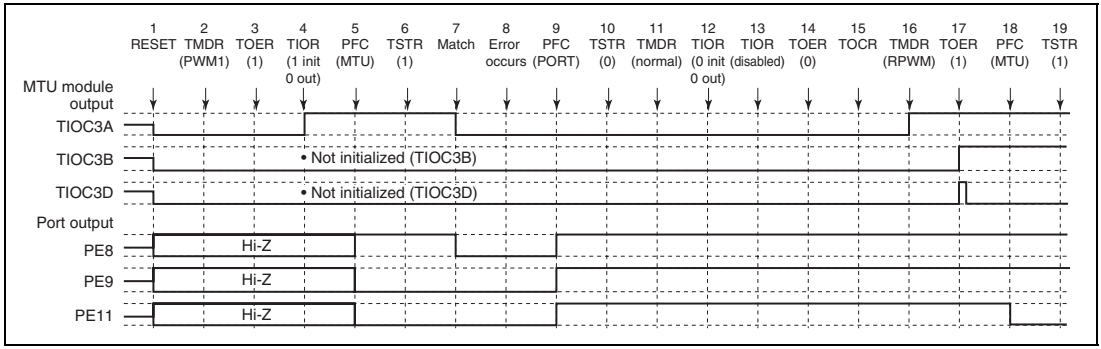


Figure 8.95 Error Occurrence in PWM Mode 1, Recovery in Reset-Synchronous PWM Mode

1 to 14 are the same as in figure 8.90.

15. Select the reset-synchronous PWM output level and cyclic output enabling/disabling with TOCR.
16. Set reset-synchronous PWM.
17. Enable channel 3 and 4 output with TOER.
18. Set MTU output with the PFC.
19. Operation is restarted by TSTR.

(13) Operation when Error Occurs during PWM Mode 2 Operation, and Operation is Restarted in Normal Mode

Figure 8.96 shows an explanatory diagram of the case where an error occurs in PWM mode 2 and operation is restarted in normal mode after re-setting.

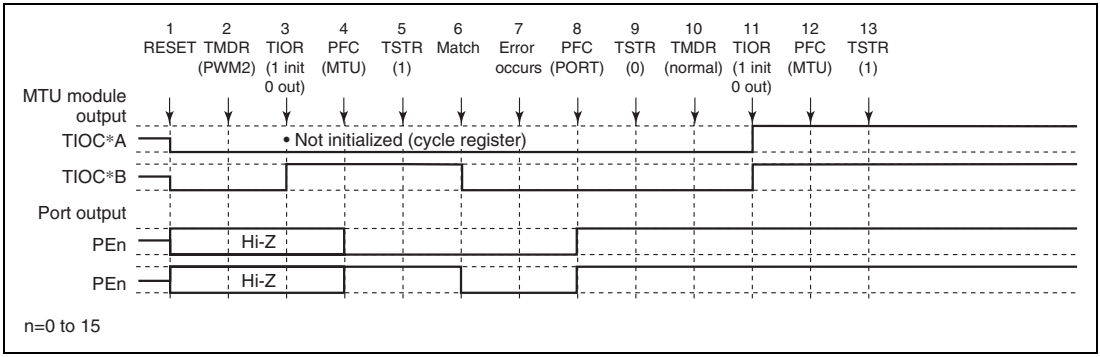


Figure 8.96 Error Occurrence in PWM Mode 2, Recovery in Normal Mode

1. After a reset, MTU output is low and ports are in the high-impedance state.
2. Set PWM mode 2.
3. Initialize the pins with TIOR. (The example shows initial high output, with low output on compare-match occurrence. In PWM mode 2, the cycle register pins are not initialized. In the example, TIOC *A is the cycle register.)
4. Set MTU output with the PFC.
5. The count operation is started by TSTR.
6. Output goes low on compare-match occurrence.
7. An error occurs.
8. Set port output with the PFC and output the inverse of the active level.
9. The count operation is stopped by TSTR.
10. Set normal mode.
11. Initialize the pins with TIOR.
12. Set MTU output with the PFC.
13. Operation is restarted by TSTR.

(14) Operation when Error Occurs during PWM Mode 2 Operation, and Operation is Restarted in PWM Mode 1

Figure 8.97 shows an explanatory diagram of the case where an error occurs in PWM mode 2 and operation is restarted in PWM mode 1 after re-setting.

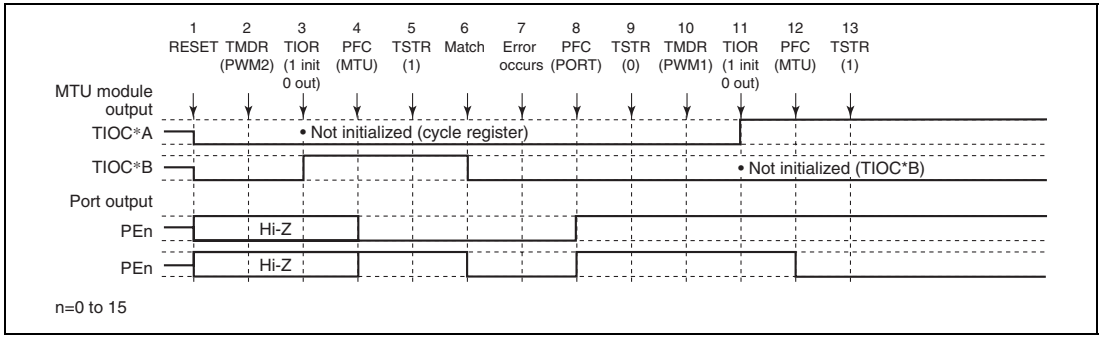


Figure 8.97 Error Occurrence in PWM Mode 2, Recovery in PWM Mode 1

1 to 9 are the same as in figure 8.96.

10. Set PWM mode 1.
11. Initialize the pins with TIOR. (In PWM mode 1, the TIOC*B side is not initialized.)
12. Set MTU output with the PFC.
13. Operation is restarted by TSTR.

(15) Operation when Error Occurs during PWM Mode 2 Operation, and Operation is Restarted in PWM Mode 2

Figure 8.98 shows an explanatory diagram of the case where an error occurs in PWM mode 2 and operation is restarted in PWM mode 2 after re-setting.

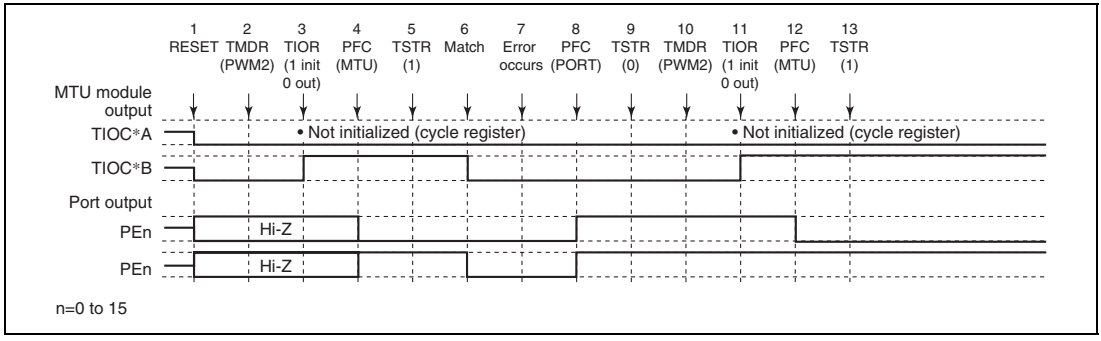


Figure 8.98 Error Occurrence in PWM Mode 2, Recovery in PWM Mode 2

1 to 9 are the same as in figure 8.96.

10. Not necessary when restarting in PWM mode 2.
11. Initialize the pins with TIOR. (In PWM mode 2, the cycle register pins are not initialized.)
12. Set MTU output with the PFC.
13. Operation is restarted by TSTR.

(16) Operation when Error Occurs during PWM Mode 2 Operation, and Operation is Restarted in Phase Counting Mode

Figure 8.99 shows an explanatory diagram of the case where an error occurs in PWM mode 2 and operation is restarted in phase counting mode after re-setting.

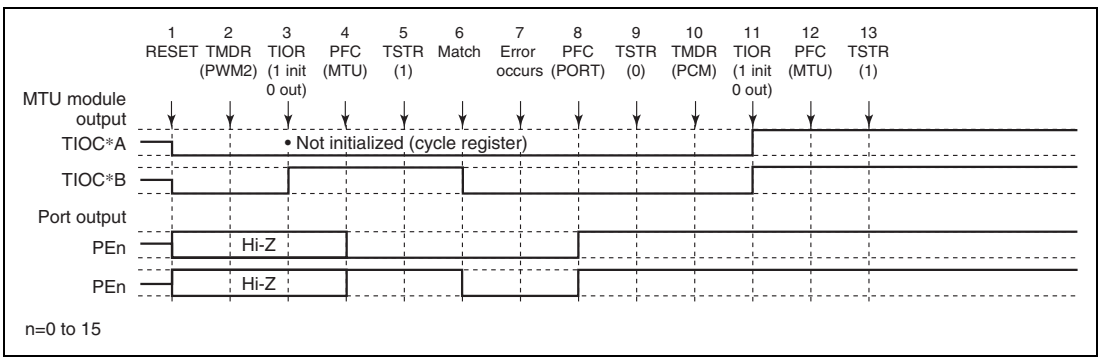


Figure 8.99 Error Occurrence in PWM Mode 2, Recovery in Phase Counting Mode

1 to 9 are the same as in figure 8.96.

10. Set phase counting mode.
11. Initialize the pins with TIOR.
12. Set MTU output with the PFC.
13. Operation is restarted by TSTR.

(17) Operation when Error Occurs during Phase Counting Mode Operation, and Operation is Restarted in Normal Mode

Figure 8.100 shows an explanatory diagram of the case where an error occurs in phase counting mode and operation is restarted in normal mode after re-setting.

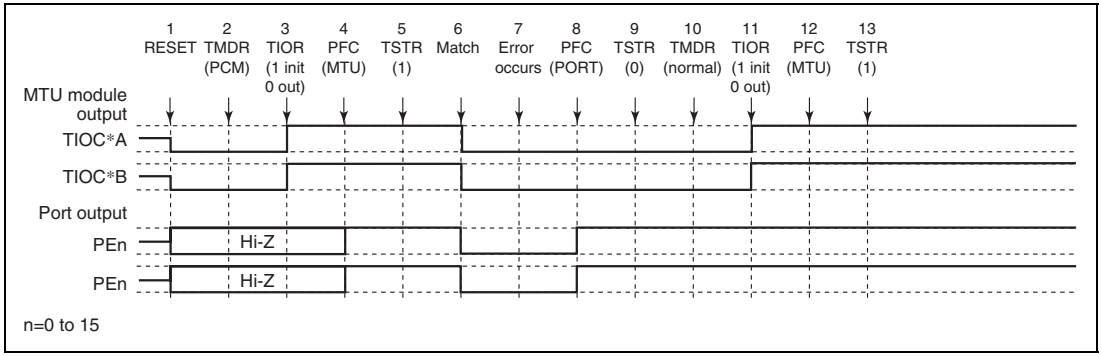


Figure 8.100 Error Occurrence in Phase Counting Mode, Recovery in Normal Mode

1. After a reset, MTU output is low and ports are in the high-impedance state.
2. Set phase counting mode.
3. Initialize the pins with TIOR. (The example shows initial high output, with low output on compare-match occurrence.)
4. Set MTU output with the PFC.
5. The count operation is started by TSTR.
6. Output goes low on compare-match occurrence.
7. An error occurs.
8. Set port output with the PFC and output the inverse of the active level.
9. The count operation is stopped by TSTR.
10. Set in normal mode.
11. Initialize the pins with TIOR.
12. Set MTU output with the PFC.
13. Operation is restarted by TSTR.

(18) Operation when Error Occurs during Phase Counting Mode Operation, and Operation is Restarted in PWM Mode 1

Figure 8.101 shows an explanatory diagram of the case where an error occurs in phase counting mode and operation is restarted in PWM mode 1 after re-setting.

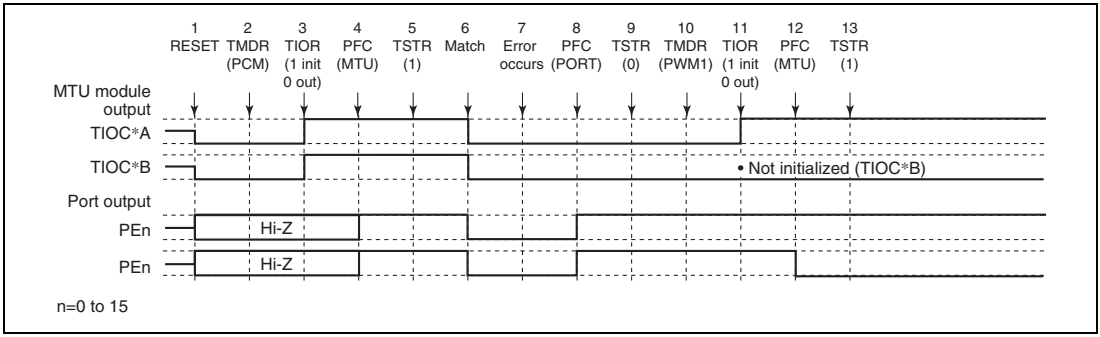


Figure 8.101 Error Occurrence in Phase Counting Mode, Recovery in PWM Mode 1

1 to 9 are the same as in figure 8.100.

10. Set PWM mode 1.
11. Initialize the pins with TIOR. (In PWM mode 1, the TIOC *B side is not initialized.)
12. Set MTU output with the PFC.
13. Operation is restarted by TSTR.

(19) Operation when Error Occurs during Phase Counting Mode Operation, and Operation is Restarted in PWM Mode 2

Figure 8.102 shows an explanatory diagram of the case where an error occurs in phase counting mode and operation is restarted in PWM mode 2 after re-setting.

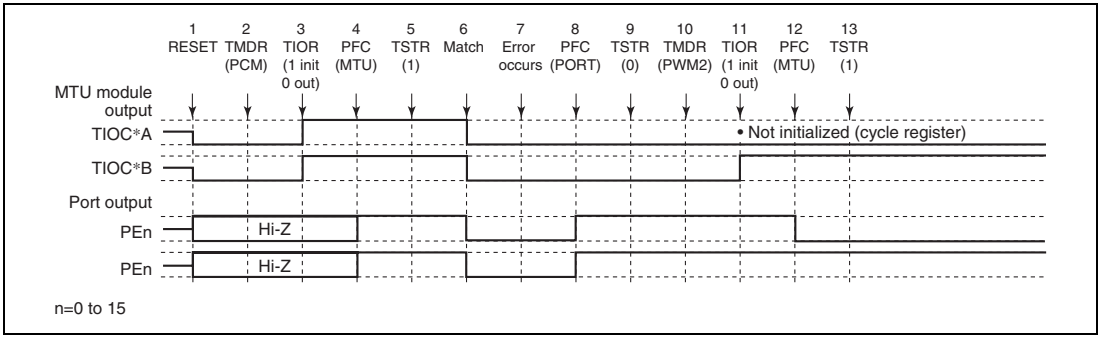


Figure 8.102 Error Occurrence in Phase Counting Mode, Recovery in PWM Mode 2

1 to 9 are the same as in figure 8.100.

10. Set PWM mode 2.
11. Initialize the pins with TIOR. (In PWM mode 2, the cycle register pins are not initialized.)
12. Set MTU output with the PFC.
13. Operation is restarted by TSTR.

(20) Operation when Error Occurs during Phase Counting Mode Operation, and Operation is Restarted in Phase Counting Mode

Figure 8.103 shows an explanatory diagram of the case where an error occurs in phase counting mode and operation is restarted in phase counting mode after re-setting.

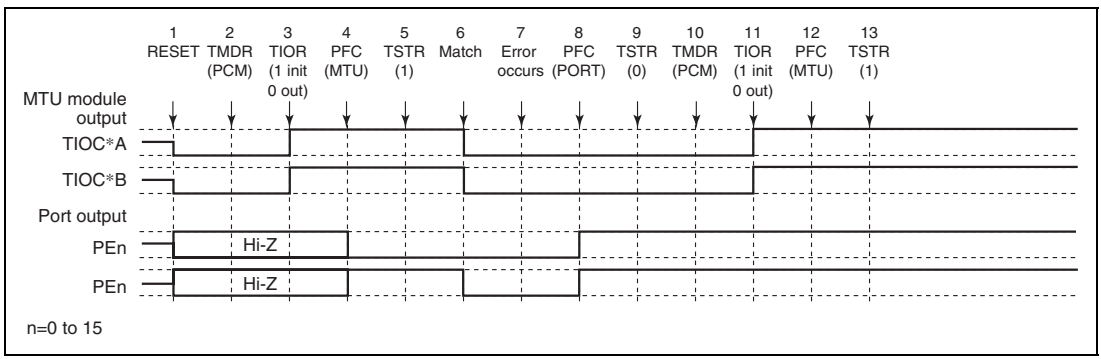


Figure 8.103 Error Occurrence in Phase Counting Mode, Recovery in Phase Counting Mode

1 to 9 are the same as in figure 8.100.

10. Not necessary when restarting in phase counting mode.
11. Initialize the pins with TIOR.
12. Set MTU output with the PFC.
13. Operation is restarted by TSTR.

(21) Operation when Error Occurs during Complementary PWM Mode Operation, and Operation is Restarted in Normal Mode

Figure 8.104 shows an explanatory diagram of the case where an error occurs in complementary PWM mode and operation is restarted in normal mode after re-setting.

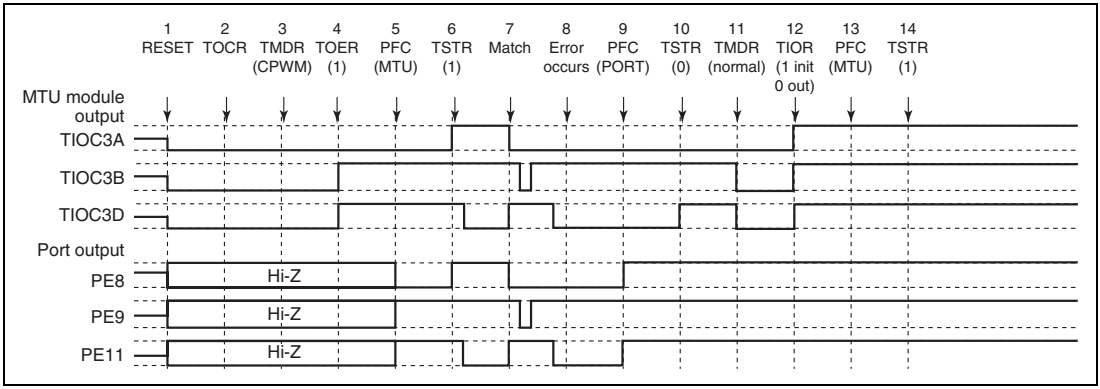


Figure 8.104 Error Occurrence in Complementary PWM Mode, Recovery in Normal Mode

1. After a reset, MTU output is low and ports are in the high-impedance state.
2. Select the complementary PWM output level and cyclic output enabling/disabling with TOCR.
3. Set complementary PWM.
4. Enable channel 3 and 4 output with TOER.
5. Set MTU output with the PFC.
6. The count operation is started by TSTR.
7. The complementary PWM waveform is output on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR. (MTU output becomes the complementary PWM output initial value.)
11. Set normal mode. (MTU output goes low.)
12. Initialize the pins with TIOR.
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

(22) Operation when Error Occurs during Complementary PWM Mode Operation, and Operation is Restarted in PWM Mode 1

Figure 8.105 shows an explanatory diagram of the case where an error occurs in complementary PWM mode and operation is restarted in PWM mode 1 after re-setting.

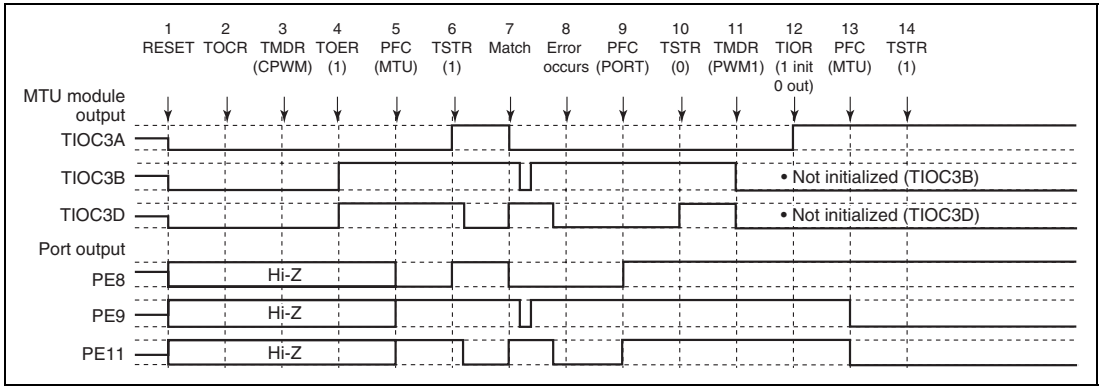


Figure 8.105 Error Occurrence in Complementary PWM Mode, Recovery in PWM Mode 1

1 to 10 are the same as in figure 8.104.

11. Set PWM mode 1. (MTU output goes low.)
12. Initialize the pins with TIOR. (In PWM mode 1, the TIOC *B side is not initialized.)
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

(23) Operation when Error Occurs during Complementary PWM Mode Operation, and Operation is Restarted in Complementary PWM Mode

Figure 8.106 shows an explanatory diagram of the case where an error occurs in complementary PWM mode and operation is restarted in complementary PWM mode after re-setting (when operation is restarted using the cycle and duty cycle settings at the time the counter was stopped).

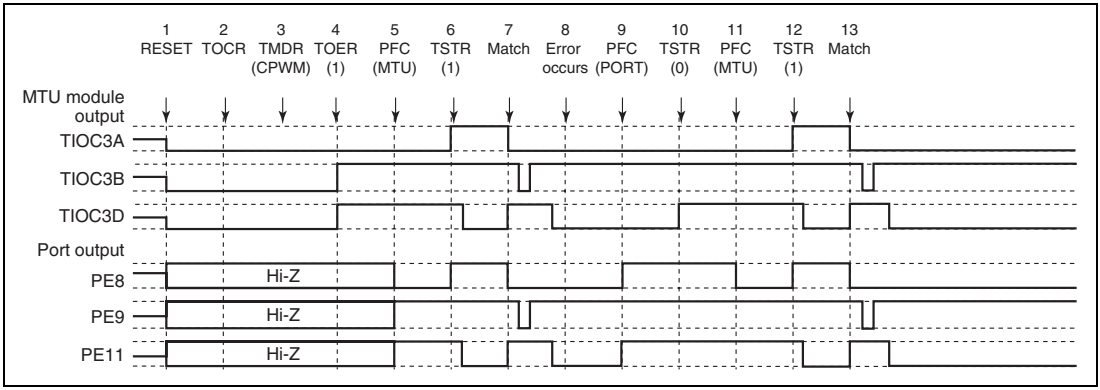


Figure 8.106 Error Occurrence in Complementary PWM Mode, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 8.104.

11. Set MTU output with the PFC.
12. Operation is restarted by TSTR.
13. The complementary PWM waveform is output on compare-match occurrence.

(24) Operation when Error Occurs during Complementary PWM Mode Operation, and Operation is Restarted in Complementary PWM Mode

Figure 8.107 shows an explanatory diagram of the case where an error occurs in complementary PWM mode and operation is restarted in complementary PWM mode after re-setting (when operation is restarted using completely new cycle and duty cycle settings).

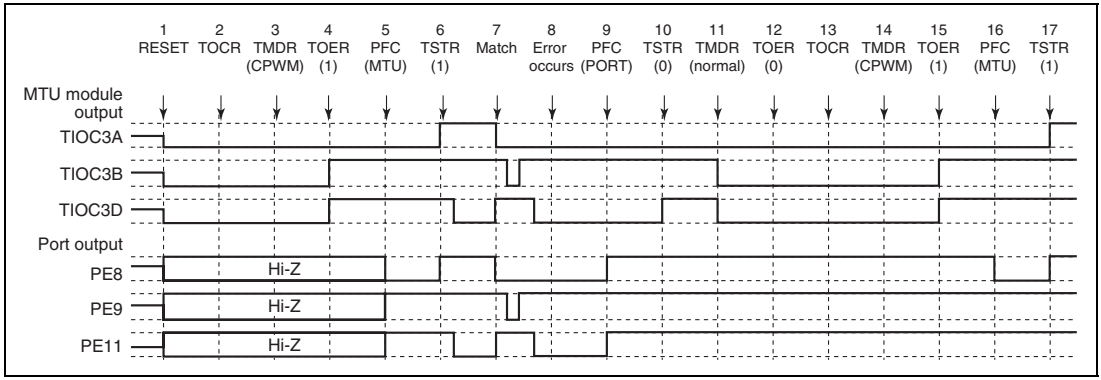


Figure 8.107 Error Occurrence in Complementary PWM Mode, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 8.104.

11. Set normal mode and make new settings. (MTU output goes low.)
12. Disable channel 3 and 4 output with TOER.
13. Select the complementary PWM mode output level and cyclic output enabling/disabling with TOCR.
14. Set complementary PWM.
15. Enable channel 3 and 4 output with TOER.
16. Set MTU output with the PFC.
17. Operation is restarted by TSTR.

(25) Operation when Error Occurs during Complementary PWM Mode Operation, and Operation is Restarted in Reset-Synchronous PWM Mode

Figure 8.108 shows an explanatory diagram of the case where an error occurs in complementary PWM mode and operation is restarted in reset-synchronous PWM mode.

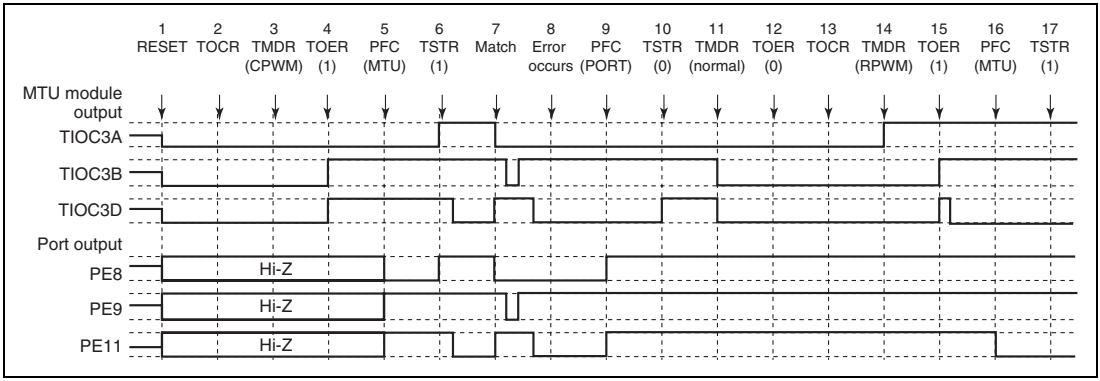


Figure 8.108 Error Occurrence in Complementary PWM Mode, Recovery in Reset-Synchronous PWM Mode

1 to 10 are the same as in figure 8.104.

11. Set normal mode. (MTU output goes low.)
12. Disable channel 3 and 4 output with TOER.
13. Select the reset-synchronous PWM mode output level and cyclic output enabling/disabling with TOCR.
14. Set reset-synchronous PWM.
15. Enable channel 3 and 4 output with TOER.
16. Set MTU output with the PFC.
17. Operation is restarted by TSTR.

(26) Operation when Error Occurs during Reset-Synchronous PWM Mode Operation, and Operation is Restarted in Normal Mode

Figure 8.109 shows an explanatory diagram of the case where an error occurs in reset-synchronous PWM mode and operation is restarted in normal mode after re-setting.

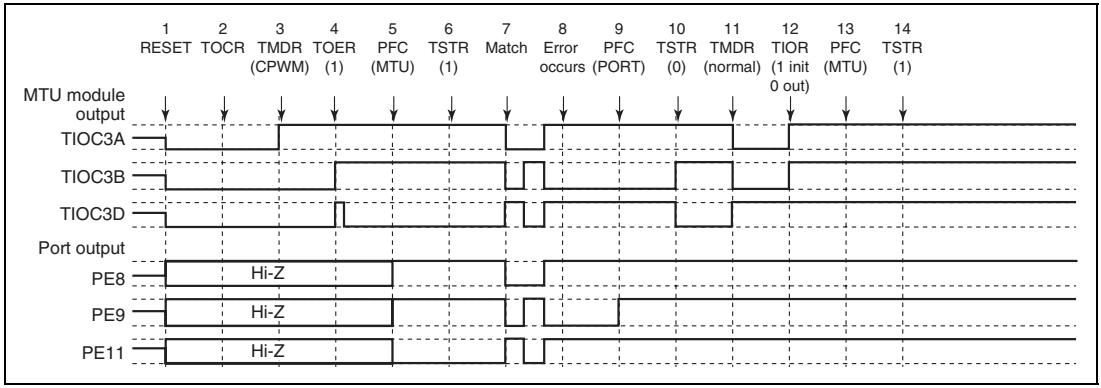


Figure 8.109 Error Occurrence in Reset-Synchronous PWM Mode, Recovery in Normal Mode

1. After a reset, MTU output is low and ports are in the high-impedance state.
2. Select the reset-synchronous PWM output level and cyclic output enabling/disabling with TOCR.
3. Set reset-synchronous PWM.
4. Enable channel 3 and 4 output with TOER.
5. Set MTU output with the PFC.
6. The count operation is started by TSTR.
7. The reset-synchronous PWM waveform is output on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR. (MTU output becomes the reset-synchronous PWM output initial value.)
11. Set normal mode. (MTU positive phase output is low, and negative phase output is high.)
12. Initialize the pins with TIOR.
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

(27) Operation when Error Occurs during Reset-Synchronous PWM Mode Operation, and Operation is Restarted in PWM Mode 1

Figure 8.110 shows an explanatory diagram of the case where an error occurs in reset-synchronous PWM mode and operation is restarted in PWM mode 1 after re-setting.

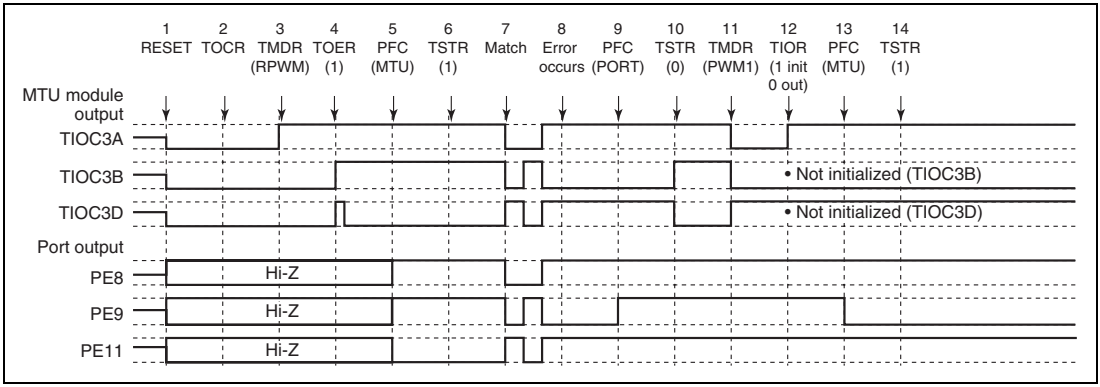


Figure 8.110 Error Occurrence in Reset-Synchronous PWM Mode, Recovery in PWM Mode 1

1 to 10 are the same as in figure 8.109.

11. Set PWM mode 1. (MTU positive phase output is low, and negative phase output is high.)
12. Initialize the pins with TIOR. (In PWM mode 1, the TIOC *B side is not initialized.)
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

(28) Operation when Error Occurs during Reset-Synchronous PWM Mode Operation, and Operation is Restarted in Complementary PWM Mode

Figure 8.111 shows an explanatory diagram of the case where an error occurs in reset-synchronous PWM mode and operation is restarted in complementary PWM mode after re-setting.

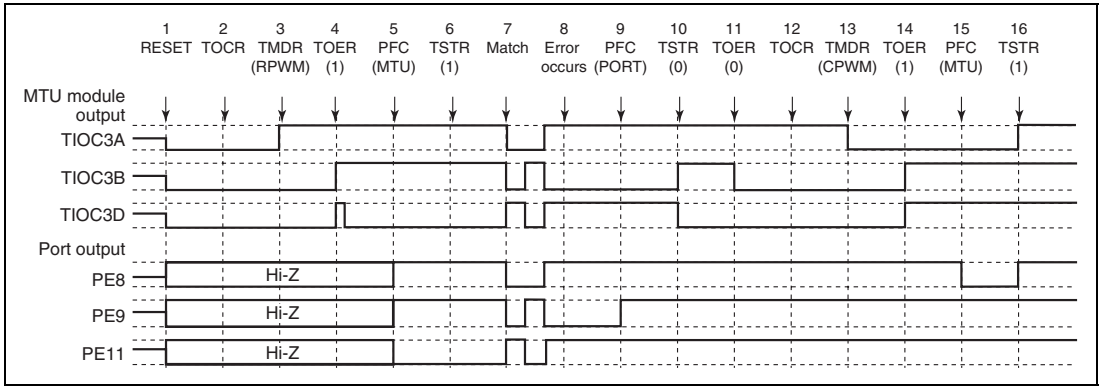


Figure 8.111 Error Occurrence in Reset-Synchronous PWM Mode, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 8.109.

11. Disable channel 3 and 4 output with TOER.
12. Select the complementary PWM output level and cyclic output enabling/disabling with TOCR.
13. Set complementary PWM. (The MTU cyclic output pin goes low.)
14. Enable channel 3 and 4 output with TOER.
15. Set MTU output with the PFC.
16. Operation is restarted by TSTR.

(29) Operation when Error Occurs during Reset-Synchronous PWM Mode Operation, and Operation is Restarted in Reset-Synchronous PWM Mode

Figure 8.112 shows an explanatory diagram of the case where an error occurs in reset-synchronous PWM mode and operation is restarted in reset-synchronous PWM mode after re-setting.

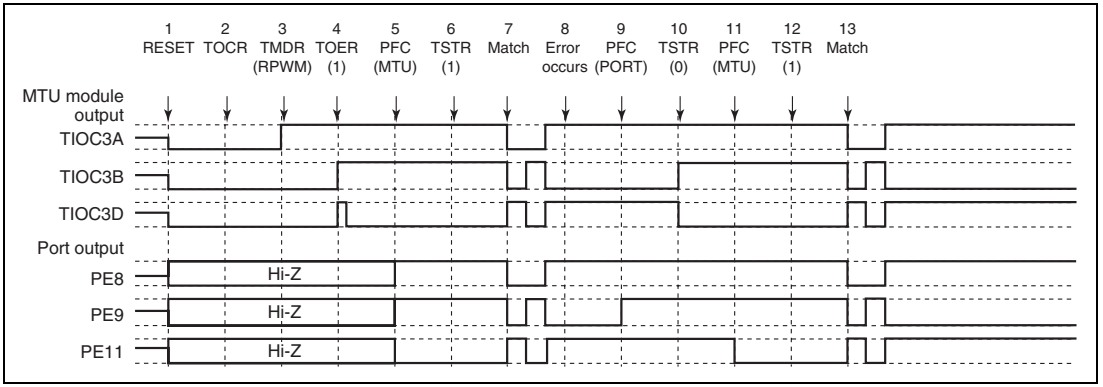


Figure 8.112 Error Occurrence in Reset-Synchronous PWM Mode, Recovery in Reset-Synchronous PWM Mode

1 to 10 are the same as in figure 8.109.

11. Set MTU output with the PFC.
12. Operation is restarted by TSTR.
13. The reset-synchronous PWM waveform is output on compare-match occurrence.

8.9 Port Output Enable (POE)

The port output enable (POE) can be used to establish a high-impedance state for high-current pins, by changing the $\overline{\text{POE0}}$ to $\overline{\text{POE3}}$ pin input, depending on the output status of the high-current pins (PE9/TIOC3B, PE11/TIOC3D, PE12/TIOC4A, PE13/TIOC4B/$\overline{\text{MRES}}$, PE14/TIOC4C, PE15/TIOC4D/$\overline{\text{IRQOUT}}$). It can also simultaneously generate interrupt requests.

The high-current pins also become high-impedance regardless of whether these pin functions are selected in cases such as when the oscillator stops or in standby mode.

8.9.1 Features

- Each of the $\overline{\text{POE0}}$ to $\overline{\text{POE3}}$ input pins can be set for falling edge, Pϕ/8 × 16, Pϕ/16 × 16, or Pϕ/128 × 16 low-level sampling.
- High-current pins can be set to high-impedance state by $\overline{\text{POE0}}$ to $\overline{\text{POE3}}$ pin falling-edge or low-level sampling.
- High-current pins can be set to high-impedance state when the high-current pin output levels are compared and simultaneous low-level output continues for one cycle or more.
- Interrupts can be generated by input-level sampling or output-level comparison results.

The POE has input-level detection circuitry and output-level detection circuitry, as shown in the block diagram of figure 8.113.

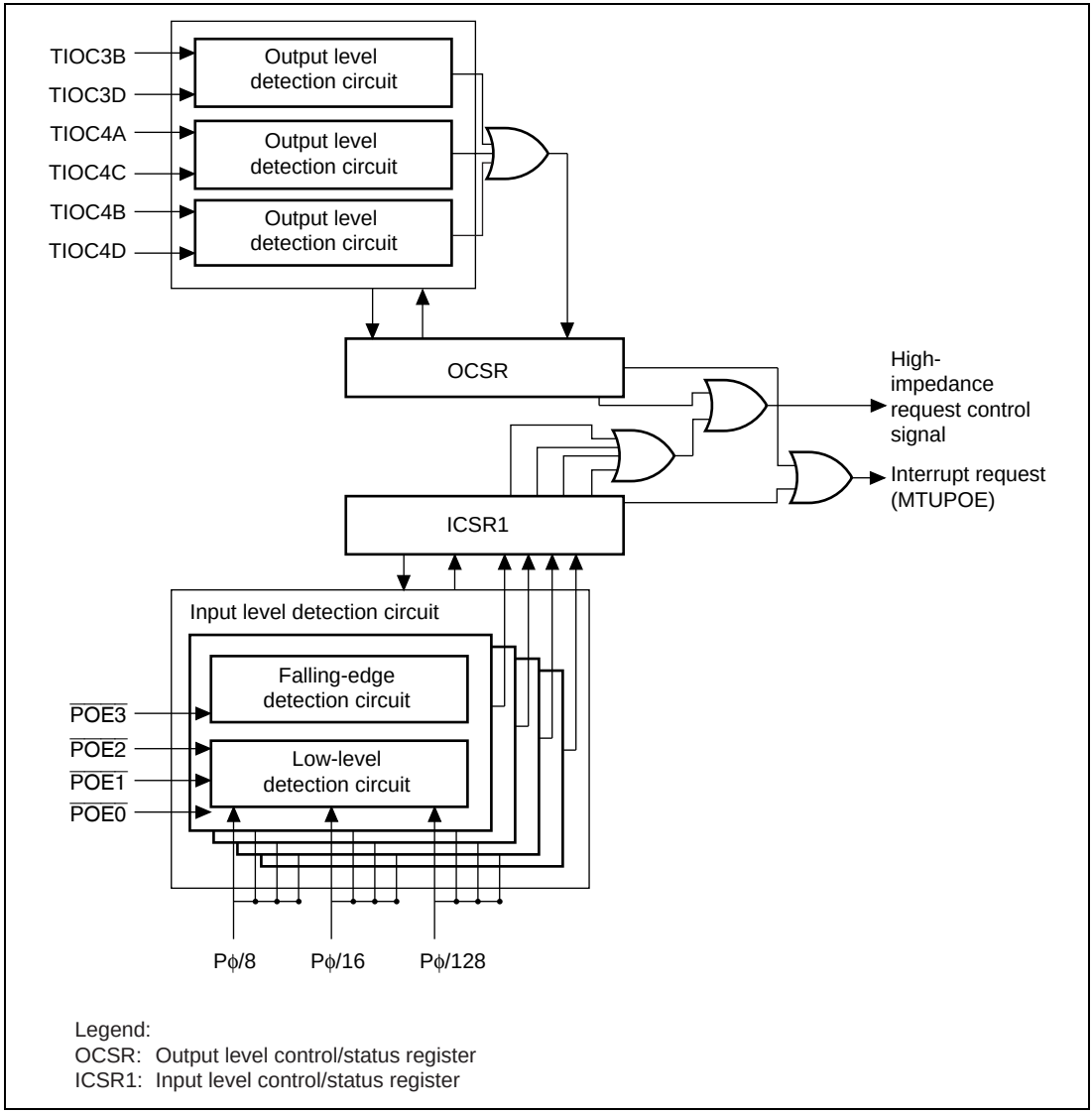


Figure 8.113 POE Block Diagram

8.9.2 Pin Configuration

Table 8.44 Pin Configuration

Name	Abbreviation	I/O	Description
Port output enable input pins	$\overline{\text{POE0}}$ to $\overline{\text{POE3}}$	Input	Input request signals to make high-current pins high-impedance state

Table 8.45 shows output-level comparisons with pin combinations.

Table 8.45 Pin Combinations

Pin Combination	I/O	Description
PE9/TIOC3B and PE11/TIOC3D	Output	All high-current pins are made high-impedance state when the pins simultaneously output low-level for longer than 1 cycle.
PE12/TIOC4A and PE14/TIOC4C	Output	All high-current pins are made high-impedance state when the pins simultaneously output low-level for longer than 1 cycle.
PE13/TIOC4B/$\overline{\text{MRES}}$ and PE15/TIOC4D/$\overline{\text{IRQOUT}}$	Output	All high-current pins are made high-impedance state when the pins simultaneously output low-level for longer than 1 cycle.

8.9.3 Register Descriptions

The POE has the two registers. The input level control/status register 1 (ICSR1) controls both $\overline{\text{POE0}}$ to $\overline{\text{POE3}}$ pin input signal detection and interrupts. The output level control/status register (OCSR) controls both the enable/disable of output comparison and interrupts.

Input Level Control/Status Register 1 (ICSR1): The input level control/status register (ICSR1) is a 16-bit readable/writable register that selects the $\overline{\text{POE0}}$ to $\overline{\text{POE3}}$ pin input modes, controls the enable/disable of interrupts, and indicates status.

Bit	Bit Name	Initial value	R/W	Description
15	POE3F	0	R/(W)*	POE3 Flag This flag indicates that a high impedance request has been input to the $\overline{\text{POE3}}$ pin. [Clearing condition] • By writing 0 to POE3F after reading POE3F = 1 [Setting condition] • When the input set by bits 7 and 6 of ICSR1 occurs at the $\overline{\text{POE3}}$ pin
14	POE2F	0	R/(W)*	POE2 Flag This flag indicates that a high impedance request has been input to the $\overline{\text{POE2}}$ pin. [Clearing condition] • By writing 0 to POE2F after reading POE2F = 1 [Setting condition] • When the input set by bits 5 and 4 of ICSR1 occurs at the $\overline{\text{POE2}}$ pin
13	POE1F	0	R/(W)*	POE1 Flag This flag indicates that a high impedance request has been input to the $\overline{\text{POE1}}$ pin. [Clearing condition] • By writing 0 to POE1F after reading POE1F = 1 [Setting condition] • When the input set by bits 3 and 2 of ICSR1 occurs at the $\overline{\text{POE1}}$ pin
12	POE0F	0	R/(W)*	POE0 Flag This flag indicates that a high impedance request has been input to the $\overline{\text{POE0}}$ pin. [Clearing condition] • By writing 0 to POE0F after reading POE0F = 1 [Setting condition] • When the input set by bits 1 and 0 of ICSR1 occurs at the $\overline{\text{POE0}}$ pin

Bit	Bit Name	Initial value	R/W	Description
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	PIE	0	R/W	Port Interrupt Enable This bit enables/disables interrupt requests when any of the POE0F to POE3F bits of the ICSR1 are set to 1. 0: Interrupt requests disabled 1: Interrupt requests enabled
7	POE3M1	0	R/W	POE3 mode 1 and 0
6	POE3M0	0	R/W	These bits select the input mode of the $\overline{\text{POE3}}$ pin. 00: Accept request on falling edge of $\overline{\text{POE3}}$ input. 01: Accept request when $\overline{\text{POE3}}$ input has been sampled for 16 Pϕ/8 clock pulses, and all are low level. 10: Accept request when $\overline{\text{POE3}}$ input has been sampled for 16 Pϕ/16 clock pulses, and all are low level. 11: Accept request when $\overline{\text{POE3}}$ input has been sampled for 16 Pϕ/128 clock pulses, and all are low level.
5	POE2M1	0	R/W	POE2 mode 1 and 0
4	POE2M0	0	R/W	These bits select the input mode of the $\overline{\text{POE2}}$ pin. 00: Accept request on falling edge of $\overline{\text{POE2}}$ input. 01: Accept request when $\overline{\text{POE2}}$ input has been sampled for 16 Pϕ/8 clock pulses, and all are low level. 10: Accept request when $\overline{\text{POE2}}$ input has been sampled for 16 Pϕ/16 clock pulses, and all are low level. 11: Accept request when $\overline{\text{POE2}}$ input has been sampled for 16 Pϕ/128 clock pulses, and all are low level.
3	POE1M1	0	R/W	POE1 mode 1 and 0
2	POE1M0	0	R/W	These bits select the input mode of the $\overline{\text{POE1}}$ pin. 00: Accept request on falling edge of $\overline{\text{POE1}}$ input. 01: Accept request when $\overline{\text{POE1}}$ input has been sampled for 16 Pϕ/8 clock pulses, and all are low level. 10: Accept request when $\overline{\text{POE1}}$ input has been sampled for 16 Pϕ/16 clock pulses, and all are low level. 11: Accept request when $\overline{\text{POE1}}$ input has been sampled for 16 Pϕ/128 clock pulses, and all are low level.

Bit	Bit Name	Initial value	R/W	Description
1	POE0M1	0	R/W	POE0 mode 1 and 0
0	POE0M0	0	R/W	These bits select the input mode of the $\overline{\text{POE0}}$ pin. 00: Accept request on falling edge of $\overline{\text{POE0}}$ input. 01: Accept request when $\overline{\text{POE0}}$ input has been sampled for 16 Pϕ/8 clock pulses, and all are low level. 10: Accept request when $\overline{\text{POE0}}$ input has been sampled for 16 Pϕ/16 clock pulses, and all are low level. 11: Accept request when $\overline{\text{POE0}}$ input has been sampled for 16 Pϕ/128 clock pulses, and all are low level.

Note: * The write value should always be 0.

Output Level Control/Status Register (OCSR): The output level control/status register (OCSR) is a 16-bit readable/writable register that controls the enable/disable of both output level comparison and interrupts, and indicates status. If the OSF bit is set to 1, the high current pins become high impedance.

Bit	Bit Name	Initial value	R/W	Description
15	OSF	0	R/(W)*	Output Short Flag This flag indicates that any one pair of the three pairs of 2 phase outputs compared have simultaneously become low level outputs. [Clearing condition] • By writing 0 to OSF after reading OSF = 1 [Setting condition] • When any one pair of the three 2-phase outputs simultaneously become low level
14 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial value	R/W	Description
9	OCE	0	R/W	Output Level Compare Enable This bit enables the start of output level comparisons. When setting this bit to 1, pay attention to the output pin combinations shown in table 8.43, Mode Transition Combinations. When 0 is output, the OSF bit is set to 1 at the same time when this bit is set, and output goes to high impedance. Accordingly, bits 15 to 11 and bit 9 of the port E data register (PEDR) are set to 1. For the MTU output comparison, set the bit to 1 after setting the MTU's output pins with the PFC. Set this bit only when using pins as outputs. When the OCE bit is set to 1, if OIE = 0 a high-impedance request will not be issued even if OSF is set to 1. Therefore, in order to have a high-impedance request issued according to the result of the output level comparison, the OIE bit must be set to 1. When OCE = 1 and OIE = 1, an interrupt request will be generated at the same time as the high-impedance request: however, this interrupt can be masked by means of an interrupt controller (INTC) setting. 0: Output level compare disabled 1: Output level compare enabled; makes an output high impedance request when OSF = 1.
8	OIE	0	R/W	Output Short Interrupt Enable This bit makes interrupt requests when the OSF bit of the OCSR is set. 0: Interrupt requests disabled 1: Interrupt request enabled
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: * The write value should always be 0.

8.9.4 Operation

Input Level Detection Operation

If the input conditions set by the ICSR1 occur on any of the $\overline{\text{POE}}$ pins, all high-current pins become high-impedance state. However, only when the general input/output function or MTU function is selected, the large-current pin is in the high-impedance state.

Falling Edge Detection: When a change from high to low level is input to the $\overline{\text{POE}}$ pins.

Low-Level Detection: Figure 8.114 shows the low-level detection operation. Sixteen continuous low levels are sampled with the sampling clock established by the ICSR1. If even one high level is detected during this interval, the low level is not accepted.

Furthermore, the timing when the large-current pins enter the high-impedance state from the sampling clock is the same in both falling-edge detection and in low-level detection.

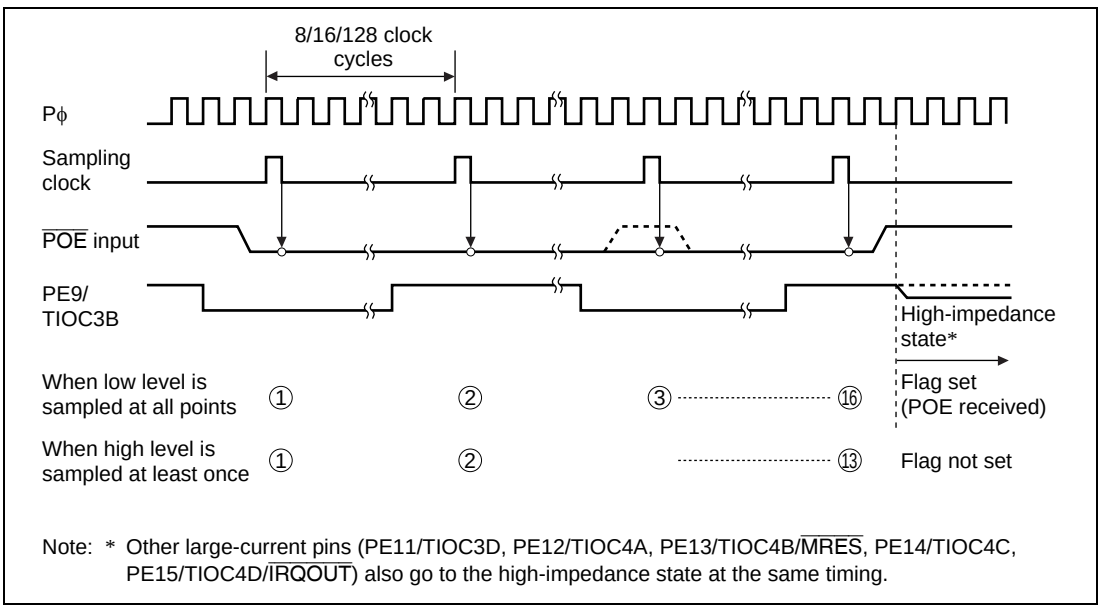


Figure 8.114 Low-Level Detection Operation

Output-Level Compare Operation

Figure 8.115 shows an example of the output-level compare operation for the combination of PE9/TIOC3B and PE11/TIOC3D. The operation is the same for the other pin combinations.

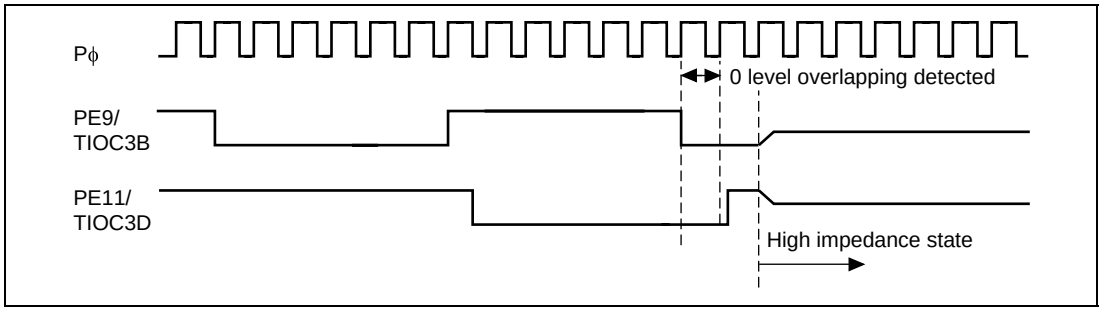


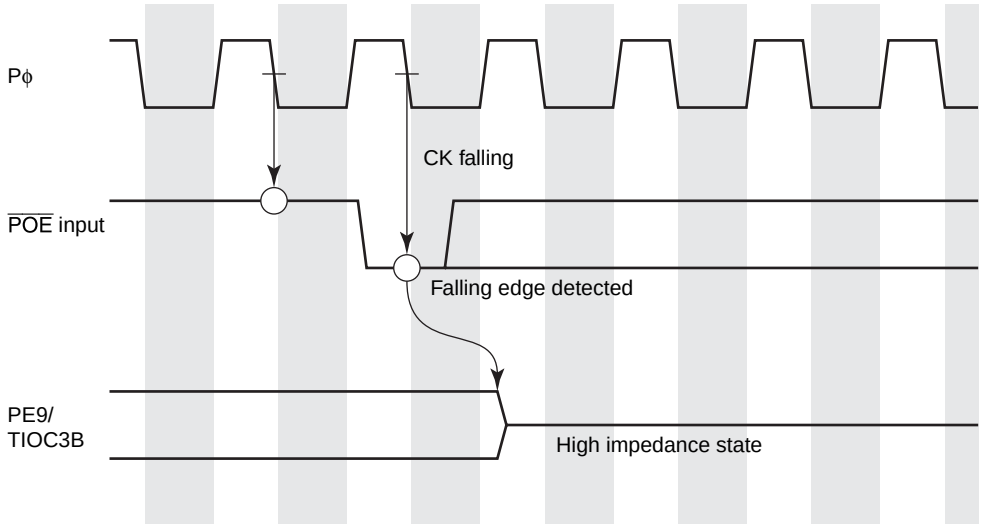
Figure 8.115 Output-Level Detection Operation

Release from High-Impedance State

High-current pins that have entered high-impedance state due to input-level detection can be released either by returning them to their initial state with a power-on reset, or by clearing all of the bit 12 to 15 (POE0F to POE3F) flags of the ICSR1. High-current pins that have become high-impedance due to output-level detection can be released either by returning them to their initial state with a power-on reset, or by first clearing bit 9 (OCE) of the OCSR to disable output-level compares, then clearing the bit 15 (OSF) flag. However, when returning from high-impedance state by clearing the OSF flag, always do so only after outputting a high level from the high-current pins (TIOC3B, TIOC3D, TIOC4A, TIOC4B, TIOC4C, and TIOC4D). High-level outputs can be achieved by setting the MTU internal registers.

POE Timing

Figure 8.116 shows an example of timing from $\overline{\text{POE}}$ input to high impedance of pin.



Note: Other large-current pins (PE11/TICO3D, PE12/TIOC4A, PE13/TIOC4B/$\overline{\text{MRES}}$, PE14/TIOC4C, PE15/TIOC4D/$\overline{\text{IRQOUT}}$) also goes to the high impedance state at the same timing

Figure 8.116 Falling Edge Detection Operation

8.9.5 Usage Note

To set the POE pin as a level detection pin, a high level signal must be firstly input to the POE pin.

Section 9 Watchdog Timer

This watchdog timer (WDT) module provides a single, 8-bit timer that can be used to monitor the system. When the counter value is not rewritten due to a system crash (such as an infinite loop) and the counter overflows, an overflow signal (WDTOVF) is output to external circuits. It is also possible to issue an IC internal reset signal at the same time.

If this module is not used as a watchdog timer, it can be used as an interval timer. If it is used as an interval timer, the interval timer interrupt (ITI) will be generated each time the counter overflows. The watchdog timer can also be used when standby mode is cleared. Figure 9.1 shows the block timer of the WDT module.

The block diagram of the WDT is shown in figure 9.1.

9.1 Features

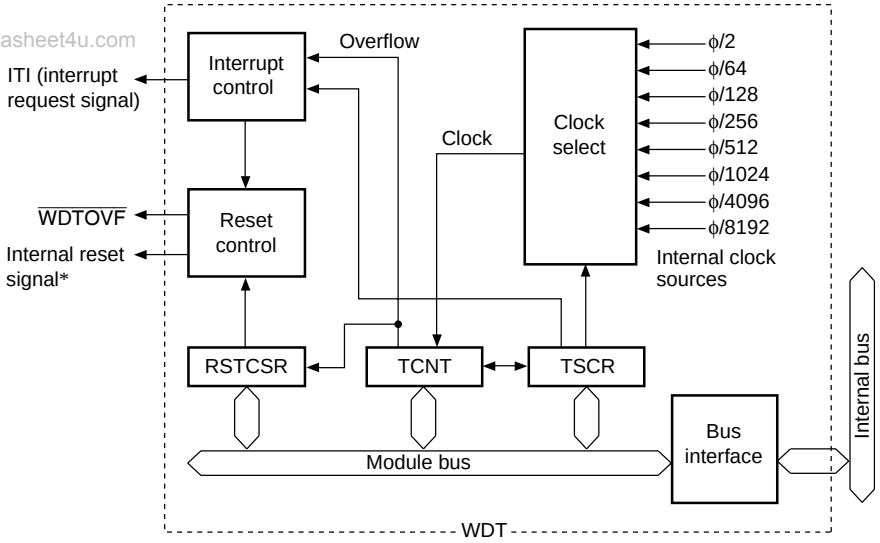
- Selectable from eight counter input clocks
- Switchable between watchdog timer mode and interval timer mode
- Used to clear software standby mode

In watchdog timer mode

- Output $\overline{\text{WDTOVF}}$ signal
- If the counter overflows, it is possible to select whether this LSI is internally reset or not.

In interval timer mode

- If the counter overflows, the WDT generates an interval timer interrupt (ITI).



Legend:
TCSR: Timer control/status register
TCNT: Timer counter
RSTCSR: Reset control/status register

Note: * The internal reset signal can be generated by making a register setting. Power-on reset or manual reset can be selected.

Figure 9.1 Block Diagram of WDT

9.2 Input/Output Pin

Table 9.1 shows the pin configuration of the watchdog timer.

Table 9.1 Pin Configuration

Pin	Abbreviation	I/O	Function
Watchdog timer overflow	$\overline{\text{WDTOVF}}$	Output	Outputs the counter overflow signal in watchdog timer mode

Note: The $\overline{\text{WDTOVF}}$ pin should not be pulled down. However, if it is necessary to pull this pin down, a resistance of 1 MΩ or higher should be used.

9.3 Register Descriptions

The WDT has the following three registers. For details, refer to section 19, List of Registers. To prevent accidental overwriting, TCSR, TCNT, and RSTCSR have to be written to in a method different from normal registers. For details, refer to section 9.6.1, Notes on Register Access.

- Timer control/status register (TCSR)
- Timer counter (TCNT)
- Reset control/status register (RSTCSR)

9.3.1 Timer Counter (TCNT)

TCNT is an 8-bit readable/writable upcounter. When the timer enable bit (TME) in the timer control/status register (TCSR) is set to 1, TCNT starts counting pulses of an internal clock selected by clock select bits 2 to 0 (CKS2 to CKS0) in TCSR. When the value of TCNT overflows (changes from H'FF to H'00), a watchdog timer overflow signal ($\overline{\text{WDTOVF}}$) or interval timer interrupt (ITI) is generated, depending on the mode selected in the WT/$\overline{\text{IT}}$ bit of TCSR. The initial value of TCNT is H'00.

9.3.2 Timer Control/Status Register (TCSR)

TCSR is an 8-bit readable/writable register. Its functions include selecting the clock source to be input to TCNT, and the timer mode.

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/(W)*[1]	Overflow Flag Indicates that TCNT has overflowed in interval timer mode. This bit should only be written with 0 to clear the flag. This flag is not set in watchdog timer mode. [Setting condition] • When TCNT overflows in interval timer mode [Clearing conditions] • Cleared by reading OVF • When 0 is written to the TME bit in interval timer mode
6	WT/$\overline{\text{IT}}$	0	R/W	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. When TCNT overflows, the WDT either generates an interval timer interrupt (ITI) or generates a $\overline{\text{WDTOVF}}$ signal, depending on the mode selected. 0: Interval timer mode Interval timer interrupt (ITI) request to the CPU when TCNT overflows 1: Watchdog timer mode $\overline{\text{WDTOVF}}$ signal output externally when TCNT overflows*[2].

Bit	Bit Name	Initial Value	R/W	Description
5	TME	0	R/W	Timer Enable Enables or disables the timer. 0: Timer disabled TCNT is initialized to H'00 and count-up stops 1: Timer enabled TCNT starts counting. A $\overline{\text{WDTOVF}}$ signal or interrupt is generated when TCNT overflows.
4, 3	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
2	CKS2	0	R/W	Clock Select 2 to 0 Select one of eight internal clock sources for input to TCNT. The clock signals are obtained by dividing the frequency of the system clock (ϕ). The overflow frequency for ϕ = 40 MHz is enclosed in parentheses*[3]. 000: Clock ϕ/2 (period: 12.8 μs) 001: Clock ϕ/64 (period: 409.6 μs) 010: Clock ϕ/128 (period: 0.8 ms) 011: Clock ϕ/256 (period: 1.6 ms) 100: Clock ϕ/512 (period: 3.3 ms) 101: Clock ϕ/1024 (period: 6.6 ms) 110: Clock ϕ/4096 (period: 26.2 ms) 111: Clock ϕ/8192 (period: 52.4 ms)
1	CKS1	0	R/W	
0	CKS0	0	R/W	

Notes: 1. Only 0 can be written after reading 1.
2. Section 9.3.3, Reset Control/Status Register (RSTCSR), describes in detail what happens when TCNT overflows in watchdog timer mode.
3. The overflow interval listed is the time from when the TCNT begins counting at H'00 until an overflow occurs.

9.3.3 Reset Control/Status Register (RSTCSR)

RSTCSR is an 8-bit readable/writable register that controls the generation of the internal reset signal when TCNT overflows, and selects the type of internal reset signal.

Bit	Bit Name	Initial Value	R/W	Description
7	WOVF	0	R/(W)*	Watchdog Overflow Flag This bit is set when TCNT overflows in watchdog timer mode. This bit cannot be set in interval timer mode. [Setting condition] • Set when TCNT overflows in watchdog timer mode [Clearing condition] • Cleared by reading WOVF, and then writing 0 to WOVF
6	RSTE	0	R/W	Reset Enable Specifies whether or not a reset signal is generated in the chip if TCNT overflows in watchdog timer mode. 0: Reset signal is not generated even if TCNT overflows (Though this LSI is not reset, TCNT and TCSR in WDT are reset) 1: Reset signal is generated if TCNT overflows
5	RSTS	0	R/W	Reset Select Selects the type of internal reset generated if TCNT overflows in watchdog timer mode. 0: Power-on reset 1: Manual reset
4 to 0	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

Note: * Only 0 can be written, for flag clearing.

9.4 Operation

9.4.1 Watchdog Timer Mode

To use the WDT as a watchdog timer, set the WT/$\overline{IT}$ and TME bits of TCSR to 1. Software must prevent TCNT overflow by rewriting the TCNT value (normally by writing H'00) before overflow occurs. No TCNT overflows will occur while the system is operating normally, but if TCNT fails to be rewritten and overflows occur due to a system crash or the like, a $\overline{WDTOVF}$ signal is output externally. The $\overline{WDTOVF}$ signal can be used to reset the system. The $\overline{WDTOVF}$ signal is output for 128 ϕ clock cycles.

If the RSTE bit in RSTCSR is set to 1, a signal to reset the chip will be generated internally simultaneous to the $\overline{WDTOVF}$ signal when TCNT overflows. Either a power-on reset or a manual reset can be selected by the RSTS bit in RSTCSR. The internal reset signal is output for 512 ϕ clock cycles.

When a WDT overflow reset is generated simultaneously with a reset input at the $\overline{RES}$ pin, the $\overline{RES}$ reset takes priority, and the WOVF bit in RSTCSR is cleared to 0.

The following are not initialized by a WDT reset signal:

- POE (port output enable) of MTU registers
- PFC (pin function controller) registers
- I/O port registers

These registers are initialized only by an external power-on reset.

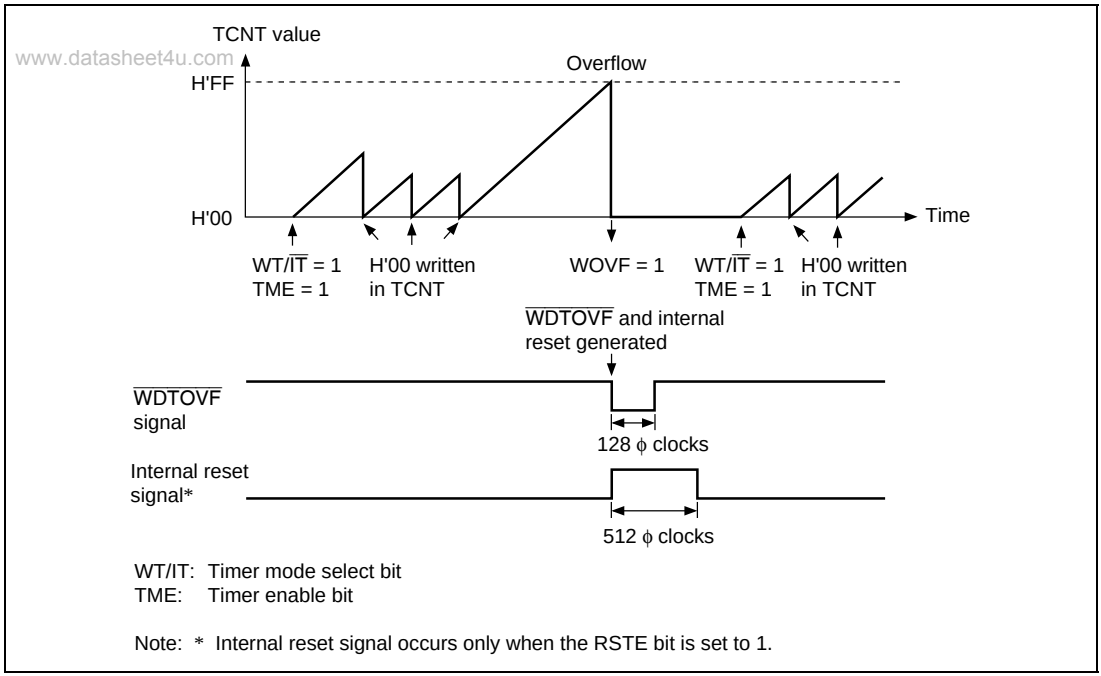


Figure 9.2 Operation in Watchdog Timer Mode

9.4.2 Interval Timer Mode

To use the WDT as an interval timer, clear WT/$\overline{IT}$ to 0 and set TME to 1 in TCSR. An interval timer interrupt (ITI) is generated each time the timer counter (TCNT) overflows. This function can be used to generate interval timer interrupts at regular intervals.

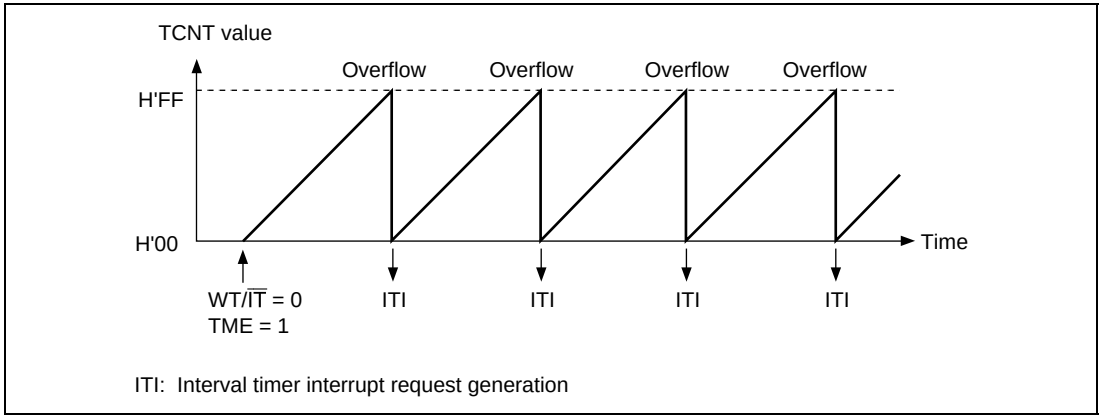


Figure 9.3 Operation in Interval Timer Mode

9.4.3 Clearing Software Standby Mode

The watchdog timer has a special function to clear software standby mode with an NMI interrupt or $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$ interrupts. When using software standby mode, set the WDT as described below.

Before Transition to Software Standby Mode: The TME bit in TCSR must be cleared to 0 to stop the watchdog timer counter before entering software standby mode. The chip cannot enter software standby mode while the TME bit is set to 1. Set bits CKS2 to CKS0 in TCSR so that the counter overflow interval is equal to or longer than the oscillation settling time. See section 20.3, AC Characteristics, for the oscillation settling time.

Recovery from Software Standby Mode: When an NMI signal or $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$ signals are received in software standby mode, the clock oscillator starts running and TCNT starts incrementing at the rate selected by bits CKS2 to CKS0 before software standby mode was entered. When TCNT overflows (changes from H'FF to H'00), the clock is presumed to be stable and usable; clock signals are supplied to the entire chip and software standby mode ends.

For details on software standby mode, see section 18, Power-Down Modes.

9.4.4 Timing of Setting the Overflow Flag (OVF)

In interval timer mode, when TCNT overflows, the OVF bit of TCSR is set to 1 and an interval timer interrupt (ITI) is simultaneously requested. Figure 9.4 shows this timing.

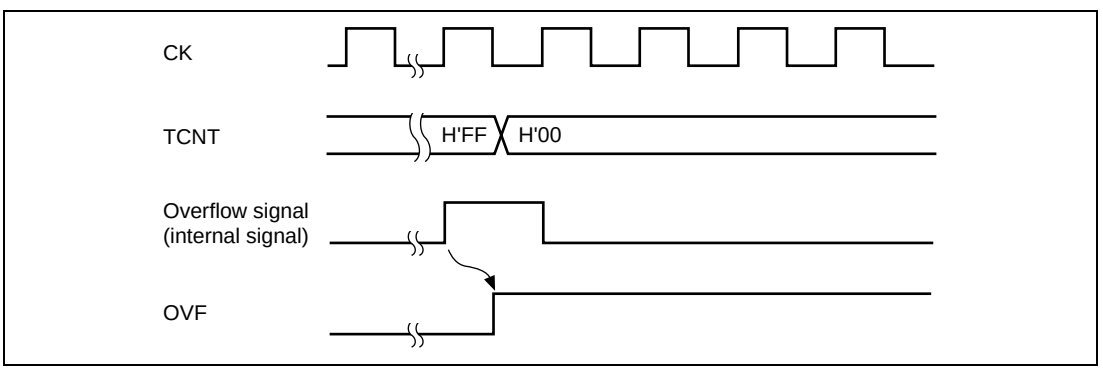


Figure 9.4 Timing of Setting OVF

9.4.5 Timing of Setting the Watchdog Timer Overflow Flag (WOVF)

When TCNT overflows in watchdog timer mode, the WOVF bit of RSTCSR is set to 1 and a $\overline{\text{WDTOVF}}$ signal is output. When the RSTE bit in RSTCSR is set to 1, TCNT overflow enables an internal reset signal to be generated for the entire chip. Figure 9.5 shows this timing.

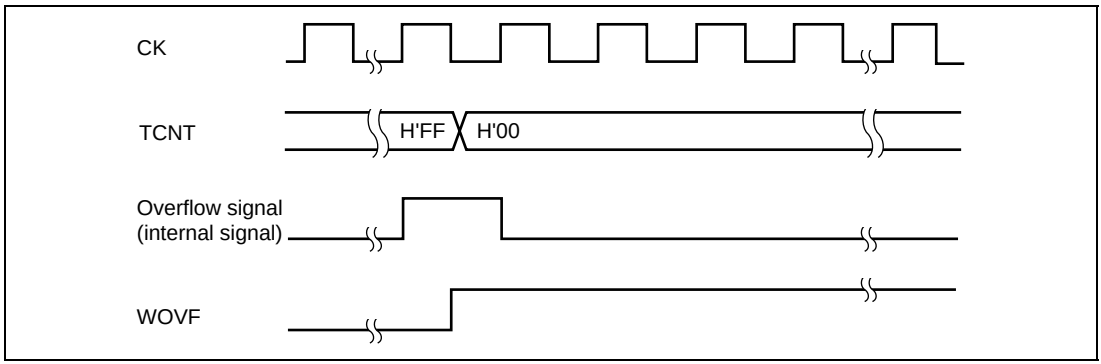


Figure 9.5 Timing of Setting WOVF

9.5 Interrupt Source

During interval timer mode operation, an overflow generates an interval timer interrupt (ITI). The interval timer interrupt is requested whenever the OVF flag is set to 1 in TCSR. OVF must be cleared to 0 in the interrupt handling routine.

Table 9.2 WDT Interrupt Source (in Interval Timer Mode)

Name	Interrupt Source	Interrupt Flag
ITI	TCNT overflow	OVF

9.6 Usage Notes

9.6.1 Notes on Register Access

The watchdog timer's TCNT, TCSR, and RSTCSR registers differ from other registers in being more difficult to write to. The procedures for writing to and reading these registers are given below.

Writing to TCNT and TCSR: These registers must be written by a word transfer instruction. They cannot be written by byte transfer instructions.

TCNT and TCSR both have the same write address. The write data must be contained in the lower byte of the written word. The upper byte must be H'5A (for TCNT) or H'A5 (for TCSR) (figure 9.6). This transfers the write data from the lower byte to TCNT or TCSR.

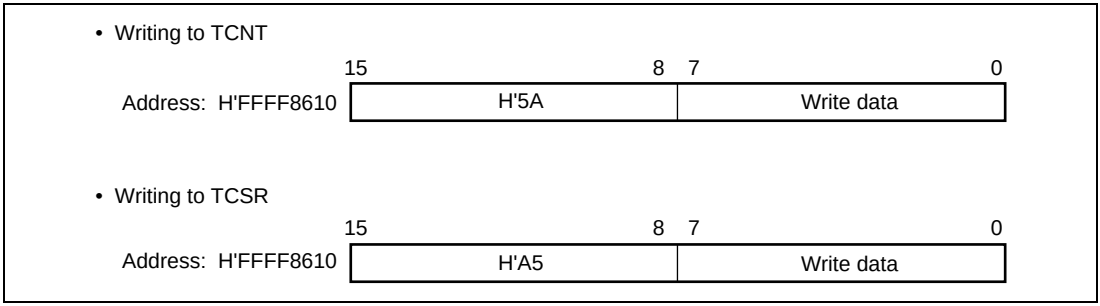


Figure 9.6 Writing to TCNT and TCSR

Writing to RSTCSR: RSTCSR must be written by a word access to address H'FFFF8612. It cannot be written by byte transfer instructions.

Procedures for writing 0 to WOVF (bit 7) and for writing to RSTE (bit 6) and RSTS (bit 5) are different, as shown in figure 9.7.

To write 0 to the WOVF bit, the write data must be H'A5 in the upper byte and H'00 in the lower byte. This clears the WOVF bit to 0. The RSTE and RSTS bits are not affected. To write to the RSTE and RSTS bits, the upper byte must be H'5A and the lower byte must be the write data. The values of bits 6 and 5 of the lower byte are transferred to the RSTE and RSTS bits, respectively. The WOVF bit is not affected.

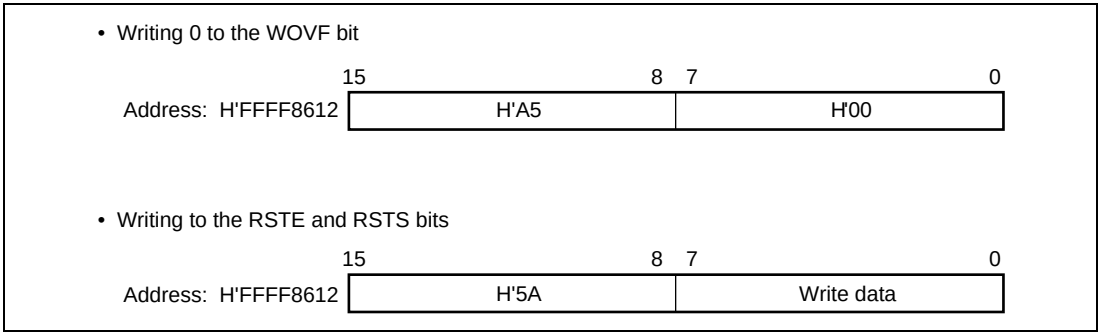


Figure 9.7 Writing to RSTCSR

Reading from TCNT, TCSR, and RSTCSR: TCNT, TCSR, and RSTCSR are read like other registers. Use byte transfer instructions. The read addresses are H'FFFF8610 for TCSR, H'FFFF8611 for TCNT, and H'FFFF8613 for RSTCSR.

9.6.2 TCNT Write and Increment Contention

If a timer counter increment clock pulse is generated during the T3 state of a write cycle to TCNT, the write takes priority and the timer counter is not incremented. Figure 9.8 shows this operation.

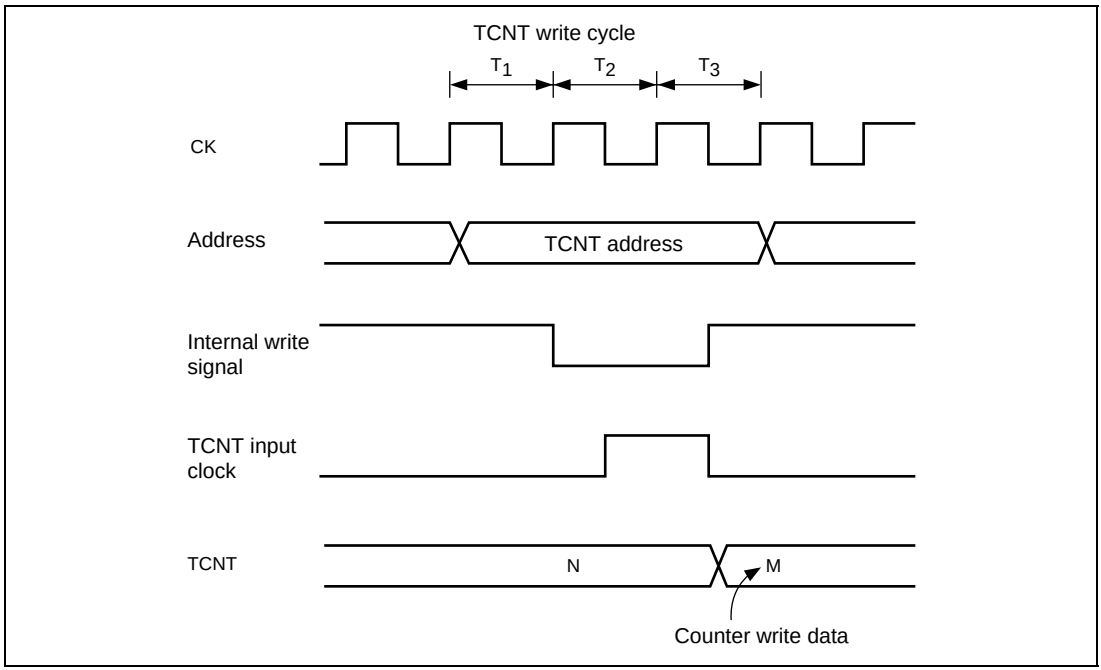


Figure 9.8 Contention between TCNT Write and Increment

9.6.3 Changing CKS2 to CKS0 Bit Values

If the values of bits CKS2 to CKS0 in the timer control/status register (TCSR) are rewritten while the WDT is running, the count may not increment correctly. Always stop the watchdog timer (by clearing the TME bit to 0) before rewriting the values of bits CKS2 to CKS0.

9.6.4 Changing between Watchdog Timer/Interval Timer Modes

To prevent incorrect operation, always stop the watchdog timer (by clearing the TME bit to 0) before switching between interval timer mode and watchdog timer mode.

9.6.5 System Reset by $\overline{\text{WDTOVF}}$ Signal

If a $\overline{\text{WDTOVF}}$ output signal is input to the $\overline{\text{RES}}$ pin, the chip cannot initialize correctly.

Avoid logical input of the $\overline{\text{WDTOVF}}$ signal to the $\overline{\text{RES}}$ input pin. To reset the entire system with the $\overline{\text{WDTOVF}}$ signal, use the circuit shown in figure 9.9.

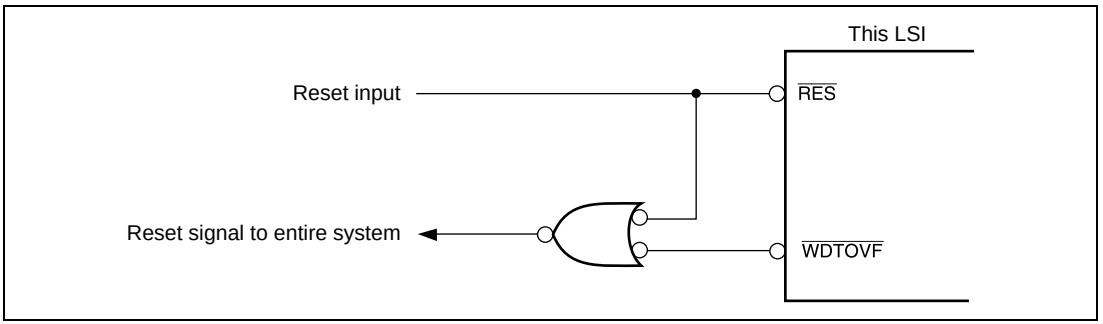


Figure 9.9 Example of System Reset Circuit Using $\overline{\text{WDTOVF}}$ Signal

9.6.6 Internal Reset in Watchdog Timer Mode

If the RSTE bit is cleared to 0 in watchdog timer mode, the chip will not be reset internally when a TCNT overflow occurs, but TCNT and TCSR in the WDT will be reset.

9.6.7 Manual Reset in Watchdog Timer Mode

When an internal reset is effected by TCNT overflow in watchdog timer mode, the processor waits until the end of the bus cycle at the time of manual reset generation before making the transition to manual reset exception processing.

9.6.8 Notes on Using $\overline{\text{WDTOVF}}$ Pin

The $\overline{\text{WDTOVF}}$ pin should not be pulled down. However, if it is necessary to pull this pin down, a resistance of 1 MΩ or higher should be used.

Section 10 Serial Communication Interface (SCI)

This LSI has two independent serial communication interface (SCI) channels. The SCI can handle both asynchronous and clocked synchronous serial communication. In asynchronous serial communication mode, serial data communication can be carried out with standard asynchronous communication chips such as a Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). A function is also provided for serial communication between processors (multiprocessor communication function).

10.1 Features

- Choice of asynchronous or clocked synchronous serial communication mode
- Full-duplex communication capability

  The transmitter and receiver are mutually independent, enabling transmission and reception to be executed simultaneously.

  Double-buffering is used in both the transmitter and the receiver, enabling continuous transmission and continuous reception of serial data.
- On-chip baud rate generator allows any bit rate to be selected

  External clock can be selected as a transfer clock source.
- Choice of LSB-first or MSB-first transfer* (except in the case of asynchronous mode 7-bit data)
- Four interrupt sources

  Four interrupt sources — transmit-end, transmit-data-empty, receive-data-full, and receive error — that can issue requests.
- Module standby mode can be set

Asynchronous mode

- Data length: 7 or 8 bits
- Stop bit length: 1 or 2 bits
- Parity: Even, odd, or none
- Multiprocessor bit: 1 or 0
- Receive error detection: Parity, overrun, and framing errors
- Break detection: Break can be detected by reading the RxD pin level directly in case of a framing error

Clocked synchronous mode

- Data length: 8 bits
- Receive error detection: Overrun errors detected

Note: * The description in this section are based on LSB-first transfer.

Figure 10.1 shows a block diagram of the SCI.

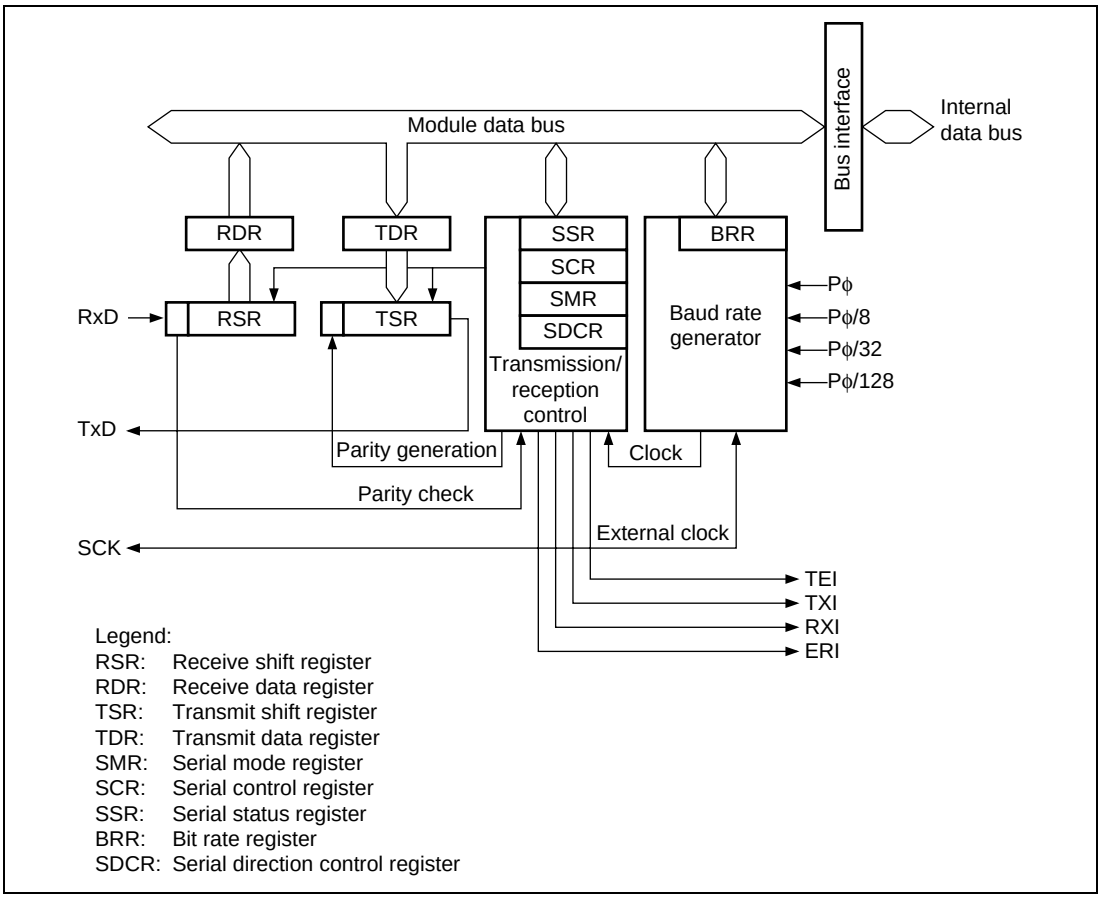


Figure 10.1 Block Diagram of SCI

10.2 Input/Output Pins

Table 10.1 shows the SCI pin configuration.

Table 10.1 Pin Configuration

Channel	Pin Name*	I/O	Function
2	SCK2	I/O	SCI_2 clock input/output
	RxD2	Input	SCI_2 receive data input
	TxD2	Output	SCI_2 transmit data output
3	SCK3	I/O	SCI_3 clock input/output
	RxD3	Input	SCI_3 receive data input
	TxD3	Output	SCI_3 transmit data output

Note: * Pin names SCK, RxD, and TxD are used in the text for all channels, omitting the channel designation.

10.3 Register Descriptions

The SCI has the following registers for each channel. For details on register addresses and register states during each processing, refer to section 19, List of Registers.

Channel 2

- Serial mode register_2 (SMR_2)
- Bit rate register_2 (BRR_2)
- Serial control register_2 (SCR_2)
- Transmit data register_2 (TDR_2)
- Serial status register_2 (SSR_2)
- Receive data register_2 (RDR_2)
- Serial direction control register_2 (SDCR_2)

Channel 3

- Serial mode register_3 (SMR_3)
- Bit rate register_3 (BRR_3)
- Serial control register_3 (SCR_3)
- Transmit data register_3 (TDR_3)
- Serial status register_3 (SSR_3)
- Receive data register_3 (RDR_3)
- Serial direction control register_3 (SDCR_3)

10.3.1 Receive Shift Register (RSR)

RSR is a shift register used to receive serial data that is input to the RxD pin and convert it into parallel data. When one byte of data has been received, it is transferred to RDR automatically. RSR cannot be directly read or written to by the CPU.

10.3.2 Receive Data Register (RDR)

RDR is an 8-bit register that stores receive data. When the SCI has received one byte of serial data, it transfers the received serial data from RSR to RDR where it is stored. After this, RSR is receive-enabled. Since RSR and RDR function as a double buffer in this way, enables continuous receive operations to be performed. After confirming that the RDRF bit in SSR is set to 1, read RDR for only once. RDR cannot be written to by the CPU. RDR is initialized to H'00.

10.3.3 Transmit Shift Register (TSR)

TSR is a shift register that transmits serial data. To perform serial data transmission, the SCI first transfers transmit data from TDR to TSR, then sends the data to the TxD pin. TSR cannot be directly accessed by the CPU.

10.3.4 Transmit Data Register (TDR)

TDR is an 8-bit register that stores transmit data. When the SCI detects that TSR is empty, it transfers the transmit data written in TDR to TSR and starts transmission. The double-buffered structures of TDR and TSR enables continuous serial transmission. If the next transmit data has already been written to TDR during serial transmission, the SCI transfers the written data to TSR to continue transmission. Although TDR can be read or written to by the CPU at all times, to achieve reliable serial transmission, write transmit data to TDR for only once after confirming that the TDRE bit in SSR is set to 1. TDR is initialized to H'FF.

10.3.5 Serial Mode Register (SMR)

SMR is used to set the SCI's serial transfer format and select the baud rate generator clock source.

Bit	Bit Name	Initial Value	R/W	Description
7	C/$\overline{A}$	0	R/W	Communication Mode 0: Asynchronous mode 1: Clocked synchronous mode
6	CHR	0	R/W	Character Length (enabled only in asynchronous mode) 0: Selects 8 bits as the data length. 1: Selects 7 bits as the data length. LSB-first is fixed and the MSB (bit 7) of TDR is not transmitted in transmission. In clocked synchronous mode, a fixed data length of 8 bits is used.
5	PE	0	R/W	Parity Enable (enabled only in asynchronous mode) When this bit is set to 1, the parity bit is added to transmit data before transmission, and the parity bit is checked in reception. For a multiprocessor format, parity bit addition and checking are not performed regardless of the PE bit setting.
4	O/$\overline{E}$	0	R/W	Parity Mode (enabled only when the PE bit is 1 in asynchronous mode) 0: Selects even parity. 1: Selects odd parity.
3	STOP	0	R/W	Stop Bit Length (enabled only in asynchronous mode) Selects the stop bit length in transmission. 0: 1 stop bit 1: 2 stop bits In reception, only the first stop bit is checked. If the second stop bit is 0, it is treated as the start bit of the next transmit character.
2	MP	0	R/W	Multiprocessor Mode (enabled only in asynchronous mode) When this bit is set to 1, the multiprocessor communication function is enabled. The PE bit and O/$\overline{E}$ bit settings are invalid in multiprocessor mode.

Bit	Bit Name	Initial Value	R/W	Description
1	CKS1	0	R/W	Clock Select 1 and 0
0	CKS0	0	R/W	These bits select the clock source for the baud rate generator. 00: Pϕ clock (n = 0) 01: Pϕ/8 clock (n = 1) 10: Pϕ/32 clock (n = 2) 11: Pϕ/128 clock (n = 3) For the relation between the bit rate register setting and the baud rate, see section 10.3.9, Bit Rate Register (BRR). n is the decimal display of the value of n in BRR (see section 10.3.9, Bit Rate Register (BRR)).

10.3.6 Serial Control Register (SCR)

SCR is a register that performs enabling or disabling of SCI transfer operations and interrupt requests, and selection of the transfer clock source. For details on interrupt requests, refer to section 10.7, Interrupt Sources.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable When this bit is set to 1, TXI interrupt request is enabled.
6	RIE	0	R/W	Receive Interrupt Enable When this bit is set to 1, RXI and ERI interrupt requests are enabled.
5	TE	0	R/W	Transmit Enable When this bit is set to 1, transmission is enabled.
4	RE	0	R/W	Receive Enable When this bit is set to 1, reception is enabled.
3	MPIE	0	R/W	Multiprocessor Interrupt Enable (enabled only when the MP bit in SMR is 1 in asynchronous mode) When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and ORER status flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed. For details, refer to section 10.5, Multiprocessor Communication Function.

Bit	Bit Name	Initial Value	R/W	Description
2	TEIE	0	R/W	Transmit End Interrupt Enable When this bit is set to 1, TEI interrupt request is enabled.
1	CKE1	0	R/W	Clock Enable 1 and 0
0	CKE0	0	R/W	Selects the clock source and SCK pin function. Asynchronous mode: 00: Internal clock, SCK pin used for input pin (input signal is ignored) or output pin (output level is undefined) 01: Internal clock, SCK pin used for clock output (The output clock frequency is the same as the bit rate) 10: External clock, SCK pin used for clock input (The input clock frequency is 16 times the bit rate) 11: External clock, SCK pin used for clock input (The input clock frequency is 16 times the bit rate) Clocked synchronous mode: 00: Internal clock, SCK pin used for synchronous clock output 01: Internal clock, SCK pin used for synchronous clock output 10: External clock, SCK pin used for synchronous clock input 11: External clock, SCK pin used for synchronous clock input

10.3.7 Serial Status Register (SSR)

SSR is a register containing status flags of the SCI and multiprocessor bits for transfer. 1 cannot be written to flags TDRE, RDRF, ORER, PER, and FER; they can only be cleared.

Bit	Bit Name	Initial Value	R/W	Description
7	TDRE	1	R/(W)*	Transmit Data Register Empty Displays whether TDR contains transmit data. [Setting conditions] • Power-on reset and software standby mode • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR [Clearing condition] • When 0 is written to TDRE after reading TDRE = 1
6	RDRF	0	R/(W)*	Receive Data Register Full Indicates that the received data is stored in RDR. [Setting condition] • When serial reception ends normally and receive data is transferred from RSR to RDR [Clearing conditions] • Power-on reset or software standby mode • When 0 is written to RDRF after reading RDRF = 1 The RDRF flag is not affected and retains their previous values when the RE bit in SCR is cleared to 0.
5	ORER	0	R/(W)*	Overrun Error [Setting condition] • When the next serial reception is completed while RDRF = 1 [Clearing conditions] • Power-on reset or software standby mode • When 0 is written to ORER after reading ORER = 1 The ORER flag is not affected and retains their previous values when the RE bit in SCR is cleared to 0.

Bit	Bit Name	Initial Value	R/W	Description
4	FER	0	R/(W)*	Framing Error [Setting condition] • When the stop bit is 0 [Clearing conditions] • Power-on reset or software standby mode • When 0 is written to FER after reading FER = 1 In 2-stop-bit mode, only the first stop bit is checked. The FER flag is not affected and retains their previous values when the RE bit in SCR is cleared to 0.
3	PER	0	R/(W)*	Parity Error [Setting condition] • When a parity error is detected during reception [Clearing conditions] • Power-on reset or software standby mode • When 0 is written to PER after reading PER = 1 The PER flag is not affected and retains their previous values when the RE bit in SCR is cleared to 0.
2	TEND	1	R	Transmit End [Setting conditions] • Power-on reset or software standby mode • When the TE bit in SCR is 0 • When TDRE = 1 at transmission of the last bit of a 1-byte serial transmit character [Clearing condition] • When 0 is written to TDRE after reading TDRE = 1
1	MPB	0	R	Multiprocessor Bit MPB stores the multiprocessor bit in the receive data. When the RE bit in SCR is cleared to 0, its previous state is retained.
0	MPBT	0	R/W	Multiprocessor Bit Transfer MPBT sets the multiprocessor bit value to be added to the transmit data.

Note: * Only 0 can be written for flag clearing.

10.3.8 Serial Direction Control Register (SDCR)

The DIR bit in SDCR selects LSB-first or MSB-first transfer. With an 8-bit data length, LSB-first/MSB-first selection is available regardless of the communication mode. With a 7-bit data length, LSB-first transfer must be selected. The description in this section assumes LSB-first transfer.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	R	Reserved The write value should always be 1. Operation cannot be guaranteed if 0 is written.
3	DIR	0	R/W	Data Transfer Direction Selects the serial/parallel conversion format. Valid for an 8-bit transmit/receive format. 0: TDR contents are transmitted in LSB-first order Receive data is stored in RDR in LSB-first 1: TDR contents are transmitted in MSB-first order Receive data is stored in RDR in MSB-first
2	—	0	R	Reserved The write value should always be 0. Operation cannot be guaranteed if 1 is written.
1	—	1	R	Reserved This bit is always read as 1, and cannot be modified.
0	—	0	R	Reserved The write value should always be 0. Operation cannot be guaranteed if 1 is written.

10.3.9 Bit Rate Register (BRR)

BRR is an 8-bit register that adjusts the bit rate. As the SCI performs baud rate generator control independently for each channel, different bit rates can be set for each channel. Table 10.2 shows the relationships between the N setting in BRR and the effective bit rate B_0 for asynchronous and clocked synchronous modes. The initial value of BRR is H'FF, and it can be read from or written to by the CPU at all times.

Table 10.2 Relationships between N Setting in BRR and Effective Bit Rate B_0

Mode	Bit Rate	Error
Asynchronous mode (n = 0)	$B_0 = \frac{P\phi \times 10^6}{32 \times 2^{2n} \times (N + 1)}$	Error (%) = $\left(\frac{B_0}{B_1} - 1\right) \times 100$
Asynchronous mode (n = 1 to 3)	$B_0 = \frac{P\phi \times 10^6}{32 \times 2^{2n+1} \times (N + 1)}$	Error (%) = $\left(\frac{B_0}{B_1} - 1\right) \times 100$
Clocked synchronous mode (n = 0)	$B_0 = \frac{P\phi \times 10^6}{4 \times 2^{2n} \times (N + 1)}$	—
Clocked synchronous mode (n = 1 to 3)	$B_0 = \frac{P\phi \times 10^6}{4 \times 2^{2n+1} \times (N + 1)}$	—

Note: B_0: Effective bit rate (bit/s) Actual transfer speed according to the register settings
B_1: Logical bit rate (bit/s) Specified transfer speed of the target system
N: BRR setting for baud rate generator ($0 \le N \le 255$)
$P\phi$: Peripheral clock operating frequency (MHz)
n : Determined by the SMR settings shown in the following tables.

SMR Setting

CKS1	CKS0	n
0	0	0
0	1	1
1	0	2
1	1	3

Table 10.3 shows sample N settings in BRR in normal asynchronous mode. Table 10.4 shows the maximum bit rate for each frequency in normal asynchronous mode. Table 10.6 shows sample N settings in BRR in clocked synchronous mode. For details, refer to section 10.4.2, Receive Data Sampling Timing and Reception Margin in Asynchronous Mode. Tables 10.5 and 10.7 show the maximum bit rates with external clock input.

Table 10.3 BRR Settings for Various Bit Rates (Asynchronous Mode) (1)

Logical Bit Rate (bit/s)	Operating Frequency Pϕ (MHz) 4			6			8			10			12		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	1	140	0.74	1	212	0.03	2	70	0.03	2	88	–0.25	2	106	–0.44
150	1	103	0.16	1	155	0.16	2	51	0.16	2	64	0.16	2	77	0.16
300	1	51	0.16	1	77	0.16	2	25	0.16	1	129	0.16	2	38	0.16
600	1	25	0.16	1	38	0.16	2	12	0.16	1	64	0.16	1	77	0.16
1200	1	12	0.16	0	155	0.16	1	25	0.16	1	32	–1.36	1	38	0.16
2400	0	51	0.16	0	77	0.16	1	12	0.16	0	129	0.16	0	155	0.16
4800	0	25	0.16	0	38	0.16	0	51	0.16	0	64	0.16	0	77	0.16
9600	0	12	0.16	0	19	–2.34	0	25	0.16	0	32	–1.36	0	38	0.16
14400	0	8	–3.55	0	12	0.16	0	16	2.12	0	21	–1.36	0	25	0.16
19200	0	6	–6.99	0	9	–2.34	0	12	0.16	0	15	1.73	0	19	–2.34
28800	0	3	8.51	0	6	–6.99	0	8	–3.55	0	10	–1.36	0	12	0.16
31250	0	3	0.00	0	5	0.00	0	7	0.00	0	9	0.00	0	11	0.00
38400	0	2	8.51	0	4	–2.34	0	6	–6.99	0	7	1.73	0	9	–2.34

Table 10.3 BRR Settings for Various Bit Rates (Asynchronous Mode) (2)

Logical Bit Rate (bit/s)	Operating Frequency Pϕ (MHz) 14			16			18			20			22		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	123	0.23	2	141	0.03	2	159	–0.12	2	177	–0.25	2	194	0.16
150	2	90	0.16	2	103	0.16	2	116	0.16	2	129	0.16	2	142	0.16
300	2	45	–0.93	2	51	0.16	2	58	–0.69	2	64	0.16	2	71	–0.54
600	2	22	–0.93	1	103	0.16	1	116	0.16	1	129	0.16	1	142	0.16
1200	1	45	–0.93	1	51	0.16	1	58	–0.69	1	64	0.16	1	71	–0.54
2400	1	22	–0.93	0	207	0.16	0	233	0.16	1	32	–1.36	1	35	–0.54
4800	0	90	0.16	0	103	0.16	0	116	0.16	0	129	0.16	0	142	0.16
9600	0	45	–0.93	0	51	0.16	0	58	–0.69	0	64	0.16	0	71	–0.54
14400	0	29	1.27	0	34	–0.79	0	38	0.16	0	42	0.94	0	47	–0.54
19200	0	22	–0.93	0	25	0.16	0	28	1.02	0	32	–1.36	0	35	–0.54
28800	0	14	1.27	0	16	2.12	0	19	–2.34	0	21	–1.36	0	23	–0.54
31250	0	13	0.00	0	15	0.00	0	17	0.00	0	19	0.00	0	21	0.00
38400	0	10	3.57	0	12	0.16	0	14	–2.34	0	15	1.73	0	17	–0.54

Table 10.3 BRR Settings for Various Bit Rates (Asynchronous Mode) (3)

Logical Bit Rate (bit/s)	Operating Frequency Pϕ (MHz) 24			25			26			28			30		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	212	0.03	2	221	–0.02	2	230	–0.08	2	248	–0.17	3	66	–0.62
150	2	155	0.16	2	162	–0.15	2	168	0.16	2	181	0.16	2	194	0.16
300	2	77	0.16	2	80	0.47	2	84	–0.43	2	90	0.16	2	97	–0.35
600	1	155	0.16	1	162	–0.15	1	168	0.16	1	181	0.16	2	48	–0.35
1200	1	77	0.16	1	80	0.47	1	84	–0.43	1	90	0.16	1	97	–0.35
2400	1	38	0.16	1	40	–0.76	1	41	0.76	1	45	–0.93	1	48	–0.35
4800	0	155	0.16	0	162	–0.15	0	168	0.16	0	181	0.16	0	194	0.16
9600	0	77	0.16	0	80	0.47	0	84	–0.43	0	90	0.16	0	97	–0.35
14400	0	51	0.16	0	53	0.47	0	55	0.76	0	60	–0.39	0	64	0.16
19200	0	38	0.16	0	40	–0.76	0	41	0.76	0	45	–0.93	0	48	–0.35
28800	0	25	0.16	0	26	0.47	0	27	0.76	0	29	1.27	0	32	–1.36
31250	0	23	0.00	0	24	0.00	0	25	0.00	0	27	0.00	0	29	0.00
38400	0	19	–2.34	0	19	1.73	0	20	0.76	0	22	–0.93	0	23	1.73

Table 10.3 BRR Settings for Various Bit Rates (Asynchronous Mode) (4)

Logical Bit Rate (bit/s)	Operating Frequency Pϕ (MHz) 32			34			36			38			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	70	0.03	3	74	0.62	3	79	–0.12	3	83	0.40	3	88	–0.25
150	2	207	0.16	2	220	0.16	2	233	0.16	2	246	0.16	3	64	0.16
300	2	103	0.16	2	110	–0.29	2	116	0.16	2	123	–0.24	2	129	0.16
600	2	51	0.16	2	54	0.62	2	58	–0.69	2	61	–0.24	2	64	0.16
1200	1	103	0.16	1	110	–0.29	1	116	0.16	1	123	–0.24	1	129	0.16
2400	1	51	0.16	1	51	6.42	1	58	–0.69	1	61	–0.24	1	64	0.16
4800	0	207	0.16	0	220	0.16	0	234	–0.27	0	246	0.16	1	32	–1.36
9600	0	103	0.16	0	110	–0.29	0	116	0.16	0	123	–0.24	0	129	0.16
14400	0	68	0.64	0	73	–0.29	0	77	0.16	0	81	0.57	0	86	–0.22
19200	0	51	0.16	0	54	0.62	0	58	–0.69	0	61	–0.24	0	64	0.16
28800	0	34	–0.79	0	36	–0.29	0	38	0.16	0	40	0.57	0	42	0.94
31250	0	31	0.00	0	33	0.00	0	35	0.00	0	37	0.00	0	39	0.00
38400	0	25	0.16	0	27	–1.18	0	28	1.02	0	30	–0.24	0	32	–1.36

Table 10.4 Maximum Bit Rate for Each Frequency when Using Baud Rate Generator (Asynchronous Mode)

Pϕ (MHz)	n	N	Maximum Bit Rate (bit/s)
4	0	0	125000
8	0	0	250000
10	0	0	312500
12	0	0	375000
14	0	0	437500
16	0	0	500000
18	0	0	562500
20	0	0	625000
22	0	0	687500
24	0	0	750000
25	0	0	781250
26	0	0	812500
28	0	0	875000
30	0	0	937500
32	0	0	1000000
34	0	0	1062500
36	0	0	1125000
38	0	0	1187500
40	0	0	1250000

Table 10.5 Maximum Bit Rate with External Clock Input (Asynchronous Mode)

Pϕ (MHz)	External Clock (MHz)	Maximum Bit Rate (bit/s)
4	1.0000	62500
6	1.5000	93750
8	2.0000	125000
10	2.5000	156250
12	3.0000	187500
14	3.5000	218750
16	4.0000	250000
18	4.5000	281250
20	5.0000	312500
22	5.5000	343750
24	6.0000	375000
25	6.2500	390625
26	6.5000	406250
28	7.0000	437500
30	7.5000	468750
32	8.0000	500000
34	8.5000	531250
36	9.0000	562500
38	9.5000	593750
40	10.0000	625000

Table 10.6 BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (1)

Logical Bit Rate (bit/s)	Operating Frequency Pϕ (MHz)									
	4		6		8		10		12	
	n	N	n	N	n	N	n	N	n	N
250	2	124	2	187	2	249	—	—	—	—
500	1	249	—	—	2	124	2	155	2	187
1000	1	124	1	187	1	249	—	—	—	—
2500	1	49	1	74	1	99	1	124	1	149
5000	1	24	—	—	1	49	—	—	1	74
10000	0	99	0	149	1	24	0	249	—	—
25000	0	39	0	59	1	9	0	99	1	14
50000	0	19	0	29	1	4	0	49	0	59
100000	0	9	0	14	0	19	0	24	0	29
250000	0	3	0	5	0	7	0	9	0	11
500000	0	1	0	2	0	3	0	4	0	5
1000000	0	0	—	—	0	1	—	—	0	2
2500000	—	—	—	—	—	—	0	0*	—	—
5000000	—	—	—	—	—	—	—	—	—	—

Table 10.6 BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (2)

Logical Bit Rate (bit/s)	Operating Frequency Pϕ (MHz)									
	14		16		18		20		22	
	n	N	n	N	n	N	n	N	n	N
250	3	108	3	124	3	140	3	155	3	171
500	2	218	2	249	—	—	—	—	—	—
1000	2	108	2	124	2	140	2	155	3	42
2500	1	174	2	49	1	224	1	249	—	—
5000	—	—	2	24	1	112	1	124	1	137
10000	—	—	1	49	—	—	—	—	—	—
25000	0	139	1	19	0	179	1	24	0	219
50000	0	69	1	9	0	89	0	99	0	109
100000	0	34	1	4	0	44	0	49	0	54
250000	0	13	1	1	0	17	0	19	0	21
500000	0	6	1	0	0	8	0	9	0	10
1000000	—	—	0	3	—	—	0	4	—	—
2500000	—	—	—	—	—	—	0	1	—	—
5000000	—	—	—	—	—	—	0	0*	—	—

Table 10.6 BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (3)

Logical Bit Rate (bit/s)	Operating Frequency Pϕ (MHz)									
	24		25		26		28		30	
	n	N	n	N	n	N	n	N	n	N
250	3	187	3	194	3	202	3	218	3	233
500	—	—	—	—	3	101	3	108	3	116
1000	2	187	2	194	2	202	2	218	2	233
2500	2	74	—	—	—	—	—	—	—	—
5000	1	149	1	155	1	162	1	174	1	187
10000	1	74	—	—	—	—	—	—	—	—
25000	1	29	0	249	—	—	1	34	—	—
50000	1	14	0	124	0	129	0	139	0	149
100000	0	59	—	—	0	64	0	69	0	74
250000	0	23	0	24	0	25	0	27	0	29
500000	0	11	—	—	0	12	0	13	0	14
1000000	0	5	—	—	—	—	0	6	—	—
2500000	—	—	—	—	—	—	—	—	0	2
5000000	—	—	—	—	—	—	—	—	—	—

Table 10.6 BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (4)

Logical Bit Rate (bit/s)	Operating Frequency Pϕ (MHz)									
	32		34		36		38		40	
	n	N	n	N	n	N	n	N	n	N
250	3	249	—	—	—	—	—	—	—	—
500	3	124	3	132	3	140	3	147	3	155
1000	2	249	—	—	—	—	—	—	—	—
2500	2	99	2	105	2	112	2	118	2	124
5000	2	49	1	212	1	224	1	237	1	249
10000	2	24	1	105	1	112	1	118	1	124
25000	2	9	—	—	1	44	—	—	1	49
50000	2	4	0	169	0	179	0	189	1	24
100000	1	9	0	84	0	89	0	94	0	99
250000	1	3	0	33	0	35	0	37	0	39
500000	1	1	0	16	0	17	0	18	0	19
1000000	1	0	—	—	0	8	—	—	0	9
2500000	—	—	—	—	—	—	—	—	0	3
5000000	—	—	—	—	—	—	—	—	0	1

Legend:
—: Can be set, but there will be a degree of error.
*: Continuous transfer is not possible.
Note: Settings with an error of 1% or less are recommended.

Table 10.7 Maximum Bit Rate with External Clock Input (Clocked Synchronous Mode)

Pϕ (MHz)	External Clock (MHz)	Maximum Bit Rate (bit/s)
4	0.6667	666666.7
6	1.0000	1000000.0
8	1.3333	1333333.3
10	1.6667	1666666.7
12	2.0000	2000000.0
14	2.3333	2333333.3
16	2.6667	2666666.7
18	3.0000	3000000.0
20	3.3333	3333333.3
22	3.6667	3666666.7
24	4.0000	4000000.0
25	4.1667	4166666.7
26	4.3333	4333333.3
28	4.6667	4666666.7
30	5.0000	5000000.0
32	5.3333	5333333.3
34	5.6667	5666666.7
36	6.0000	6000000.0
38	6.3333	6333333.3
40	6.6667	6666666.7

10.4 Operation in Asynchronous Mode

Figure 10.2 shows the general format for asynchronous serial communication. One frame consists of a start bit (low level), followed by data, a parity bit, and finally stop bits (high level). In asynchronous serial communication, the transmission line is usually held in the mark state (high level). The SCI monitors the communication line, and when it goes to the space state (low level), recognizes a start bit and starts serial communication. Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communication. Both the transmitter and the receiver also have a double-buffered structure, so that data can be read or written during transmission or reception, enabling continuous data transfer.

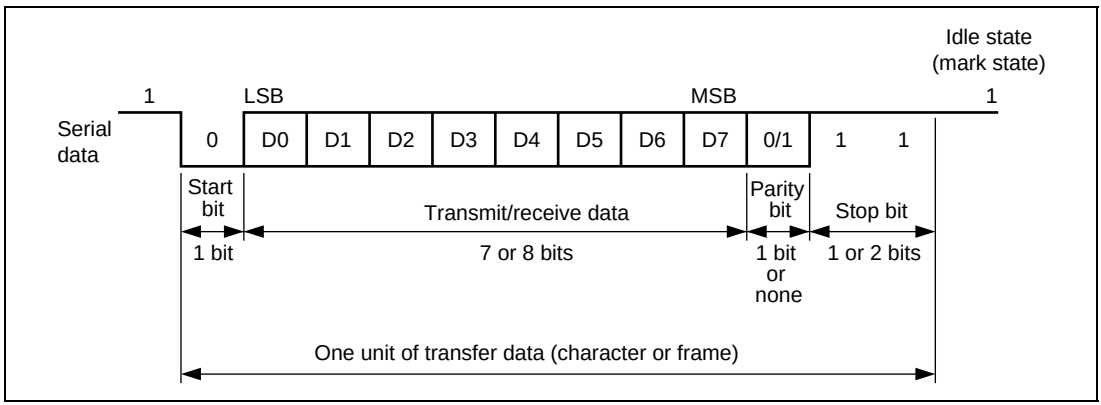


Figure 10.2 Data Format in Asynchronous Communication (Example with 8-Bit Data, Parity, Two Stop Bits)

10.4.1 Data Transfer Format

Table 10.8 shows the data transfer formats that can be used in asynchronous mode. Any of 12 transfer formats can be selected according to the SMR setting. For details on the multiprocessor bit, refer to section 10.5, Multiprocessor Communication Function.

Table 10.8 Serial Transfer Formats (Asynchronous Mode)

SMR Settings				Serial Transfer Format and Frame Length
CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12
0	0	0	0	S 8-bit data STOP
0	0	0	1	S 8-bit data STOP STOP
0	1	0	0	S 8-bit data P STOP
0	1	0	1	S 8-bit data P STOP STOP
1	0	0	0	S 7-bit data STOP
1	0	0	1	S 7-bit data STOP STOP
1	1	0	0	S 7-bit data P STOP
1	1	0	1	S 7-bit data P STOP STOP
0	X	1	0	S 8-bit data MPB STOP
0	X	1	1	S 8-bit data MPB STOP STOP
1	X	1	0	S 7-bit data MPB STOP
1	X	1	1	S 7-bit data MPB STOP STOP

Legend:
S: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multiprocessor bit
X: Don't care

10.4.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI operates on a basic clock with a frequency of 16 times the bit rate. In reception, the SCI samples the falling edge of the start bit using the basic clock, and performs internal synchronization. Receive data is latched internally at the rising edge of the 8th pulse of the basic clock as shown in figure 10.3. Thus the reception margin in asynchronous mode is given by formula (1) below.

$$M = \left\{ \left(0.5 - \frac{1}{2N}\right) - \frac{(D - 0.5)}{N} - (L - 0.5)\,F \right\} \times 100\% \quad \text{..... Formula (1)}$$

Where M: Reception margin (%)
N: Ratio of bit rate to clock (N = 16)
D: Clock duty cycle (D = 0 to 1.0)
L: Frame length (L = 9 to 12)
F: Absolute value of clock rate deviation

Assuming values of F = 0 and D = 0.5 in formula (1), a reception margin is given by formula below.

$$M = \{0.5 - 1/(2 \times 16)\} \times 100\ [\%] = 46.875\%$$

However, this is only the computed value, and a margin of 20% to 30% should be allowed in system design.

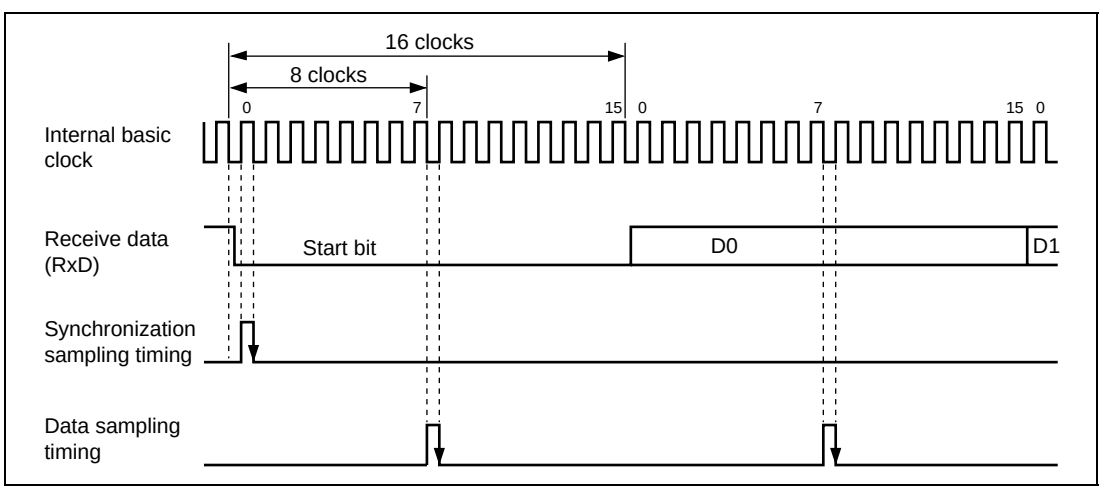


Figure 10.3 Receive Data Sampling Timing in Asynchronous Mode

10.4.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input at the SCK pin can be selected as the SCI's serial clock, according to the setting of the C/A bit in SMR and the CKE1 and CKE0 bits in SCR. When an external clock is input at the SCK pin, the clock frequency should be 16 times the bit rate used.

When the SCI is operated on an internal clock, the clock can be output from the SCK pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is in the middle of the transmit data, as shown in figure 10.4.

The clock must not be stopped during operation.

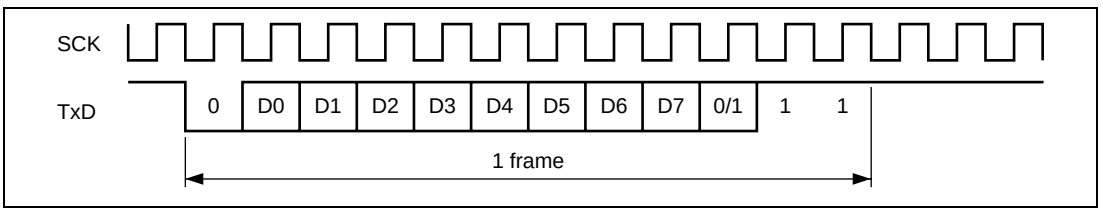
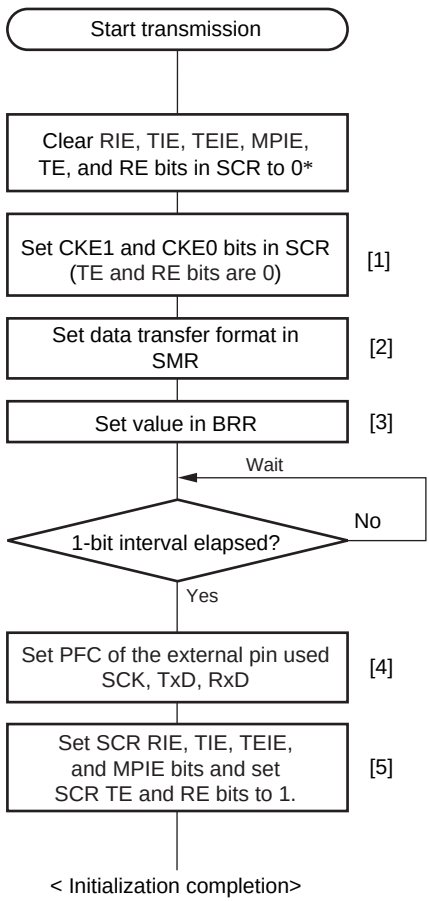


Figure 10.4 Relation between Output Clock and Transmit Data Phase (Asynchronous Mode)

10.4.4 SCI Initialization (Asynchronous Mode)

Before transmitting and receiving data, you should first clear the TE and RE bits in SCR to 0, then initialize the SCI as described below. When the operating mode, transfer format, etc., is changed, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, the TDRE flag is set to 1. Note that clearing the RE bit to 0 does not initialize the contents of the RDRF, PER, FER, and ORER flags, or the contents of RDR. When the external clock is used in asynchronous mode, the clock must be supplied even during initialization.



[1] Set the clock selection in SCR.
[2] Set the data transfer format in SMR and SCMR.
[3] Write a value corresponding to the bit rate to BRR. Not necessary if an external colck is used.
[4] Set PFC of the external pin used. Set RxD input during receiving and TxD output during transmitting. Set SCK input/output according to contents set by CKE1 and CKE0. When CKE1 and CKE0 are 0 in asynchronous mode, setting the SCK pin is unnecessary. Outputting clocks from the SCK pin starts at synchronous clock output setting.
[5] Wait at least one bit interval, then set the TE bit or RE bit in SCR to 1.* At this time, the TxD, RxD, and SCK pins can be used. The TxD pin is in a mark state during transmitting, and RxD pin is in an idle state for waiting the start bit during receiving.

Note : * In simultaneous transmit/receive operation, the TE and RE bits must be cleared to 0 or set to 1 simultaneously.

Figure 10.5 Sample SCI Initialization Flowchart

10.4.5 Data Transmission (Asynchronous Mode)

Figure 10.6 shows an example of the operation for transmission in asynchronous mode. In transmission, the SCI operates as described below.

1. The SCI monitors the TDRE flag in SSR, and if is cleared to 0, recognizes that data has been written to TDR, and transfers the data from TDR to TSR.
2. After transferring data from TDR to TSR, the SCI sets the TDRE flag to 1 and starts transmission. If the TIE bit is set to 1 at this time, a transmit data empty interrupt request (TXI) is generated. Because the TXI interrupt routine writes the next transmit data to TDR before transmission of the current transmit data has finished, continuous transmission can be enabled.
3. Data is sent from the TxD pin in the following order: start bit, transmit data, parity bit, or multiprocessor bit (may be omitted depending on the format), and stop bit.
4. The SCI checks the TDRE flag at the timing for sending the stop bit.
5. If the TDRE flag is 0, the data is transferred from TDR to TSR, the stop bit is sent, and then serial transmission of the next frame is started.
6. If the TDRE flag is 1, the TEND flag in SSR is set to 1, the stop bit is sent, and then the "mark state" is entered in which 1 is output. If the TEIE bit in SCR is set to 1 at this time, a TEI interrupt request is generated.

Figure 10.7 shows a sample flowchart for transmission in asynchronous mode.

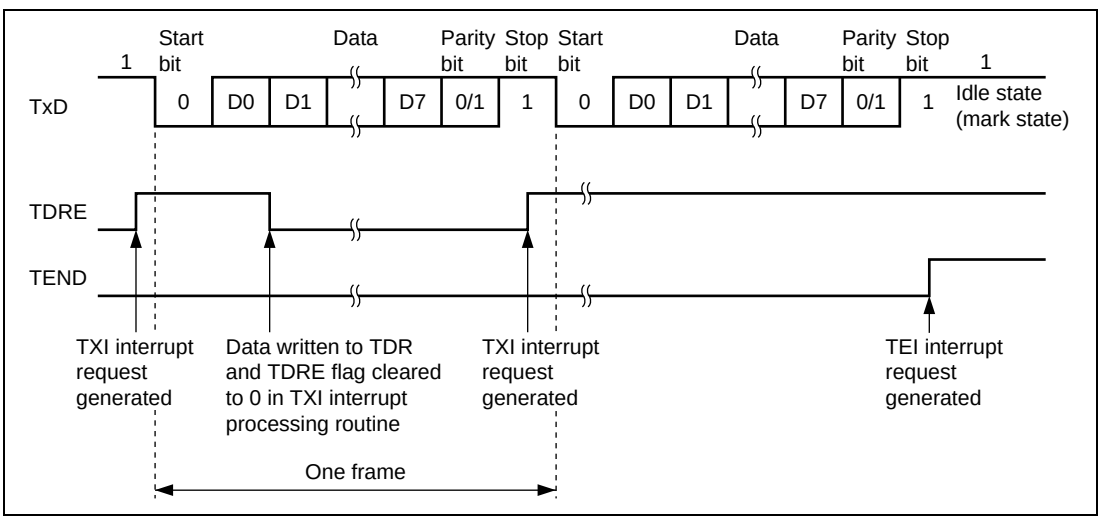
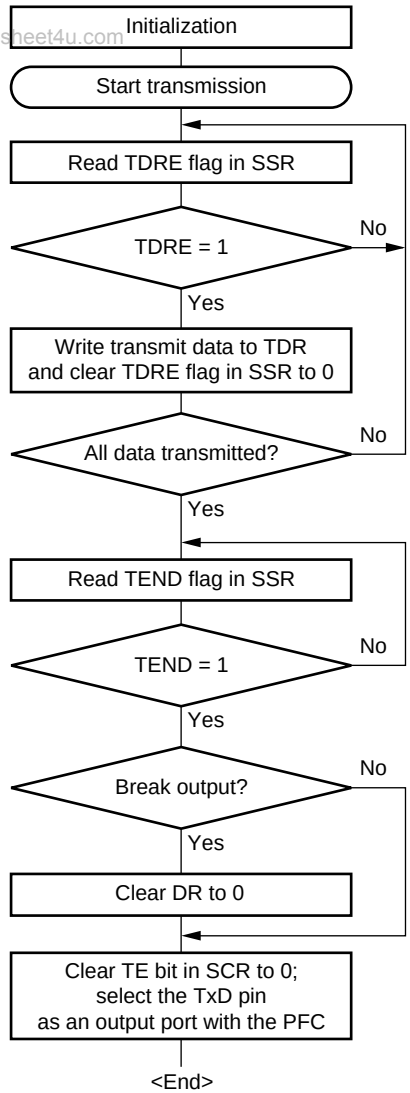


Figure 10.6 Example of Operation in Transmission in Asynchronous Mode (Example with 8-Bit Data, Parity, One Stop Bit)



[1] SCI initialization:
Set the TxD pin using the PFC. After the TE bit is set to 1, 1 is output for one frame, and transmission is enabled.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR and clear the TDRE flag to 0.

[3] Serial transmission continuation procedure:

To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR, and then clear the TDRE flag to 0.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, first clear the port data register (DR) to 0, then clear the TE bit to 0 in SCR and use the PFC to select the TxD pin as an output port.

Figure 10.7 Sample Serial Transmission Flowchart

10.4.6 Serial Data Reception (Asynchronous Mode)

Figure 10.8 shows an example of the operation for reception in asynchronous mode. In serial reception, the SCI operates as described below.

1. The SCI monitors the communication line, and if a start bit is detected, performs internal synchronization, receives receive data in RSR, and checks the parity bit and stop bit.
2. If an overrun error (when reception of the next data is completed while the RDRF flag is still set to 1) occurs, the OER bit in SSR is set to 1. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to RDR. The RDRF flag remains to be set to 1.
3. If a parity error is detected, the PER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated.
4. If a framing error (when the stop bit is 0) is detected, the FER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated.
5. If reception finishes successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI interrupt request is generated. Because the RXI interrupt processing routine reads the receive data transferred to RDR before reception of the next receive data has finished, continuous reception can be enabled.

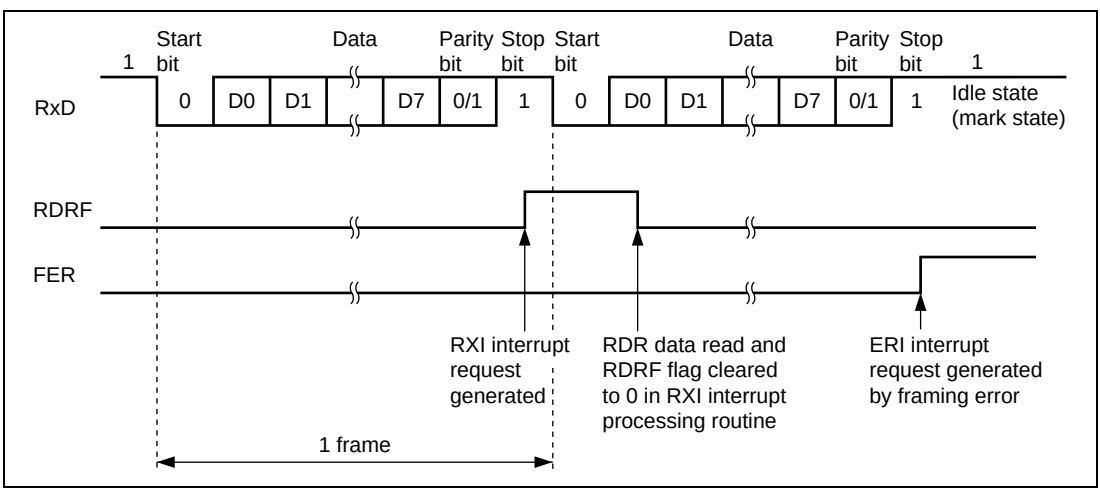


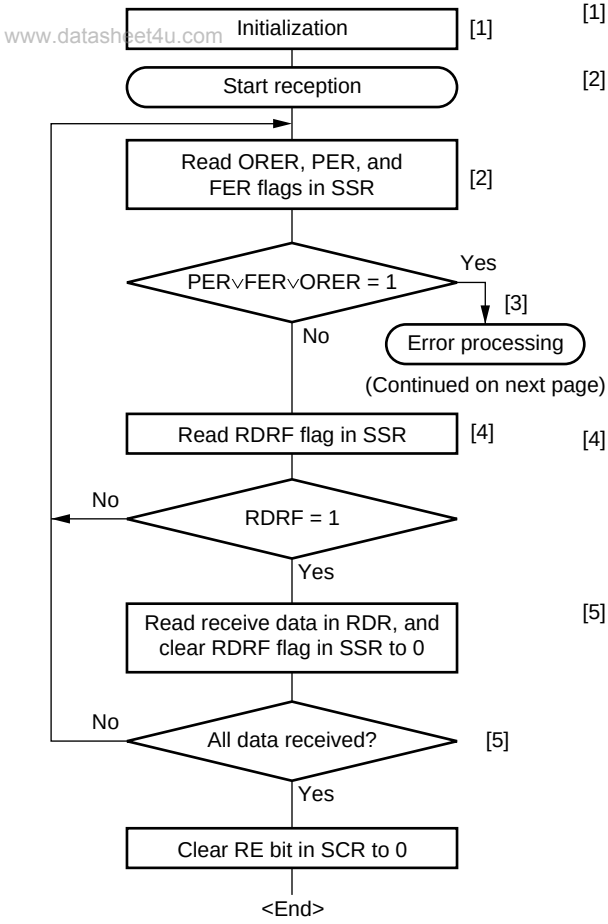
Figure 10.8 Example of SCI Operation in Reception (Example with 8-Bit Data, Parity, One Stop Bit)

Table 10.9 shows the states of the SSR status flags and receive data handling when a receive error is detected. If a receive error is detected, the RDRF flag retains its state before receiving data. Reception cannot be resumed while a receive error flag is set to 1. Accordingly, clear the OER, FER, PER, and RDRF bits to 0 before resuming reception. Figure 10.9 shows a sample flowchart for serial data reception.

Table 10.9 SSR Status Flags and Receive Data Handling

SSR Status Flag					
RDRF*	**OER**	**FER**	**PER**	**Receive Data**	**Receive Error Type**
1	1	0	0	Lost	Overrun error
0	0	1	0	Transferred to RDR	Framing error
0	0	0	1	Transferred to RDR	Parity error
1	1	1	0	Lost	Overrun error + framing error
1	1	0	1	Lost	Overrun error + parity error
0	0	1	1	Transferred to RDR	Framing error + parity error
1	1	1	1	Lost	Overrun error + framing error + parity error

Note: * The RDRF flag retains its state before data reception.



[1] SCI initialization:
Set the RxD pin using the PFC.

[2] [3] Receive error processing and break detection:
If a receive error occurs, read the ORER, PER, and FER flags in SSR to identify the error. After performing the appropriate error processing, ensure that the ORER, PER, and FER flags are all cleared to 0. Reception cannot be resumed if any of these flags are set to 1. In the case of a framing error, a break can be detected by reading the value of the input port corresponding to the RxD pin.

[4] SCI status check and receive data read:
Read SSR and check that RDRF = 1, then read the receive data in RDR and clear the RDRF flag to 0. Transition of the RDRF flag from 0 to 1 can also be identified by an RXI interrupt.

[5] Serial reception continuation procedure:
To continue serial reception, before the stop bit for the current frame is received, read the RDRF flag, read RDR, and clear the RDRF flag to 0.

Figure 10.9 Sample Serial Reception Data Flowchart (1)

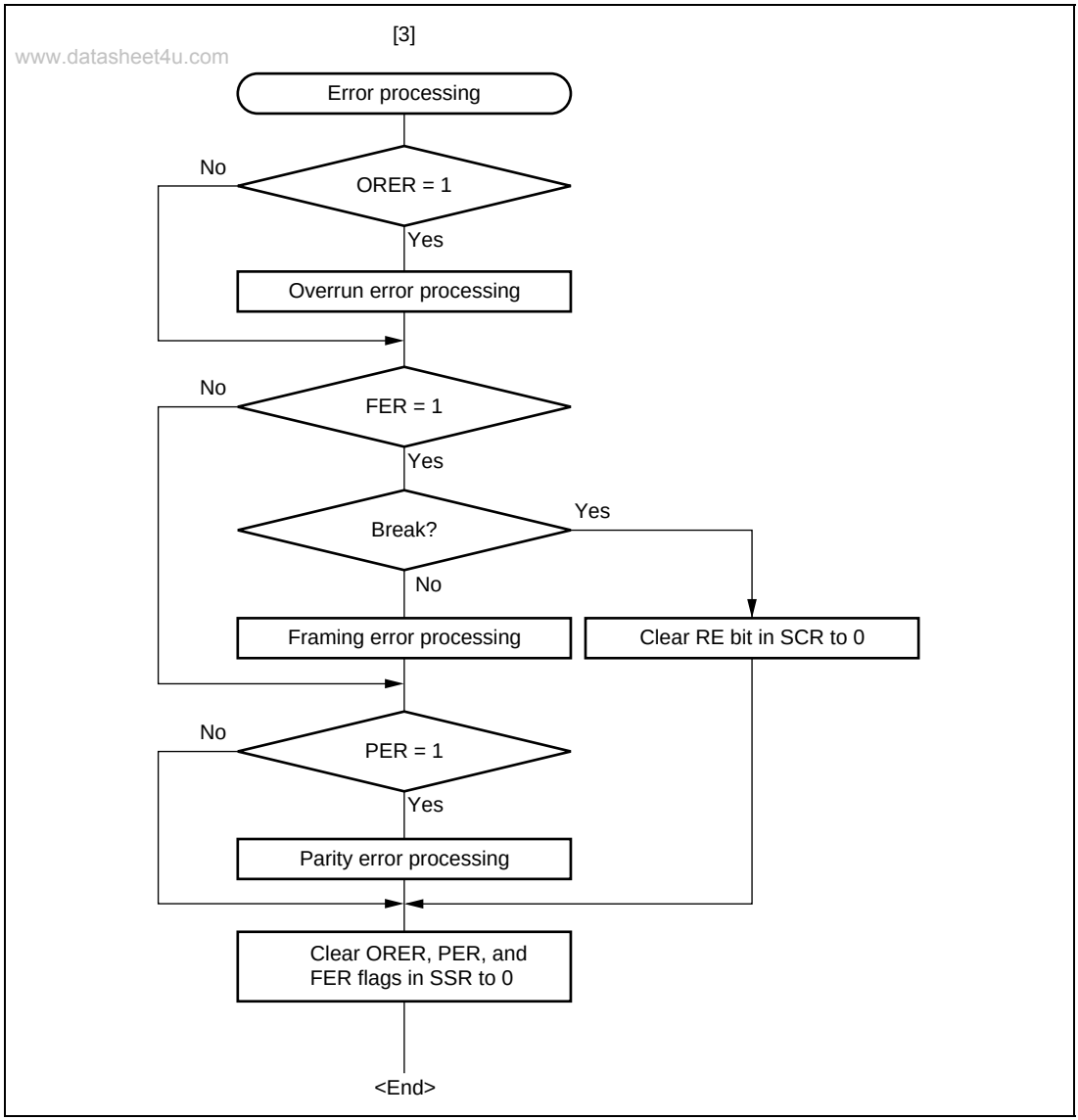


Figure 10.9 Sample Serial Reception Data Flowchart (2)

10.5 Multiprocessor Communication Function

Use of the multiprocessor communication function enables data transfer to be performed among a number of processors sharing communication lines by means of asynchronous serial communication using the multiprocessor format, in which a multiprocessor bit is added to the transfer data. When multiprocessor communication is carried out, each receiving station is addressed by a unique ID code. The serial communication cycle consists of two component cycles: an ID transmission cycle which specifies the receiving station, and a data transmission cycle. The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle. If the multiprocessor bit is 1, the cycle is an ID transmission cycle, and if the multiprocessor bit is 0, the cycle is a data transmission cycle. Figure 10.10 shows an example of inter-processor communication using the multiprocessor format. The transmitting station first sends the ID code of the receiving station with which it wants to perform serial communication as data with a 1 multiprocessor bit added. It then sends transmit data as data with a 0 multiprocessor bit added. The receiving station skips data until data with a 1 multiprocessor bit is sent. When data with a 1 multiprocessor bit is received, the receiving station compares that data with its own ID. The station whose ID matches then receives the data sent next. Stations whose ID does not match continue to skip data until data with a 1 multiprocessor bit is again received.

The SCI uses the MPIE bit in SCR to implement this function. When the MPIE bit is set to 1, transfer of receive data from RSR to RDR, error flag detection, and setting the SSR status flags, RDRF, FER, and OER to 1 are inhibited until data with a 1 multiprocessor bit is received. On reception of receive character with a 1 multiprocessor bit, the MPBR bit in SSR is set to 1 and the MPIE bit is automatically cleared, thus normal reception is resumed. If the RIE bit in SCR is set to 1 at this time, an RXI interrupt is generated.

When the multiprocessor format is selected, the parity bit setting is invalid. All other bit settings are the same as those in normal asynchronous mode. The clock used for multiprocessor communication is the same as that in normal asynchronous mode.

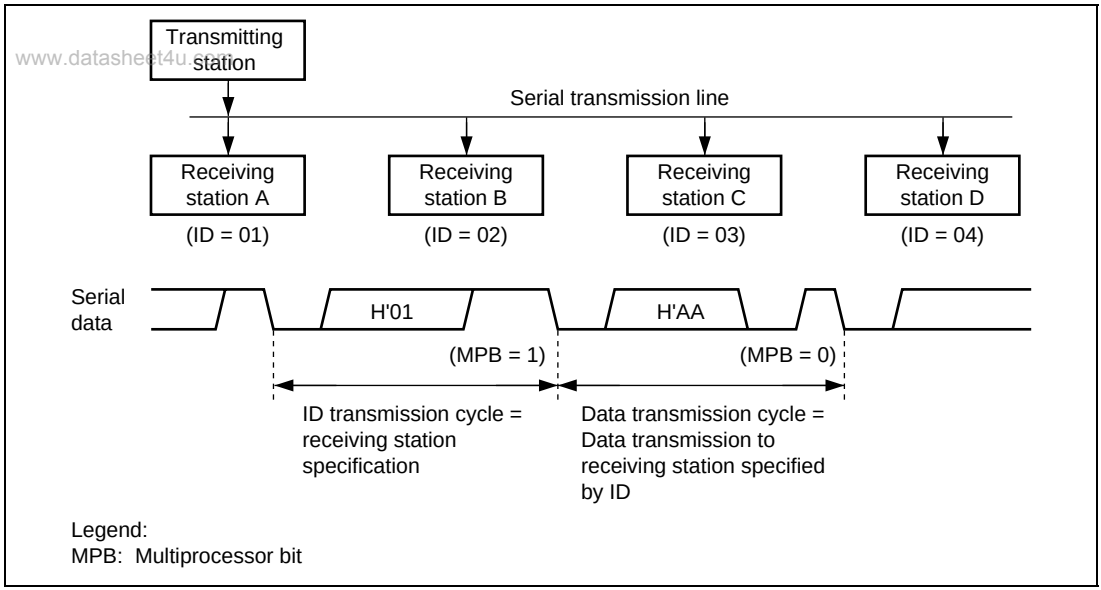


Figure 10.10 Example of Communication Using Multiprocessor Format (Transmission of Data H'AA to Receiving Station A)

10.5.1 Multiprocessor Serial Data Transmission

Figure 10.11 shows a sample flowchart for multiprocessor serial data transmission. For an ID transmission cycle, set the MPBT bit in SSR to 1 before transmission. For a data transmission cycle, clear the MPBT bit in SSR to 0 before transmission. All other SCI operations are the same as those in asynchronous mode.

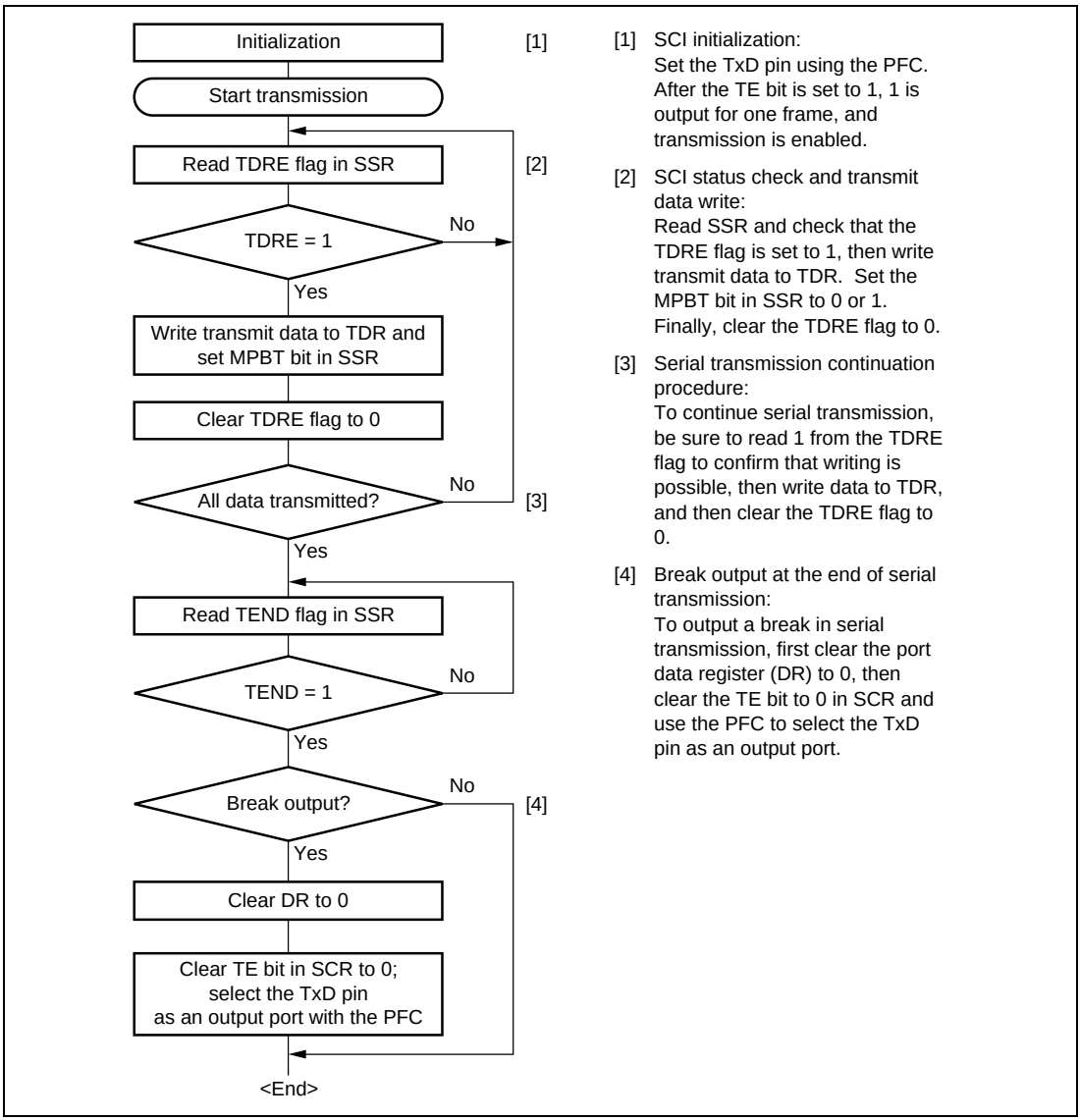


Figure 10.11 Sample Multiprocessor Serial Transmission Flowchart

10.5.2 Multiprocessor Serial Data Reception

Figure 10.13 shows a sample flowchart for multiprocessor serial data reception. If the MPIE bit in SCR is set to 1, data is skipped until data with a 1 multiprocessor bit is sent. On receiving data with a 1 multiprocessor bit, the receive data is transferred to RDR. An RXI interrupt request is generated at this time. All other SCI operations are the same as in asynchronous mode. Figure 10.12 shows an example of SCI operation for multiprocessor format reception.

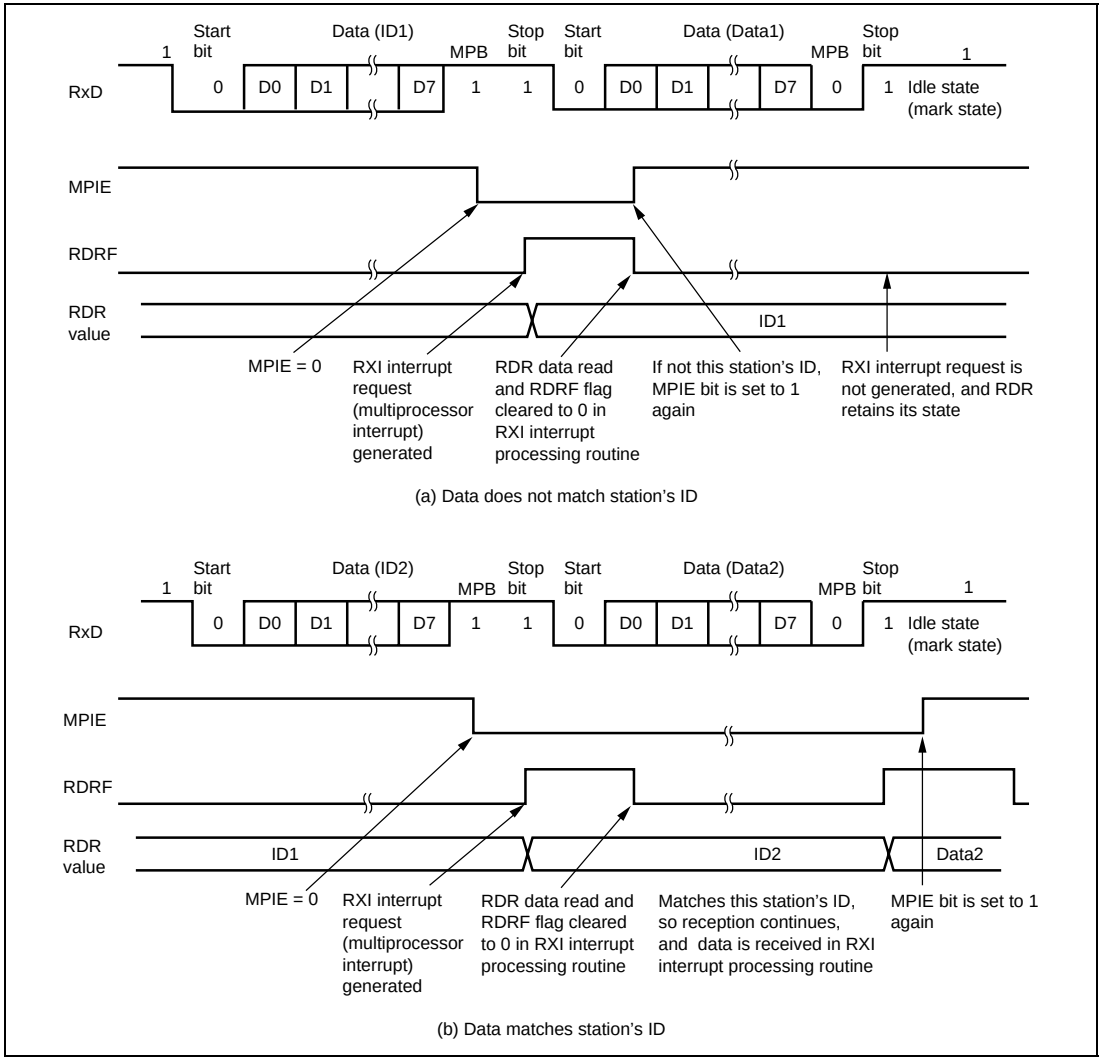
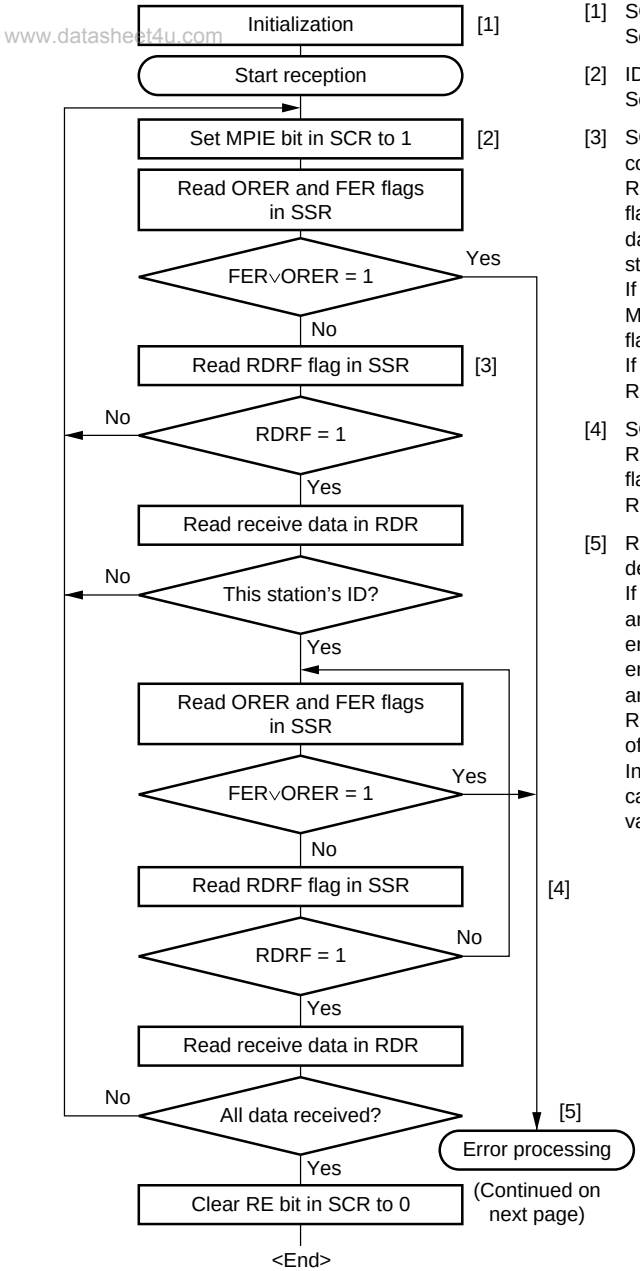


Figure 10.12 Example of SCI Operation in Reception (Example with 8-Bit Data, Multiprocessor Bit, One Stop Bit)



[1] SCI initialization:
Set the RxD pin using the PFC.

[2] ID reception cycle:
Set the MPIE bit in SCR to 1.

[3] SCI status check, ID reception and comparison:
Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR and compare it with this station's ID.
If the data is not this station's ID, set the MPIE bit to 1 again, and clear the RDRF flag to 0.
If the data is this station's ID, clear the RDRF flag to 0.

[4] SCI status check and data reception:
Read SSR and check that the RDRF flag is set to 1, then read the data in RDR.

[5] Receive error processing and break detection:
If a receive error occurs, read the ORER and FER flags in SSR to identify the error. After performing the appropriate error processing, ensure that the ORER and FER flags are all cleared to 0. Reception cannot be resumed if either of these flags is set to 1.
In the case of a framing error, a break can be detected by reading the RxD pin value.

Figure 10.13 Sample Multiprocessor Serial Reception Flowchart (1)

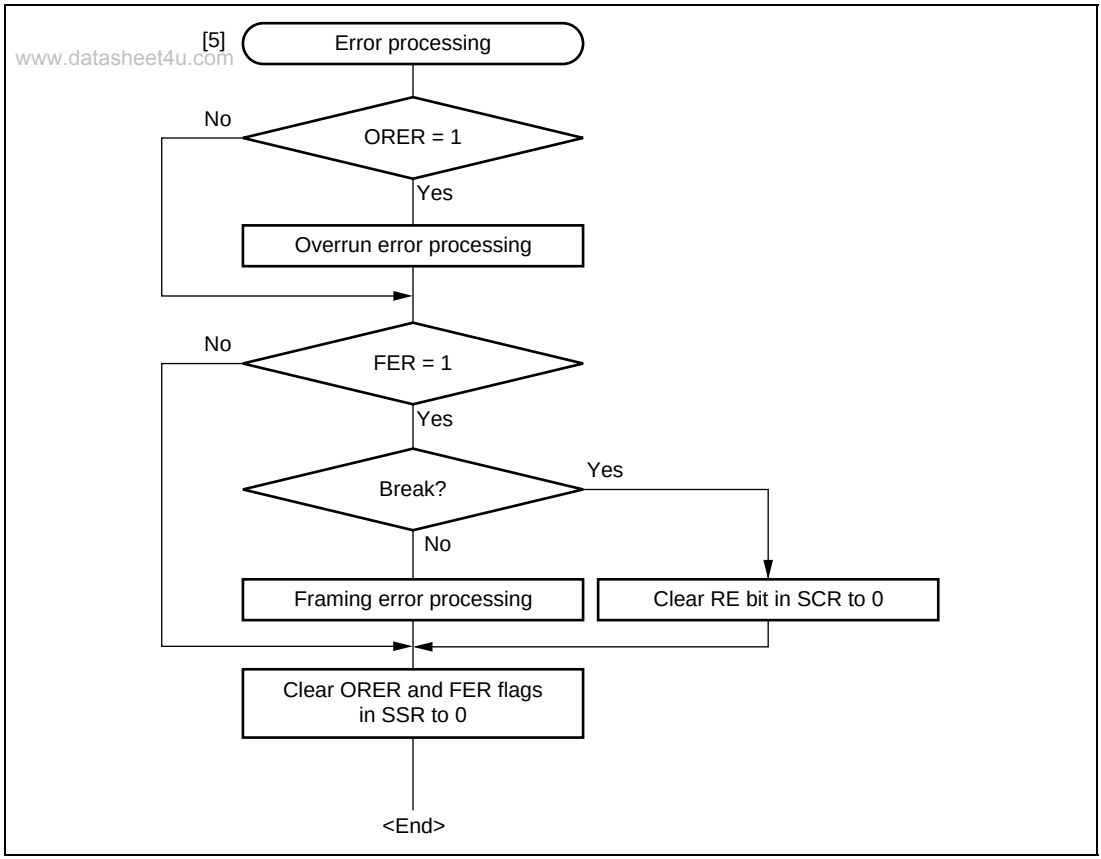


Figure 10.13 Sample Multiprocessor Serial Reception Flowchart (2)

10.6 Operation in Clocked Synchronous Mode

Figure 10.14 shows the general format for clocked synchronous communication. In clocked synchronous mode, data is transmitted or received in synchronization with clock pulses. Data is transferred in 8-bit units. In clocked synchronous serial communication, data on the transmission line is output from one falling edge of the serial clock to the next. In clocked synchronous mode, the SCI receives data in synchronization with the rising edge of the serial clock. After 8-bit data is output, the transmission line holds the MSB state. In clocked synchronous mode, no parity or multiprocessor bit is added. Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communication by use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so that data can be read or written during transmission or reception, enabling continuous data transfer.

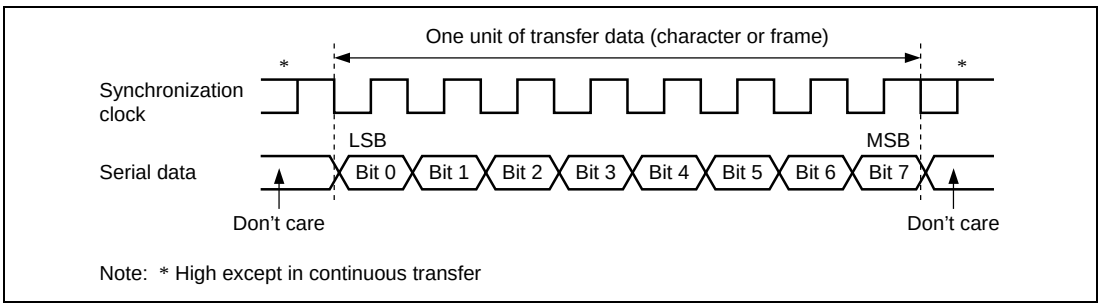


Figure 10.14 Data Format in Clocked Synchronous Communication (For LSB-First)

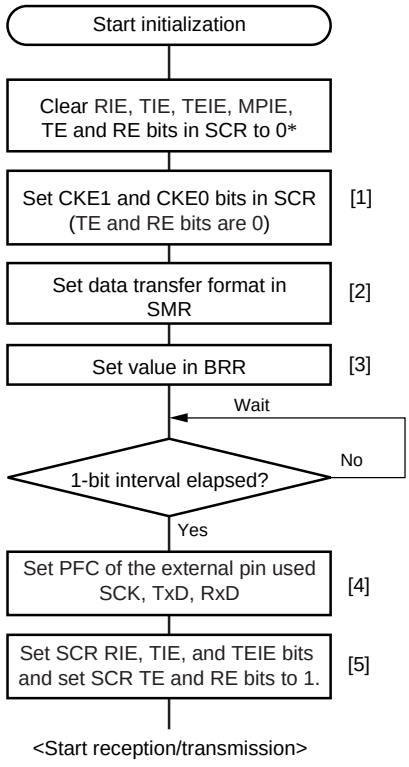
10.6.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCK pin can be selected, according to the setting of the CKE1 and CKE0 bits in SCR. When the SCI is operated on an internal clock, the serial clock is output from the SCK pin. Eight serial clock pulses are output in the transfer of one character, and when no transfer is performed, the clock is fixed high. Note, however, that in receive mode only, the sync clock will be output until either an overrun error occurs or the RE bit is cleared to 0. Select the external clock as the clock source to perform reception operations in single character units.

10.6.2 SCI Initialization (Clocked Synchronous Mode)

Before transmitting and receiving data, you should first clear the TE and RE bits in SCR to 0, then initialize the SCI as described in a sample flowchart in figure 10.15. When the operating mode, transfer format, etc., is changed, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, the TDRE flag is set to 1.

Note that clearing the RE bit to 0 does not initialize the RDRF, PER, FER, and ORER flags, or the contents of RDR.



[1] Set the clock selection in SCR.

[2] Set the data transfer format in SMR.

[3] Write a value corresponding to the bit rate to BRR. Not necessary if an external clock is used.

[4] Set PFC of the external pin used. Set RxD input during receiving and TxD output during transmitting. Set SCK input/output according to contents set by the CKE1 and CKE0 bits.

[5] Wait at least one bit interval, then set the TE bit or RE bit in SCR to 1.* At this time, the TxD, RxD, and SCK pins can be used. The TxD pin is in a mark state during transmitting. When synchronous clock output (clock master) is set during receiving in clocked synchronous mode, outputting clocks from the SCK pin starts.

Note: * In simultaneous transmit and receive operations, the TE and RE bits should both be cleared to 0 or set to 1 simultaneously.

Figure 10.15 Sample SCI Initialization Flowchart

10.6.3 Serial Data Transmission (Clocked Synchronous Mode)

Figure 10.16 shows an example of SCI operation for transmission in clocked synchronous mode. In serial transmission, the SCI operates as described below.

1. The SCI monitors the TDRE flag in SSR, and if it is cleared to 0, recognizes that data has been written to TDR, and transfers the data from TDR to TSR.
2. After transferring data from TDR to TSR, the SCI sets the TDRE flag to 1 and starts transmission. If the TIE bit in SCR is set to 1 at this time, a transmit data empty (TXI) interrupt request is generated. Because the TXI interrupt routine writes the next transmit data

to TDR before transmission of the current transmit data has finished, continuous transmission can be enabled.

3. 8-bit data is sent from the TxD pin synchronized with the output clock when output clock mode has been specified and synchronized with the input clock when use of an external clock has been specified.
4. The SCI checks the TDRE flag at the timing for sending the MSB (bit 7).
5. If the TDRE flag is cleared to 0, data is transferred from TDR to TSR, and serial transmission of the next frame is started.
6. If the TDRE flag is set to 1, the TEND flag in SSR is set to 1, and the TxD pin maintains the output state of the last bit. If the TEIE bit in SCR is set to 1 at this time, a TEI interrupt request is generated. The SCK pin is fixed high.

Figure 10.17 shows a sample flowchart for serial data transmission. Even if the TDRE flag is cleared to 0, transmission will not start while a receive error flag (ORER, FER, or PER) is set to 1. Make sure to clear the receive error flags to 0 before starting transmission. Note that clearing the RE bit to 0 does not clear the receive error flags.

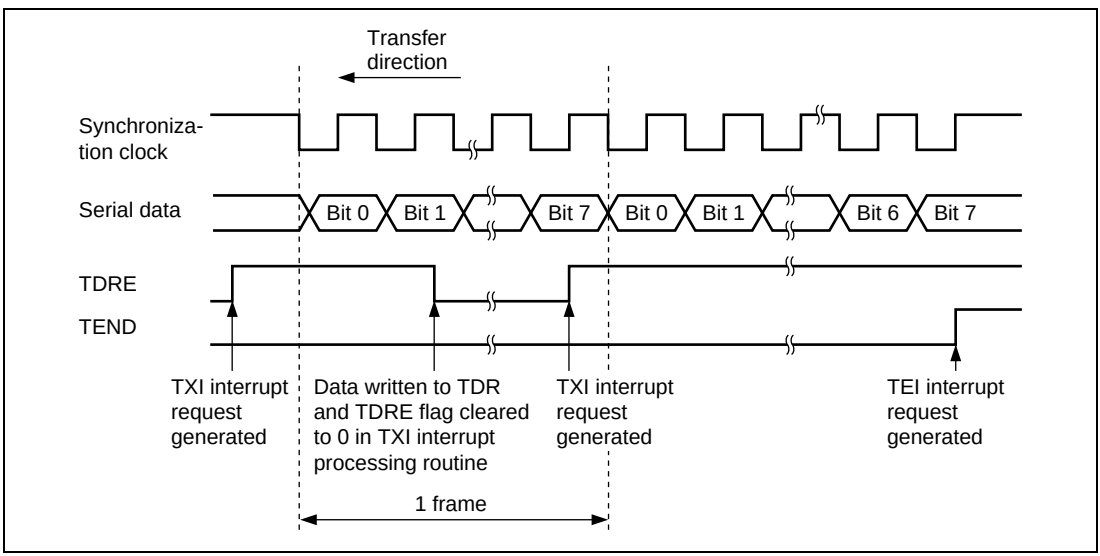
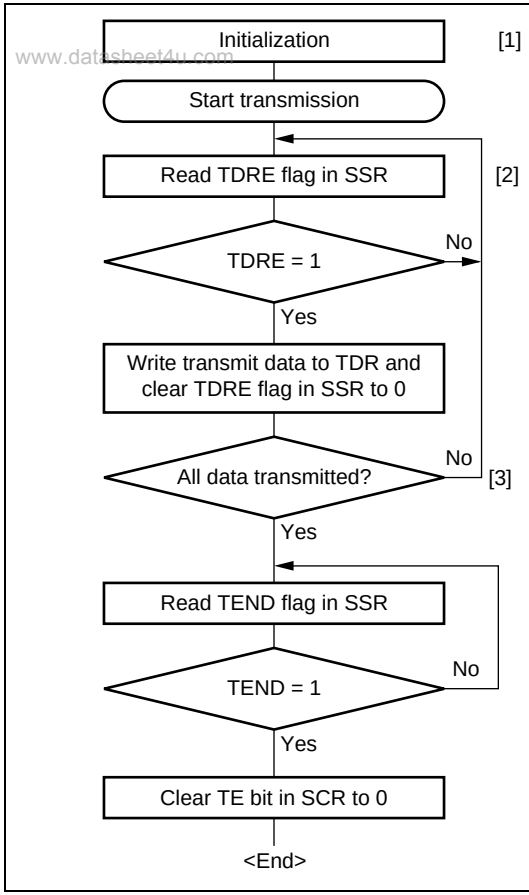


Figure 10.16 Sample SCI Transmission Operation in Clocked Synchronous Mode



[1] SCI initialization:
Set the TxD pin using the PFC.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR and clear the TDRE flag to 0.

[3] Serial transmission continuation procedure:
To continue serial transmission, be sure to read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR, and then clear the TDRE flag to 0.

Figure 10.17 Sample Serial Transmission Flowchart

10.6.4 Serial Data Reception (Clocked Synchronous Mode)

Figure 10.18 shows an example of SCI operation for reception in clocked synchronous mode. In serial reception, the SCI operates as described below.

1. The SCI performs internal initialization in synchronization with a synchronization clock input or output, starts receiving data, and stores the received data in RSR.
2. If an overrun error (when reception of the next data is completed while the RDRF flag is still set to 1) occurs, the ORER bit in SSR is set to 1. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to RDR. The RDRF flag remains to be set to 1.
3. If reception finishes successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI interrupt request is generated. Because the RXI interrupt processing routine reads the receive data transferred to RDR before reception of the next receive data has finished, continuous reception can be enabled.

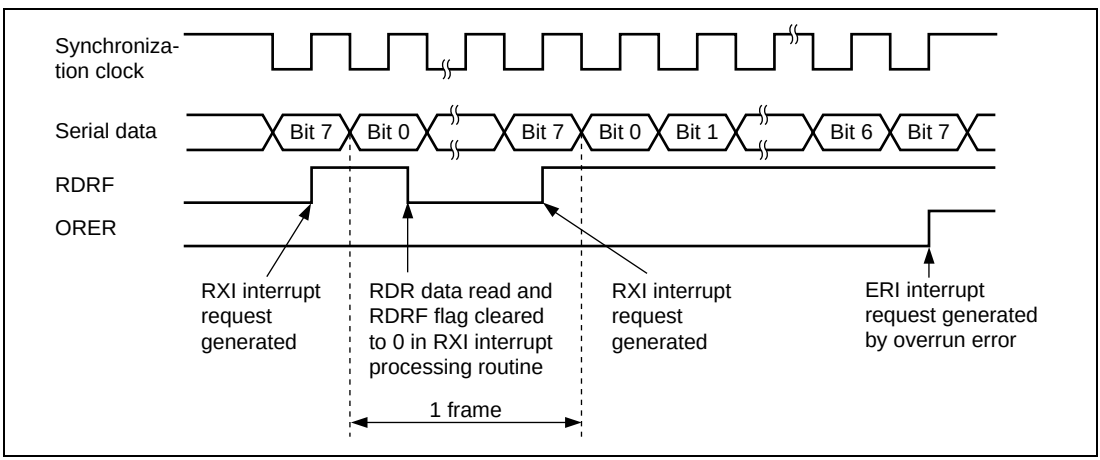


Figure 10.18 Example of SCI Operation in Reception

Reception cannot be resumed while a receive error flag is set to 1. Accordingly, clear the ORER, FER, PER, and RDRF bits to 0 before resuming reception. Figure 10.19 shows a sample flowchart for serial data reception.

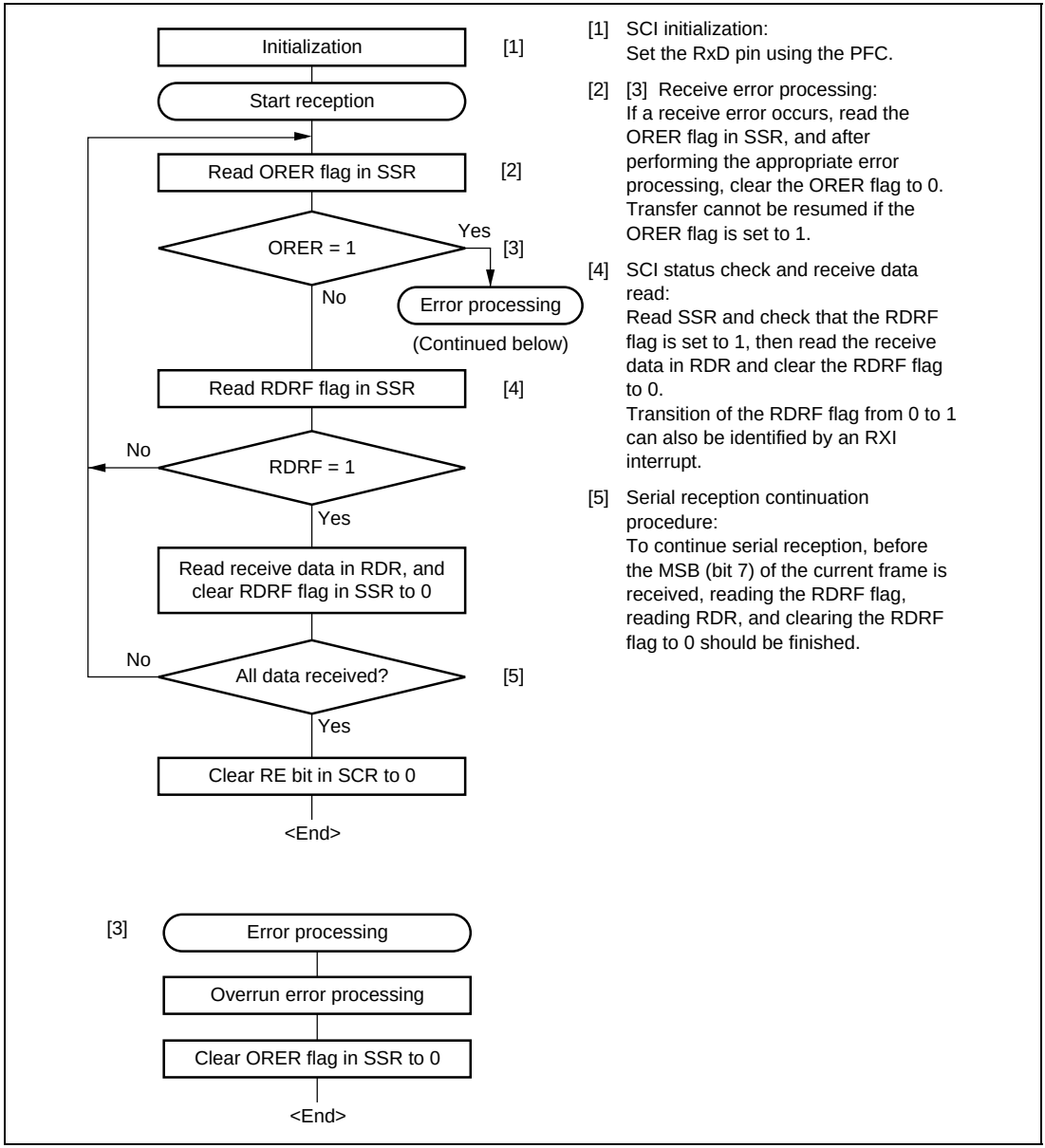
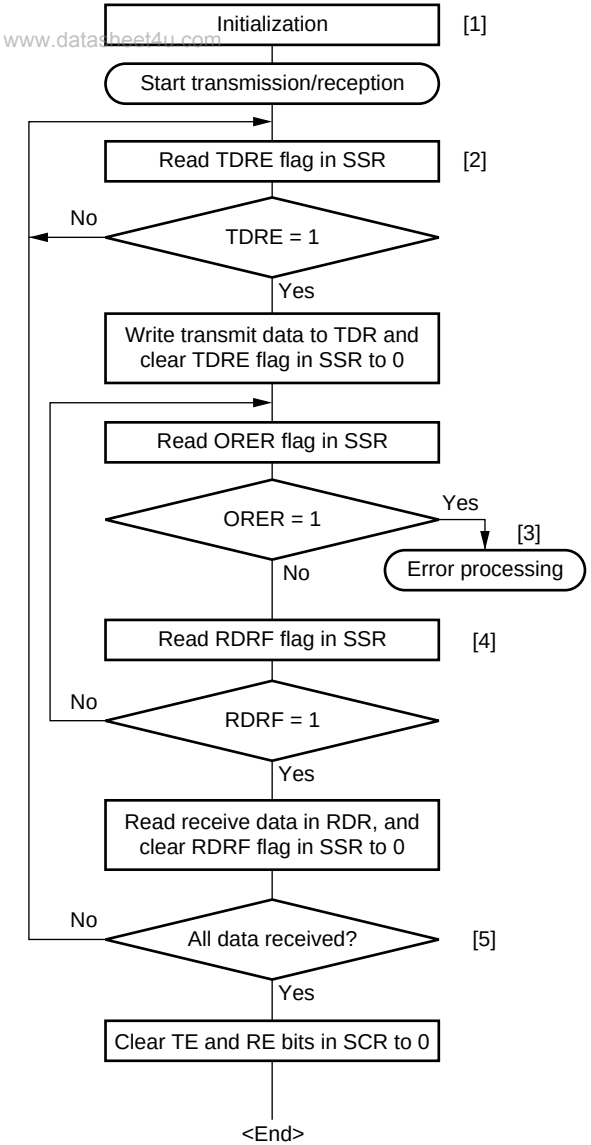


Figure 10.19 Sample Serial Reception Flowchart

10.6.5 Simultaneous Serial Data Transmission and Reception (Clocked Synchronous Mode)

Figure 10.20 shows a sample flowchart for simultaneous serial transmit and receive operations. The following procedure should be used for simultaneous serial data transmit and receive operations after the SCI initialization. To switch from transmit mode to simultaneous transmit and receive mode, after checking that the SCI has finished transmission and the TDRE and TEND flags are set to 1, clear TE to 0. Then simultaneously set TE and RE to 1 with a single instruction. To switch from receive mode to simultaneous transmit and receive mode, after checking that the SCI has finished reception, clear RE to 0. Then after checking that the RDRF and receive error flags (ORER, FER, and PER) are cleared to 0, simultaneously set TE and RE to 1 with a single instruction.



[1] SCI initialization:
Set the TxD and RxD pins using the PFC.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR and clear the TDRE flag to 0. Transition of the TDRE flag from 0 to 1 can also be identified by a TXI interrupt.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR, and after performing the appropriate error processing, clear the ORER flag to 0. Transmission/reception cannot be resumed if the ORER flag is set to 1.

[4] SCI status check and receive data read:
Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR and clear the RDRF flag to 0. Transition of the RDRF flag from 0 to 1 can also be identified by an RXI interrupt.

[5] Serial transmission/reception continuation procedure:
To continue serial transmission/reception, before the MSB (bit 7) of the current frame is received, finish reading the RDRF flag, reading RDR, and clearing the RDRF flag to 0. Also, before the MSB (bit 7) of the current frame is transmitted, read 1 from the TDRE flag to confirm that writing is possible. Then write data to TDR and clear the TDRE flag to 0.

Note: When switching from transmit or receive operation to simultaneous transmit and receive operations, first clear the TE bit and RE bit to 0, then set both these bits to 1 simultaneously.

Figure 10.20 Sample Flowchart of Simultaneous Serial Transmit and Receive Operations

10.7 Interrupt Sources

10.7.1 Interrupts in Normal Serial Communication Interface Mode

Table 10.10 shows the interrupt sources in normal serial communication interface mode. A different interrupt vector is assigned to each interrupt source, and individual interrupt sources can be enabled or disabled using the enable bits in SCR.

When the TDRE flag in SSR is set to 1, a TXI interrupt request is generated. When the TEND flag in SSR is set to 1, a TEI interrupt request is generated.

When the RDRF flag in SSR is set to 1, an RXI interrupt request is generated. When the ORER, PER, or FER flag in SSR is set to 1, an ERI interrupt request is generated.

A TEI interrupt is generated when the TEND flag is set to 1 while the TEIE bit is set to 1. If a TEI interrupt and a TXI interrupt are generated simultaneously, the TXI interrupt has priority for acceptance. However, note that if the TDRE and TEND flags are cleared simultaneously by the TXI interrupt routine, the SCI cannot branch to the TEI interrupt routine later.

Table 10.10 SCI Interrupt Sources

Channel	Name	Interrupt Source	Interrupt Flag
2	ERI_2	Receive error	ORER, FER, PER
	RXI_2	Receive data full	RDRF
	TXI_2	Transmit data empty	TDRE
	TEI_2	Transmission end	TEND
3	ERI_3	Receive error	ORER, FER, PER
	RXI_3	Receive data full	RDRF
	TXI_3	Transmit data empty	TDRE
	TEI_3	Transmission end	TEND

10.8 Usage Notes

10.8.1 TDR Write and TDRE Flag

The TDRE bit in the serial status register (SSR) is a status flag indicating transferring of transmit data from TDR into TSR. The SCI sets the TDRE bit to 1 when it transfers data from TDR to TSR.

Data can be written to TDR regardless of the TDRE bit status.

If new data is written in TDR when the TDRE bit is 0, however, the old data stored in TDR will be lost because the data has not yet been transferred to TSR. Before writing transmit data to TDR, be sure to check that the TDRE bit is set to 1.

10.8.2 Module Standby Mode Setting

SCI operation can be disabled or enabled using the module standby control register. The initial setting is for SCI operation to be halted. Register access is enabled by clearing module standby mode. For details, refer to section 18, Power-Down Modes.

10.8.3 Break Detection and Processing (Asynchronous Mode Only)

When framing error detection is performed, a break can be detected by reading the RxD pin value directly. In a break, the input from the RxD pin becomes all 0s, and so the FER flag is set, and the PER flag may also be set. Note that, since the SCI continues the receive operation after receiving a break, even if the FER flag is cleared to 0, it will be set to 1 again.

10.8.4 Sending Break Signal (Asynchronous Mode Only)

The TxD pin becomes of the I/O port general I/O pin with the I/O direction and level determined by the port data register (DR) and the port I/O register (IOR) of the pin function controller (PFC). These conditions allow break signals to be sent.

The DR value is substituted for the marking status until the PFC is set. Consequently, the output port is set to initially output a 1.

To send a break in serial transmission, first clear the DR to 0, then establish the TxD pin as an output port using the PFC.

When the TE bit is cleared to 0, the transmission section is initialized regardless of the present transmission status.

10.8.5 Receive Error Flags and Transmit Operations (Clocked Synchronous Mode Only)

Transmission cannot be started when a receive error flag (ORER, PER, or FER) is set to 1, even if the TDRE flag is cleared to 0. Be sure to clear the receive error flags to 0 before starting transmission. Note also that receive error flags cannot be cleared to 0 even if the RE bit is cleared to 0.

10.8.6 Cautions on Clocked Synchronous External Clock Mode

1. Set TE = RE = 1 only when external clock SCK is 1.
2. Do not set TE = RE = 1 until at least four Pϕ clocks after external clock SCK has changed from 0 to 1.
3. When receiving, RDRF is 1 when RE is cleared to 0 after 2.5 to 3.5 Pϕ clocks from the rising edge of the SCK input of the D7 bit in RxD, but copying to RDR is not possible.

10.8.7 Caution on Clocked Synchronous Internal Clock Mode

When receiving, RDRF is 1 when RE is cleared to 0 after 1.5 Pϕ clocks from the rising edge of the SCK output of the D7 bit in RxD, but copying to RDR is not possible.

Section 11 A/D Converter

This LSI includes a successive approximation type 10-bit A/D converter. The block diagram of the A/D converter is shown in figure 11.1.

11.1 Features

- 10-bit resolution
- Input channels

  SH7108: 12 channels (three independent A/D conversion modules)

  SH7109: 16 channels (two independent A/D conversion modules)
- Conversion time: 6.7 μs (at Pϕ = 20-MHz operation) or 5.4 μs (at Pϕ = 25-MHz operation) per channel
- Three operating modes

  Single mode: Single-channel A/D conversion

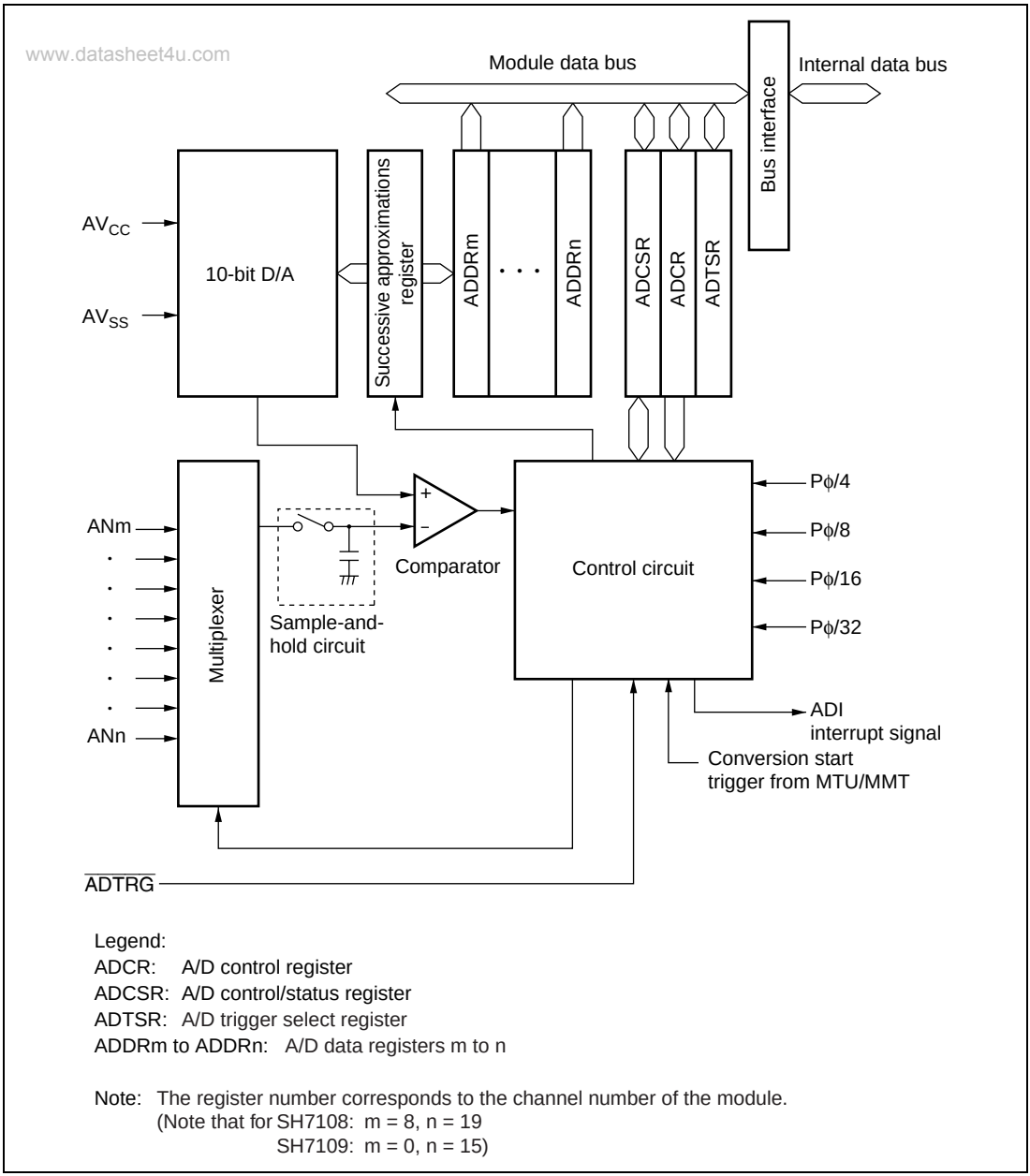
  Continuous scan mode: Repetitive A/D conversion on 1 to 4 channels in the SH7108 and on 1 to 8 channels in the SH7109

  Single-cycle scan mode: Continuous A/D conversion on 1 to 4 channels in the SH7108 and on 1 to 8 channels in the SH7109
- Data registers: Conversion results are held in a 16-bit data register for each channel
- Sample and hold function
- Three methods for conversion start

  Software

  Conversion start trigger from multifunction timer pulse unit (MTU) or motor management timer (MMT)

  External trigger signal
- Interrupt request: An A/D conversion end interrupt request (ADI) can be generated
- Module standby mode can be set



Legend:
ADCR: A/D control register
ADCSR: A/D control/status register
ADTSR: A/D trigger select register
ADDRm to ADDRn: A/D data registers m to n

Note: The register number corresponds to the channel number of the module.
(Note that for SH7108: m = 8, n = 19
SH7109: m = 0, n = 15)

Figure 11.1 Block Diagram of A/D Converter (For One Module)

11.2 Input/Output Pins

Table 11.1 summarizes the input pins used by the A/D converter. The SH7108 has three A/D conversion modules and the SH7109 two A/D conversion modules, each of which can be operated independently. The input channels are divided into four channel sets.

The analog input pins that can be used differ in each product type, as shown in table 11.1.

Table 11.1 Pin Configuration

					Product Type	
Module Type	**Pin Name**	**I/O**	**Function**		**SH7108**	**SH7109**
Common	AV_{CC}	Input	Analog block power supply and reference voltage		Usable	Usable
	AV_{SS}	Input	Analog block ground and reference voltage		Usable	Usable
	$\overline{ADTRG}$	Input	A/D external trigger input pin		Usable	Usable
A/D module 0 (A/D0)	AN0	Input	Analog input pin 0	Group 0	Not usable	Usable
	AN1	Input	Analog input pin 1			
	AN2	Input	Analog input pin 2			
	AN3	Input	Analog input pin 3			
	AN8	Input	Analog input pin 8	Group 1	Usable	Usable
	AN9	Input	Analog input pin 9			
	AN10	Input	Analog input pin 10			
	AN11	Input	Analog input pin 11			
A/D module 1 (A/D1)	AN4	Input	Analog input pin 4	Group 0	Not usable	Usable
	AN5	Input	Analog input pin 5			
	AN6	Input	Analog input pin 6			
	AN7	Input	Analog input pin 7			
	AN12	Input	Analog input pin 12	Group 1	Usable	Usable
	AN13	Input	Analog input pin 13			
	AN14	Input	Analog input pin 14			
	AN15	Input	Analog input pin 15			
A/D module 2 (A/D2)	AN16	Input	Analog input pin 16	Group 0	Usable	Not usable
	AN17	Input	Analog input pin 17			
	AN18	Input	Analog input pin 18			
	AN19	Input	Analog input pin 19			

Note: The connected A/D module differs for each pin. The control registers of each module must be set.

11.3 Register Descriptions

The A/D converter has the following registers. For details on register addresses, refer to section 19, List of Registers.

- A/D data register 0 (H/L) (ADDR0)
- A/D data register 1 (H/L) (ADDR1)
- A/D data register 2 (H/L) (ADDR2)
- A/D data register 3 (H/L) (ADDR3)
- A/D data register 4 (H/L) (ADDR4)
- A/D data register 5 (H/L) (ADDR5)
- A/D data register 6 (H/L) (ADDR6)
- A/D data register 7 (H/L) (ADDR7)
- A/D data register 8 (H/L) (ADDR8)
- A/D data register 9 (H/L) (ADDR9)
- A/D data register 10 (H/L) (ADDR10)
- A/D data register 11 (H/L) (ADDR11)
- A/D data register 12 (H/L) (ADDR12)
- A/D data register 13 (H/L) (ADDR13)
- A/D data register 14 (H/L) (ADDR14)
- A/D data register 15 (H/L) (ADDR15)
- A/D data register 16 (H/L) (ADDR16)
- A/D data register 17 (H/L) (ADDR17)
- A/D data register 18 (H/L) (ADDR18)
- A/D data register 19 (H/L) (ADDR19)
- A/D control/status register_0 (ADCSR_0)
- A/D control/status register_1 (ADCSR_1)
- A/D control/status register_2 (ADCSR_2)
- A/D control register_0 (ADCR_0)
- A/D control register_1 (ADCR_1)
- A/D control register_2 (ADCR_2)
- A/D trigger select register (ADTSR)

11.3.1 A/D Data Registers 0 to 19 (ADDR0 to ADDR19)

ADDRs are 16-bit read-only registers. The conversion result for each analog input channel is stored in ADDR with the corresponding number. (For example, the conversion result of AN4 is stored in ADDR4.)

The converted 10-bit data is stored in bits 6 to 15. The lower 6 bits are always read as 0.

The data bus between the CPU and the A/D converter is 8 bits wide. The upper byte can be read directly from the CPU, however the lower byte should be read via a temporary register. The temporary register contents are transferred from the ADDR when the upper byte data is read. When reading the ADDR, read the upper byte before the lower byte, or read in word unit. The initial value of ADDR is H'0000.

11.3.2 A/D Control/Status Registers_0 to 2 (ADCSR_0 to ADCSR_2)

ADCSR for each module controls A/D conversion operations.

Bit	Bit Name	Initial Value	R/W	Description
7	ADF	0	R/(W)*	A/D End Flag A status flag that indicates the end of A/D conversion. [Setting conditions] • When A/D conversion ends in single mode • When A/D conversion ends on all specified channels in scan mode [Clearing condition] • When 0 is written after reading ADF = 1
6	ADIE	0	R/W	A/D Interrupt Enable The A/D conversion end interrupt (ADI) request is enabled when this bit is set to 1. When changing the operating mode, first clear the ADST bit in the A/D control registers (ADCRs) to 0.
5	ADM1	0	R/W	A/D Mode 1 and 0
4	ADM0	0	R/W	Select the A/D conversion mode. 00: Single mode 01: 4-channel scan mode 10: 8-channel scan mode 11: Setting prohibited When changing the operating mode, first clear the ADST bit in the A/D control registers (ADCRs) to 0. For A/D2, the ADM1 bit must be cleared to 0.
3	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
2	CH2	0	R/W	Channel Select 2 to 0
1	CH1	0	R/W	Select analog input channels. See table 11.2.
0	CH0	0	R/W	When changing the operating mode, first clear the ADST bit in the A/D control registers (ADCRs) to 0.

Note: * Only 0 can be written to clear the flag.

Table 11.2 Channel Select List

			Analog Input Channels					
Bit 2	**Bit 1**	**Bit 0**	**Single Mode**			**4-Channel Scan Mode*2**		
CH2	**CH1**	**CH0**	**A/D0**	**A/D1**	**A/D2**	**A/D0**	**A/D1**	**A/D2**
0	0	0	AN0	AN4	AN16	AN0	AN4	AN16
		1	AN1	AN5	AN17	AN0, AN1	AN4, AN5	AN16, AN17
	1	0	AN2	AN6	AN18	AN0 to AN2	AN4 to AN6	AN16 to AN18
		1	AN3	AN7	AN19	AN0 to AN3	AN4 to AN7	AN16 to AN19
1	0	0	AN8	AN12	Setting prohibited	AN8	AN12	Setting prohibited
		1	AN9	AN13		AN8, AN9	AN12, AN13	
	1	0	AN10	AN14		AN8 to AN10	AN12 to AN14	
		1	AN11	AN15		AN8 to AN11	AN12 to AN15	

			Analog Input Channels	
Bit 2	**Bit 1**	**Bit 0**	**8-Channel Scan Mode (Only in SH7109)*2**	
CH2	**CH1**	**CH0**	**A/D0**	**A/D1**
0*1	0	0	AN0, AN8	AN4, AN12
		1	AN0, AN1, AN8, AN9	AN4, AN5, AN12, AN13
	1	0	AN0 to AN2, AN8 to AN10	AN4 to AN6, AN12 to AN14
		1	AN0 to AN3, AN8 to AN11	AN4 to AN7, AN12 to AN15

Notes: 1. In 8-channel scan mode, the CH2 bit must be cleared to 0.
2. Continuous scan mode or single-cycle scan mode can be selected with the ADCS bit.

11.3.3 A/D Control Registers_0 to 2 (ADCR_0 to ADCR_2)

ADCR for each module controls A/D conversion started by an external trigger signal and selects the operating clock.

Bit	Bit Name	Initial Value	R/W	Description
7	TRGE	0	R/W	Trigger Enable Enables or disables triggering of A/D conversion by $\overline{\text{ADTRG}}$, an MTU trigger, or an MMT trigger. 0: A/D conversion triggering is disabled 1: A/D conversion triggering is enabled
6	CKS1	0	R/W	Clock Select 0 and 1
5	CKS0	0	R/W	Select the A/D conversion time. 00: Pϕ/32 01: Pϕ/16 10: Pϕ/8 11: Pϕ/4 When changing the A/D conversion time, first clear the ADST bit in the A/D control registers (ADCRs) to 0. CKS[1,0] = b'11 can be set while P$\phi \leq$ 25 MHz.
4	ADST	0	R/W	A/D Start Starts or stops A/D conversion. When this bit is set to 1, A/D conversion is started. When this bit is cleared to 0, A/D conversion is stopped and the A/D converter enters the idle state. In single or single-cycle scan mode, this bit is automatically cleared to 0 when A/D conversion ends on the selected single channel. In continuous scan mode, A/D conversion is continuously performed for the selected channels in sequence until this bit is cleared by a software, reset, or in software standby mode, hardware standby mode, or module standby mode.
3	ADCS	0	R/W	A/D Continuous Scan Selects either single-cycle scan or continuous scan in scan mode. This bit is valid only when scan mode is selected. 0: Single-cycle scan 1: Continuous scan When changing the operating mode, first clear the ADST bit in the A/D control registers (ADCRs) to 0.
2 to 0	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

11.3.4 A/D Trigger Select Register (ADTSR)

ADTSR enables an A/D conversion started by an external trigger signal.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	TRG2S1	0	R/W	AD Trigger 2 Select 1 and 0
4	TRG2S0	0	R/W	Enable the start of A/D conversion by A/D2 with a trigger signal. 00: A/D conversion start by external trigger pin ($\overline{\text{ADTRG}}$) or MTU trigger is enabled 01: A/D conversion start by external trigger pin ($\overline{\text{ADTRG}}$) is enabled 10: A/D conversion start by MTU trigger is enabled 11: A/D conversion start by MMT trigger is enabled When changing the operating mode, first clear the TRGE and ADST bits in the A/D control registers (ADCRs) to 0.
3	TRG1S1	0	R/W	AD Trigger 1 Select 1 and 0
2	TRG1S0	0	R/W	Enable the start of A/D conversion by A/D1 with a trigger signal. 00: A/D conversion start by external trigger pin ($\overline{\text{ADTRG}}$) or MTU trigger is enabled 01: A/D conversion start by external trigger pin ($\overline{\text{ADTRG}}$) is enabled 10: A/D conversion start by MTU trigger is enabled 11: A/D conversion start by MMT trigger is enabled When changing the operating mode, first clear the TRGE and ADST bits in the A/D control registers (ADCRs) to 0.

Bit	Bit Name	Initial Value	R/W	Description
1	TRG0S1	0	R/W	AD Trigger 0 Select 1 and 0
0	TRG0S0	0	R/W	Enable the start of A/D conversion by A/D0 with a trigger signal. 00: A/D conversion start by external trigger pin ($\overline{\text{ADTRG}}$) or MTU trigger is enabled 01: A/D conversion start by external trigger pin ($\overline{\text{ADTRG}}$) is enabled 10: A/D conversion start by MTU trigger is enabled 11: A/D conversion start by MMT trigger is enabled When changing the operating mode, first clear the TRGE and ADST bits in the A/D control registers (ADCRs) to 0.

11.4 Operation

The A/D converter operates by successive approximation with 10-bit resolution. It has two operating modes; single mode and scan mode. There are two kinds of scan mode: continuous mode and single-cycle mode. When changing the operating mode or analog input channel, in order to prevent incorrect operation, first clear the ADST bit to 0 in ADCR. The ADST bit can be set at the same time when the operating mode is changed.

11.4.1 Single Mode

In single mode, A/D conversion is to be performed only once on the specified single channel. The operations are as follows.

1. A/D conversion is started when the ADST bit in ADCR is set to 1, according to software, MTU, MMT, or external trigger input.
2. When A/D conversion is completed, the result is transferred to the A/D data register corresponding to the channel.
3. On completion of conversion, the ADF bit in ADCSR is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt request is generated.
4. The ADST bit remains set to 1 during A/D conversion. When A/D conversion ends, the ADST bit is automatically cleared to 0 and the A/D converter enters the idle state.
   When the ADST bit is cleared to 0 during A/D conversion, A/D conversion stops and the A/D converter enters the idle state.

11.4.2 Continuous Scan Mode

In continuous scan mode, A/D conversion is to be performed sequentially on the specified channels (four channels maximum in the SH7108 and eight channels maximum in the SH7109). The operations are as follows.

1. When the ADST bit in ADCR is set to 1 by software, MTU, MMT, or external trigger input, A/D conversion starts on the channel with the lowest number in the group (AN0, AN1, ..., AN7).
2. When A/D conversion for each channel is completed, the result is sequentially transferred to the A/D data register corresponding to each channel.
3. When conversion of all the selected channels is completed, the ADF bit in ADCSR is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt is requested after A/D conversion ends. Conversion of the first channel in the group starts again.
4. The ADST bit is not cleared automatically. Steps 2 to 3 are repeated as long as the ADST bit remains set to 1. When the ADST bit is cleared to 0, A/D conversion stops and the A/D converter enters the idle state.

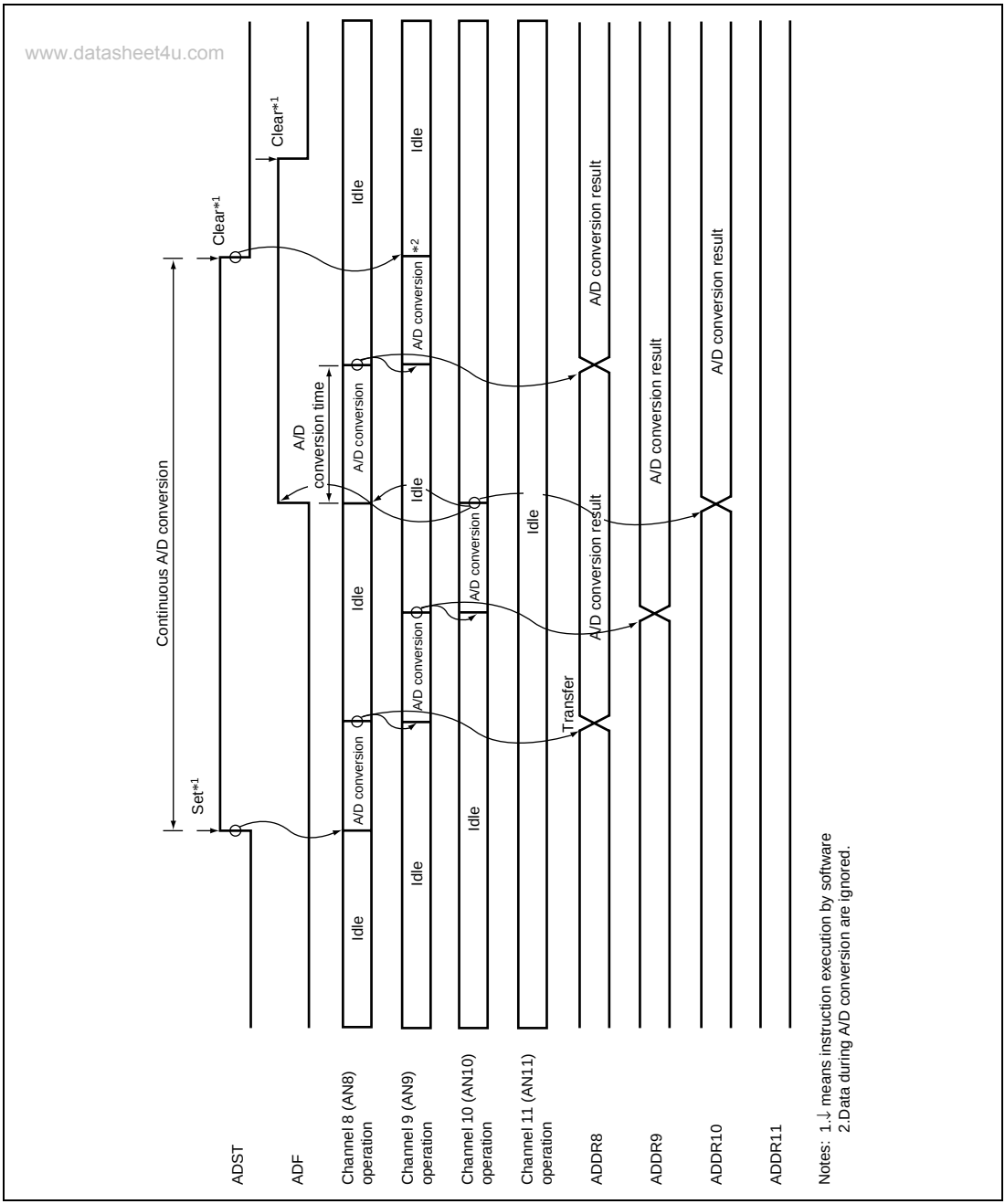


Figure 11.2 Example of Continuous Scan Mode Operation (when Three Channels, AN8 to AN10, Are Selected)

11.4.3 Single-Cycle Scan Mode

In single-cycle scan mode, A/D conversion is to be performed once on the specified channels (four channels maximum in the SH7108 and eight channels maximum in the SH7109). Operations are as follows.

1. When the ADST bit in ADCR is set to 1 by software, MTU, MMT, or external trigger input, A/D conversion starts on the channel with the lowest number in the group (AN0, AN1, ..., AN7).
2. When A/D conversion for each channel is completed, the result is sequentially transferred to the A/D data register corresponding to each channel.
3. When conversion of all the selected channels is completed, the ADF bit in ADCSR is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt is requested.
4. After A/D conversion ends, the ADST bit is automatically cleared to 0 and the A/D converter enters the idle state. When the ADST bit is cleared to 0 during A/D conversion, A/D conversion stops and the A/D converter enters the idle state.

11.4.4 Input Sampling and A/D Conversion Time

The A/D converter has an on-chip sample-and-hold circuit for each module. The A/D converter samples the analog input when the A/D conversion start delay time (t_D) has passed after the ADST bit in ADCR is set to 1, then starts conversion. Figure 11.3 shows the A/D conversion timing. Table 11.3 shows the A/D conversion time.

As indicated in figure 11.3, the A/D conversion time (t_{CONV}) includes t_D and the input sampling time (t_{SPL}). The length of t_D varies depending on the timing of the write access to ADCR. The total conversion time therefore varies within the ranges indicated in table 11.3.

In scan mode, the values given in table 11.3 apply to the first conversion time. The values given in table 11.4 apply to the second and subsequent conversions.

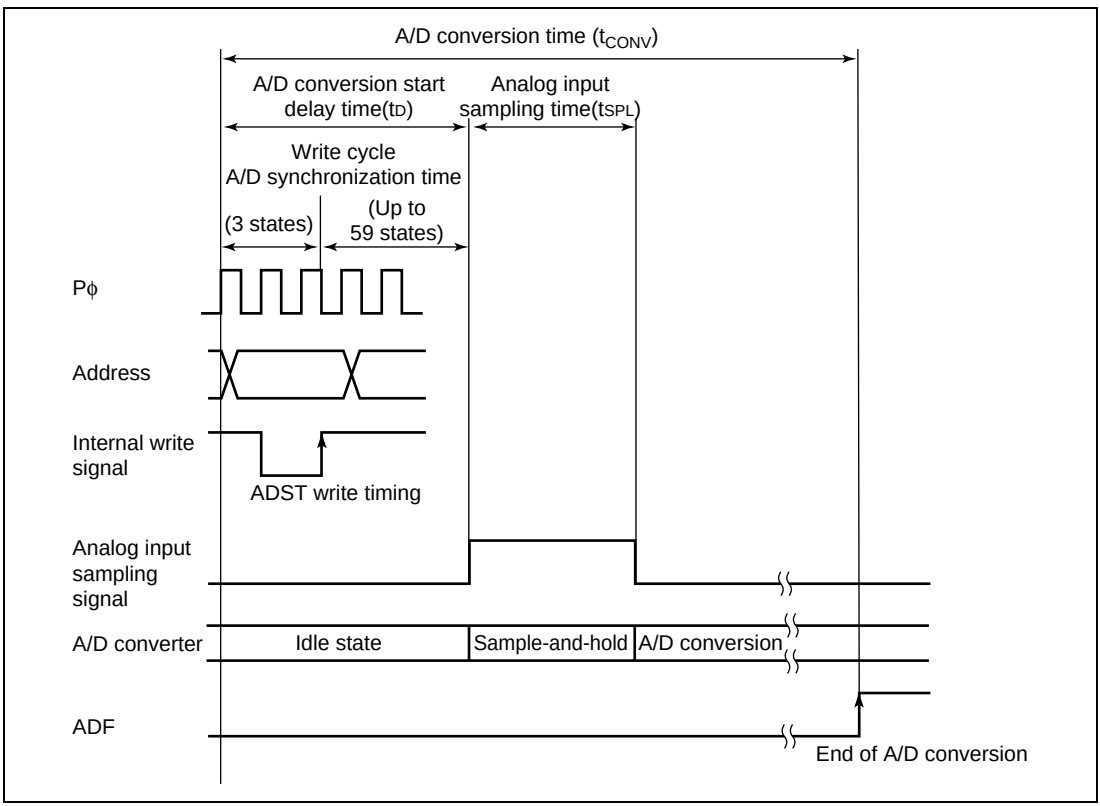


Figure 11.3 A/D Conversion Timing

Table 11.3 A/D Conversion Time (Single Mode)

		CKS1 = 0						CKS1 = 1					
		CKS0 = 0			CKS0 = 1			CKS0 = 0			CKS0 = 1		
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A/D conversion start delay time	t_D	31	—	62	15	—	30	7	—	14	3	—	6
Input sampling time	t_{SPL}	—	256	—	—	128	—	—	64	—	—	32	—
A/D conversion time	t_{CONV}	1024	—	1055	515	—	530	259	—	266	131	—	134

Note: All values represent the number of states for Pϕ.

Table 11.4 A/D Conversion Time (Scan Mode)

CKS1	CKS0	Conversion Time (State)
0	0	1024 (Fixed)
	1	512 (Fixed)
1	0	256 (Fixed)
	1	128 (Fixed)

11.4.5 A/D Converter Activation by MTU or MMT

The A/D converter can be independently activated by an A/D conversion request from the interval timer of the MTU or MMT.

To activate the A/D converter by the MTU or MMT, set the A/D trigger select register (ADTSR). After this register setting has been made, the ADST bit in ADCR is automatically set to 1 when an A/D conversion request from the interval timer of the MTU or MMT occurs. The timing from setting of the ADST bit until the start of A/D conversion is the same as when 1 is written to the ADST bit by software.

11.4.6 External Trigger Input Timing

A/D conversion can be externally triggered. When the TRGS0 and TRGS1 bits are set to 00 or 01 in ADTSR, external trigger input is enabled at the $\overline{\text{ADTRG}}$ pin. A falling edge of the $\overline{\text{ADTRG}}$ pin sets the ADST bit to 1 in ADCR, starting A/D conversion. Other operations, in both single and scan modes, are the same as when the ADST bit has been set to 1 by software. Figure 11.4 shows the timing.

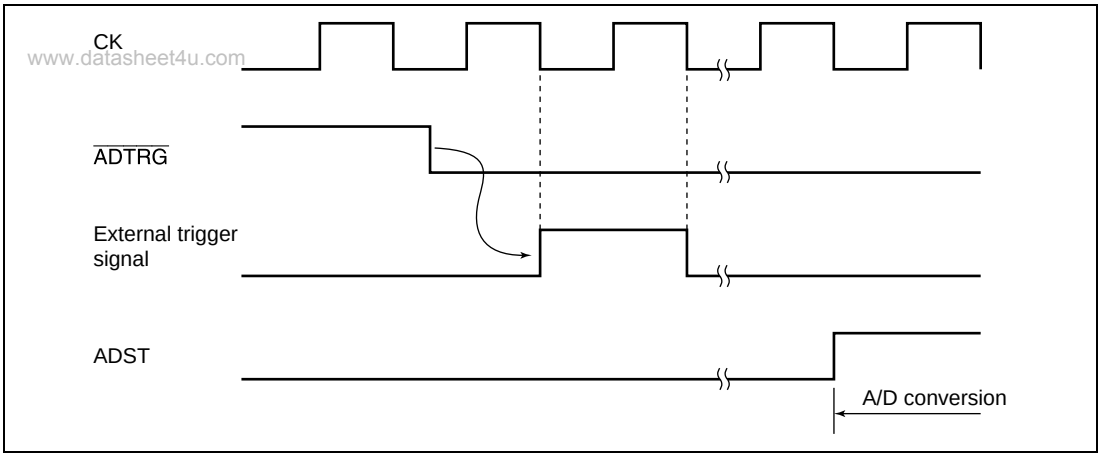


Figure 11.4 External Trigger Input Timing

11.5 Interrupt Source

The A/D converter generates an A/D conversion end interrupt (ADI) upon the completion of A/D conversion. ADI interrupt requests are enabled when the ADIE bit is set to 1 while the ADF bit in ADCSR is set to 1 after A/D conversion is completed.

The A/D converter can generate an A/D conversion end interrupt request. The ADI interrupt can be enabled by setting the ADIE bit in the A/D control/status register (ADCSR) to 1, or disabled by clearing the ADIE bit to 0.

Table 11.5 A/D Converter Interrupt Source

Name	Interrupt Source	Interrupt Flag
ADI	A/D conversion end	ADF

11.6 Definitions of A/D Conversion Accuracy

This LSI's A/D conversion accuracy definitions are given below.

- Resolution

  The number of A/D converter digital output codes
- Quantization error

  The deviation inherent in the A/D converter, given by 1/2 LSB (see figure 11.5).
- Offset error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from the minimum voltage value B'0000000000 (H'00) to B'0000000001 (H'01) (see figure 11.6).
- Full-scale error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from B'1111111110 (H'3FE) to B'1111111111 (H'3FF) (see figure 11.6).
- Nonlinearity error

  The error with respect to the ideal A/D conversion characteristic between zero voltage and full-scale voltage. Does not include offset error, full-scale error, or quantization error (see figure 11.6).
- Absolute accuracy

  The deviation between the digital value and the analog input value. Includes offset error, full-scale error, quantization error, and nonlinearity error.

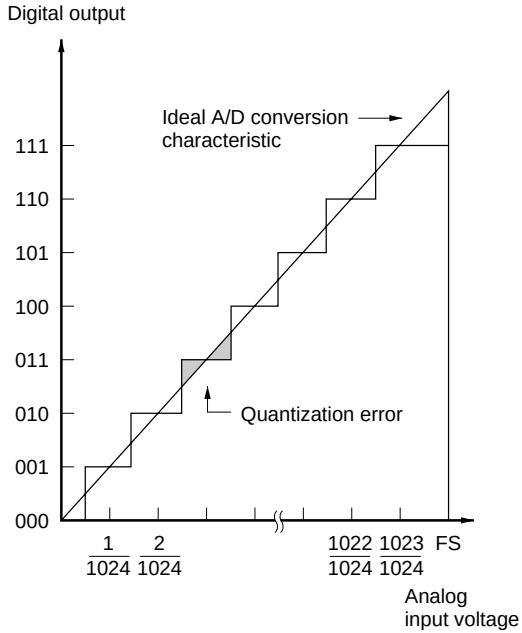


Figure 11.5 Definitions of A/D Conversion Accuracy

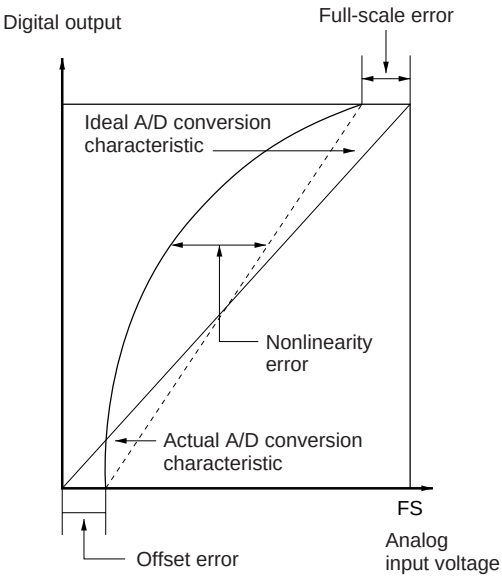


Figure 11.6 Definitions of A/D Conversion Accuracy

11.7 Usage Notes

11.7.1 Module Standby Mode Setting

Operation of the A/D converter can be disabled or enabled using the module standby control register. The initial setting is for operation of the A/D converter to be halted. Register access is enabled by clearing module standby mode. For details, refer to section 18, Power-Down Modes.

11.7.2 Permissible Signal Source Impedance

This LSI's analog input is designed such that conversion accuracy is guaranteed for an input signal for which the signal source impedance is 1 kΩ or less than 3 kΩ. (For details, see table 11.6.) This specification is provided to enable the A/D converter's sample-and-hold circuit input capacitance to be charged within the sampling time; if the sensor output impedance is 1 kΩ or exceeds 3 kΩ, charging may be insufficient and it may not be possible to guarantee A/D conversion accuracy. However, for A/D conversion in single mode with a large capacitance provided externally, the input load will essentially comprise only the internal input resistance of 10 kΩ, and the signal source impedance is ignored. However, as a low-pass filter effect is obtained in this case, it may not be possible to follow an analog signal with a large differential coefficient (e.g., 5 mV/μs or greater) (see figure 11.7). When converting a high-speed analog signal or converting in scan mode, a low-impedance buffer should be inserted.

11.7.3 Influences on Absolute Accuracy

Adding capacitance results in coupling with GND, and therefore noise in GND may adversely affect absolute accuracy. Be sure to make the connection to an electrically stable GND such as AVss.

Care is also required to insure that filter circuits do not communicate with digital signals on the mounting board (i.e, acting as antennas).

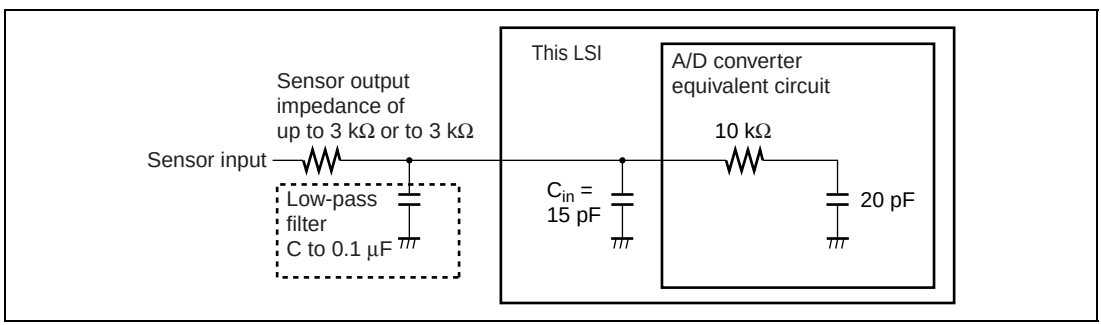


Figure 11.7 Example of Analog Input Circuit

11.7.4 Range of Analog Power Supply and Other Pin Settings

If the conditions below are not met, the reliability of the device may be adversely affected.

- Analog input voltage range

  The voltage applied to analog input pin ANn during A/D conversion should be in the range AVss ≤ VAN ≤ AVcc.
- Relationship between AVcc, AVss and Vcc, Vss

  Set AVss = Vss for the relationship between AVcc, AVss and Vcc, Vss. If the A/D converter is not used, the AVcc and AVss pins must not be left open.

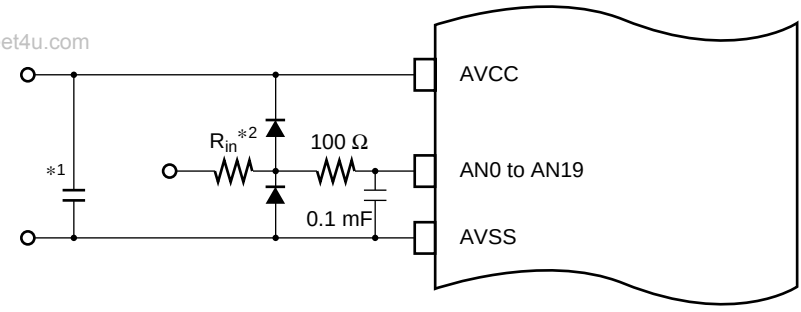
11.7.5 Notes on Board Design

In board design, digital circuitry and analog circuitry should be as mutually isolated as possible, and layout in which digital circuit signal lines and analog circuit signal lines cross or are in close proximity should be avoided as far as possible. Failure to do so may result in incorrect operation of the analog circuitry due to inductance, adversely affecting A/D conversion values. Also, digital circuitry must be isolated from the analog input signals (AN0 to AN19), and analog power supply (AVcc) by the analog ground (AVss). Also, the analog ground (AVss) should be connected at one point to a stable ground (Vss) on the board.

11.7.6 Notes on Noise Countermeasures

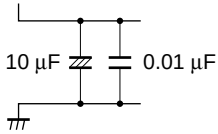
A protection circuit should be connected in order to prevent damage due to abnormal voltage, such as an excessive surge at the analog input pins (AN0 to AN19), between AVcc and AVss, as shown in figure 11.8. Also, the bypass capacitors connected to AVcc and the filter capacitor connected to AN0 to AN19 must be connected to AVss.

If a filter capacitor is connected, the input currents at the analog input pins (AN0 to AN19) are averaged, and so an error may arise. Also, when A/D conversion is performed frequently, as in scan mode, if the current charged and discharged by the capacitance of the sample-and-hold circuit in the A/D converter exceeds the current input via the input impedance (R_{in}), an error will arise in the analog input pin voltage. Careful consideration is therefore required when deciding circuit constants.



Notes: Values are reference values.

1

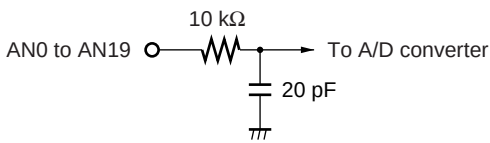


2 R_{in}: Input impedance

Figure 11.8 Example of Analog Input Protection Circuit

Table 11.6 Analog Pin Specifications

Item	Min.	Max.	Unit.	Measurement Condition
Analog input capacitance	—	20	pF	
Permissible signal source impedance	—	3	kΩ	≤ 20 MHz
	—	1	kΩ	20 to 25 MHz



Note: Values are reference values.

Figure 11.9 Analog Input Pin Equivalent Circuit

Section 12 Compare Match Timer (CMT)

This LSI has an on-chip compare match timer (CMT) comprising two 16-bit timer channels. The CMT has 16-bit counters and can generate interrupts at set intervals.

12.1 Features

- Four types of counter input clock can be selected
  One of four internal clocks (Pϕ/8, Pϕ/32, Pϕ/128, Pϕ/512) can be selected independently for each channel.
- Interrupt sources
  A compare match interrupt can be requested independently for each channel.
- Module standby mode can be set

Figure 12.1 shows a block diagram of the CMT.

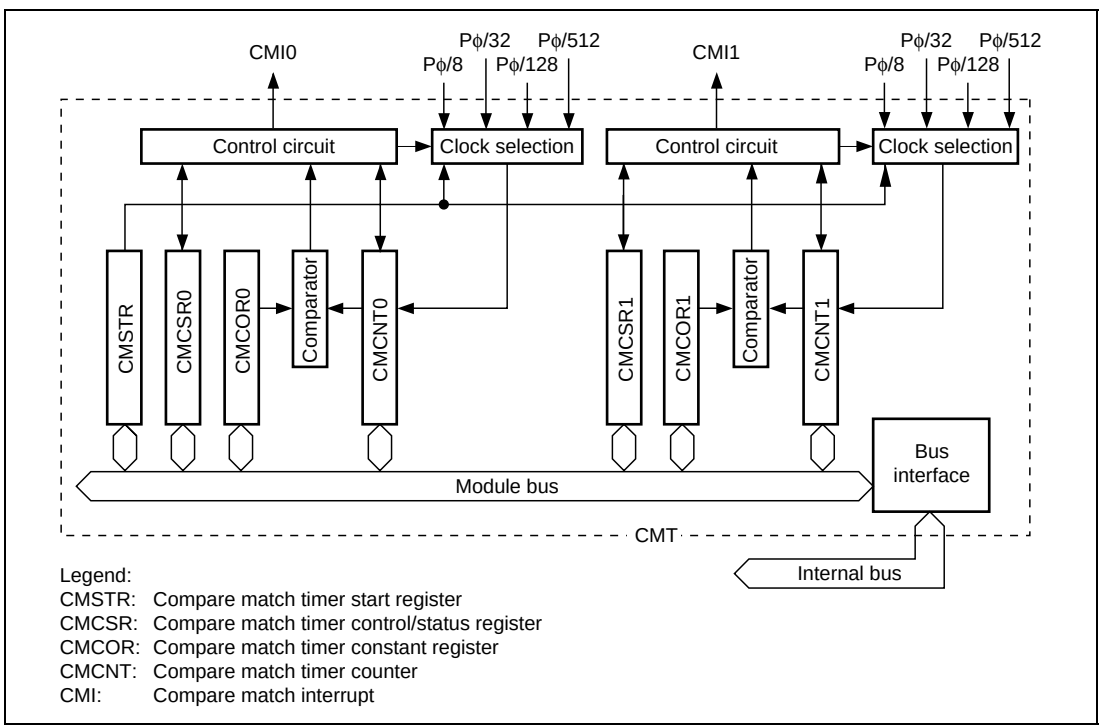


Figure 12.1 CMT Block Diagram

12.2 Register Descriptions

The CMT has the following registers. For details on register addresses and register states during each processing, refer to section 19, List of Registers.

- Compare match timer start register (CMSTR)
- Compare match timer control/status register_0 (CMCSR_0)
- Compare match timer counter_0 (CMCNT_0)
- Compare match timer constant register_0 (CMCOR_0)
- Compare match timer control/status register_1 (CMCSR_1)
- Compare match timer counter_1 (CMCNT_1)
- Compare match timer constant register_1 (CMCOR_1)

12.2.1 Compare Match Timer Start Register (CMSTR)

CMSTR is a 16-bit register that selects whether to operate or halt the channel 0 and channel 1 counters (CMCNT).

Bit	Bit Name	Initial Value	R/W	Description
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	STR1	0	R/W	Count Start 1 Selects whether to operate or halt the compare match timer counter_1. 0: CMCNT_1 count operation halted 1: CMCNT_1 count operation
0	STR0	0	R/W	Count Start 0 Selects whether to operate or halt the compare match timer counter_0. 0: CMCNT_0 count operation halted 1: CMCNT_0 count operation

12.2.2 Compare Match Timer Control/Status Registers_0 and 1 (CMCSR_0, CMCSR_1)

CMCSR is a 16-bit register that indicates the occurrence of compare matches, enables or disables interrupts, and sets the clock used for incrementation.

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	CMF	0	R/(W)*	Compare Match Flag Indicates whether or not the CMCNT and CMCOR values have matched. 0: CMCNT and CMCOR values have not matched [Clearing condition] • Write 0 to CMF after reading 1 from it 1: CMCNT and CMCOR values have matched
6	CMIE	0	R/W	Compare Match Interrupt Enable Selects whether to enable or disable a compare match interrupt (CMI) when the CMCNT and CMCOR values have matched (CMF = 1). 0: Compare match interrupt (CMI) disabled 1: Compare match interrupt (CMI) enabled
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	CKS1	0	R/W	Select the clock input to CMCNT among the four internal clocks obtained by dividing the peripheral clock (Pϕ). When the STR bit in CMSTR is set to 1, CMCNT begins incrementing with the clock selected by the CKS1 and CKS0 bits. 00: Pϕ/8 01: Pϕ/32 10: Pϕ/128 11: Pϕ/512
0	CKS0	0	R/W	

Note: * Only 0 can be written for flag clearing.

12.2.3 Compare Match Timer Counters_0 and 1 (CMCNT_0, CMCNT_1)

CMCNT is a 16-bit register used as an up-counter for generating interrupt requests. CMCNT is initialized to H'0000.

12.2.4 Compare Match Timer Constant Registers_0 and 1 (CMCOR_0, CMCOR_1)

CMCOR is a 16-bit register that sets the period for compare match with CMCNT. CMCOR is initialized to H'FFFF.

12.3 Operation

12.3.1 Cyclic Count Operation

When an internal clock is selected with the CKS1 and CKS0 bits in CMCSR and the STR bit in CMSTR is set to 1, CMCNT begins incrementing with the selected clock. When the CMCNT counter value matches that of the compare match constant register (CMCOR), the CMCNT counter is cleared to H'0000 and the CMF flag in CMCSR is set to 1. If the CMIE bit in CMCSR is set to 1 at this time, a compare match interrupt (CMI) is requested. The CMCNT counter begins counting up again from H'0000.

Figure 12.2 shows the compare match counter operation.

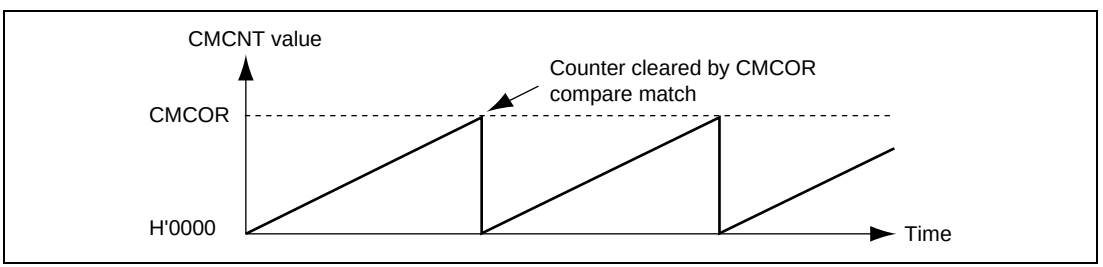


Figure 12.2 Counter Operation

12.3.2 CMCNT Count Timing

One of four internal clocks (Pϕ/8, Pϕ/32, Pϕ/128, Pϕ/512) obtained by dividing the peripheral clock (Pϕ) can be selected by the CKS1 and CKS0 bits in CMCSR. Figure 12.3 shows the timing.

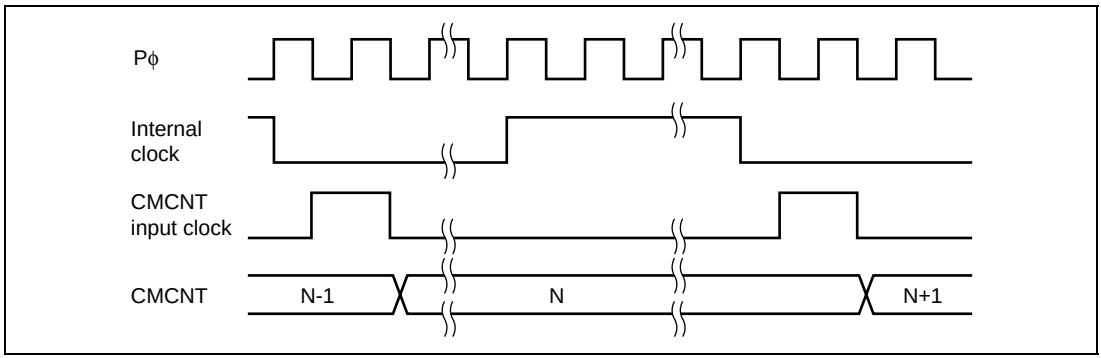


Figure 12.3 Count Timing

12.4 Interrupts

12.4.1 Interrupt Sources

The CMT has a compare match interrupt for each channel, with independent vector addresses allocated to each of them. The corresponding interrupt request is output when the interrupt request flag (CMF) is set to 1 and interrupt enable bit (CMIE) has also been set to 1.

When activating CPU interrupts by an interrupt request, the priority between the channels can be changed by means of interrupt controller settings. See section 6, Interrupt Controller (INTC), for details.

12.4.2 Compare Match Flag Set Timing

The CMF bit in CMCSR is set to 1 by the compare match signal generated when CMCOR and CMCNT match. The compare match signal is generated upon the final state of the match (timing at which the CMCNT matching count value is updated). Consequently, after CMCOR and CMCNT match, a compare match signal will not be generated until a CMCNT counter input clock occurs. Figure 12.4 shows the CMF bit set timing.

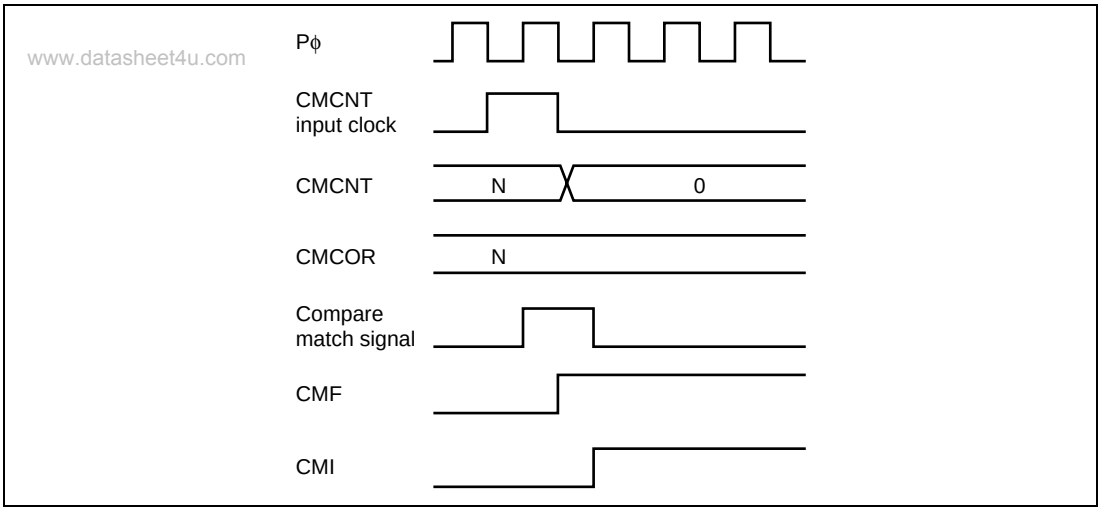


Figure 12.4 CMF Set Timing

12.4.3 Compare Match Flag Clear Timing

The CMF bit in CMCSR is cleared by writing 0 to it after reading 1. Figure 12.5 shows the timing when the CMF bit is cleared by the CPU.

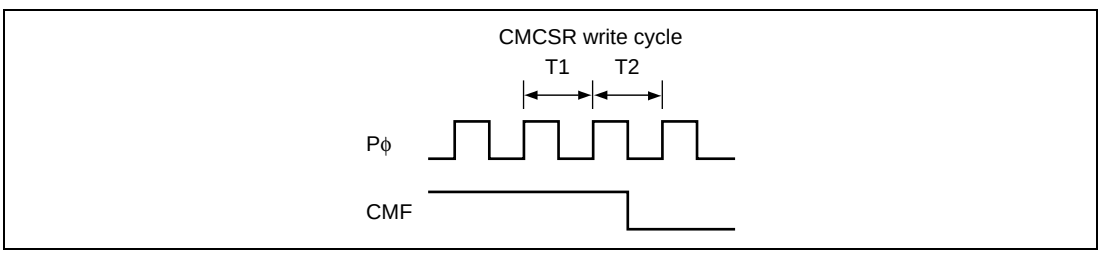


Figure 12.5 Timing of CMF Clear by CPU

12.5 Usage Notes

12.5.1 Contention between CMCNT Write and Compare Match

If a compare match signal is generated during the T2 state of the CMCNT counter write cycle, the CMCNT counter clear has priority, so the write to the CMCNT counter is not performed. Figure 12.6 shows the timing.

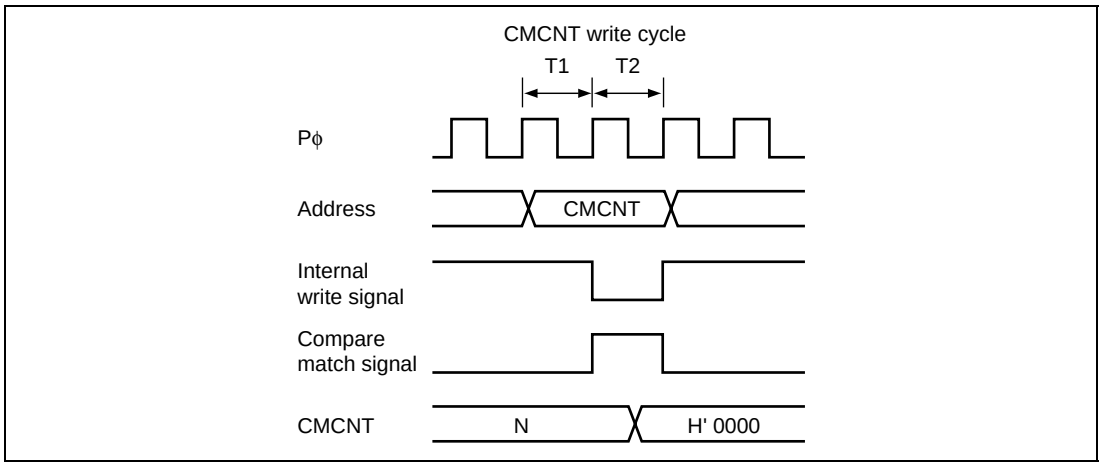


Figure 12.6 CMCNT Write and Compare Match Contention

12.5.2 Contention between CMCNT Word Write and Incrementation

If an increment occurs during the T2 state of the CMCNT counter word write cycle, the counter write has priority, so no increment occurs. Figure 12.7 shows the timing.

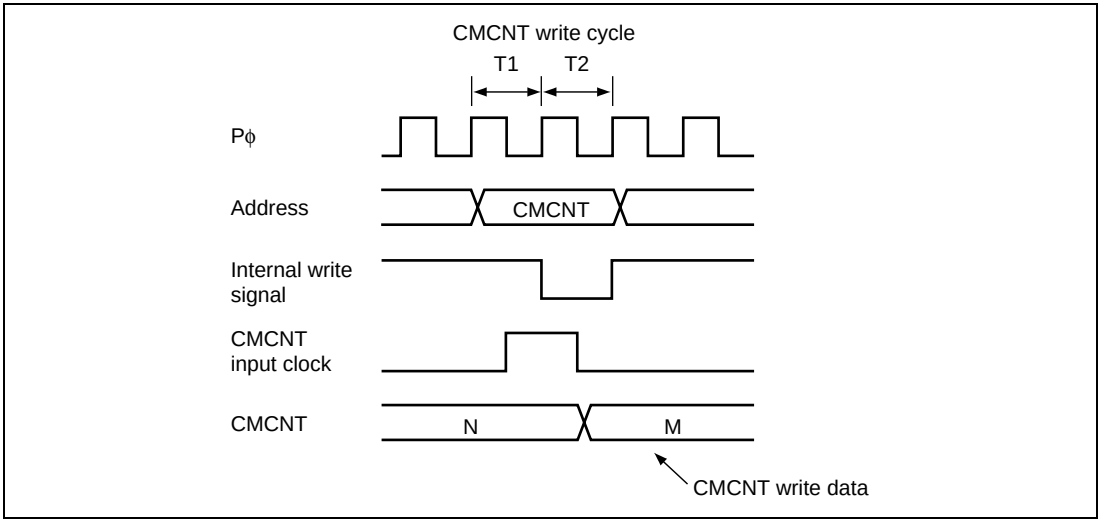


Figure 12.7 CMCNT Word Write and Increment Contention

12.5.3 Contention between CMCNT Byte Write and Incrementation

If an increment occurs during the T2 state of the CMCNT byte write cycle, the counter write has priority, so no increment of the write data results on the side on which the write was performed. The byte data on the side on which writing was not performed is also not incremented, so the contents are those before the write.

Figure 12.8 shows the timing when an increment occurs during the T2 state of the CMCNTH write cycle.

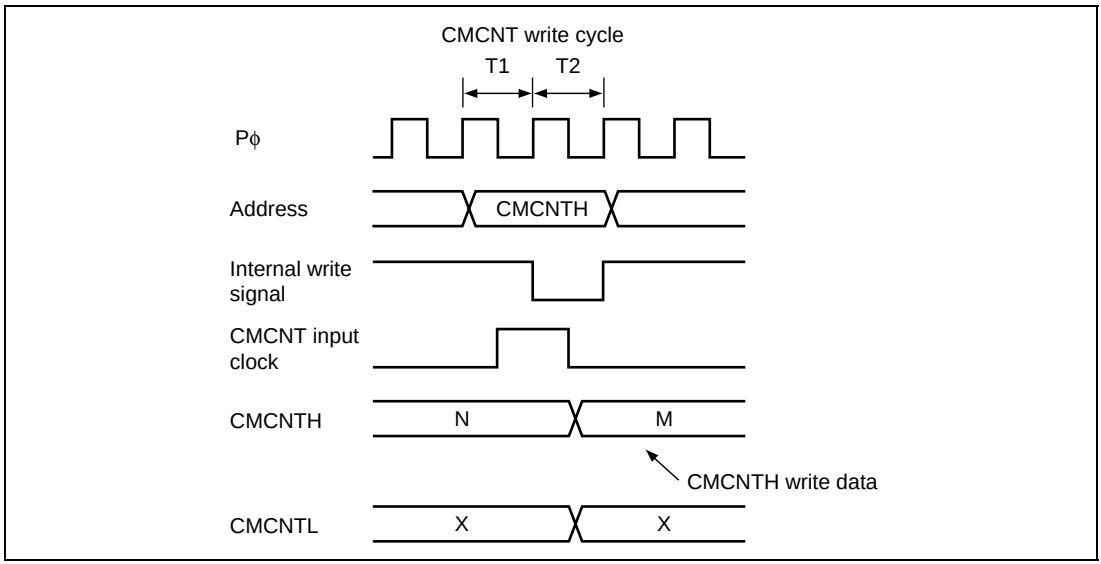


Figure 12.8 CMCNT Byte Write and Increment Contention

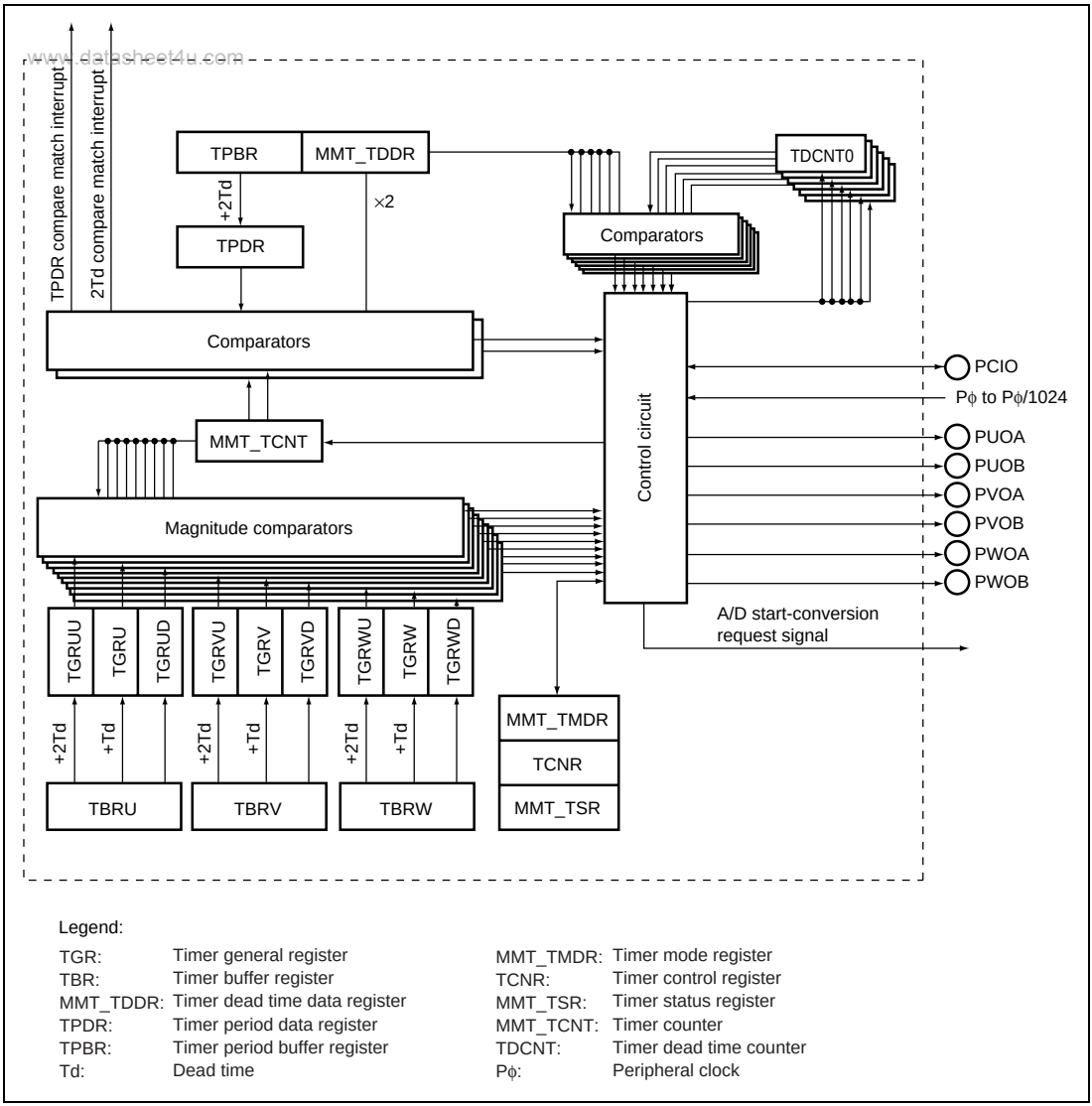
Section 13 Motor Management Timer (MMT)

The motor management timer (MMT) can output six-phase PWM waveforms with non-overlap times.

Figure 13.1 shows a block diagram of the MMT.

13.1 Features

- Six-phase PWM waveform output of the triangular wave comparison type with non-overlap times
- Non-overlap times generated by timer dead time counters
- Toggle output synchronized with PWM period
- Counter clearing on an external signal
- Generation of a trigger for the start of conversion by the A/D converter is available
- Output-off functions
- PWM output halted by an external signal
- PWM output halted when oscillation stops
- Module standby mode can be set



Legend:

TGR:	Timer general register	MMT_TMDR:	Timer mode register
TBR:	Timer buffer register	TCNR:	Timer control register
MMT_TDDR:	Timer dead time data register	MMT_TSR:	Timer status register
TPDR:	Timer period data register	MMT_TCNT:	Timer counter
TPBR:	Timer period buffer register	TDCNT:	Timer dead time counter
Td:	Dead time	Pϕ:	Peripheral clock

Figure 13.1 Block Diagram of MMT

13.2 Input/Output Pins

Table 13.1 shows the pin configuration of the MMT.

Table 13.1 Pin Configuration

Name	I/O	Function
PCIO	I/O	Counter clear signal input when set as an input by PAIORL; toggle output in synchronization with the PWM cycle when set as an output by PAIORL.
PUOA	Output	PWMU phase output (positive phase)
PUOB	Output	PWMU phase output (negative phase)
PVOA	Output	PWMV phase output (positive phase)
PVOB	Output	PWMV phase output (negative phase)
PWOA	Output	PWMW phase output (positive phase)
PWOB	Output	PWMW phase output (negative phase)

13.3 Register Descriptions

The MMT has the following registers. For details on register addresses and the register states during each processing, refer to section 19, List of Registers.

- Timer mode register (MMT_TMDR*)
- Timer control register (TCNR)
- Timer status register (MMT_TSR*)
- Timer counter (MMT_TCNT*)
- Timer buffer register U (TBRU)
- Timer buffer register V (TBRV)
- Timer buffer register W (TBRW)
- Timer general register UU (TGRUU)
- Timer general register VU (TGRVU)
- Timer general register WU (TGRWU)
- Timer general register U (TGRU)
- Timer general register V (TGRV)
- Timer general register W (TGRW)
- Timer general register UD (TGRUD)
- Timer general register VD (TGRVD)

- Timer general register WD (TGRWD)
- Timer dead time counter 0 (TDCNT0)
- Timer dead time counter 1 (TDCNT1)
- Timer dead time counter 2 (TDCNT2)
- Timer dead time counter 3 (TDCNT3)
- Timer dead time counter 4 (TDCNT4)
- Timer dead time counter 5 (TDCNT5)
- Timer dead time data register (MMT_TDDR*)
- Timer period buffer register (TPBR)
- Timer period data register (TPDR)

Note: * In this section, the names of these registers are further abbreviated to TMDR, TSR, TCNT, and TDDR hereafter.

13.3.1 Timer Mode Register (MMT_TMDR)

MMT_TMDR sets the operating mode and selects the PWM output level. (In this section, the name of this register is abbreviated to TMDR hereafter.)

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	CKS2	0	R/W	Clock Select 2 to 0
5	CKS1	0	R/W	Select the clock input to MMT.
4	CKS0	0	R/W	000: Pϕ 001: Pϕ/4 010: Pϕ/16 011: Pϕ/64 100: Pϕ/256 101: Pϕ/1024 11x: Setting prohibited [Legend] x: Don't care.
3	OLSN	0	R/W	Output Level Select N Selects the negative phase output level in the operating modes. 0: Active level is low 1: Active level is high
2	OLSP	0	R/W	Output Level Select P Selects the positive phase output level in the operating modes. 0: Active level is low 1: Active level is high
1	MD1	0	R/W	Mode 3 to 0
0	MD0	0	R/W	Set the timer operating mode. 00: Operation halted 01: Operating mode 1 (Transfer at TCNT = TPDR) 10: Operating mode 2 (Transfer at TCNT = TDDR × 2) 11: Operating mode 3 (Transfer at TCNT = TPDR or TCNT = TDDR × 2)

13.3.2 Timer Control Register (TCNR)

TCNR controls the enabling or disabling of interrupt requests, selects the enabling or disabling of register access, selects counter operation or halting, and controls the enabling or disabling of toggle output synchronized with the PWM period.

Bit	Bit Name	Initial Value	R/W	Description
7	TTGE	0	R/W	A/D Conversion Start Request Enable Enables or disables the generation of A/D conversion start requests when the TGFN or TGFM bit in the timer status register (TSR) is set. 0: Disables the request 1: Enables the request
6	CST	0	R/W	Timer Counter Start Selects operation or halting of the timer counter (TCNT) and timer dead time counter (TDCNT). 0: TCNT and TDCNT operation is halted 1: TCNT and TDCNT perform count operations
5	RPRO	0	R/W	Register Protects Enables or disables the reading of registers other than TSR, and enables or disables the writing to registers other than TBRU to TBRW, TPBR, and TSR. Writes to TCNR itself are also disabled. Note that reset input is necessary in order to write to these registers again. 0: Register access enabled 1: Register access disabled
4 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	TGIEN	0	R/W	TGR Interrupt Enable N Enables or disables interrupt requests by the TGFN bit when the TGFN bit is set to 1 in TSR. 0: Interrupt requests by TGFN bit disabled 1: Interrupt requests by TGFN bit enabled
0	TGIEM	0	R/W	TGR Interrupt Enable M Enables or disables interrupt requests by the TGFM bit when the TGFM bit is set to 1 in TSR. 0: Interrupt requests by TGFM bit disabled 1: Interrupt requests by TGFM bit enabled

13.3.3 Timer Status Register (MMT_TSR)

MMT_TSR holds status flags. (In this section, the name of this register is abbreviated to TSR hereafter.)

Bit	Bit Name	Initial Value	R/W	Description
7	TCFD	1	R	Count Direction Flag Status flag that indicates the count direction of the TCNT counter. 0: TCNT counts down 1: TCNT counts up
6 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	TGFN	0	R/(W)*	Output Compare Flag N Status flag that indicates a compare match between TCNT and 2Td (Td: TDDR value). [Setting condition] • When TCNT = 2Td [Clearing condition] • When 0 is written to TGFN after reading TGFN = 1
0	TGFM	0	R/(W)*	Output Compare Flag M Status flag that indicates a compare match between TCNT and TPDR. [Setting condition] • When TCNT = TPDR [Clearing condition] • When 0 is written to TGFM after reading TGFM = 1

Note: * Only 0 can be written for flag clearing.

13.3.4 Timer Counter (MMT_TCNT)

MMT_TCNT is a 16-bit counter. The initial value is H'0000. Only 16-bit access can be used on MMT_TCNT; 8-bit access is not possible. (In this section, the name of this register is abbreviated to TCNT hereafter.)

13.3.5 Timer Buffer Registers (TBR)

TBR function as 16-bit buffer registers. The MMT has three TBR registers; TBRU, TBRV, and TBRW, each of which has two addresses; a buffer operation address (shown first) and a free operation address (shown second). A value written to the buffer operation address is transferred to the corresponding TGR at the timing set in bits MD1 and MD0 in the timer mode register (TMDR). A value set in the free operation address is transferred to the corresponding TGR immediately. The initial value of TBR is H'FFFF. Only 16-bit access can be used on the TBR registers; 8-bit access is not possible.

13.3.6 Timer General Registers (TGR)

TGR function as 16-bit compare registers. The MMT has nine TGR registers, that are compared with the TCNT counter in the operating modes. The initial value of TGR is H'FFFF. Only 16-bit access can be used on the TGR registers; 8-bit access is not possible.

13.3.7 Timer Dead Time Counter (TDCNT)

TDCNT is a 16-bit read-only counter. The initial value of TDCNT is H'0000. Only 16-bit access can be used on TDCNT; 8-bit access is not possible.

13.3.8 Timer Dead Time Data Register (MMT_TDDR)

MMT_TDDR is a 16-bit register that sets the positive phase and negative phase non-overlap time (dead time). The initial value of MMT_TDDR is H'FFFF. Only 16-bit access can be used on MMT_TDDR; 8-bit access is not possible. (In this section, the name of this register is further abbreviated to TDDR hereafter.)

13.3.9 Timer Period Buffer Register (TPBR)

TPBR is a 16-bit register that functions as a buffer register for TPDR. A value of 1/2 the PWM carrier period should be set as the TPBR value. The TPBR value is transferred to TPDR at the transfer timing set in TMDR. The initial value of TPBR is H'FFFF. Only 16-bit access can be used on TPBR; 8-bit access is not possible.

13.3.10 Timer Period Data Register (TPDR)

TPDR functions as a 16-bit compare register. In the operating modes, the TPDR value is constantly compared with the TCNT counter value, and when they match, the TCNT counter changes its count direction from up to down. The initial value of TPDR is H'FFFF. Only 16-bit access can be used on TPDR; 8-bit access is not possible.

13.4 Operation

When the operating mode is selected, a three-phase PWM waveform is output with a non-overlap relationship between the positive and negative phases.

The PUOA, PUOB, PVOA, PVOB, PWOA, and PWOB pins are PWM output pins, the PCIO pin (when set to output) functions as a toggle output synchronized with the PWM waveform, and the PCI0 pin (when set to input) functions as the counter clear signal input. The TCNT counter performs up- and down-count operations, whereas the TDCNT counters perform up-count operations.

13.4.1 Sample Setting Procedure

An example of the operating mode setting procedure is shown in figure 13.2.

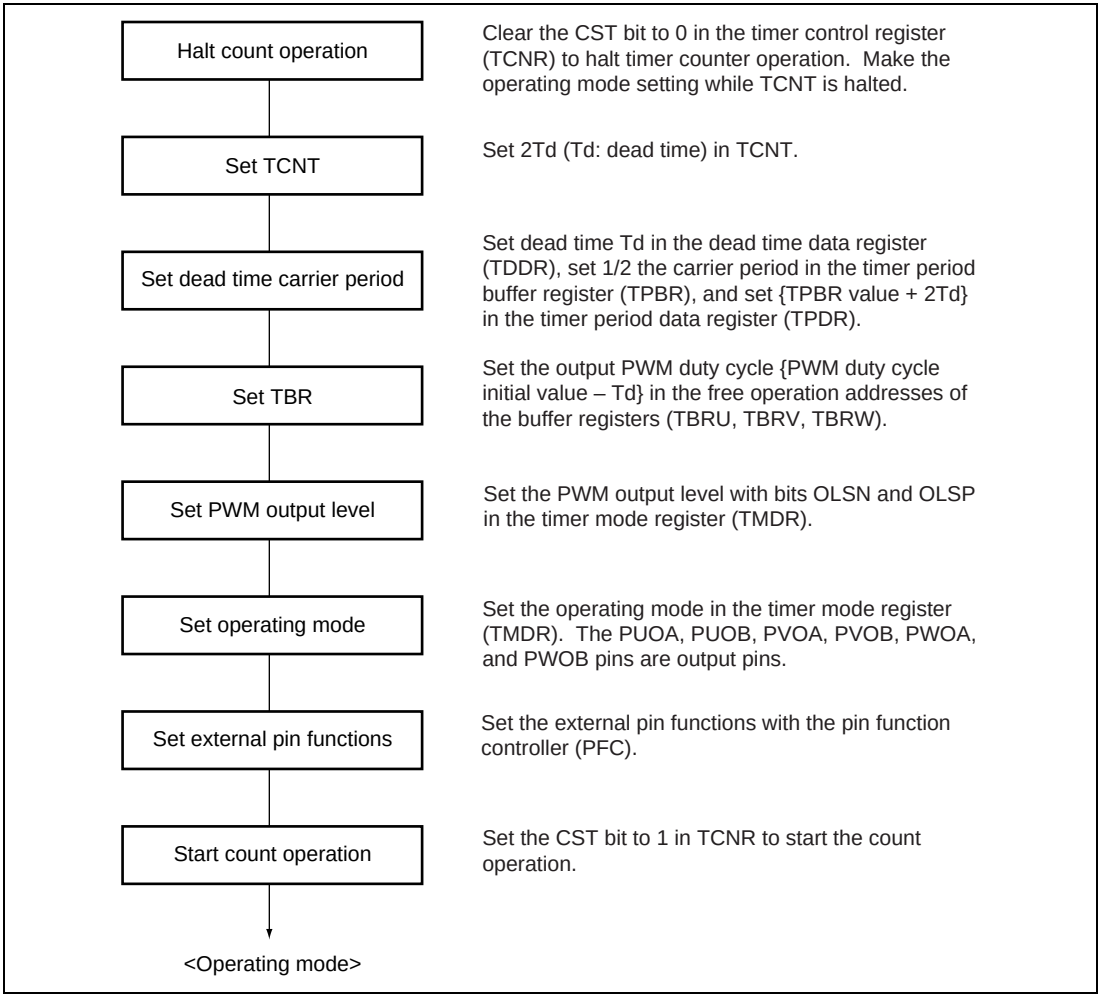


Figure 13.2 Sample Operating Mode Setting Procedure

(1) Count Operation

Set 2Td (Td: value set in TDDR) as the initial value of the TCNT counter when the CST bit in TCNR is cleared to 0.

When the CST bit is set to 1, TCNT counts up to {the value set in TPBR + 2Td}, and then starts counting down. When TCNT reaches 2Td, it starts counting up again, and continues in this way.

TCNT is constantly compared with TGRU, TGRV, and TGRW. In addition, it is compared with TGRUU, TGRVU, TGRWU, and TPDR when counting up, and with TGRUD, TGRVD, TGRWD, and 2Td when counting down.

TDCNT0 to TDCNT5 are read-only counters. It is not necessary to set their initial values.

TDCNT0, TDCNT2, and TDCNT4 start counting up at the falling edge of a positive phase compare match output when TCNT is counting down. When they become equal to TDDR they are cleared to 0 and halt.

TDCNT1, TDCNT3, and TDCNT5 start counting up at the falling edge of a negative phase compare match output when TCNT is counting up. When they match TDDR they are cleared to 0 and halt.

TDCNT0 to TDCNT5 are compared with TDDR only while a count operation is in progress. No count operation is performed when the TDDR value is 0.

Figure 13.3 shows an example of the TCNT count operation.

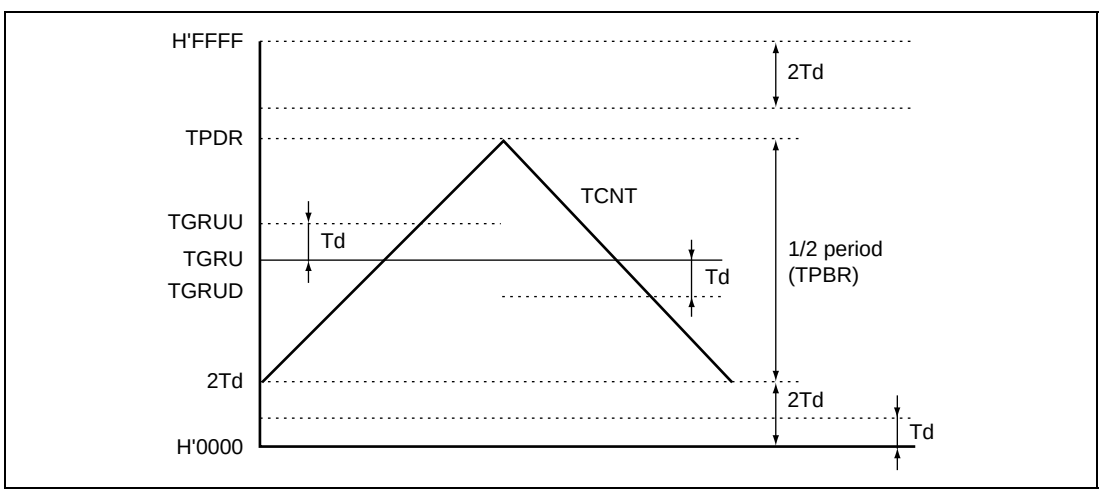


Figure 13.3 Example of TCNT Count Operation

(2) Register Operation

In the operating modes, four buffer registers and ten compare registers are used.

The registers that are constantly compared with the TCNT counter are TGRU, TGRV, and TGRW. In addition, TGRUU, TGRVU, TGRWU, and TPDR are compared with TCNT when TCNT is counting up, and TGRUD, TGRVD, TGRWD are compared with TCNT when TCNT is counting down. The buffer register for TPDR is TPBR; the buffer register for TGRUU, TGRU, and TGRUD is TBRU; the buffer register for TGRVU, TGRV, and TGRVD is TBRV; and the buffer register for TGRWU, TGRW, and TGRWD is TBRW.

To change compare register data, the new data should be written to the corresponding buffer register. The buffer registers can be read from or written to at all times. Data written to the buffer operation addresses for TPBR and TBRU to TBRW is transferred at the timing specified by bits MD1 and MD0 in the timer mode register (TMDR). Data written to the free operation addresses for TBRU to TBRW is transferred immediately.

After data transfer is completed, the relationship between the compare registers and buffer registers is as follows:

TGRU (TGRV, TGRW) value = TBRU (TBRV, TBRW) value + Td (Td: value set in TDDR)
TGRUU (TGRVU, TGRWU) value = TBRU (TBRV, TBRW) value + 2Td
TGRUD (TGRVD, TGRWD) value = TBRU (TBRV, TBRW) value
TPDR value = TPBR value + 2Td

The values of TBRU to TBRW should always be set in the range H'0000 to H'FFFF – 2Td, and the value of TPBR should always be set in the range H'0000 to H'FFFF – 4Td.

Figure 13.4 shows examples of counter and register operations.

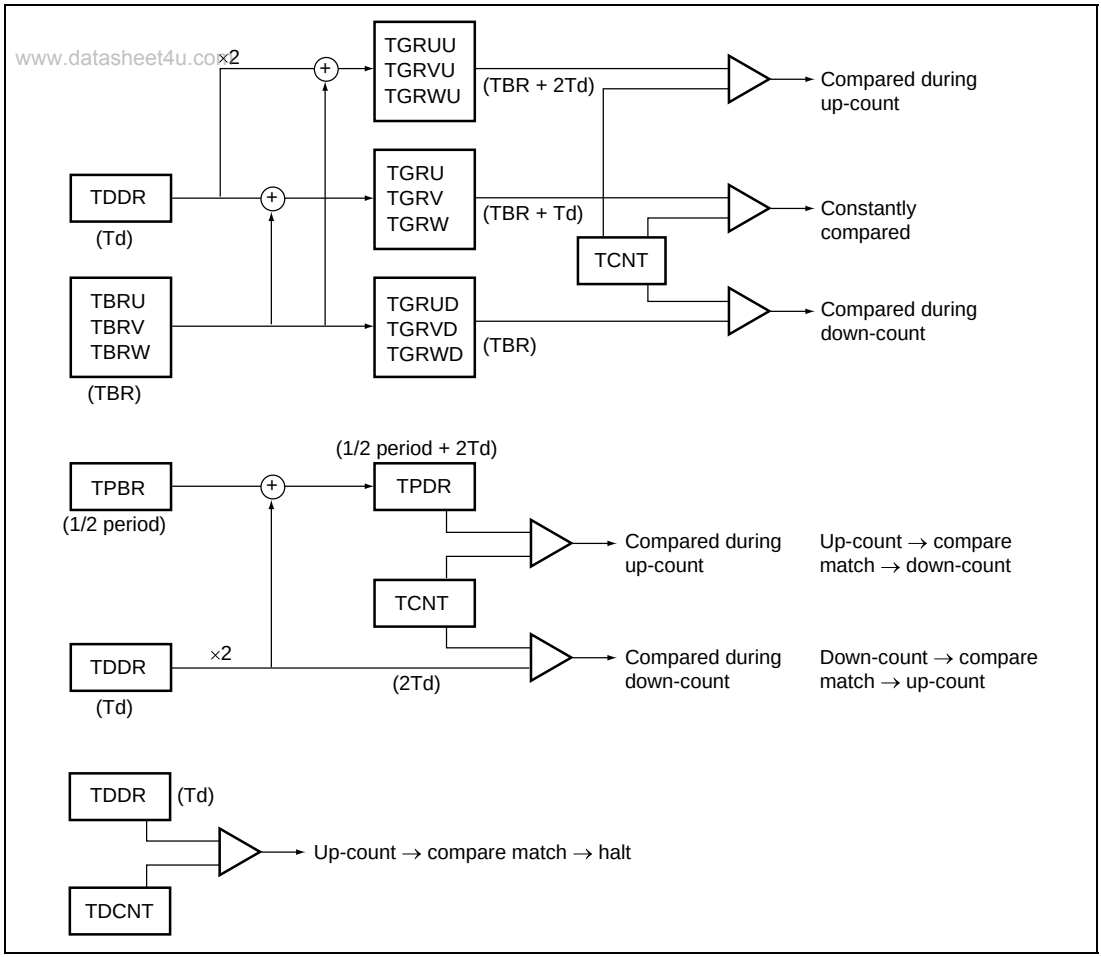


Figure 13.4 Examples of Counter and Register Operations

(3) Initial Settings

In the operating modes, there are five registers that require initialization.

Make the following register settings before setting the operating mode with bits MD1 and MD0 in the timer mode register (TMDR).

Set the timer period buffer register (TPBR) to 1/2 the PWM carrier period, set dead time Td in the timer dead time data register (TDDR) (when outputting an ideal waveform, Td = H'0000), and set {TPBR value + 2Td} in the timer period data register (TPDR).

Set {PWM duty initial value – Td} in the free write operation addresses for TBRU to TBRW.

The values of TBRU to TBRW should always be set in the range H'0000 to H'FFFF – 2Td, and the value of TPBR should always be set in the range H'0000 to H'FFFF – 4Td.

(4) PWM Output Active Level Setting

In the operating modes, the active level of PWM pulses is set with bits OLSN and OLSP in the timer mode register (TMDR).

The output level can be set for the three positive phases and the three negative phases of six-phase output. The operating mode must be exited before setting or changing the output level.

(5) Dead Time Setting

In the operating modes, PWM pulses are output with a non-overlap relationship between the positive and negative phases. This non-overlap time is known as the dead time. The non-overlap time is set in the timer dead time data register (TDDR). The dead time generation waveform is generated by comparing the value set in TDDR with the timer dead time counters (TDCNT) for each phase. The operating mode must be exited before changing the contents of TDDR.

(6) PWM Period Setting

In the operating modes, 1/2 the PWM pulse period is set in TPBR. The TPBR value should always be set in the range H'0000 to H'FFFF – 4Td. The value set in TPBR is transferred to TPDR at the timing selected with bits MD1 and MD0 in the timer mode register (TMDR). After the transfer, the value in TPDR is {TPBR value + 2Td}.

The new PWM period is effective from the next period when data is updated at the TCNT counter peak, and from the same period when data is updated at the trough.

(7) Register Updating

In the operating modes, buffer registers are used to update compare register data. Update data can be written to a buffer register at all times. The buffer register value is transferred to the compare register at the timing set by bits MD1 and MD0 in the timer mode register (TMDR) (except in the case of a write to the free operation address for TBRU to TBRW, in which case the value is transferred to the corresponding compare register immediately).

(8) Initial Output in Operating Modes

The initial output in the operating modes is determined by the initial values of TBRU to TBRW.

Table 13.2 shows the relationship between the initial value of TBRU to TBRW and the initial output.

Table 13.2 Initial Values of TBRU to TBRW and Initial Output

	Initial Output	
Initial Value of TBRU to TBRW	**OLSP = 1, OLSN = 1**	**OLSP = 0, OLSN = 0**
TBR = H'0000	Positive phase: 1 Negative phase: 0	Positive phase: 0 Negative phase: 1
H'0000 < TBR ≤ Td	Positive phase: 0 Negative phase: 0	Positive phase: 1 Negative phase: 1
Td < TBR ≤ H'FFFF – 2Td	Positive phase: 0 Negative phase: 1	Positive phase: 1 Negative phase: 0

(9) PWM Output Generation in Operating Modes

In the operating modes, a three-phase PWM waveform is output with a non-overlap relationship between the positive and negative phases. This non-overlap time is called the dead time.

The PWM waveform is generated from an output generation waveform generated by ANDing the compare output waveform with the dead time generation waveform. Waveform generation for one phase (the U-phase) is shown here. The V-phase and W-phase waveforms are generated in the same way.

(a) Compare Output Waveform

The compare output waveform is generated by comparing the values in TCNT and TGR.

For compare output waveform U phase A (CMOUA), 0 is output if TGRUU > TCNT in the T1 interval (when TCNT is counting up), and 1 is output if TGRUU ≤ TCNT. In the T2 interval (when TCNT is counting down), 0 is output if TGRU > TCNT, and 1 is output if TGRU ≤ TCNT.

For compare output waveform U phase B (CMOUB), 1 is output if TGRU > TCNT in the T1 interval, and 0 is output if TGRU ≤ TCNT. In the T2 interval, 1 is output if TGRUD > TCNT, and 0 is output if TGRUD ≤ TCNT.

(b) Dead Time Generation Waveform

For dead time generation waveform U phases A (DTGUA) and B (DTGUB), 1 is output as the initial value.

TDCNT0 starts counting at the falling edge of CMOUA. DTGUA outputs 0 if TDCNT0 is counting, and 1 otherwise.

TDCNT1 starts counting at the falling edge of CMOUB. DTGUB outputs 0 if TDCNT1 is counting, and 1 otherwise.

(c) Output Generation Waveform

Output generation waveform U phase A (OGUA) is generated by ANDing CMOUA and DTGUB, and output generation waveform U phase B (OGUB) is generated by ANDing CMOUB and DTGUA.

(d) PWM Waveform

The PWM waveform is generated by converting the output generation waveform to the output level set in bits OLSN and OLSP in the timer mode register (TMDR).

Figure 13.5 shows an example of PWM waveform generation (operating mode 3, OLSN = 1, OLSP = 1).

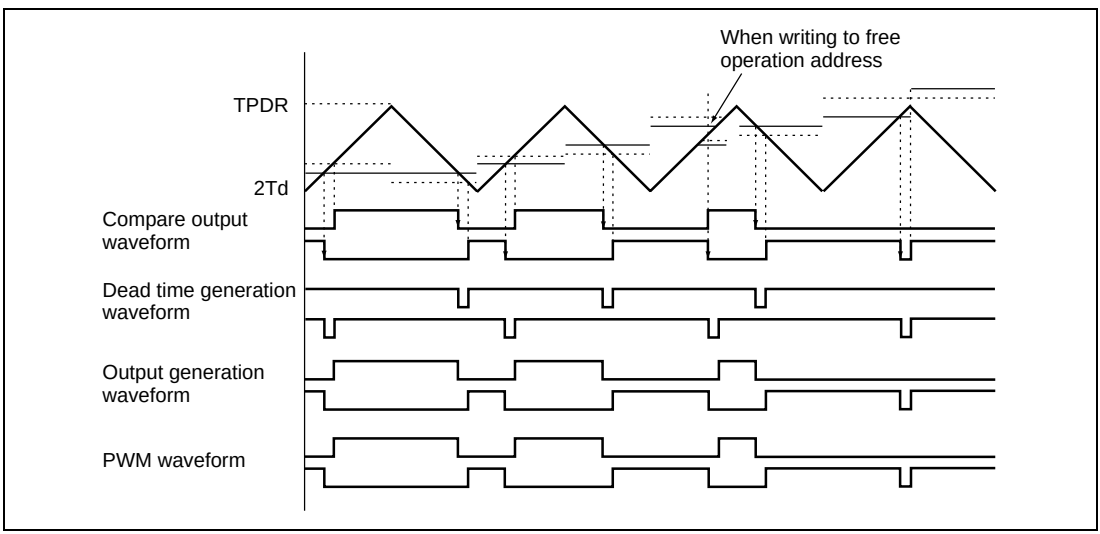


Figure 13.5 Example of PWM Waveform Generation

(10) 0% to 100% Duty Cycle Output

In the operating modes, PWM waveforms with any duty cycle from 0% to 100% can be output. The output PWM duty cycle is set using the buffer registers (TBRU to TBRW).

100% duty cycle output is performed when the buffer register (TBRU to TBRW) value is set to H'0000. The waveform in this case has positive phase in the 100% on state. 0% duty cycle output

is performed when a value greater than the TPDR value is set as the buffer register (TBRU to TBRW) value. The waveform in this case has positive phase in the 100% off state.

(11) External Counter Clear Function

In the operating modes, the TCNT counter can be cleared from an external source. When using the counter clearing function, the port A I/O register L (PAIORL) should be used to set the PCIO pin as an input.

On the falling edge of the PCIO pin (when set to input), the TCNT counter is reset to 2Td (the initial setting). It then counts up until it reaches the value in TPDR, then starts counting down. When the count returns to 2Td, TCNT starts counting up again, and this sequence is repeated. Figure 13.6 shows the example for counter clearing.

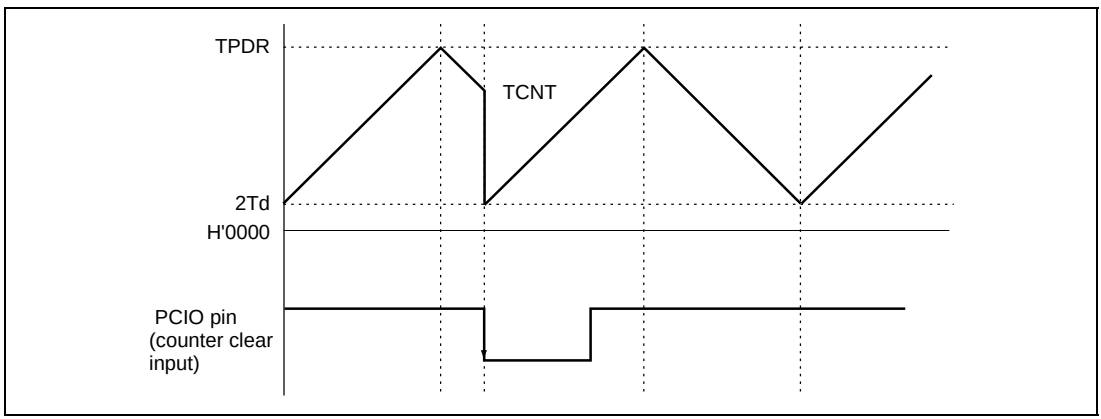


Figure 13.6 Example of TCNT Counter Clearing

(12) Toggle Output Synchronized with PWM Cycle

In the operating modes, output can be toggled synchronously with the PWM carrier cycle. When outputting the PWM cycle, the pin function controller (PFC) should be used to set the PCIO pin as an output (when set to output). An example of the toggle output waveform is shown in figure 13.7.

PWM cycle output is toggled according to the TCNT count direction. The toggle output pin is PCIO (when set to output). The PCIO pin outputs 1 when TCNT is counting up, and 0 when counting down.

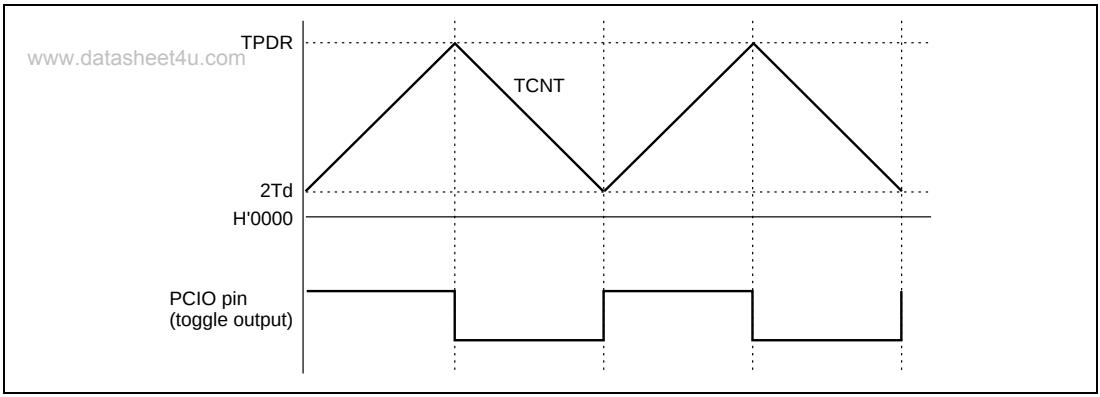


Figure 13.7 Example of Toggle Output Waveform Synchronized with PWM Cycle

(13) Settings for A/D Conversion Start Requests

Requests to start A/D conversion can be set up to be issued when TCNT matches TPDR or 2Td. When the start requests are set up for issue when TCNT matches TPDR, A/D conversion will start at the center of the PWM pulse (the peak value of the TCNT counter). When the start requests are set up for issue when TCNT matches 2Td, A/D conversion will start on the edge of the PWM pulse (the minimum value of the TCNT counter).

Requests to start A/D conversion is enabled by setting the TTGE bit in the timer control register (TCNR) to 1.

Table 13.3 shows the relationship between A/D conversion start timing and operating mode.

Table 13.3 Relationship between A/D Conversion Start Timing and Operating Mode

Operating Mode	A/D Conversion Start Timing
Operating mode 1 (transfer at peak)	A/D conversion start at trough
Operating mode 2 (transfer at trough)	A/D conversion start at peak
Operating mode 3 (transfer at peak and trough)	A/D conversion start at peak and trough

13.4.2 Output Protection Functions

Operating mode output has the following protection functions:

- Halting MMT output by external signal

  The six-phase PWM output pins can be placed in the high-impedance state automatically by inputting a specified external signal. There are three external signal input pins. For details, see section 13.8, Port Output Enable (POE).

- Halting MMT output when oscillation stops

The six-phase PWM output pins are placed in the high-impedance state automatically when stoppage of the clock input is detected. However, pin states are not guaranteed when the clock is restarted.

13.5 Interrupt Sources

When the TGFM (TGFN) flag is set to 1 in the timer status register (TSR) by a compare match between TCNT and TPDR (2Td), and if the TGIEM (TGIEN) bit setting in the timer control register (TCNR) is 1, an interrupt is requested. The interrupt request is cleared by clearing the TGF flag to 0.

Table 13.4 MMT Interrupt Sources

Name	Interrupt Source	Interrupt Flag
TGIMN	Compare match between TCNT and TPDR	TGFM
TGINN	Compare match between TCNT and 2Td	TGFN

The on-chip A/D converter can be activated when TCNT matches TPDR or 2Td. When the TGF flag in the timer status register (TSR) is set to 1 as a result of either match, a request to start A/D conversion is sent to the A/D converter. If the conversion start trigger of the MMT is selected in the A/D converter at that time, A/D conversion starts.

13.6 Operation Timing

13.6.1 Input/Output Timing

(1) TCNT and TDCNT Count Timing

Figure 13.8 shows the TCNT and TDCNT count timing.

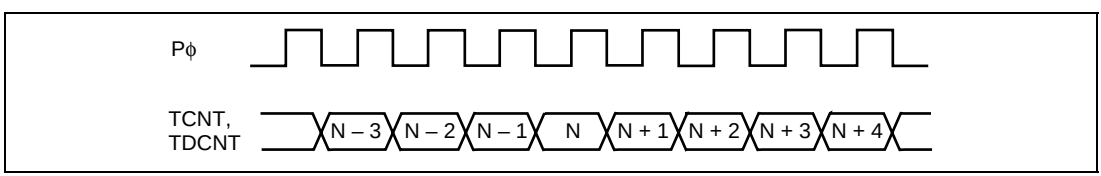


Figure 13.8 Count Timing

(2) TCNT Counter Clearing Timing

Figure 13.9 shows the timing of TCNT counter clearing by an external signal.

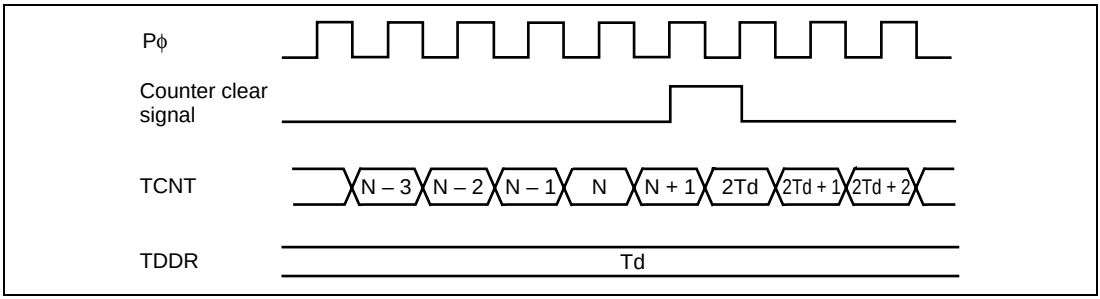


Figure 13.9 TCNT Counter Clearing Timing

(3) TDCNT Operation Timing

Figure 13.10 shows the TDCNT operation timing.

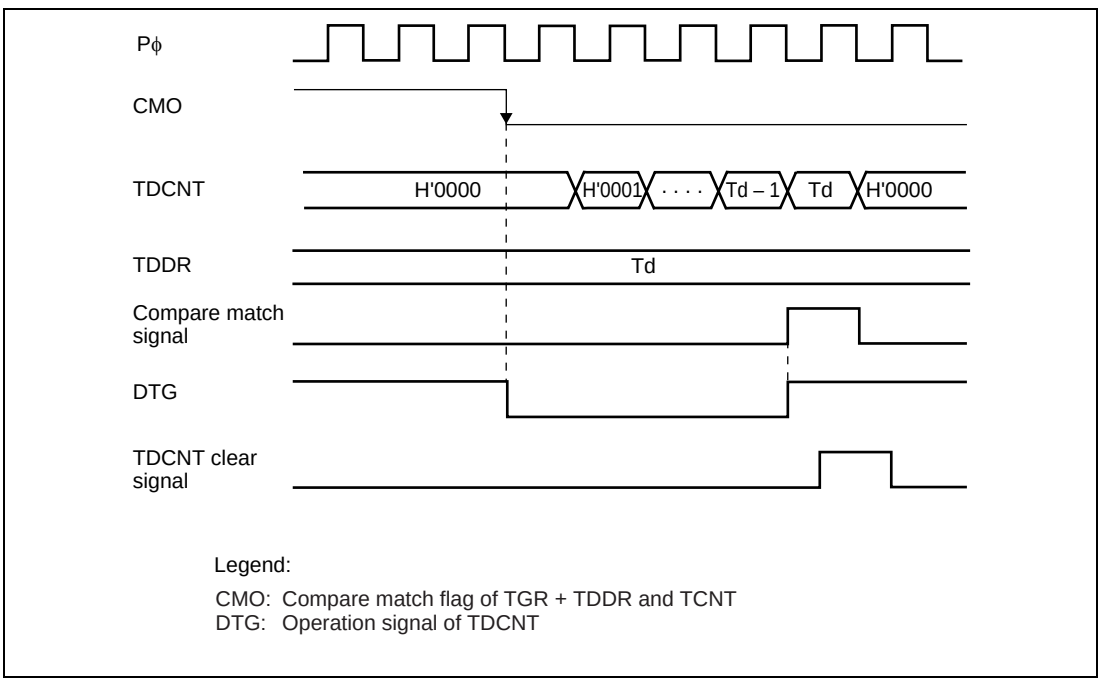


Figure 13.10 TDCNT Operation Timing

(4) Buffer Operation Timing

Figure 13.11 shows the compare match buffer operation timing.

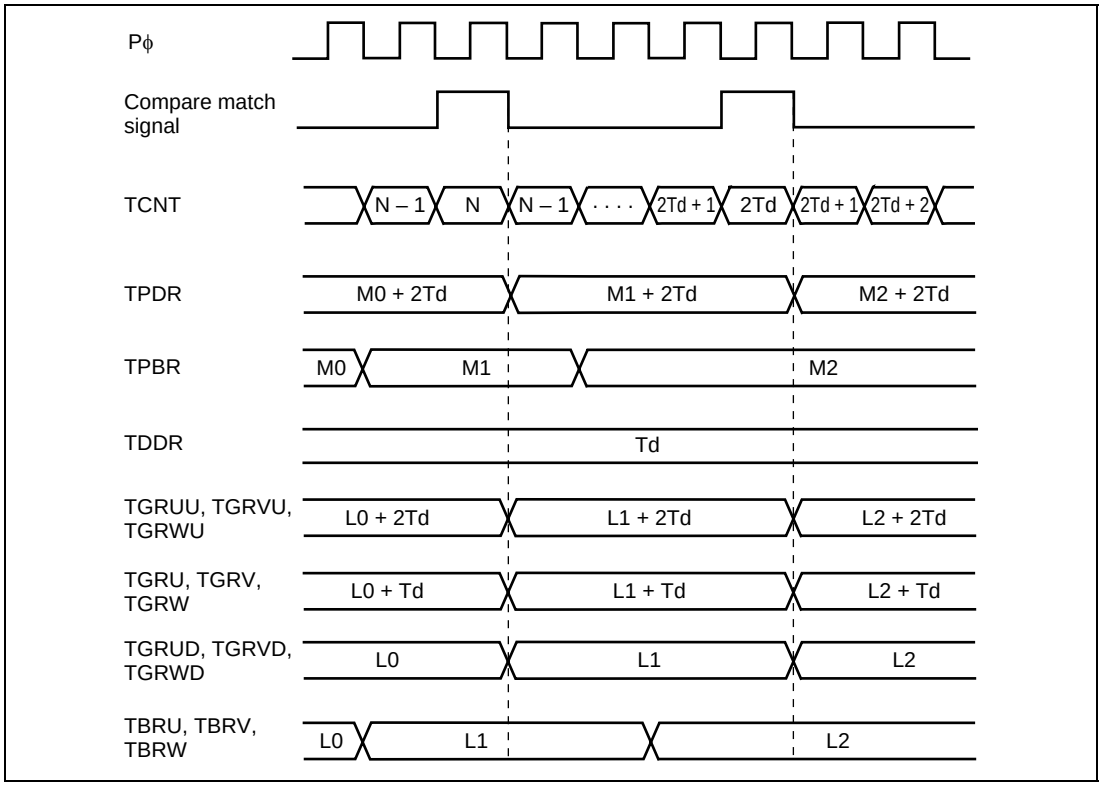


Figure 13.11 Buffer Operation Timing

13.6.2 Interrupt Signal Timing

(1) Timing of TGF Flag Setting by Compare Match

Figure 13.12 shows the timing of setting of the TGF flag in the timer status register (TSR) on a compare match between TCNT and TPDR, and the timing of the TGI interrupt request signal. The timing is the same for a compare match between TCNT and 2Td.

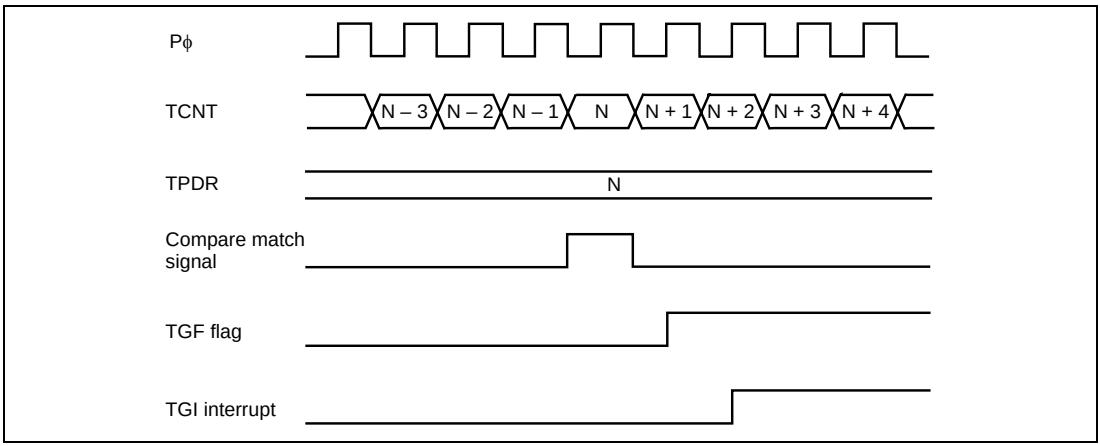


Figure 13.12 TGI Interrupt Timing

(2) Status Flag Clearing Timing

A status flag is cleared when the CPU reads 1 from the flag, then 0 is written to it. Figure 13.13 shows the timing of status flag clearing by the CPU.

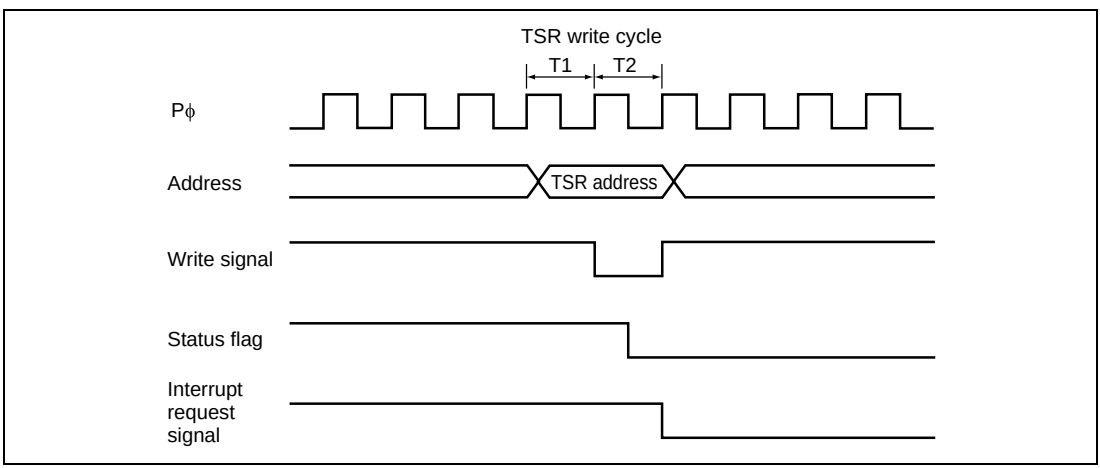


Figure 13.13 Timing of Status Flag Clearing by CPU

13.7 Usage Notes

13.7.1 Module Standby Mode Setting

MMT operation can be disabled or enabled using the module standby control register. The initial setting is for MMT operation to be halted. Register access is enabled by clearing module standby mode. For details, refer to section 18, Power-Down Modes.

13.7.2 Notes on MMT Operation

Note that the kinds of operation and contention described below occur during MMT operation.

(1) Contention between Buffer Register Write and Compare Match

If a compare match occurs in the T2 state of a buffer register (TBRU to TBRW, or TPBR) write cycle, data is transferred from the buffer register to the compare register (TGR or TPDR) by a buffer operation. The data transferred is the buffer register write data.

Figure 13.14 shows the timing in this case.

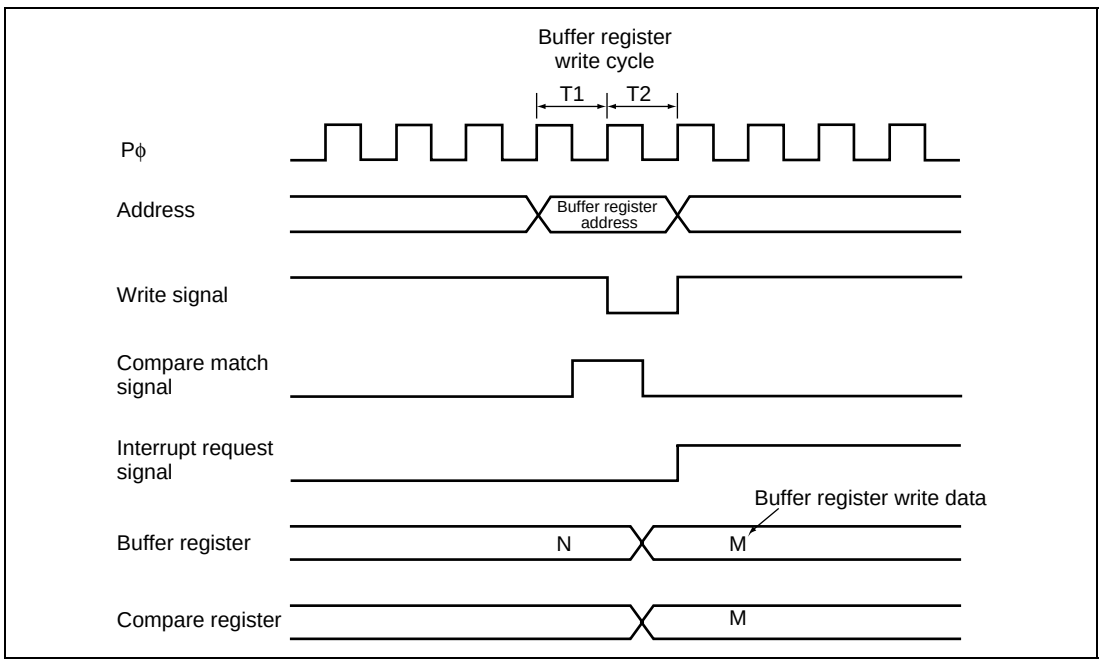


Figure 13.14 Contention between Buffer Register Write and Compare Match

(2) Contention between Compare Register Write and Compare Match

If a compare match occurs in the T2 state of a compare register (TGR or TPDR) write cycle, the compare register write is not performed, and data is transferred from the buffer register (TBRU, TBRV, TBRW, or TPBR) to the compare register by a buffer operation.

Figure 13.15 shows the timing in this case.

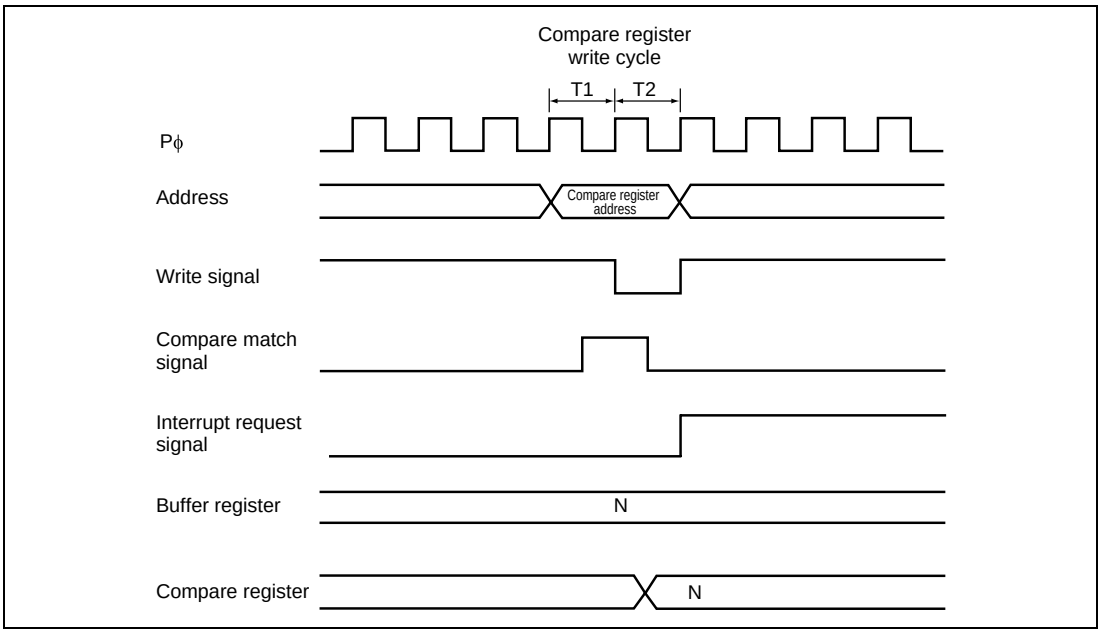


Figure 13.15 Contention between Compare Register Write and Compare Match

(3) Pay Attention to the Notices Below, When a Value is Written into the Timer General Register U (TGRU), Timer General Register V (TGRV), Timer General Register W (TGRW), and in Case of Written into Free Operation Address (*)

- In case of counting up: Do not write a value {Previous value of TGRU + Td} into TGRU.
- In case of counting down: Do not write a value {Previous value of TGRU - Td} into TGRU.

In the same manner to TGRV and TGRW. When a value {Previous value of TGRU + Td} is written (in case of counting down {Previous value of TGRU - Td}), the output of PUOA/PUOB, PVOA/PVOB, PWOA/PWOB (corresponding to U, V, W phase) may not be output for 1 cycle. Figure 15.17 shows the error case. When writing into the buffer operation address, these notes are not relevant.

Note: * When addresses, H'FFFF8A1C, H'FFFF8A2C, H'FFFF8A3C are used as register address for TBRU, TBRV, TBRW, respectively.

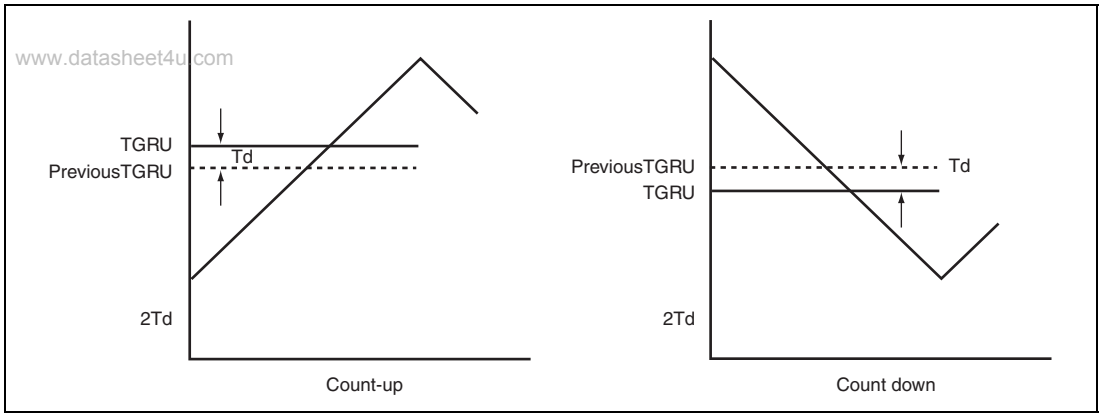


Figure 13.16 Writing into Timer General Registers (When One Cycle is Not Output)

(4) Writing Operation into Timer Period Data Register (TPDR) and Timer Dead Time Data Register (TDDR) When MMT is Operating

- Do not revise TPDR register when MMT is operating. Always use a buffer-write operation through TPBR register.
- Do not revise TDDR register once an operation of MMT is invoked. When TDDR is revised, a wave may not be output for as much as 1 cycle (full count period of 16 bits in TDCNT), because a value cannot be written into TDCNT, which is compared to a value set in TDDR.

(5) Notes on Halting TCNT Counter Operation

If TCNT counter operation is halted, a PCM waveform may be output with dead time (non-overlap time) shorter than the value set in the timer dead time register (MMT_TDDR) or no dead time at all (value of 0). To prevent this, use one of the following methods.

(a) Set the CST bit in the timer control register (TCNR) to 1 and do not clear it to 0 after MMT counter operation starts. If the CST bit is cleared to 0, do not set it to 1 again.

(b) When setting, clearing, and then resetting the CST bit, use the following procedure for clearing and then resetting.

(1) Use the pin function controller (PFC) to set the PWM output pin as a general input port.

(2) Set the free operation addresses for all the buffer registers (TBRU, TBRV, and TBRW) to H'0000.

(3) After the specified dead time duration has elapsed, set TCNR to H'00 and clear the CST bit to 0.

(4) Once again, set the CST bit to 1.

(c) When setting, clearing, and then resetting the CST bit, use the following procedure for clearing and then resetting.

(1) Clear the CST bit in TCNR to 0 to halt counter operation.

(2) Use the pin function controller to set the PWM output pin as a general input port.

(3) Clear the MSTP14 bit in module standby control register 2 (MSTCR2) to 0 to transition to module standby mode, and initialize the internal status of MMT.

(4) Immediately set the MSTP14 bit to 1 to transition back from module standby mode. Reinitialize MMT and the pin.

(5) Set the CST bit in TCNR to 1 to restart counter operation.

13.8 Port Output Enable (POE)

The port output enable (POE) circuit enables the MMT's output pins (POUA, POUB, POVA, POVB, POWA, and POWB) to be placed in the high-impedance state by varying the input to pins $\overline{\text{POE4}}$ to $\overline{\text{POE6}}$. An interrupt can also be requested at the same time. In addition, the MMT's output pins will also enter the high-impedance state in standby mode or when the oscillator halts.

13.8.1 Features

The POE circuit has the following features:

- Falling edge, Pϕ/8 × 16 times, Pϕ/16 × 16 times, or Pϕ/128 × 16 times low-level sampling can be set for each of input pins $\overline{\text{POE4}}$ to $\overline{\text{POE6}}$.
- The MMT's output pins can be placed in the high-impedance state at the falling edge or low-level sampling of pins $\overline{\text{POE4}}$ to $\overline{\text{POE6}}$.
- An interrupt can be generated by input level sampling.

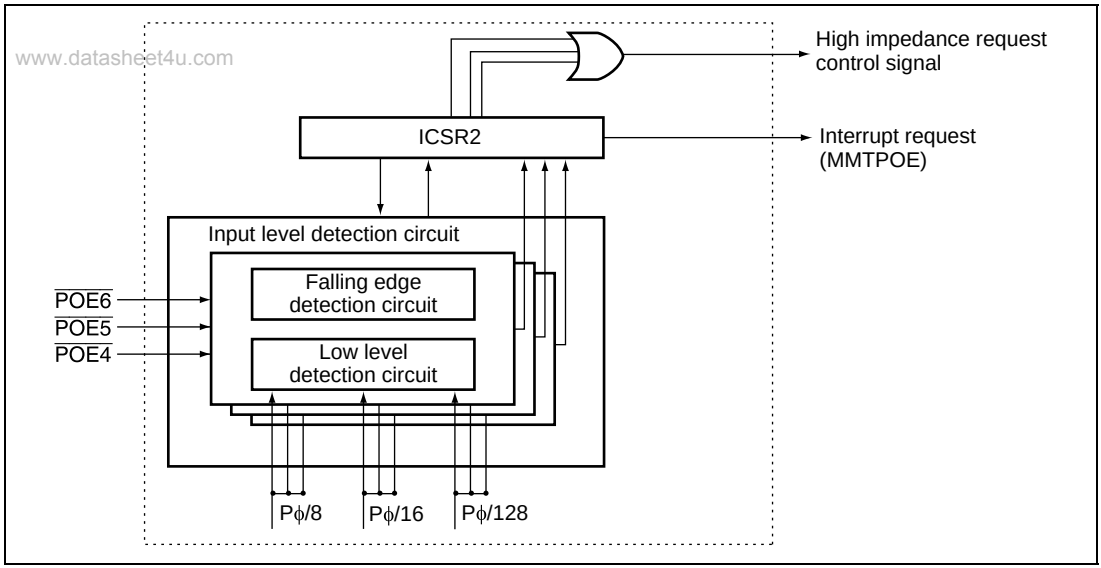


Figure 13.17 Block Diagram of POE

13.8.2 Input/Output Pins

Table13.5 shows the pin configuration of the POE circuit.

Table 13.5 Pin Configuration

Name	Abbreviation	I/O	Function
Port output enable input pins	$\overline{\text{POE4}}$ to $\overline{\text{POE6}}$	Input	Input request signals for placing MMT's output pins in high-impedance state

13.8.3 Register Description

The POE circuit has the following register.

- Input level control/status register 2 (ICSR2)

(1) Input Level Control/Status Register 2 (ICSR2)

ICSR2 is a 16-bit readable/writable register that selects the input mode for pins $\overline{\text{POE4}}$ to $\overline{\text{POE6}}$, controls enabling or disabling of interrupts, and holds status information.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	POE6F	0	R/(W)*	POE6 Flag Indicates that a high impedance request has been input to the $\overline{\text{POE6}}$ pin. [Clearing condition] • When 0 is written to POE6F after reading POE6F = 1 [Setting condition] • When the input set by bits 4 and 5 in ICSR2 occurs at the $\overline{\text{POE6}}$ pin
13	POE5F	0	R/(W)*	POE5 Flag Indicates that a high impedance request has been input to the $\overline{\text{POE5}}$ pin. [Clearing condition] • When 0 is written to POE5F after reading POE5F = 1 [Setting condition] • When the input set by bits 2 and 3 in ICSR2 occurs at the $\overline{\text{POE5}}$ pin
12	POE4F	0	R/(W)*	POE4 Flag Indicates that a high impedance request has been input to the $\overline{\text{POE4}}$ pin. [Clearing condition] • When 0 is written to POE4F after reading POE4F = 1 [Setting condition] • When the input set by bits 0 and 1 in ICSR2 occurs at the $\overline{\text{POE4}}$ pin

Bit	Bit Name	Initial Value	R/W	Description
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	PIE	0	R/W	Port Interrupt Enable Enables or disables an interrupt request when 1 is set in any of bits POE4F to POE6F in ICSR2. 0: Interrupt request disabled 1: Interrupt request enabled
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	POE6M1	0	R/W	POE6 Mode 1 and 0
4	POE6M0	0	R/W	Select the input mode of the $\overline{\text{POE6}}$ pin. 00: Request accepted at falling edge of $\overline{\text{POE6}}$ input 01: $\overline{\text{POE6}}$ input is sampled for low level 16 times every Pϕ/8 clock, and request is accepted when all samples are low level 10: $\overline{\text{POE6}}$ input is sampled for low level 16 times every Pϕ/16 clock, and request is accepted when all samples are low level 11: $\overline{\text{POE6}}$ input is sampled for low level 16 times every Pϕ/128 clock, and request is accepted when all samples are low level
3	POE5M1	0	R/W	POE5 Mode 1 and 0
2	POE5M0	0	R/W	Select the input mode of the $\overline{\text{POE5}}$ pin. 00: Request accepted at falling edge of $\overline{\text{POE5}}$ input 01: $\overline{\text{POE5}}$ input is sampled for low level 16 times every Pϕ/8 clock, and request is accepted when all samples are low level 10: $\overline{\text{POE5}}$ input is sampled for low level 16 times every Pϕ/16 clock, and request is accepted when all samples are low level 11: $\overline{\text{POE5}}$ input is sampled for low level 16 times every Pϕ/128 clock, and request is accepted when all samples are low level

Bit	Bit Name	Initial Value	R/W	Description
1	POE4M1	0	R/W	POE4 Mode 1 and 0
0	POE4M0	0	R/W	Select the input mode of the $\overline{\text{POE4}}$ pin. 00: Request accepted at falling edge of $\overline{\text{POE4}}$ input 01: $\overline{\text{POE4}}$ input is sampled for low level 16 times every Pϕ/8 clock, and request is accepted when all samples are low level 10: $\overline{\text{POE4}}$ input is sampled for low level 16 times every Pϕ/16 clock, and request is accepted when all samples are low level 11: $\overline{\text{POE4}}$ input is sampled for low level 16 times every Pϕ/128 clock, and request is accepted when all samples are low level

Note: * Only 0 can be written to clear the flag.

13.8.4 Operation

(1) Input Level Detection

When the input condition set in ICSR2 occurs on any one of the $\overline{\text{POE}}$ pins, the MMT output pins enter the high-impedance state.

- Pins placed in the high-impedance state (the MMT's output pins)
  The six pins PWOB, PWOA, PVOB, PVOA, PUOB, and PUOA in the motor management timer (MMT) are placed in the high-impedance state.

Note: These pins are in the high-impedance state only when each pin is used as the general input/output function or MMT output pin.

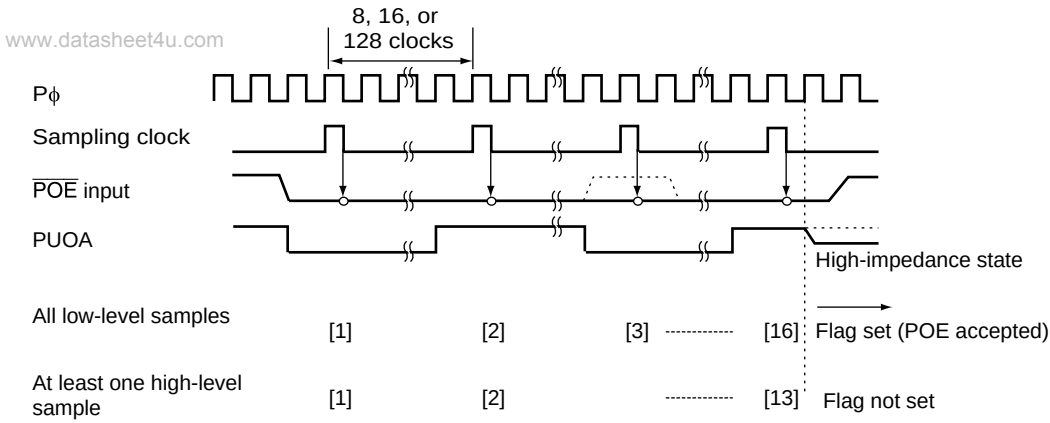
(a) Falling Edge Detection

When a transition from high- to low-level input occurs on a $\overline{\text{POE}}$ pin

(b) Low Level Detection

Figure 13.18 shows the low level detection operation. Low level sampling is performed 16 times in succession using the sampling clock set in ICSR2. The input is not accepted if a high level is detected even once among these samples.

The timing of entry of the MMT's output pins into the high-impedance state from the sampling clock is the same for falling edge detection and low level detection.



Note: The other MMT output pins also enter the high-impedance state at the same timing.

Figure 13.18 Low Level Detection Operation

(2) Exiting High-Impedance State

The MMT output pins that have entered the high-impedance state by the input level detection are released from this state by restoring them to their initial states by means of a power-on reset, or by clearing all the POE flags in ICSR2 (POE4F to POE6F: bits 12 to 14).

13.8.5 Usage Note

To set the POE pin as a level-detective pin, a high level signal must be firstly input to the POE pin.

Section 14 Pin Function Controller (PFC)

The pin function controller (PFC) is composed of those registers that are used to select the functions of multiplexed pins and assign pins to be inputs or outputs. Tables 14.1 to 14.10 list the multiplexed pins of this LSI.

Tables 14.11 and 14.12 list the pin functions in each operating mode.

Table 14.1 SH7108 Multiplexed Pins (Port A)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)	Function 6 (Related Module)	Function 7 (Related Module)	Function 8 (Related Module)
A	PA0 I/O (port)	—	—	—	—	$\overline{\text{POE0}}$ input (port)	RxD2 input (SCI)	—
	PA1 I/O (port)	—	—	—	—	$\overline{\text{POE1}}$ input (port)	TxD2 output (SCI)	—
	PA2 I/O (port)	—	—	$\overline{\text{IRQ0}}$ input (INTC)	—	PCIO I/O (MMT)	SCK2 I/O (SCI)	—
	PA3 I/O (port)	—	—	—	—	—	RxD3 input (SCI)	—
	PA4 I/O (port)	—	—	—	—	—	TxD3 output (SCI)	—
	PA5 I/O (port)	—	—	$\overline{\text{IRQ1}}$ input (INTC)	—	—	SCK3 I/O (SCI)	—
	PA6 I/O (port)	TCLKA input (MTU)	—	—	—	RxD2 input (SCI)	—	—
	PA7 I/O (port)	TCLKB input (MTU)	—	—	—	TxD2 output (SCI)	—	—
	PA8 I/O (port)	TCLKC input (MTU)	—	—	—	RxD3 input (SCI)	—	—
	PA9 I/O (port)	TCLKD input (MTU)	—	—	—	TxD3 output (SCI)	—	—
	PA10 I/O (port)	—	—	—	—	SCK2 I/O (SCI)	—	—
	PA11 I/O (port)	—	$\overline{\text{ADTRG}}$ input (A/D)	—	—	SCK3 I/O (SCI)	—	—
	PA12 I/O (port)	—	—	—	—	—	—	—
	PA13 I/O (port)	—	$\overline{\text{POE4}}$ input (port)	—	—	—	—	—
	PA14 I/O (port)	—	$\overline{\text{POE5}}$ input (port)	—	—	—	—	—
	PA15 I/O (port)	—	$\overline{\text{POE6}}$ input (port)	—	—	—	—	—

Table 14.2 SH7108 Multiplexed Pins (Port B)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)
B	PB2 I/O (port)	$\overline{\text{IRQ0}}$ input (INTC)	$\overline{\text{POE0}}$ input (port)	—
	PB3 I/O (port)	$\overline{\text{IRQ1}}$ input (INTC)	$\overline{\text{POE1}}$ input (port)	—
	PB4 I/O (port)	$\overline{\text{IRQ2}}$ input (INTC)	$\overline{\text{POE2}}$ input (port)	—
	PB5 I/O (port)	$\overline{\text{IRQ3}}$ input (INTC)	$\overline{\text{POE3}}$ input (port)	—

Table 14.3 SH7108 Multiplexed Pins (Port E)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)
E	PE0 I/O (port)	TIOC0A I/O (MTU)	—	—
	PE1 I/O (port)	TIOC0B I/O (MTU)	—	—
	PE2 I/O (port)	TIOC0C I/O (MTU)	—	—
	PE3 I/O (port)	TIOC0D I/O (MTU)	—	—
	PE4 I/O (port)	TIOC1A I/O (MTU)	RxD3 input (SCI)	—
	PE5 I/O (port)	TIOC1B I/O (MTU)	TxD3 output (SCI)	—
	PE6 I/O (port)	TIOC2A I/O (MTU)	SCK3 I/O (SCI)	—
	PE7 I/O (port)	TIOC2B I/O (MTU)	RxD2 input (SCI)	—
	PE8 I/O (port)	TIOC3A I/O (MTU)	SCK2 I/O (SCI)	—
	PE9 I/O (port)	TIOC3B I/O (MTU)	—	—
	PE10 I/O (port)	TIOC3C I/O (MTU)	TxD2 output (SCI)	—
	PE11 I/O (port)	TIOC3D I/O (MTU)	—	—
	PE12 I/O (port)	TIOC4A I/O (MTU)	—	—
	PE13 I/O (port)	TIOC4B I/O (MTU)	$\overline{\text{MRES}}$ input (INTC)	—
	PE14 I/O (port)	TIOC4C I/O (MTU)	—	—
	PE15 I/O (port)	TIOC4D I/O (MTU)	—	$\overline{\text{IRQOUT}}$ output (INTC)
	PE16 I/O (port)	PUOA output (MMT)	—	—
	PE17 I/O (port)	PVOA output (MMT)	—	—
	PE18 I/O (port)	PWOA output (MMT)	—	—
	PE19 I/O (port)	PUOB output (MMT)	—	—
	PE20 I/O (port)	PVOB output (MMT)	—	—
	PE21 I/O (port)	PWOB output (MMT)	—	—

Table 14.4 SH7108 Multiplexed Pins (Port F)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)
F	PF8 input (port)	AN8 input (A/D-0)	—	—
	PF9 input (port)	AN9 input (A/D-0)	—	—
	PF10 input (port)	AN10 input (A/D-0)	—	—
	PF11 input (port)	AN11 input (A/D-0)	—	—
	PF12 input (port)	AN12 input (A/D-1)	—	—
	PF13 input (port)	AN13 input (A/D-1)	—	—
	PF14 input (port)	AN14 input (A/D-1)	—	—
	PF15 input (port)	AN15 input (A/D-1)	—	—

Table 14.5 SH7108 Multiplexed Pins (Port G)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)
G	PG0 input (port)	AN16 input (A/D-2)	—	—
	PG1 input (port)	AN17 input (A/D-2)	—	—
	PG2 input (port)	AN18 input (A/D-2)	—	—
	PG3 input (port)	AN19 input (A/D-2)	—	—

Table 14.6 SH7109 Multiplexed Pins (Port A)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)	Function 6 (Related Module)	Function 7 (Related Module)	Function 8 (Related Module)
A	PA0 I/O (port)	—	—	—	A0 output (BSC)	$\overline{\text{POE0}}$ input (port)	RxD2 input (SCI)	—
	PA1 I/O (port)	—	—	—	A1 output (BSC)	$\overline{\text{POE1}}$ input (port)	TxD2 output (SCI)	—
	PA2 I/O (port)	—	—	$\overline{\text{IRQ0}}$ input (INTC)	A2 output (BSC)	PCIO I/O (MMT)	SCK2 I/O (SCI)	—
	PA3 I/O (port)	—	—	—	A3 output (BSC)	—	RxD3 input (SCI)	—
	PA4 I/O (port)	—	—	—	A4 output (BSC)	—	TxD3 output (SCI)	—
	PA5 I/O (port)	—	—	$\overline{\text{IRQ1}}$ input (INTC)	A5 output (BSC)	—	SCK3 I/O (SCI)	—
	PA6 I/O (port)	TCLKA input (MTU)	—	$\overline{\text{RD}}$ output (BSC)	—	RxD2 input (SCI)	—	—
	PA7 I/O (port)	TCLKB input (MTU)	—	$\overline{\text{WAIT}}$ input (BSC)	—	TxD2 output (SCI)	—	—
	PA8 I/O (port)	TCLKC input (MTU)	—	—	—	RxD3 input (SCI)	—	—
	PA9 I/O (port)	TCLKD input (MTU)	—	—	—	TxD3 output (SCI)	—	—
	PA10 I/O (port)	$\overline{\text{CS0}}$ output (BSC)	—	—	—	SCK2 I/O (SCI)	—	—
	PA11 I/O (port)	—	$\overline{\text{ADTRG}}$ input (A/D)	—	—	SCK3 I/O (SCI)	—	—
	PA12 I/O (port)	$\overline{\text{WRL}}$ output (BSC)	—	—	—	—	—	—
	PA13 I/O (port)	—	$\overline{\text{POE4}}$ input (port)	—	—	$\overline{\text{BREQ}}$ input (BSC)	—	—
	PA14 I/O (port)	$\overline{\text{RD}}$ output (BSC)	$\overline{\text{POE5}}$ input (port)	—	—	—	—	—
	PA15 I/O (port)	CK output (CPG)	$\overline{\text{POE6}}$ input (port)	—	—	$\overline{\text{BACK}}$ output (BSC)	—	—

Table 14.7 SH7109 Multiplexed Pins (Port B)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)	Function 6 (Related Module)	Function 7 (Related Module)	Function 8 (Related Module)
B	PB0 I/O (port)	A16 output (BSC)	—	—	—	—	—	—
	PB1 I/O (port)	A17 output (BSC)	—	—	—	—	—	—
	PB2 I/O (port)	$\overline{\text{IRQ0}}$ input (INTC)	$\overline{\text{POE0}}$ input (port)	—	—	—	—	—
	PB3 I/O (port)	$\overline{\text{IRQ1}}$ input (INTC)	$\overline{\text{POE1}}$ input (port)	—	—	—	—	—
	PB4 I/O (port)	$\overline{\text{IRQ2}}$ input (INTC)	$\overline{\text{POE2}}$ input (port)	—	—	—	—	—
	PB5 I/O (port)	$\overline{\text{IRQ3}}$ input (INTC)	$\overline{\text{POE3}}$ input (port)	—	—	CK output (CPG)	—	—

Table 14.8 SH7109 Multiplexed Pins (Port D)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)
D	PD0 I/O (port)	D0 I/O (BSC)	RxD2 input (SCI)	—
	PD1 I/O (port)	D1 I/O (BSC)	TxD2 output (SCI)	—
	PD2 I/O (port)	D2 I/O (BSC)	SCK2 I/O (SCI)	—
	PD3 I/O (port)	D3 I/O (BSC)	—	—
	PD4 I/O (port)	D4 I/O (BSC)	—	—
	PD5 I/O (port)	D5 I/O (BSC)	—	—
	PD6 I/O (port)	D6 I/O (BSC)	—	—
	PD7 I/O (port)	D7 I/O (BSC)	—	—
	PD8 I/O (port)	—	—	—

Table 14.9 SH7109 Multiplexed Pins (Port E)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)
E	PE0 I/O (port)	TIOC0A I/O (MTU)	—	$\overline{CS0}$ output (BSC)
	PE1 I/O (port)	TIOC0B I/O (MTU)	—	—
	PE2 I/O (port)	TIOC0C I/O (MTU)	—	—
	PE3 I/O (port)	TIOC0D I/O (MTU)	—	—
	PE4 I/O (port)	TIOC1A I/O (MTU)	RxD3 input (SCI)	A6 output (BSC)
	PE5 I/O (port)	TIOC1B I/O (MTU)	TxD3 output (SCI)	A7 output (BSC)
	PE6 I/O (port)	TIOC2A I/O (MTU)	SCK3 I/O (SCI)	A8 output (BSC)
	PE7 I/O (port)	TIOC2B I/O (MTU)	RxD2 input (SCI)	A9 output (BSC)
	PE8 I/O (port)	TIOC3A I/O (MTU)	SCK2 I/O (SCI)	—
	PE9 I/O (port)	TIOC3B I/O (MTU)	—	—
	PE10 I/O (port)	TIOC3C I/O (MTU)	TxD2 output (SCI)	$\overline{WRL}$ output (BSC)
	PE11 I/O (port)	TIOC3D I/O (MTU)	—	—
	PE12 I/O (port)	TIOC4A I/O (MTU)	—	—
	PE13 I/O (port)	TIOC4B I/O (MTU)	$\overline{MRES}$ input (INTC)	—
	PE14 I/O (port)	TIOC4C I/O (MTU)	—	—
	PE15 I/O (port)	TIOC4D I/O (MTU)	—	$\overline{IRQOUT}$ output (INTC)
	PE16 I/O (port)	PUOA output (MMT)	—	A10 output (BSC)
	PE17 I/O (port)	PVOA output (MMT)	$\overline{WAIT}$ input (BSC)	A11 output (BSC)
	PE18 I/O (port)	PWOA output (MMT)	—	A12 output (BSC)
	PE19 I/O (port)	PUOB output (MMT)	—	A13 output (BSC)
	PE20 I/O (port)	PVOB output (MMT)	—	A14 output (BSC)
	PE21 I/O (port)	PWOB output (MMT)	—	A15 output (BSC)

Table 14.10 SH7109 Multiplexed Pins (Port F)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)
F	PF0 input (port)	AN0 input (A/D-0)	—	—
	PF1 input (port)	AN1 input (A/D-0)	—	—
	PF2 input (port)	AN2 input (A/D-0)	—	—
	PF3 input (port)	AN3 input (A/D-0)	—	—
	PF4 input (port)	AN4 input (A/D-1)	—	—
	PF5 input (port)	AN5 input (A/D-1)	—	—
	PF6 input (port)	AN6 input (A/D-1)	—	—
	PF7 input (port)	AN7 input (A/D-1)	—	—
	PF8 input (port)	AN8 input (A/D-0)	—	—
	PF9 input (port)	AN9 input (A/D-0)	—	—
	PF10 input (port)	AN10 input (A/D-0)	—	—
	PF11 input (port)	AN11 input (A/D-0)	—	—
	PF12 input (port)	AN12 input (A/D-1)	—	—
	PF13 input (port)	AN13 input (A/D-1)	—	—
	PF14 input (port)	AN14 input (A/D-1)	—	—
	PF15 input (port)	AN15 input (A/D-1)	—	—

Table 14.11 SH7108 Pin Functions in Each Operating Mode

Pin No.	Pin Name	
	Single Chip Mode	
SH7108	Initial Function	Settable Function by PFC
11, 43, 66	Vcc	Vcc
9, 24, 41, 64	Vss	Vss
22, 62	VCL	VCL
27, 38	AVcc	AVcc
25, 40	AVss	AVss
1	PE2	PE2/TIOC0C
2	PE3	PE3/TIOC0D
3	PE4	PE4/TIOC1A/RxD3
4	PE5	PE5/TIOC1B/TxD3
5	PE6	PE6/TIOC2A/SCK3
6	PE7	PE7/TIOC2B/RxD2
7	PE8	PE8/TIOC3A/SCK2
8	PE9	PE9/TIOC3B
10	PE10	PE10/TIOC3C/TxD2
12	PE11	PE11/TIOC3D
13	PE12	PE12/TIOC4A
14	PE13	PE13/TIOC4B/$\overline{\text{MRES}}$
15	PE14	PE14/TIOC4C
16	PE15	PE15/TIOC4D/$\overline{\text{IRQOUT}}$
17	PE16	PE16/PUOA
18	PE17	PE17/PVOA
19	PE18	PE18/PWOA
20	PE19	PE19/PUOB
21	PE20	PE20/PVOB
23	PE21	PE21/PWOB
26	PF15/AN15	PF15/AN15
28	PF14/AN14	PF14/AN14
29	PF13/AN13	PF13/AN13
30	PF12/AN12	PF12/AN12
31	PG3/AN19	PG3/AN19
32	PG2/AN18	PG2/AN18

Pin No.	Pin Name	
	Single Chip Mode	
SH7108	Initial Function	Settable Function by PFC
33	PG1/AN17	PG1/AN17
34	PG0/AN16	PG0/AN16
35	PF11/AN11	PF11/AN11
36	PF10/AN10	PF10/AN10
37	PF9/AN9	PF9/AN9
39	PF8/AN8	PF8/AN8
42	PB5	PB5/$\overline{\text{IRQ3}}$/$\overline{\text{POE3}}$
44	PB4	PB4/$\overline{\text{IRQ2}}$/$\overline{\text{POE2}}$
45	PB3	PB3/$\overline{\text{IRQ1}}$/$\overline{\text{POE1}}$
46	PB2	PB2/$\overline{\text{IRQ0}}$/$\overline{\text{POE0}}$
47	PA15	PA15/$\overline{\text{POE6}}$
48	PA14	PA14/$\overline{\text{POE5}}$
49	PA13	PA13/$\overline{\text{POE4}}$
50	PA12	PA12
51	PA11	PA11/$\overline{\text{ADTRG}}$/SCK3
52	PA10	PA10/SCK2
53	PA9	PA9/TCLKD/TxD3
54	PA8	PA8/TCLKC/RxD3
55	PA7	PA7/TCLKB/TxD2
56	PA6	PA6/TCLKA/RxD2
57	PA5	PA5/$\overline{\text{IRQ1}}$/SCK3
58	PA4	PA4/TxD3
59	PA3	PA3/RxD3
60	PA2	PA2/$\overline{\text{IRQ0}}$/PCIO/SCK2
61	PA1	PA1/$\overline{\text{POE1}}$/TxD2
63	PA0	PA0/$\overline{\text{POE0}}$/RxD2
65	FWP	FWP
67	$\overline{\text{RES}}$	$\overline{\text{RES}}$
68	NMI	NMI
69	MD3	MD3
70	MD2	MD2
71	MD1	MD1
72	MD0	MD0

Pin No.	Pin Name	
	Single Chip Mode	
SH7108	Initial Function	Settable Function by PFC
73	EXTAL	EXTAL
74	XTAL	XTAL
75	PLLVCL	PLLVCL
76	PLLCAP	PLLCAP
77	PLLVss	PLLVss
78	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$
79	PE0	PE0/TIOC0A
80	PE1	PE1/TIOC0B

Table 14.12 SH7109 Pin Functions in Each Operating Mode (1)

Pin No.	Pin Name			
	On-Chip ROM Disabled		On-Chip ROM Enabled	
SH7109	Initial Function	Settable Function by PFC	Initial Function	Settable Function by PFC
15, 53, 72, 84	Vcc	Vcc	Vcc	Vcc
13, 29, 50, 74, 82	Vss	Vss	Vss	Vss
27, 77	VCL	VCL	VCL	VCL
33, 46	AVcc	AVcc	AVcc	AVcc
30, 49	AVss	AVss	AVss	AVss
1	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$
2	$\overline{\text{CS0}}$	$\overline{\text{CS0}}$	PE0	PE0/TIOC0A/$\overline{\text{CS0}}$
3	PE1	PE1/TIOC0B	PE1	PE1/TIOC0B
4	PE2	PE2/TIOC0C	PE2	PE2/TIOC0C
5	PE3	PE3/TIOC0D	PE3	PE3/TIOC0D
6	A6	A6	PE4	PE4/TIOC1A/RxD3/A6
7	A7	A7	PE5	PE5/TIOC1B/TxD3/A7
8	A8	A8	PE6	PE6/TIOC2A/SCK3/A8
9	A9	A9	PE7	PE7/TIOC2B/RxD2/A9
10	PE8	PE8/TIOC3A/SCK2	PE8	PE8/TIOC3A/SCK2
11	$\overline{\text{ASEBRKAK}}$	$\overline{\text{ASEBRKAK}}$	$\overline{\text{ASEBRKAK}}$	$\overline{\text{ASEBRKAK}}$
12	PE9	PE9/TIOC3B	PE9	PE9/TIOC3B
14	$\overline{\text{WRL}}$	$\overline{\text{WRL}}$	PE10	PE10/TIOC3C/TxD2/$\overline{\text{WRL}}$
16	$\overline{\text{DBGMD}}$	$\overline{\text{DBGMD}}$	$\overline{\text{DBGMD}}$	$\overline{\text{DBGMD}}$
17	PE11	PE11/TIOC3D	PE11	PE11/TIOC3D
18	PE12	PE12/TIOC4A	PE12	PE12/TIOC4A
19	PE13	PE13/TIOC4B/$\overline{\text{MRES}}$	PE13	PE13/TIOC4B/$\overline{\text{MRES}}$
20	PE14	PE14/TIOC4C	PE14	PE14/TIOC4C
21	PE15	PE15/TIOC4D/$\overline{\text{IRQOUT}}$	PE15	PE15/TIOC4D/$\overline{\text{IRQOUT}}$
22	A10	A10	PE16	PE16/PUOA/A10
23	A11	A11	PE17	PE17/PVOA/$\overline{\text{WAIT}}$/A11
24	A12	A12	PE18	PE18/PWOA/A12
25	A13	A13	PE19	PE19/PUOB/A13
26	A14	A14	PE20	PE20/PVOB/A14
28	A15	A15	PE21	PE21/PWOB/A15
31	PF7/AN7	PF7/AN7	PF7/AN7	PF7/AN7

Pin No.	Pin Name			
	On-Chip ROM Disabled		On-Chip ROM Enabled	
SH7109	Initial Function	Settable Function by PFC	Initial Function	Settable Function by PFC
32	PF15/AN15	PF15/AN15	PF15/AN15	PF15/AN15
34	PF6/AN6	PF6/AN6	PF6/AN6	PF6/AN6
35	PF14/AN14	PF14/AN14	PF14/AN14	PF14/AN14
36	PF5/AN5	PF5/AN5	PF5/AN5	PF5/AN5
37	PF13/AN13	PF13/AN13	PF13/AN13	PF13/AN13
38	PF4/AN4	PF4/AN4	PF4/AN4	PF4/AN4
39	PF12/AN12	PF12/AN12	PF12/AN12	PF12/AN12
40	PF11/AN11	PF11/AN11	PF11/AN11	PF11/AN11
41	PF3/AN3	PF3/AN3	PF3/AN3	PF3/AN3
42	PF10/AN10	PF10/AN10	PF10/AN10	PF10/AN10
43	PF2/AN2	PF2/AN2	PF2/AN2	PF2/AN2
44	PF9/AN9	PF9/AN9	PF9/AN9	PF9/AN9
45	PF1/AN1	PF1/AN1	PF1/AN1	PF1/AN1
47	PF8/AN8	PF8/AN8	PF8/AN8	PF8/AN8
48	PF0/AN0	PF0/AN0	PF0/AN0	PF0/AN0
51	CK	PB5/$\overline{\text{IRQ3}}$/$\overline{\text{POE3}}$/CK	CK	PB5/$\overline{\text{IRQ3}}$/$\overline{\text{POE3}}$/CK
52	PB4	PB4/$\overline{\text{IRQ2}}$/$\overline{\text{POE2}}$	PB4	PB4/$\overline{\text{IRQ2}}$/$\overline{\text{POE2}}$
54	PB3	PB3/$\overline{\text{IRQ1}}$/$\overline{\text{POE1}}$	PB3	PB3/$\overline{\text{IRQ1}}$/$\overline{\text{POE1}}$
55	PB2	PB2/$\overline{\text{IRQ0}}$/$\overline{\text{POE0}}$	PB2	PB2/$\overline{\text{IRQ0}}$/$\overline{\text{POE0}}$
56	A17	A17	PB1	PB1/A17
57	A16	A16	PB0	PB0/A16
58	PA15	PA15/CK/$\overline{\text{POE6}}$/$\overline{\text{BACK}}$	PA15	PA15/CK/$\overline{\text{POE6}}$/$\overline{\text{BACK}}$
59	PA14	PA14/$\overline{\text{RD}}$/$\overline{\text{POE5}}$	PA14	PA14/$\overline{\text{RD}}$/$\overline{\text{POE5}}$
60	PA13	PA13/$\overline{\text{POE4}}$/$\overline{\text{BREQ}}$	PA13	PA13/$\overline{\text{POE4}}$/$\overline{\text{BREQ}}$
61	PA12	PA12/$\overline{\text{WRL}}$	PA12	PA12/$\overline{\text{WRL}}$
62	PA11	PA11/$\overline{\text{ADTRG}}$/SCK3	PA11	PA11/$\overline{\text{ADTRG}}$/SCK3
63	PA10	PA10/$\overline{\text{CS0}}$/SCK2	PA10	PA10/$\overline{\text{CS0}}$/SCK2
64	PA9	PA9/TCLKD/TxD3	PA9	PA9/TCLKD/TxD3
65	PA8	PA8/TCLKC/RxD3	PA8	PA8/TCLKC/RxD3
66	PA7	PA7/TCLKB/$\overline{\text{WAIT}}$/TxD2	PA7	PA7/TCLKB/$\overline{\text{WAIT}}$/TxD2
67	$\overline{\text{RD}}$	$\overline{\text{RD}}$	PA6	PA6/TCLKA/$\overline{\text{RD}}$/RxD2
68	A5	A5	PA5	PA5/$\overline{\text{IRQ1}}$/A5/SCK3
69	A4	A4	PA4	PA4/A4/TxD3
70	A3	A3	PA3	PA3/A3/RxD3

Pin No.	Pin Name			
	On-Chip ROM Disabled		On-Chip ROM Enabled	
SH7109	Initial Function	Settable Function by PFC	Initial Function	Settable Function by PFC
71	A2	A2	PA2	PA2/$\overline{\text{IRQ0}}$/A2/PCIO/SCK2
73	A1	A1	PA1	PA1/A1/$\overline{\text{POE1}}$/TxD2
75	A0	A0	PA0	PA0/A0/$\overline{\text{POE0}}$/RxD2
76	PD8	PD8	PD8	PD8
78	D7	D7	PD7	PD7/D7
79	D6	D6	PD6	PD6/D6
80	D5	D5	PD5	PD5/D5
81	D4	D4	PD4	PD4/D4
83	FWP	FWP	FWP	FWP
85	$\overline{\text{HSTBY}}$	$\overline{\text{HSTBY}}$	$\overline{\text{HSTBY}}$	$\overline{\text{HSTBY}}$
86	D3	D3	PD3	PD3/D3
87	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$
88	D2	D2	PD2	PD2/D2/SCK2
89	NMI	NMI	NMI	NMI
90	D1	D1	PD1	PD1/D1/TxD2
91	MD3	MD3	MD3	MD3
92	D0	D0	PD0	PD0/D0/RxD2
93	MD2	MD2	MD2	MD2
94	MD1	MD1	MD1	MD1
95	MD0	MD0	MD0	MD0
96	EXTAL	EXTAL	EXTAL	EXTAL
97	XTAL	XTAL	XTAL	XTAL
98	PLLVCL	PLLVCL	PLLVCL	PLLVCL
99	PLLCAP	PLLCAP	PLLCAP	PLLCAP
100	PLLVss	PLLVss	PLLVss	PLLVss

Table 14.13 SH7109 Pin Functions in Each Operating Mode (2)

Pin No.	Pin Name	
	Single Chip Mode	
SH7109	Initial Function	Settable Function by PFC
15, 53, 72, 84	Vcc	Vcc
13, 29, 50, 74, 82	Vss	Vss
27, 77	VCL	VCL
33, 46	Avcc	Avcc
30, 49	AVss	AVss
1	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$
2	PE0	PE0/TIOC0A
3	PE1	PE1/TIOC0B
4	PE2	PE2/TIOC0C
5	PE3	PE3/TIOC0D
6	PE4	PE4/TIOC1A/RxD3
7	PE5	PE5/TIOC1B/TxD3
8	PE6	PE6/TIOC2A/SCK3
9	PE7	PE7/TIOC2B/RxD2
10	PE8	PE8/TIOC3A/SCK2
11	$\overline{\text{ASEBRKAK}}$	$\overline{\text{ASEBRKAK}}$
12	PE9	PE9/TIOC3B
14	PE10	PE10/TIOC3C/TxD2
16	$\overline{\text{DBGMD}}$	$\overline{\text{DBGMD}}$
17	PE11	PE11/TIOC3D
18	PE12	PE12/TIOC4A
19	PE13	PE13/TIOC4B/$\overline{\text{MRES}}$
20	PE14	PE14/TIOC4C
21	PE15	PE15/TIOC4D/$\overline{\text{IRQOUT}}$
22	PE16	PE16/PUOA
23	PE17	PE17/PVOA
24	PE18	PE18/PWOA
25	PE19	PE19/PUOB
26	PE20	PE20/PVOB
28	PE21	PE21/PWOB
31	PF7/AN7	PF7/AN7
32	PF15/AN15	PF15/AN15
34	PF6/AN6	PF6/AN6

Pin No.	Pin Name	
	Single Chip Mode	
SH7109	Initial Function	Settable Function by PFC
35	PF14/AN14	PF14/AN14
36	PF5/AN5	PF5/AN5
37	PF13/AN13	PF13/AN13
38	PF4/AN4	PF4/AN4
39	PF12/AN12	PF12/AN12
40	PF11/AN11	PF11/AN11
41	PF3/AN3	PF3/AN3
42	PF10/AN10	PF10/AN10
43	PF2/AN2	PF2/AN2
44	PF9/AN9	PF9/AN9
45	PF1/AN1	PF1/AN1
47	PF8/AN8	PF8/AN8
48	PF0/AN0	PF0/AN0
51	PB5	PB5/$\overline{\text{IRQ3}}$/$\overline{\text{POE3}}$/CK
52	PB4	PB4/$\overline{\text{IRQ2}}$/$\overline{\text{POE2}}$
54	PB3	PB3/$\overline{\text{IRQ1}}$/$\overline{\text{POE1}}$
55	PB2	PB2/$\overline{\text{IRQ0}}$/$\overline{\text{POE0}}$
56	PB1	PB1
57	PB0	PB0
58	PA15	PA15/CK/$\overline{\text{POE6}}$
59	PA14	PA14/$\overline{\text{POE5}}$
60	PA13	PA13/$\overline{\text{POE4}}$
61	PA12	PA12
62	PA11	PA11/$\overline{\text{ADTRG}}$/SCK3
63	PA10	PA10/SCK2
64	PA9	PA9/TCLKD/TxD3
65	PA8	PA8/TCLKC/RxD3
66	PA7	PA7/TCLKB/TxD2
67	PA6	PA6/TCLKA/RxD2
68	PA5	PA5/$\overline{\text{IRQ1}}$/SCK3
69	PA4	PA4/TxD3
70	PA3	PA3/RxD3
71	PA2	PA2/$\overline{\text{IRQ0}}$/PCIO/SCK2
73	PA1	PA1/$\overline{\text{POE1}}$/TxD2

Pin No.	Pin Name	
	Single Chip Mode	
SH7109	Initial Function	Settable Function by PFC
75	PA0	PA0/$\overline{\text{POE0}}$/RxD2
78	PD7	PD7
79	PD6	PD6
80	PD5	PD5
81	PD4	PD4
83	FWP	FWP
85	$\overline{\text{HSTBY}}$	$\overline{\text{HSTBY}}$
86	PD3	PD3
87	$\overline{\text{RES}}$	$\overline{\text{RES}}$
88	PD2	PD2/SCK2
89	NMI	NMI
90	PD1	PD1/TxD2
91	MD3	MD3
92	PD0	PD0/RxD2
93	MD2	MD2
94	MD1	MD1
95	MD0	MD0
96	EXTAL	EXTAL
97	XTAL	XTAL
98	PLLVCL	PLLVCL
99	PLLCAP	PLLCAP
100	PLLVss	PLLVss

14.1 Register Descriptions

The PFC has the following registers. For details on the addresses of the registers and their states during each process, refer to section 19, List of Registers.

- Port A I/O register L (PAIORL)
- Port A control register L3 (PACRL3)
- Port A control register L2 (PACRL2)
- Port A control register L1 (PACRL1)
- Port B I/O register (PBIOR)
- Port B control register 1 (PBCR1)
- Port B control register 2 (PBCR2)
- Port D I/O register L (PDIORL)
- Port D control register L1 (PDCRL1)
- Port D control register L2 (PDCRL2)
- Port E I/O register H (PEIORH)
- Port E I/O register L (PEIORL)
- Port E control register H (PECRH)
- Port E control register L1 (PECRL1)
- Port E control register L2 (PECRL2)

14.1.1 Port A I/O Register L (PAIORL)

PAIORL is a 16-bit readable/writable register that sets the pins on port A as inputs or outputs. Bits PA15IOR to PA0IOR correspond to pins PA15 to PA0 (names of multiplexed pins are here given as port names and pin numbers alone). PAIORL is enabled when the port A pins are functioning as general-purpose inputs/outputs (PA15 to PA0), SCK2 and SCK3 pins are functioning as inputs/outputs of the SCI, and PCIO pin is functioning as an input/output of the MMT. In other states, PAIORL is disabled.

A given pin on port A will be an output pin if the corresponding bit in PAIORL is set to 1, and an input pin if the bit is cleared to 0.

The initial value of PAIORL is H'0000.

14.1.2 Port A Control Registers L3 to L1 (PACRL3 to PACRL1)

PACRL3 to PACRL1 are 16-bit readable/writable registers that select the functions of the multiplexed pins on port A.

(1) Port A Control Registers L3 to L1 (PACRL3 to PACRL1) in SH7108

Register	Bit	Bit Name	Initial Value	R/W	Description
PACRL3	15	PA15MD2	0	R/W	PA15 Mode
PACRL1	15	PA15MD1	0	R/W	Select the function of the PA15/$\overline{\text{POE6}}$ pin.
PACRL1	14	PA15MD0	0	R/W	000: PA15 I/O (port) 011: Setting prohibited 001: Setting prohibited 1xx: Setting prohibited 010: $\overline{\text{POE6}}$ input (port)
PACRL3	14	PA14MD2	0	R/W	PA14 Mode
PACRL1	13	PA14MD1	0	R/W	Select the function of the PA14/$\overline{\text{POE5}}$ pin.
PACRL1	12	PA14MD0	0	R/W	000: PA14 I/O (port) 011: Setting prohibited 001: Setting prohibited 1xx: Setting prohibited 010: $\overline{\text{POE5}}$ input (port)
PACRL3	13	PA13MD2	0	R/W	PA13 Mode
PACRL1	11	PA13MD1	0	R/W	Select the function of the PA13/$\overline{\text{POE4}}$ pin.
PACRL1	10	PA13MD0	0	R/W	000: PA13 I/O (port) 011: Setting prohibited 001: Setting prohibited 1xx: Setting prohibited 010: $\overline{\text{POE4}}$ input (port)
PACRL3	12	PA12MD2	0	R/W	PA12 Mode
PACRL1	9	PA12MD1	0	R/W	Select the function of the PA12 pin.
PACRL1	8	PA12MD0	0	R/W	000: PA12 I/O (port) 011: Setting prohibited 001: Setting prohibited 1xx: Setting prohibited 010: Setting prohibited
PACRL3	11	PA11MD2	0	R/W	PA11 Mode
PACRL1	7	PA11MD1	0	R/W	Select the function of the PA11/$\overline{\text{ADTRG}}$/SCK3 pin.
PACRL1	6	PA11MD0	0	R/W	000: PA11 I/O (port) 100: Setting prohibited 001: Setting prohibited 101: SCK3 I/O (SCI) 010: $\overline{\text{ADTRG}}$ input (A/D) 110: Setting prohibited 011: Setting prohibited 111: Setting prohibited
PACRL3	10	PA10MD2	0	R/W	PA10 Mode
PACRL1	5	PA10MD1	0	R/W	Select the function of the PA10/SCK2 pin.
PACRL1	4	PA10MD0	0	R/W	000: PA10 I/O (port) 100: Setting prohibited 001: Setting prohibited 101: SCK2 I/O (SCI) 010: Setting prohibited 110: Setting prohibited 011: Setting prohibited 111: Setting prohibited

Register	Bit	Bit Name	Initial Value	R/W	Description	
PACRL3	9	PA9MD2	0	R/W	PA9 Mode	
PACRL1	3	PA9MD1	0	R/W	Select the function of the PA9/TCLKD/TxD3 pin.	
PACRL1	2	PA9MD0	0	R/W	000: PA9 I/O (port)	100: Setting prohibited
					001: TCLKD input (MTU)	101: TxD3 output (SCI)
					010: Setting prohibited	110: Setting prohibited
					011: Setting prohibited	111: Setting prohibited
PACRL3	8	PA8MD2	0	R/W	PA8 Mode	
PACRL1	1	PA8MD1	0	R/W	Select the function of the PA8/TCLKC/RxD3 pin.	
PACRL1	0	PA8MD0	0	R/W	000: PA8 I/O (port)	100: Setting prohibited
					001: TCLKC input (MTU)	101: RxD3 input (SCI)
					010: Setting prohibited	110: Setting prohibited
					011: Setting prohibited	111: Setting prohibited
PACRL3	7	PA7MD2	0	R/W	PA7 Mode	
PACRL2	15	PA7MD1	0	R/W	Select the function of the PA7/TCLKB/TxD2 pin.	
PACRL2	14	PA7MD0	0	R/W	000: PA7 I/O (port)	100: Setting prohibited
					001: TCLKB input (MTU)	101: TxD2 output (SCI)
					010: Setting prohibited	110: Setting prohibited
					011: Setting prohibited	111: Setting prohibited
PACRL3	6	PA6MD2	0	R/W	PA6 Mode	
PACRL2	13	PA6MD1	0	R/W	Select the function of the PA6/TCLKA/RxD2 pin.	
PACRL2	12	PA6MD0	0	R/W	000: PA6 I/O (port)	100: Setting prohibited
					001: TCLKA input (MTU)	101: RxD2 input (SCI)
					010: Setting prohibited	110: Setting prohibited
					011: Setting prohibited	111: Setting prohibited
PACRL3	5	PA5MD2	0	R/W	PA5 Mode	
PACRL2	11	PA5MD1	0	R/W	Select the function of the PA5/$\overline{\text{IRQ1}}$/SCK3 pin.	
PACRL2	10	PA5MD0	0	R/W	000: PA5 I/O (port)	100: Setting prohibited
					001: Setting prohibited	101: Setting prohibited
					010: Setting prohibited	110: SCK3 I/O (SCI)
					011: $\overline{\text{IRQ1}}$ input (INTC)	111: Setting prohibited
PACRL3	4	PA4MD2	0	R/W	PA4 Mode	
PACRL2	9	PA4MD1	0	R/W	Select the function of the PA4/TxD3 pin.	
PACRL2	8	PA4MD0	0	R/W	000: PA4 I/O (port)	100: Setting prohibited
					001: Setting prohibited	101: Setting prohibited
					010: Setting prohibited	110: TxD3 output (SCI)
					011: Setting prohibited	111: Setting prohibited

Register	Bit	Bit Name	Initial Value	R/W	Description	
PACRL3	3	PA3MD2	0	R/W	PA3 Mode	
PACRL2	7	PA3MD1	0	R/W	Select the function of the PA3/RxD3 pin.	
PACRL2	6	PA3MD0	0	R/W	000: PA3 I/O (port)	100: Setting prohibited
					001: Setting prohibited	101: Setting prohibited
					010: Setting prohibited	110: RxD3 input (SCI)
					011: Setting prohibited	111: Setting prohibited
PACRL3	2	PA2MD2	0	R/W	PA2 Mode	
PACRL2	5	PA2MD1	0	R/W	Select the function of the PA2/$\overline{\text{IRQ0}}$/PCIO/SCK2 pin.	
PACRL2	4	PA2MD0	0	R/W	000: PA2 I/O (port)	100: Setting prohibited
					001: Setting prohibited	101: PCIO I/O (MMT)
					010: Setting prohibited	110: SCK2 I/O (SCI)
					011: $\overline{\text{IRQ0}}$ input (INTC)	111: Setting prohibited
PACRL3	1	PA1MD2	0	R/W	PA1 Mode	
PACRL2	3	PA1MD1	0	R/W	Select the function of the PA1/$\overline{\text{POE1}}$/TxD2 pin.	
PACRL2	2	PA1MD0	0	R/W	000: PA1 I/O (port)	100: Setting prohibited
					001: Setting prohibited	101: $\overline{\text{POE1}}$ input (port)
					010: Setting prohibited	110: TxD2 output (SCI)
					011: Setting prohibited	111: Setting prohibited
PACRL3	0	PA0MD2	0	R/W	PA0 Mode	
PACRL2	1	PA0MD1	0	R/W	Select the function of the PA0/$\overline{\text{POE0}}$/RxD2 pin.	
PACRL2	0	PA0MD0	0	R/W	000: PA0 I/O (port)	100: Setting prohibited
					001: Setting prohibited	101: $\overline{\text{POE0}}$ input (port)
					010: Setting prohibited	110: RxD2 input (SCI)
					011: Setting prohibited	111: Setting prohibited

Legend: x: Don't care.

(2) Port A Control Registers L3 to L1 (PACRL3 to PACRL1) in SH7109

Register	Bit	Bit Name	Initial Value	R/W	Description
PACRL3	15	PA15MD2	0	R/W	PA15 Mode
PACRL1	15	PA15MD1	0	R/W	Select the function of the PA15/CK/$\overline{\text{POE6}}$/$\overline{\text{BACK}}$ pin.
PACRL1	14	PA15MD0	0	R/W	000: PA15 I/O (port) 100: Setting prohibited 001: CK output (CPG) 101: $\overline{\text{BACK}}$ output (BSC) 010: $\overline{\text{POE6}}$ input (port) 110: Setting prohibited 011: Setting prohibited 111: Setting prohibited
PACRL3	14	PA14MD2	0	R/W	PA14 Mode
PACRL1	13	PA15MD1	0	R/W	Select the function of the PA14/$\overline{\text{RD}}$/$\overline{\text{POE5}}$ pin.
PACRL1	12	PA14MD0	0	R/W	000: PA14 I/O (port) 100: Setting prohibited 001: $\overline{\text{RD}}$ output (BSC) 101: Setting prohibited 010: $\overline{\text{POE5}}$ input (port) 110: Setting prohibited 011: Setting prohibited 111: Setting prohibited
PACRL3	13	PA13MD2	0	R/W	PA13 Mode
PACRL1	11	PA13MD1	0	R/W	Select the function of the PA13/$\overline{\text{POE4}}$/$\overline{\text{BREQ}}$ pin.
PACRL1	10	PA13MD0	0	R/W	000: PA13 I/O (port) 100: Setting prohibited 001: Setting prohibited 101: $\overline{\text{BREQ}}$ input (BSC) 010: $\overline{\text{POE4}}$ input (port) 110: Setting prohibited 011: Setting prohibited 111: Setting prohibited
PACRL3	12	PA12MD2	0	R/W	PA12 Mode
PACRL1	9	PA12MD1	0	R/W	Select the function of the PA12/$\overline{\text{WRL}}$ pin.
PACRL1	8	PA12MD0	0	R/W	000: PA12 I/O (port) 100: Setting prohibited 001: $\overline{\text{WRL}}$ output (BSC) 101: Setting prohibited 010: Setting prohibited 110: Setting prohibited 011: Setting prohibited 111: Setting prohibited
PACRL3	11	PA11MD2	0	R/W	PA11 Mode
PACRL1	7	PA11MD1	0	R/W	Select the function of the PA11/$\overline{\text{ADTRG}}$/SCK3 pin.
PACRL1	6	PA11MD0	0	R/W	000: PA11 I/O (port) 100: Setting prohibited 001: Setting prohibited 101: SCK3 I/O (SCI) 010: $\overline{\text{ADTRG}}$ input (A/D) 110: Setting prohibited 011: Setting prohibited 111: Setting prohibited

Register	Bit	Bit Name	Initial Value	R/W	Description	
PACRL3	10	PA10MD2	0	R/W	PA10 Mode	
PACRL1	5	PA10MD1	0	R/W	Select the function of the PA10/$\overline{CS0}$/SCK2 pin.	
PACRL1	4	PA10MD0	0	R/W	000: PA10 I/O (port)	100: Setting prohibited
					001: $\overline{CS0}$ output (BSC)	101: SCK2 I/O (SCI)
					010: Setting prohibited	110: Setting prohibited
					011: Setting prohibited	111: Setting prohibited
PACRL3	9	PA9MD2	0	R/W	PA9 Mode	
PACRL1	3	PA9MD1	0	R/W	Select the function of the PA9/TCLKD/TxD3 pin.	
PACRL1	2	PA9MD0	0	R/W	000: PA9 I/O (port)	100: Setting prohibited
					001: TCLKD input (MTU)	101: TxD3 output (SCI)
					010: Setting prohibited	110: Setting prohibited
					011: Setting prohibited	111: Setting prohibited
PACRL3	8	PA8MD2	0	R/W	PA8 Mode	
PACRL1	1	PA8MD1	0	R/W	Select the function of the PA8/TCLKC/RxD3 pin.	
PACRL1	0	PA8MD0	0	R/W	000: PA8 I/O (port)	100: Setting prohibited
					001: TCLKC input (MTU)	101: RxD3 input (SCI)
					010: Setting prohibited	110: Setting prohibited
					011: Setting prohibited	111: Setting prohibited
PACRL3	7	PA7MD2	0	R/W	PA7 Mode	
PACRL2	15	PA7MD1	0	R/W	Select the function of the PA7/TCLKB/$\overline{WAIT}$/TxD2 pin.	
PACRL2	14	PA7MD0	0	R/W	000: PA7 I/O (port)	100: Setting prohibited
					001: TCLKB input (MTU)	101: TxD2 output (SCI)
					010: Setting prohibited	110: Setting prohibited
					011: $\overline{WAIT}$ input (BSC)	111: Setting prohibited
PACRL3	6	PA6MD2	0	R/W	PA6 Mode	
PACRL2	13	PA6MD1	0*	R/W	Select the function of the PA6/TCLKA/$\overline{RD}$/RxD2 pin.	
PACRL2	12	PA6MD0	0*	R/W	000: PA6 I/O (port)	100: Setting prohibited
					001: TCLKA input (MTU)	101: RxD2 input (SCI)
					010: Setting prohibited	110: Setting prohibited
					011: $\overline{RD}$ output (BSC)	111: Setting prohibited
PACRL3	5	PA5MD2	0*	R/W	PA5 Mode	
PACRL2	11	PA5MD1	0	R/W	Select the function of the PA5/$\overline{IRQ1}$/A5/SCK3 pin.	
PACRL2	10	PA5MD0	0	R/W	000: PA5 I/O (port)	100: A5 output (BSC)
					001: Setting prohibited	101: Setting prohibited
					010: Setting prohibited	110: SCK3 I/O (SCI)
					011: $\overline{IRQ1}$ input (INTC)	111: Setting prohibited

Register	Bit	Bit Name	Initial Value	R/W	Description	
PACRL3	4	PA4MD2	0*	R/W	PA4 Mode	
PACRL2	9	PA4MD1	0	R/W	Select the function of the PA4/A4/TxD3 pin.	
PACRL2	8	PA4MD0	0	R/W	000: PA4 I/O (port)	100: A4 output (BSC)
					001: Setting prohibited	101: Setting prohibited
					010: Setting prohibited	110: TxD3 output (SCI)
					011: Setting prohibited	111: Setting prohibited
PACRL3	3	PA3MD2	0*	R/W	PA3 Mode	
PACRL2	7	PA3MD1	0	R/W	Select the function of the PA3/A3/RxD3 pin.	
PACRL2	6	PA3MD0	0	R/W	000: PA3 I/O (port)	100: A3 output (BSC)
					001: Setting prohibited	101: Setting prohibited
					010: Setting prohibited	110: RxD3 input (SCI)
					011: Setting prohibited	111: Setting prohibited
PACRL3	2	PA2MD2	0*	R/W	PA2 Mode	
PACRL2	5	PA2MD1	0	R/W	Select the function of the PA2/$\overline{\text{IRQ0}}$/A2/PCIO/SCK2 pin.	
PACRL2	4	PA2MD0	0	R/W	000: PA2 I/O (port)	100: A2 output (BSC)
					001: Setting prohibited	101: PCIO I/O (MMT)
					010: Setting prohibited	110: SCK2 I/O (SCI)
					011: $\overline{\text{IRQ0}}$ input (INTC)	111: Setting prohibited
PACRL3	1	PA1MD2	0*	R/W	PA1 Mode	
PACRL2	3	PA1MD1	0	R/W	Select the function of the PA1/A1/$\overline{\text{POE1}}$/TxD2 pin.	
PACRL2	2	PA1MD0	0	R/W	000: PA1 I/O (port)	100: A1 output (BSC)
					001: Setting prohibited	101: $\overline{\text{POE1}}$ input (port)
					010: Setting prohibited	110: TxD2 output (SCI)
					011: Setting prohibited	111: Setting prohibited
PACRL3	0	PA0MD2	0*	R/W	PA0 Mode	
PACRL2	1	PA0MD1	0	R/W	Select the function of the PA0/A0/$\overline{\text{POE0}}$/RxD2 pin.	
PACRL2	0	PA0MD0	0	R/W	000: PA0 I/O (port)	100: A0 output (BSC)
					001: Setting prohibited	101: $\overline{\text{POE0}}$ input (port)
					010: Setting prohibited	110: RxD2 input (SCI)
					011: Setting prohibited	111: Setting prohibited

Note: * The initial value is 1 in 8-bit external extended mode with the on-chip ROM disabled.

14.1.3 Port B I/O Register (PBIOR)

PBIOR is a 16-bit readable/writable register that sets the pins on port B as inputs or outputs. Bits PB5IOR to PB0IOR correspond to pins PB5 to PB0 (names of multiplexed pins are here given as port names and pin numbers alone). PBIOR is enabled when port B pins are functioning as general-purpose inputs/outputs (PB5 to PB0). In other states, PBIOR is disabled.

A given pin on port B will be an output pin if the corresponding bit in PBIOR is set to 1, and an input pin if the bit is cleared to 0.

Note that bits 1 and 0 are disabled in the SH7108.

Bits 15 to 6 are reserved. These bits are always read as 0. The write value should always be 0.

The initial vale of PBIOR is H'0000.

14.1.4 Port B Control Registers 1 and 2 (PBCR1 and PBCR2)

PBCR1 and PBCR2 are 16-bit readable/writable registers that select the multiplexed pin function of the pins on port B.

Note that bit 9 in PBCR1 and bits 3 to 0 in PBCR2 are disabled in the SH7108.

(1) Port B Control Registers 1 and 2 (PBCR1 and PBCR2) in SH7108

Register	Bit	Bit Name	Initial Value	R/W	Description
PBCR1	15, 14	—	All 0	R	Reserved
PBCR1	8 to 0	—	All 0	R	These bits are always read as 0. The write value should always be 0.
PBCR1	9	—	0	R	
PBCR2	15 to 12	—	All 0	R	
PBCR2	3 to 0	—	All 0	R	
PBCR1	13	PB5MD2	0	R/W	PB5 Mode
PBCR2	11	PB5MD1	0	R/W	Select the function of the PB5/$\overline{\text{IRQ3}}$/$\overline{\text{POE3}}$ pin.
PBCR2	10	PB5MD0	0	R/W	000: PB5 I/O (port) 011: Setting prohibited 001: $\overline{\text{IRQ3}}$ input (INTC) 1xx: Setting prohibited 010: $\overline{\text{POE3}}$ input (port)
PBCR1	12	PB4MD2	0	R/W	PB4 Mode
PBCR2	9	PB4MD1	0	R/W	Select the function of the PB4/$\overline{\text{IRQ2}}$/$\overline{\text{POE2}}$ pin.
PBCR2	8	PB4MD0	0	R/W	000: PB4 I/O (port) 011: Setting prohibited 001: $\overline{\text{IRQ2}}$ input (INTC) 1xx: Setting prohibited 010: $\overline{\text{POE2}}$ input (port)
PBCR1	11	PB3MD2	0	R/W	PB3 Mode
PBCR2	7	PB3MD1	0	R/W	Select the function of the PB3/$\overline{\text{IRQ1}}$/$\overline{\text{POE1}}$ pin.
PBCR2	6	PB3MD0	0	R/W	000: PB3 I/O (port) 011: Setting prohibited 001: $\overline{\text{IRQ1}}$ input (INTC) 1xx: Setting prohibited 010: $\overline{\text{POE1}}$ input (port)
PBCR1	10	PB2MD2	0	R/W	PB2 Mode
PBCR2	5	PB2MD1	0	R/W	Select the function of the PB2/$\overline{\text{IRQ0}}$/$\overline{\text{POE0}}$ pin.
PBCR2	4	PB2MD0	0	R/W	000: PB2 I/O (port) 011: Setting prohibited 001: $\overline{\text{IRQ0}}$ input (INTC) 1xx: Setting prohibited 010: $\overline{\text{POE0}}$ input (port)

Legend: x: Don't care.

(2) Port B Control Registers 1 and 2 (PBCR1 and PBCR2) in SH7109

Register	Bit	Bit Name	Initial Value	R/W	Description
PBCR1	15 to 14	—	All 0	R	Reserved
PBCR1	8 to 0	—	All 0	R	These bits are always read as 0. The write value should always be 0.
PBCR2	15 to 12	—	All 0	R	
PBCR1	13	PB5MD2	0*1	R/W	PB5 Mode
PBCR2	11	PB5MD1	0	R/W	Select the function of the PB5/$\overline{\text{IRQ3}}$/$\overline{\text{POE3}}$/CK pin.
PBCR2	10	PB5MD0	0*1	R/W	000: PB5 I/O (port) 100: Setting prohibited 001: $\overline{\text{IRQ3}}$ input (INTC) 101: CK output (CPG) 010: $\overline{\text{POE3}}$ input (port) 110: Setting prohibited 011: Setting prohibited 111: Setting prohibited
PBCR1	12	PB4MD2	0	R/W	PB4 Mode
PBCR2	9	PB4MD1	0	R/W	Select the function of the PB4/$\overline{\text{IRQ2}}$/$\overline{\text{POE2}}$ pin.
PBCR2	8	PB4MD0	0	R/W	000: PB4 I/O (port) 100: Setting prohibited 001: $\overline{\text{IRQ2}}$ input (INTC) 101: Setting prohibited 010: $\overline{\text{POE2}}$ input (port) 110: Setting prohibited 011: Setting prohibited 111: Setting prohibited
PBCR1	11	PB3MD2	0	R/W	PB3 Mode
PBCR2	7	PB3MD1	0	R/W	Select the function of the PB3/$\overline{\text{IRQ1}}$/$\overline{\text{POE1}}$ pin.
PBCR2	6	PB3MD0	0	R/W	000: PB3 I/O (port) 100: Setting prohibited 001: $\overline{\text{IRQ1}}$ input (INTC) 101: Setting prohibited 010: $\overline{\text{POE1}}$ input (port) 110: Setting prohibited 011: Setting prohibited 111: Setting prohibited
PBCR1	10	PB2MD2	0	R/W	PB2 Mode
PBCR2	5	PB2MD1	0	R/W	Select the function of the PB2/$\overline{\text{IRQ0}}$/$\overline{\text{POE0}}$ pin.
PBCR2	4	PB2MD0	0	R/W	000: PB2 I/O (port) 100: Setting prohibited 001: $\overline{\text{IRQ0}}$ input (INTC) 101: Setting prohibited 010: $\overline{\text{POE0}}$ input (port) 110: Setting prohibited 011: Setting prohibited 111: Setting prohibited
PBCR1	9	PB1MD2	0	R/W	PB1 Mode
PBCR2	3	PB1MD1	0	R/W	Select the function of the PB1/A17 pin.
PBCR2	2	PB1MD0	0*2	R/W	000: PB1 I/O (port) 100: Setting prohibited 001: A17 output (BSC) 101: Setting prohibited 010: Setting prohibited 110: Setting prohibited 011: Setting prohibited 111: Setting prohibited

Register	Bit	Bit Name	Initial Value	R/W	Description
PBCR2	1	PB0MD1	0	R/W	PB0 Mode
PBCR2	0	PB0MD0	0*2	R/W	Select the function of the PB0/A16 pin. 00: PB0 I/O (port) 10: Setting prohibited 01: A16 output (BSC) 11: Setting prohibited

Notes: 1. The initial value is 1 in 8-bit external extended mode with on-chip ROM enabled/disabled.
2. The initial value is 1 in 8-bit external extended mode with the on-chip ROM disabled.

14.1.5 Port D I/O Register L (PDIORL)

PDIORL is a 16-bit readable/writable register that sets the pins on port D as inputs or outputs. Bits PD8IOR to PD0IOR correspond to pins PD8 to PD0 (names of multiplexed pins are here given as port names and pin numbers alone). PDIORL is enabled when the port D pins are functioning as general-purpose inputs/outputs (PD8 to PD0) and SCK2 pins are functioning as inputs/outputs of the SCI. In other states, PDIORL is disabled.

A given pin on port D will be an output pin if the corresponding bit in PDIORL is set to 1, and an input pin if the bit is cleared to 0.

Note that PDIORL is disabled in the SH7108.

Bits 15 to 9 in PDIORL are reserved. These bits are always read as 0. The write value should always be 0.

The initial value of PDIORL is H'0000.

14.1.6 Port D Control Registers L1 and L2 (PDCRL1 and PDCRL2)

PDCRL1 and PDCRL2 are 16-bit readable/writable registers that select the multiplexed pin function of the pins on port D.

Note that PDCRL1 and PDCRL2 are disabled in the SH7108.

(1) Port D Control Registers L1 and L2 (PDCRL1 and PDCRL2) in SH7109

Register	Bit	Bit Name	Initial Value	R/W	Description
PDCRL2	15 to 9	—	All 0	R	Reserved
PDCRL1	15 to 9	—	All 0	R	These bits are always read as 0. The write value should always be 0.
PDCRL2	8	PD8MD1	0	R/W	PD8 Mode
PDCRL1	8	PD8MD0	0	R/W	Select the function of the PD8 pin. 00: PD8 I/O (port) 10: Setting prohibited 01: Setting prohibited 11: Setting prohibited
PDCRL2	7	PD7MD1	0	R/W	PD7 Mode
PDCRL1	7	PD7MD0	0*[1]	R/W	Select the function of the PD7/D7 pin. 00: PD7 I/O (port) 10: Setting prohibited 01: D7 I/O (BSC)*[2] 11: Setting prohibited
PDCRL2	6	PD6MD1	0	R/W	PD6 Mode
PDCRL1	6	PD6MD0	0*[1]	R/W	Select the function of the PD6/D6 pin. 00: PD6 I/O (port) 10: Setting prohibited 01: D6 I/O (BSC)*[2] 11: Setting prohibited
PDCRL2	5	PD5MD1	0	R/W	PD5 Mode
PDCRL1	5	PD5MD0	0*[1]	R/W	Select the function of the PD5/D5 pin. 00: PD5 I/O (port) 10: Setting prohibited 01: D5 I/O (BSC)*[2] 11: Setting prohibited
PDCRL2	4	PD4MD1	0	R/W	PD4 Mode
PDCRL1	4	PD4MD0	0*[1]	R/W	Select the function of the PD4/D4 pin. 00: PD4 I/O (port) 10: Setting prohibited 01: D4 I/O (BSC)*[2] 11: Setting prohibited
PDCRL2	3	PD3MD1	0	R/W	PD3 Mode
PDCRL1	3	PD3MD0	0*[1]	R/W	Select the function of the PD3/D3 pin. 00: PD3 I/O (port) 10: Setting prohibited 01: D3 I/O (BSC)*[2] 11: Setting prohibited
PDCRL2	2	PD2MD1	0	R/W	PD2 Mode
PDCRL1	2	PD2MD0	0*[1]	R/W	Select the function of the PD2/D2/SCK2 pin. 00: PD2 I/O (port) 10: SCK2 I/O (SCI) 01: D2 I/O (BSC)*[2] 11: Setting prohibited

Register	Bit	Bit Name	Initial Value	R/W	Description
PDCRL2	1	PD1MD1	0	R/W	PD1 Mode
PDCRL1	1	PD1MD0	0*1	R/W	Select the function of the PD1/D1/TxD2 pin.
					00: PD1 I/O (port) 10: TxD2 output (SCI)
					01: D1 I/O (BSC)*2 11: Setting prohibited
PDCRL2	0	PD0MD1	0	R/W	PD0 Mode
PDCRL1	0	PD0MD0	0*1	R/W	Select the function of the PD0/D0/RxD2 pin.
					00: PD0 I/O (port) 10: RxD2 input (SCI)
					01: D0 I/O (BSC)*2 11: Setting prohibited

Notes: 1. The initial value is 1 in 8-bit external extended mode with the on-chip ROM disabled.
2. When using the external buses, set D7 to D0 at input/output pins.

14.1.7 Port E I/O Registers L and H (PEIORL and PEIORH)

PEIORL and PEIORH are 16-bit readable/writable registers that set the pins on port E as inputs or outputs. Bits PE21IOR to PE0IOR correspond to pins PE21 to PE0 (names of multiplexed pins are here given as port names and pin numbers alone). PEIORL is enabled when the port E pins are functioning as general-purpose inputs/outputs (PE15 to PE0), TIOC pins are functioning as inputs/outputs of the MTU, and SCK2 and SCK3 pins are functioning as inputs/outputs of the SCI. In other states, PEIORL is disabled. PEIORH is enabled when the port E pins are functioning as general-purpose inputs/outputs (PE21 to PE16). In other states, PEIORH is disabled.

A given pin on port E will be an output pin if the corresponding PEIORL or PEIORH bit is set to 1, and an input pin if the bit is cleared to 0.

Bits 15 to 6 in PEIORH are reserved. These bits are always read as 0. The write value should always be 0.

The initial values of PEIORL and PEIORH are H'0000.

14.1.8 Port E Control Registers L1, L2, and H (PECRL1, PECRL2, and PECRH)

PECRL1, PECRL2, and PECRH are 16-bit readable/writable registers that select the multiplexed pin function of the pins on port E.

(1) Port E Control Registers L1, L2, and H (PECRL1, PECRL2, and PECRH) in SH7108

Register	Bit	Bit Name	Initial Value	R/W	Description
PECRH	15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
PECRH	11	PE21MD1	0	R/W	PE21 Mode
PECRH	10	PE21MD0	0	R/W	Select the function of the PE21/PWOB pin. 00: PE21 I/O (port) 10: Setting prohibited 01: PWOB output (MMT) 11: Setting prohibited
PECRH	9	PE20MD1	0	R/W	PE20 Mode
PECRH	8	PE20MD0	0	R/W	Select the function of the PE20/PVOB pin. 00: PE20 I/O (port) 10: Setting prohibited 01: PVOB output (MMT) 11: Setting prohibited
PECRH	7	PE19MD1	0	R/W	PE19 Mode
PECRH	6	PE19MD0	0	R/W	Select the function of the PE19/PUOB pin. 00: PE19 I/O (port) 10: Setting prohibited 01: PUOB output (MMT) 11: Setting prohibited
PECRH	5	PE18MD1	0	R/W	PE18 Mode
PECRH	4	PE18MD0	0	R/W	Select the function of the PE18/PWOA pin. 00: PE18 I/O (port) 10: Setting prohibited 01: PWOA output (MMT) 11: Setting prohibited
PECRH	3	PE17MD1	0	R/W	PE17 Mode
PECRH	2	PE17MD0	0	R/W	Select the function of the PE17/PVOA pin. 00: PE17 I/O (port) 10: Setting prohibited 01: PVOA output (MMT) 11: Setting prohibited
PECRH	1	PE16MD1	0	R/W	PE16 Mode
PECRH	0	PE16MD0	0	R/W	Select the function of the PE16/PUOA pin. 00: PE16 I/O (port) 10: Setting prohibited 01: PUOA output (MMT) 11: Setting prohibited
PECRL1	15	PE15MD1	0	R/W	PE15 Mode
PECRL1	14	PE15MD0	0	R/W	Select the function of the PE15/TIOC4D/$\overline{\text{IRQOUT}}$ pin. 00: PE15 I/O (port) 10: Setting prohibited 01: TIOC4D I/O (MTU) 11: $\overline{\text{IRQOUT}}$ output (INTC)
PECRL1	13	PE14MD1	0	R/W	PE14 Mode
PECRL1	12	PE14MD0	0	R/W	Select the function of the PE14/TIOC4C pin. 00: PE14 I/O (port) 10: Setting prohibited 01: TIOC4C I/O (MTU) 11: Setting prohibited

Register	Bit	Bit Name	Initial Value	R/W	Description
PECRL1	11	PE13MD1	0	R/W	PE13 Mode
PECRL1	10	PE13MD0	0	R/W	Select the function of the PE13/TIOC4B/$\overline{\text{MRES}}$ pin. 00: PE13 I/O (port) 10: $\overline{\text{MRES}}$ input (INTC) 01: TIOC4B I/O (MTU) 11: Setting prohibited
PECRL1	9	PE12MD1	0	R/W	PE12 Mode
PECRL1	8	PE12MD0	0	R/W	Select the function of the PE12/TIOC4A pin. 00: PE12 I/O (port) 10: Setting prohibited 01: TIOC4A I/O (MTU) 11: Setting prohibited
PECRL1	7	PE11MD1	0	R/W	PE11 Mode
PECRL1	6	PE11MD0	0	R/W	Select the function of the PE11/TIOC3D pin. 00: PE11 I/O (port) 10: Setting prohibited 01: TIOC3D I/O (MTU) 11: Setting prohibited
PECRL1	5	PE10MD1	0	R/W	PE10 Mode
PECRL1	4	PE10MD0	0	R/W	Select the function of the PE10/TIOC3C/TxD2 pin. 00: PE10 I/O (port) 10: TxD2 output (SCI) 01: TIOC3C I/O (MTU) 11: Setting prohibited
PECRL1	3	PE9MD1	0	R/W	PE9 Mode
PECRL1	2	PE9MD0	0	R/W	Select the function of the PE9/TIOC3B pin. 00: PE9 I/O (port) 10: Setting prohibited 01: TIOC3B I/O (MTU) 11: Setting prohibited
PECRL1	1	PE8MD1	0	R/W	PE8 Mode
PECRL1	0	PE8MD0	0	R/W	Select the function of the PE8/TIOC3A/SCK2 pin. 00: PE8 I/O (port) 10: SCK2 I/O (SCI) 01: TIOC3A I/O (MTU) 11: Setting prohibited
PECRL2	15	PE7MD1	0	R/W	PE7 Mode
PECRL2	14	PE7MD0	0	R/W	Select the function of the PE7/TIOC2B/RxD2 pin. 00: PE7 I/O (port) 10: RxD2 input (SCI) 01: TIOC2B I/O (MTU) 11: Setting prohibited
PECRL2	13	PE6MD1	0	R/W	PE6 Mode
PECRL2	12	PE6MD0	0	R/W	Select the function of the PE6/TIOC2A/SCK3 pin. 00: PE6 I/O (port) 10: SCK3 I/O (SCI) 01: TIOC2A I/O (MTU) 11: Setting prohibited
PECRL2	11	PE5MD1	0	R/W	PE5 Mode
PECRL2	10	PE5MD0	0	R/W	Select the function of the PE5/TIOC1B/TxD3 pin. 00: PE5 I/O (port) 10: TxD3 output (SCI) 01: TIOC1B I/O (MTU) 11: Setting prohibited

Register	Bit	Bit Name	Initial Value	R/W	Description
PECRL2	9	PE4MD1	0	R/W	PE4 Mode
PECRL2	8	PE4MD0	0	R/W	Select the function of the PE4/TIOC1A/RxD3 pin. 00: PE4 I/O (port) 10: RxD3 input (SCI) 01: TIOC1A I/O (MTU) 11: Setting prohibited
PECRL2	7	PE3MD1	0	R/W	PE3 Mode
PECRL2	6	PE3MD0	0	R/W	Select the function of the PE3/TIOC0D pin. 00: PE3 I/O (port) 10: Setting prohibited 01: TIOC0D I/O (MTU) 11: Setting prohibited
PECRL2	5	PE2MD1	0	R/W	PE2 Mode
PECRL2	4	PE2MD0	0	R/W	Select the function of the PE2/TIOC0C pin. 00: PE2 I/O (port) 10: Setting prohibited 01: TIOC0C I/O (MTU) 11: Setting prohibited
PECRL2	3	PE1MD1	0	R/W	PE1 Mode
PECRL2	2	PE1MD0	0	R/W	Select the function of the PE1/TIOC0B pin. 00: PE1 I/O (port) 10: Setting prohibited 01: TIOC0B I/O (MTU) 11: Setting prohibited
PECRL2	1	PE0MD1	0	R/W	PE0 Mode
PECRL2	0	PE0MD0	0	R/W	Select the function of the PE0/TIOC0A pin. 00: PE0 I/O (port) 10: Setting prohibited 01: TIOC0A I/O (MTU) 11: Setting prohibited

(2) Port E Control Registers L1, L2, and H (PECRL1, PECRL2, and PECRH) in SH7109

Register	Bit	Bit Name	Initial Value	R/W	Description
PECRH	15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
PECRH	11	PE21MD1	0*	R/W	PE21 Mode
PECRH	10	PE21MD0	0*	R/W	Select the function of the PE21/PWOB/A15 pin. 00: PE21 I/O (port) 10: Setting prohibited 01: PWOB output (MMT) 11: A15 output (BSC)
PECRH	9	PE20MD1	0*	R/W	PE20 Mode
PECRH	8	PE20MD0	0*	R/W	Select the function of the PE20/PVOB/A14 pin. 00: PE20 I/O (port) 10: Setting prohibited 01: PVOB output (MMT) 11: A14 output (BSC)
PECRH	7	PE19MD1	0*	R/W	PE19 Mode
PECRH	6	PE19MD0	0*	R/W	Select the function of the PE19/PUOB/A13 pin. 00: PE19 I/O (port) 10: Setting prohibited 01: PUOB output (MMT) 11: A13 output (BSC)
PECRH	5	PE18MD1	0*	R/W	PE18 Mode
PECRH	4	PE18MD0	0*	R/W	Select the function of the PE18/PWOA/A12 pin. 00: PE18 I/O (port) 10: Setting prohibited 01: PWOA output (MMT) 11: A12 output (BSC)
PECRH	3	PE17MD1	0*	R/W	PE17 Mode
PECRH	2	PE17MD0	0*	R/W	Select the function of the PE17/PVOA/$\overline{\text{WAIT}}$/A11 pin. 00: PE17 I/O (port) 10: $\overline{\text{WAIT}}$ input (BSC) 01: PVOA output (MMT) 11: A11 output (BSC)
PECRH	1	PE16MD1	0*	R/W	PE16 Mode
PECRH	0	PE16MD0	0*	R/W	Select the function of the PE16/PUOA/A10 pin. 00: PE16 I/O (port) 10: Setting prohibited 01: PUOA output (MMT) 11: A10 output (BSC)
PECRL1	15	PE15MD1	0	R/W	PE15 Mode
PECRL1	14	PE15MD0	0	R/W	Select the function of the PE15/TIOC4D/$\overline{\text{IRQOUT}}$ pin. 00: PE15 I/O (port) 10: Setting prohibited 01: TIOC4D I/O (MTU) 11: $\overline{\text{IRQOUT}}$ output (INTC)
PECRL1	13	PE14MD1	0	R/W	PE14 Mode
PECRL1	12	PE14MD0	0	R/W	Select the function of the PE14/TIOC4C pin. 00: PE14 I/O (port) 10: Setting prohibited 01: TIOC4C I/O (MTU) 11: Setting prohibited

Register	Bit	Bit Name	Initial Value	R/W	Description
PECRL1	11	PE13MD1	0	R/W	PE13 Mode
PECRL1	10	PE13MD0	0	R/W	Select the function of the PE13/TIOC4B/$\overline{\text{MRES}}$ pin. 00: PE13 I/O (port) 10: $\overline{\text{MRES}}$ input (INTC) 01: TIOC4B I/O (MTU) 11: Setting prohibited
PECRL1	9	PE12MD1	0	R/W	PE12 Mode
PECRL1	8	PE12MD0	0	R/W	Select the function of the PE12/TIOC4A pin. 00: PE12 I/O (port) 10: Setting prohibited 01: TIOC4A I/O (MTU) 11: Setting prohibited
PECRL1	7	PE11MD1	0	R/W	PE11 Mode
PECRL1	6	PE11MD0	0	R/W	Select the function of the PE11/TIOC3D pin. 00: PE11 I/O (port) 10: Setting prohibited 01: TIOC3D I/O (MTU) 11: Setting prohibited
PECRL1	5	PE10MD1	0*	R/W	PE10 Mode
PECRL1	4	PE10MD0	0*	R/W	Select the function of the PE10/TIOC3C/TxD2/$\overline{\text{WRL}}$ pin. 00: PE10 I/O (port) 10: TxD2 output (SCI) 01: TIOC3C I/O (MTU) 11: $\overline{\text{WRL}}$ output (BSC)
PECRL1	3	PE9MD1	0	R/W	PE9 Mode
PECRL1	2	PE9MD0	0	R/W	Select the function of the PE9/TIOC3B pin. 00: PE9 I/O (port) 10: Setting prohibited 01: TIOC3B I/O (MTU) 11: Setting prohibited
PECRL1	1	PE8MD1	0	R/W	PE8 Mode
PECRL1	0	PE8MD0	0	R/W	Select the function of the PE8/TIOC3A/SCK2 pin. 00: PE8 I/O (port) 10: SCK2 I/O (SCI) 01: TIOC3A I/O (MTU) 11: Setting prohibited
PECRL2	15	PE7MD1	0*	R/W	PE7 Mode
PECRL2	14	PE7MD0	0*	R/W	Select the function of the PE7/TIOC2B/RxD2/A9 pin. 00: PE7 I/O (port) 10: RxD2 input (SCI) 01: TIOC2B I/O (MTU) 11: A9 output (BSC)
PECRL2	13	PE6MD1	0*	R/W	PE6 Mode
PECRL2	12	PE6MD0	0*	R/W	Select the function of the PE6/TIOC2A/SCK3/A8 pin. 00: PE6 I/O (port) 10: SCK3 I/O (SCI) 01: TIOC2A I/O (MTU) 11: A8 output (BSC)
PECRL2	11	PE5MD1	0*	R/W	PE5 Mode
PECRL2	10	PE5MD0	0*	R/W	Select the function of the PE5/TIOC1B/TxD3/A7 pin. 00: PE5 I/O (port) 10: TxD3 output (SCI) 01: TIOC1B I/O (MTU) 11: A7 output (BSC)

Register	Bit	Bit Name	Initial Value	R/W	Description
PECRL2	9	PE4MD1	0*	R/W	PE4 Mode
PECRL2	8	PE4MD0	0*	R/W	Select the function of the PE4/TIOC1A/RxD3/A6 pin. 00: PE4 I/O (port) 10: RxD3 input (SCI) 01: TIOC1A I/O (MTU) 11: A6 output (BSC)
PECRL2	7	PE3MD1	0	R/W	PE3 Mode
PECRL2	6	PE3MD0	0	R/W	Select the function of the PE3/TIOC0D pin. 00: PE3 I/O (port) 10: Setting prohibited 01: TIOC0D I/O (MTU) 11: Setting prohibited
PECRL2	5	PE2MD1	0	R/W	PE2 Mode
PECRL2	4	PE2MD0	0	R/W	Select the function of the PE2/TIOC0C pin. 00: PE2 I/O (port) 10: Setting prohibited 01: TIOC0C I/O (MTU) 11: Setting prohibited
PECRL2	3	PE1MD1	0	R/W	PE1 Mode
PECRL2	2	PE1MD0	0	R/W	Select the function of the PE1/TIOC0B pin. 00: PE1 I/O (port) 10: Setting prohibited 01: TIOC0B I/O (MTU) 11: Setting prohibited
PECRL2	1	PE0MD1	0*	R/W	PE0 Mode
PECRL2	0	PE0MD0	0*	R/W	Select the function of the PE0/TIOC0A/$\overline{CS0}$ pin. 00: PE0 I/O (port) 10: Setting prohibited 01: TIOC0A I/O (MTU) 11: $\overline{CS0}$ output (BSC)

Note: * The initial value is 1 in 8-bit external extended mode with the on-chip ROM disabled.

14.2 Usage Note

In this LSI, individual functions are available as multiplexed functions on multiple pins. This approach is intended to increase the number of selectable pin functions and to allow the easier design of boards.

When the pin function controller (PFC) is used to select a function, only a single pin can be specified for each function. If one function is specified for two or more pins, the function will not work properly.

Section 15 I/O Ports

The SH7108 has five ports: A, B, E, F, and G. Port A is a 16-bit port, port B is a 4-bit port, and port E is a 22-bit port, all supporting both input and output. Port F is an 8-bit port and port G is a 4-bit port, both for input-only.

The SH7109 has five ports: A, B, D, E, and F. Port A is a 16-bit port, port B is a 6-bit port, port D is a 9-bit port, and port E is a 22-bit port, all supporting both input and output. Port F is a 16-bit input-only port.

All the port pins are multiplexed as general input/output pins and special function pins. The functions of the multiplex pins are selected by means of the pin function controller (PFC).

Each port is provided with a data register for storing the pin data.

15.1 Port A

Port A in the SH7108 is an input/output port with the 16 pins shown in figure 15.1.

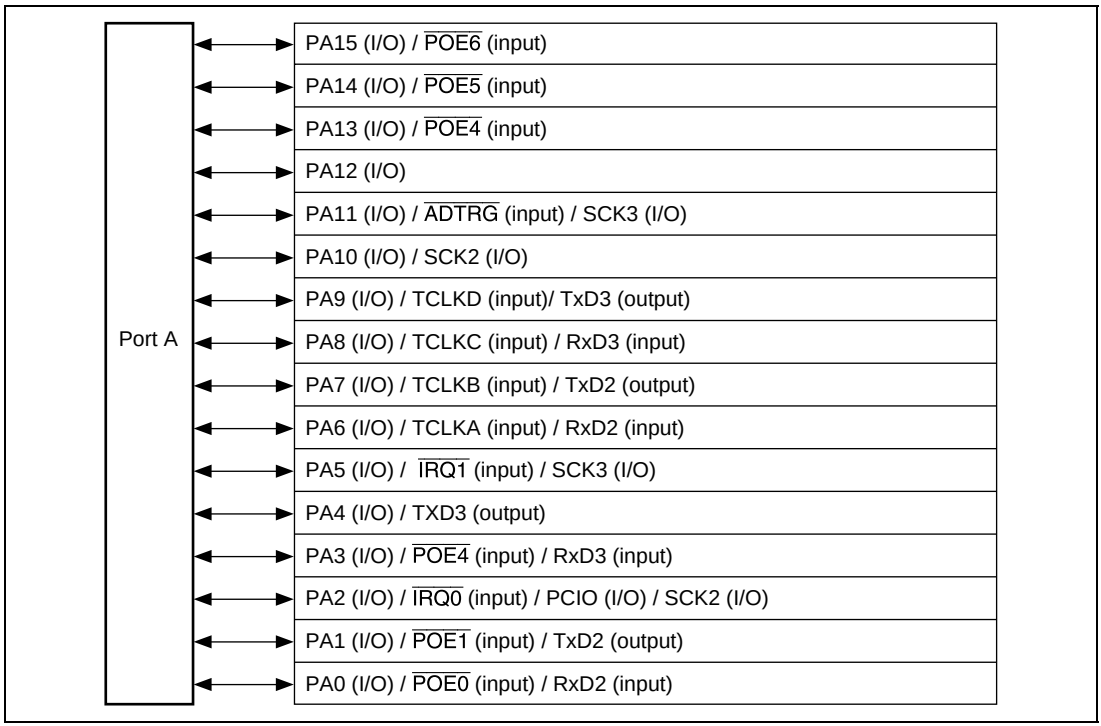


Figure 15.1 Port A (SH7108)

Port A in the SH7109 is an input/output port with the 16 pins shown in figure 15.2.

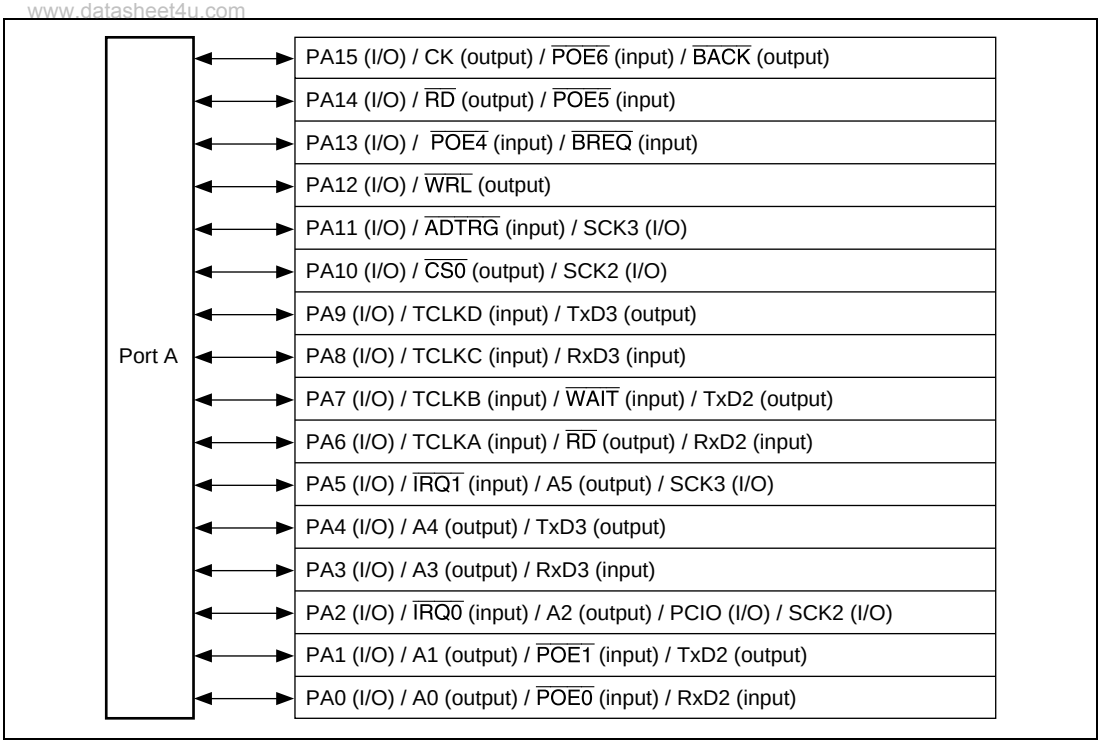


Figure 15.2 Port A (SH7109)

15.1.1 Register Description

Port A is a 16-bit input/output port. Port A has the following register. For details on register addresses and register states during each processing, refer to section 19, List of Registers.

- Port A data register L (PADRL)

15.1.2 Port A Data Register L (PADRL)

PADRL is a 16-bit readable/writable register that stores port A data. Bits PA15DR to PA0DR correspond to pins PA15 to PA0 (multiplexed functions omitted here).

When a pin functions is a general output, if a value is written to PADRL, that value is output directly from the pin, and if PADRL is read, the register value is returned directly regardless of the pin state.

When a pin functions is a general input, if PADRL is read, the pin state, not the register value, is returned directly. If a value is written to PADRL, although that value is written into PADRL, it does not affect the pin state. Table 15.1 summarizes port A data register L read/write operations.

Bit	Bit Name	Initial Value	R/W	Description
15	PA15DR	0	R/W	See table 15.1.
14	PA14DR	0	R/W	
13	PA13DR	0	R/W	
12	PA12DR	0	R/W	
11	PA11DR	0	R/W	
10	PA10DR	0	R/W	
9	PA9DR	0	R/W	
8	PA8DR	0	R/W	
7	PA7DR	0	R/W	
6	PA6DR	0	R/W	
5	PA5DR	0	R/W	
4	PA4DR	0	R/W	
3	PA3DR	0	R/W	
2	PA2DR	0	R/W	
1	PA1DR	0	R/W	
0	PA0DR	0	R/W	

Table 15.1 Port A Data Register L (PADRL) Read/Write Operations

- Bits 15 to 0

PAIORL	Pin Function	Read	Write
0	General input	Pin state	Can write to PADRL, but it has no effect on pin state
	Other than general input	Pin state	Can write to PADRL, but it has no effect on pin state
1	General output	PADRL value	Value written is output from pin
	Other than general output	PADRL value	Can write to PADRL, but it has no effect on pin state

15.2 Port B

Port B in the SH7108 is an input/output port with the four pins shown in figure 15.3.

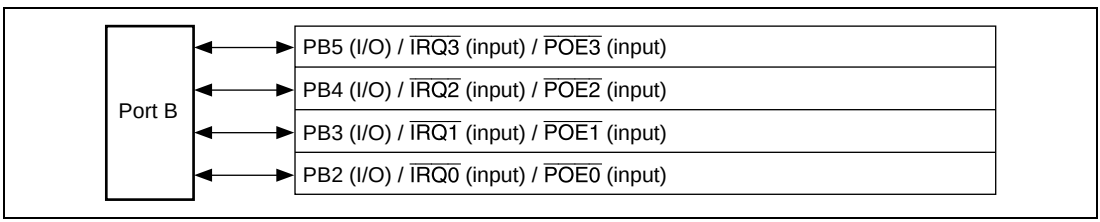


Figure 15.3 Port B (SH7108)

Port B in the SH7109 is an input/output port with the six pins shown in figure 15.4.

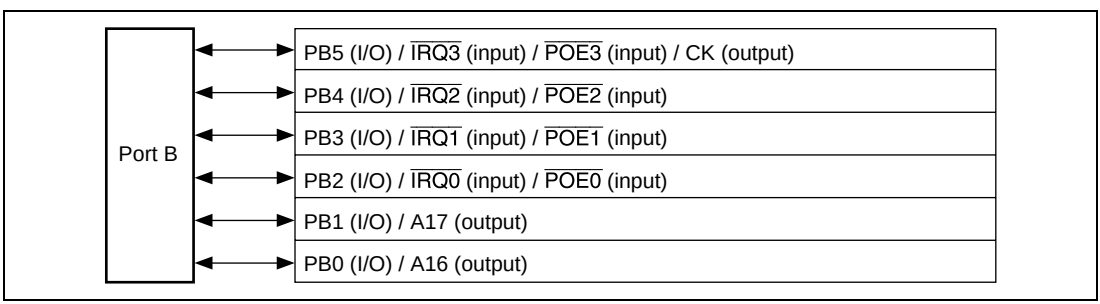


Figure 15.4 Port B (SH7109)

15.2.1 Register Description

Port B is a 4-bit input/output port in the SH7108 and a 6-bit input/output port in the SH7109. Port B has the following register. For details on register addresses and register states during each processing, refer to section 19, List of Registers.

- Port B data register (PBDR)

15.2.2 Port B Data Register (PBDR)

PBDR is a 16-bit readable/writable register that stores port B data. In the SH7108, bits PB5DR to PB2DR correspond to pins PB5 to PB2 (multiplexed functions omitted here). In the SH7109, bits PB5DR to PB0DR correspond to pins PB5 to PB0 (multiplexed functions omitted here).

When a pin functions is a general output, if a value is written to PBDR, that value is output directly from the pin, and if PBDR is read, the register value is returned directly regardless of the pin state.

When a pin functions is a general input, if PBDR is read, the pin state, not the register value, is returned directly. If a value is written to PBDR, although that value is written into PBDR, it does not affect the pin state. Table 15.2 summarizes port B data register read/write operations.

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	PB5DR	0	R/W	See table 15.2.
4	PB4DR	0	R/W	
3	PB3DR	0	R/W	
2	PB2DR	0	R/W	
1	PB1DR	0/1	R/W	See table 15.2.*
0	PB0DR	0/1	R/W	

Note: * These bits are reserved in the SH7108. They have no corresponding pins. The write value should always be 0.

Table 15.2 Port B Data Register (PBDR) Read/Write Operations

- Bits 5 to 0

PBIOR	Pin Function	Read	Write
0	General input	Pin state	Can write to PBDR, but it has no effect on pin state
	Other than general input	Pin state	Can write to PBDR, but it has no effect on pin state
1	General output	PBDR value	Value written is output from pin
	Other than general output	PBDR value	Can write to PBDR, but it has no effect on pin state

15.3 Port D

Port D that can only be used in the SH7109 is an input/output port with the nine pins shown in figure 15.5.

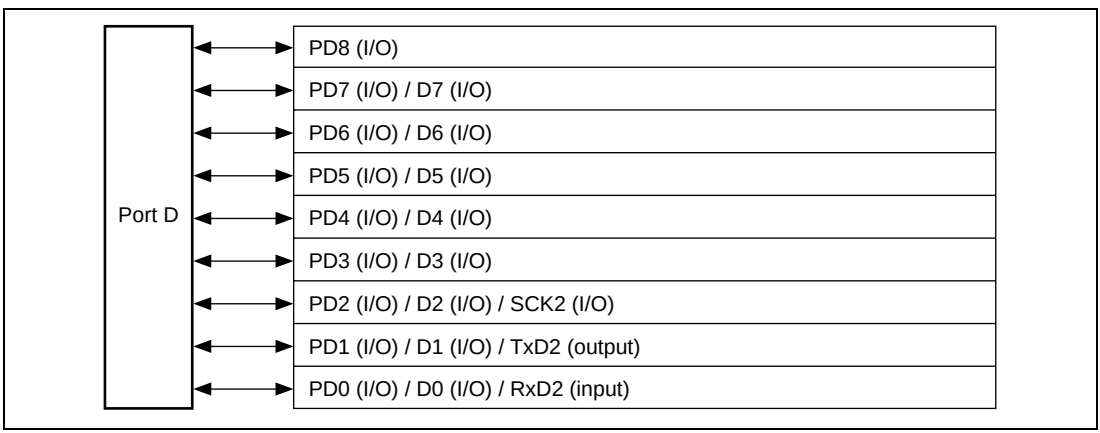


Figure 15.5 Port D (SH7109)

15.3.1 Register Description

Port D has the following register. For details on register addresses and register states during each processing, refer to section 19, List of Registers.

- Port D data register L (PDDRL)

15.3.2 Port D Data Register L (PDDRL)

PDDRL is a 16-bit readable/writable register that stores port D data. Bits PD8DR to PD0DR correspond to pins PD8 to PD0 (multiplexed functions omitted here).

When a pin functions is a general output, if a value is written to PDDRL, that value is output directly from the pin, and if PDDRL is read, the register value is returned directly regardless of the pin state.

When a pin functions is a general input, if PDDRL is read, the pin state, not the register value, is returned directly. If a value is written to PDDRL, although that value is written into PDDRL, it does not affect the pin state. Table 15.3 summarizes port D data register L read/write operations.

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	PD8DR	0	R/W	See table 15.3.
7	PD7DR	0	R/W	
6	PD6DR	0	R/W	
5	PD5DR	0	R/W	
4	PD4DR	0	R/W	
3	PD3DR	0	R/W	
2	PD2DR	0	R/W	
1	PD1DR	0	R/W	
0	PD0DR	0	R/W	

Table 15.3 Port D Data Register L (PDDRL) Read/Write Operations

- Bits 8 to 0

PDIORL	Pin Function	Read	Write
0	General input	Pin state	Can write to PDDRL, but it has no effect on pin state
	Other than general input	Pin state	Can write to PDDRL, but it has no effect on pin state
1	General output	PDDRL value	Value written is output from pin
	Other than general output	PDDRL value	Can write to PDDRL, but it has no effect on pin state

15.4 Port E

Port E in the SH7108 is an input/output port with the 22 pins shown in figure 15.6.

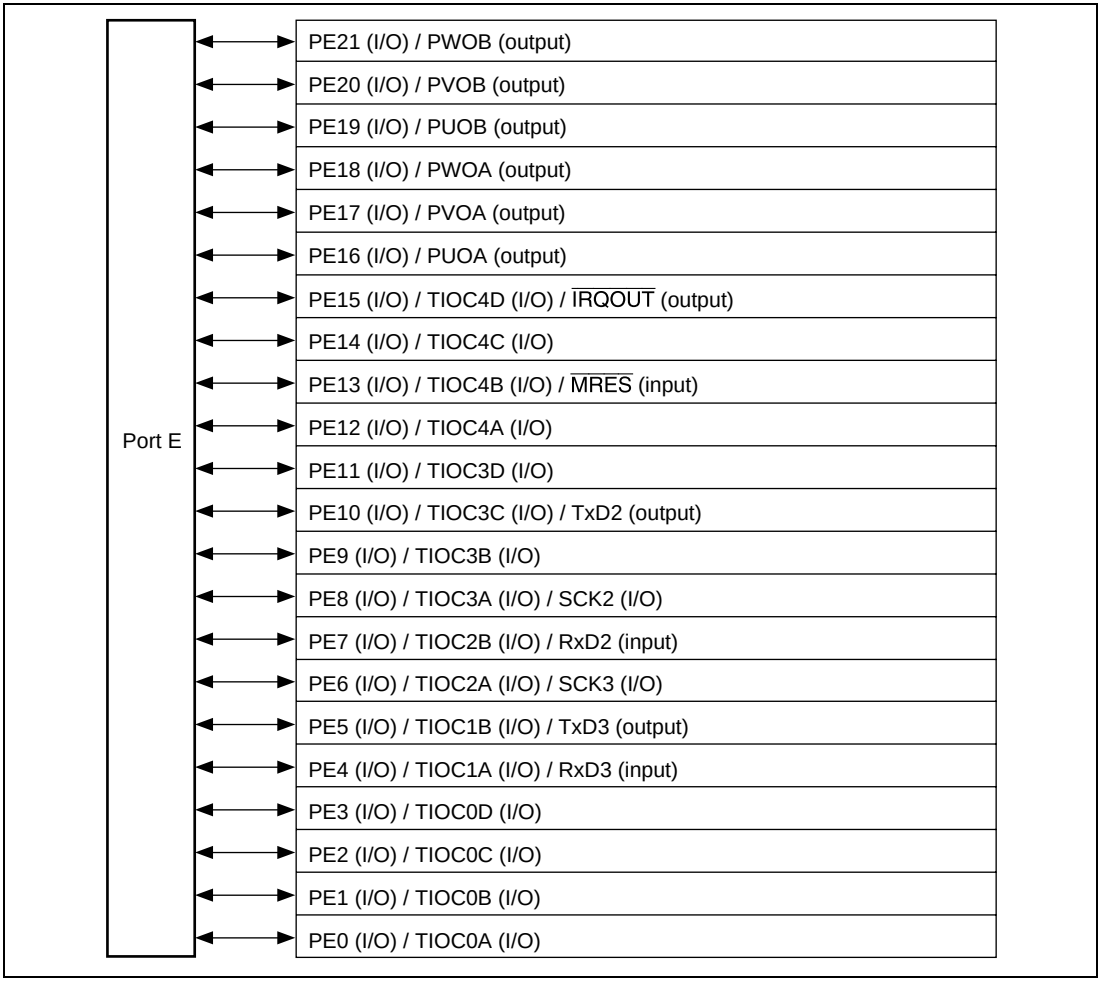


Figure 15.6 Port E (SH7108)

Port E in the SH7109 is an input/output port with the 22 pins shown in figure 15.7.

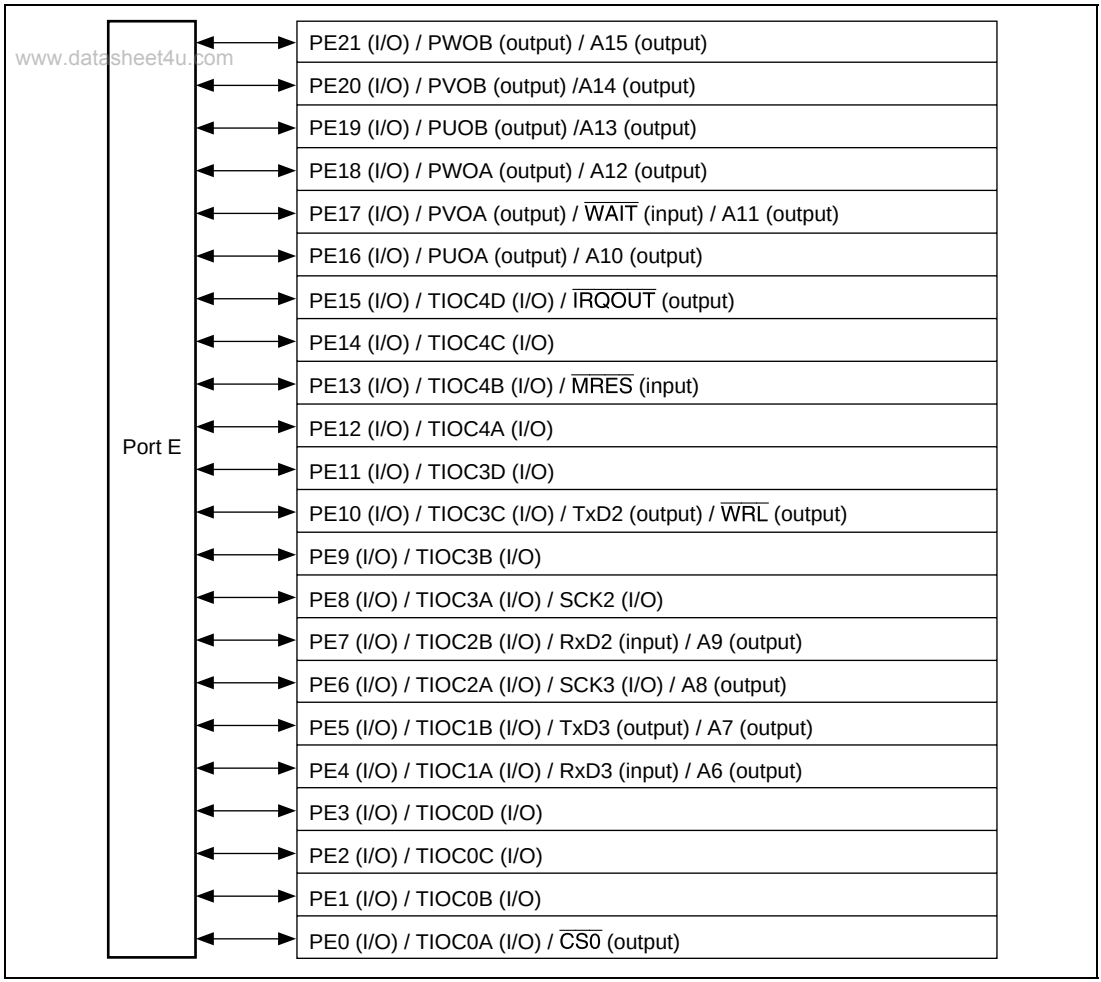


Figure 15.7 Port E (SH7109)

15.4.1 Register Descriptions

Port E has the following registers. For details on register addresses and register states during each processing, refer to section 19, List of Registers.

- Port E data register H (PEDRH)
- Port E data register L (PEDRL)

15.4.2 Port E Data Registers H and L (PEDRH and PEDRL)

PEDRH and PEDRL are 16-bit readable/writable registers that store port E data. Bits PE21DR to PE0DR correspond to pins PE21 to PE0 (multiplexed functions omitted here).

When a pin functions is a general output, if a value is written to PEDRH or PEDRL, that value is output directly from the pin, and if PEDRH or PEDRL is read, the register value is returned directly regardless of the pin state.

When a pin functions is a general input, if PEDRH or PEDRL is read, the pin state, not the register value, is returned directly. If a value is written to PEDRH or PEDRL, although that value is written into PEDRH or PEDRL it does not affect the pin state. Table 15.4 summarizes port E data register read/write operations.

- PEDRH

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	PE21DR	0	R/W	See table 15.4.
4	PE20DR	0	R/W	
3	PE19DR	0	R/W	
2	PE18DR	0	R/W	
1	PE17DR	0	R/W	
0	PE16DR	0	R/W	

- PEDRL

Bit	Bit Name	Initial Value	R/W	Description
15	PE15DR	0	R/W	See table 15.4.
14	PE14DR	0	R/W	
13	PE13DR	0	R/W	
12	PE12DR	0	R/W	
11	PE11DR	0	R/W	
10	PE10DR	0	R/W	
9	PE9DR	0	R/W	
8	PE8DR	0	R/W	
7	PE7DR	0	R/W	
6	PE6DR	0	R/W	
5	PE5DR	0	R/W	
4	PE4DR	0	R/W	
3	PE3DR	0	R/W	
2	PE2DR	0	R/W	
1	PE1DR	0	R/W	
0	PE0DR	0	R/W	

Table 15.4 Port E Data Registers H and L (PEDRH and PEDRL) Read/Write Operations

- Bits 5 to 0 in PEDRH and bits 15 to 0 in PEDRL

PEIOR	Pin Function	Read	Write
0	General input	Pin state	Can write to PEDRH or PEDRL, but it has no effect on pin state
	Other than general input	Pin state	Can write to PEDRH or PEDRL, but it has no effect on pin state
1	General output	PEDRH or PEDRL value	Value written is output from pin ($\overline{\text{POE}}$ pin = high)*
			High impedance regardless of PEDRH or PEDRL value ($\overline{\text{POE}}$ pin = low)*
	Other than general output	PEDRH or PEDRL value	Can write to PEDRH or PEDRL, but it has no effect on pin state

Note: * Control by the $\overline{\text{POE}}$ pin is only available for large current-output pins (PE9 and PE11 to PE21).

15.5 Port F

Port F in the SH7108 is an input-only port with the eight pins shown in figure 15.8.

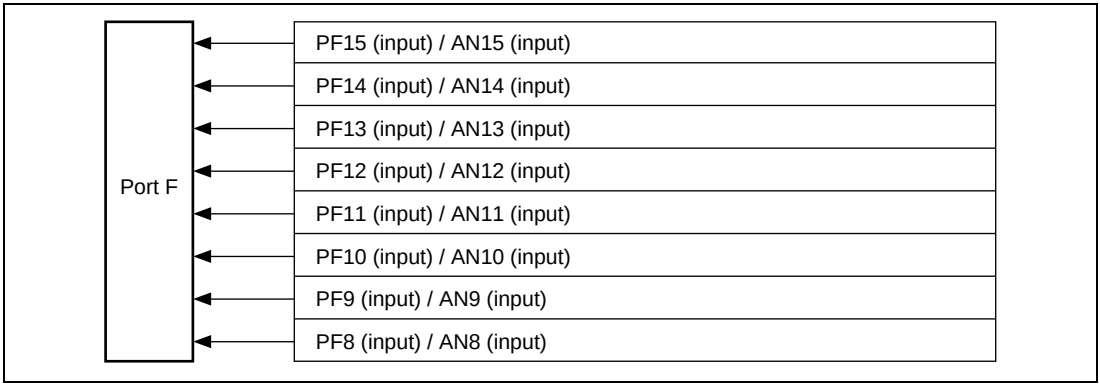


Figure 15.8 Port F (SH7108)

Port F in the SH7109 is an input-only port with the 16 pins shown in figure 15.9.

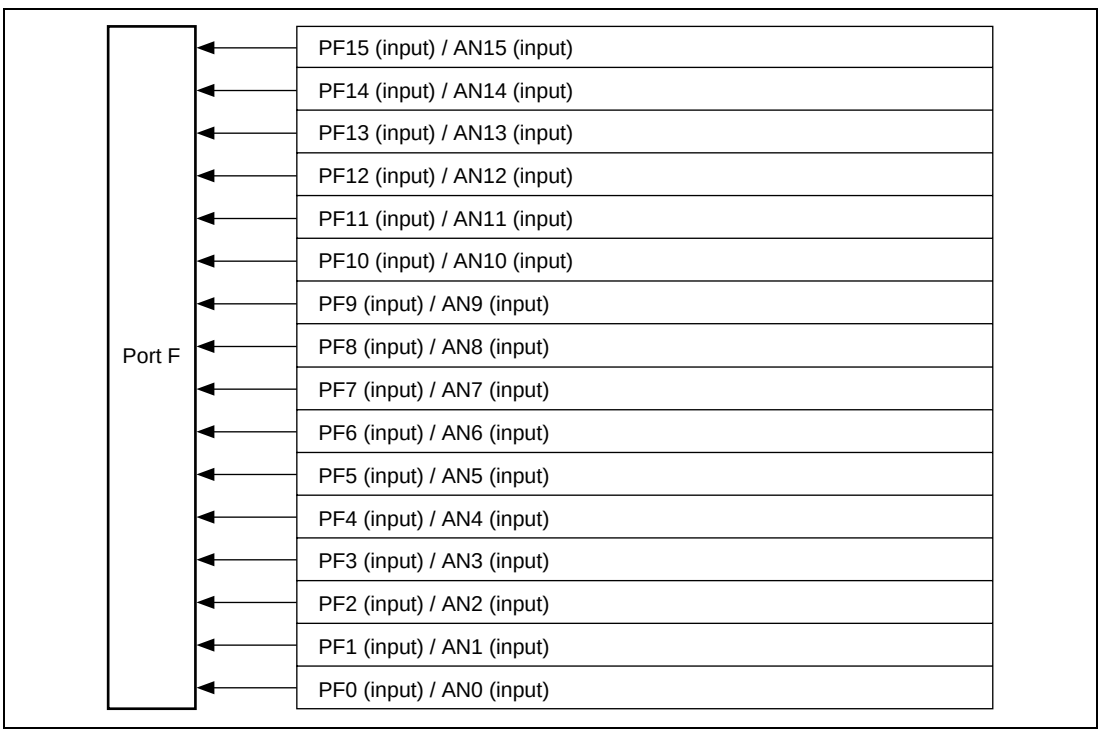


Figure 15.9 Port F (SH7109)

15.5.1 Register Description

Port F is an 8-bit input-only port in the SH7108 and a 16-bit input-only port in the SH7109. Port F has the following register. For details on register addresses and register states during each processing, refer to section 19, List of Registers.

- Port F data register (PFDR)

15.5.2 Port F Data Register (PFDR)

PFDR is a 16-bit read-only register that stores port F data.

In the SH7108, bits PF15DR to PF8DR correspond to pins PF15 to PF8 (multiplexed functions omitted here). In the SH7109, bits PF15DR to PF0DR correspond to pins PF15 to PF0 (multiplexed functions omitted here).

Any value written into these bits is ignored, and there is no effect on the state of the pins. When any of the bits are read, the pin state rather than the bit value is read directly. However, when an A/D converter analog input is being sampled, values of 1 are read. Table 15.5 summarizes port F data register read/write operations.

Bit	Bit Name	Initial Value	R/W	Description
15	PF15DR	0/1*[1]	R	See table 15.5.
14	PF14DR	0/1*[1]	R	
13	PF13DR	0/1*[1]	R	
12	PF12DR	0/1*[1]	R	
11	PF11DR	0/1*[1]	R	
10	PF10DR	0/1*[1]	R	
9	PF9DR	0/1*[1]	R	
8	PF8DR	0/1*[1]	R	
7	PF7DR	0/1*[1]	R	See table 15.5.*[2]
6	PF6DR	0/1*[1]	R	
5	PF5DR	0/1*[1]	R	
4	PF4DR	0/1*[1]	R	
3	PF3DR	0/1*[1]	R	
2	PF2DR	0/1*[1]	R	
1	PF1DR	0/1*[1]	R	
0	PF0DR	0/1*[1]	R	

Notes: 1. Initial values are dependent on the state of the external pins.
2. These bits are reserved in the SH7108. The write value should always be 0.

Table 15.5 Port F Data Register (PFDR) Read/Write Operations

- Bits 15 to 8 in SH7108 and bits 15 to 0 in SH7109

Pin Function	Read	Write
General input	Pin state	Ignored (no effect on pin state)
ANn input	1	Ignored (no effect on pin state)

15.6 Port G

Port G that can only be used in the SH7108 is an input-only port with the four pins shown in figure 15.10.

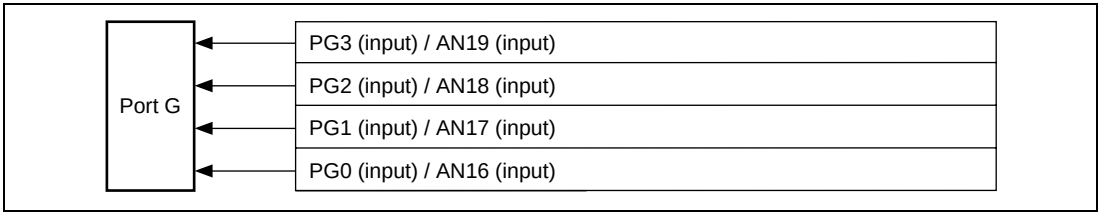


Figure 15.10 Port G (SH7108)

15.6.1 Register Description

Port G is a 4-bit input-only port. Port G has the following register. For details on register addresses and register states during each processing, refer to section 19, List of Registers.

- Port G data register (PGDR)

15.6.2 Port G Data Register (PGDR)

PGDR is an 8-bit read-only register that stores port G data. Bits PG3DR to PG0DR correspond to pins PG3 to PG0 (multiplexed functions omitted here).

Any value written into these bits is ignored, and there is no effect on the state of the pins. When any of the bits are read, the pin state rather than the bit value is read directly. However, when an A/D converter analog input is being sampled, values of 1 are read. Table 15.6 summarizes port G data register read/write operations.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	R	Reserved These bits are always read as 0.
3	PG3DR	0/1*	R	See table 15.6.
2	PG2DR	0/1*	R	
1	PG1DR	0/1*	R	
0	PG0DR	0/1*	R	

Note: * Initial values are dependent on the state of the external pins.

Table 15.6 Port G Data Register (PGDR) Read/Write Operations

- Bits 3 to 0

Pin Function	Read	Write
General input	Pin state	Ignored (no effect on pin state)
ANn input	1	Ignored (no effect on pin state)

Section 16 Masked ROM

This LSI is available with 64 kbytes or 128 kbytes of on-chip masked ROM. The on-chip ROM is connected to the CPU through a 32-bit data bus (figures 16.1 and 16.2). The CPU can access the on-chip ROM in 8, 16, or 32-bit width. Data in the on-chip ROM can always be accessed in one cycle.

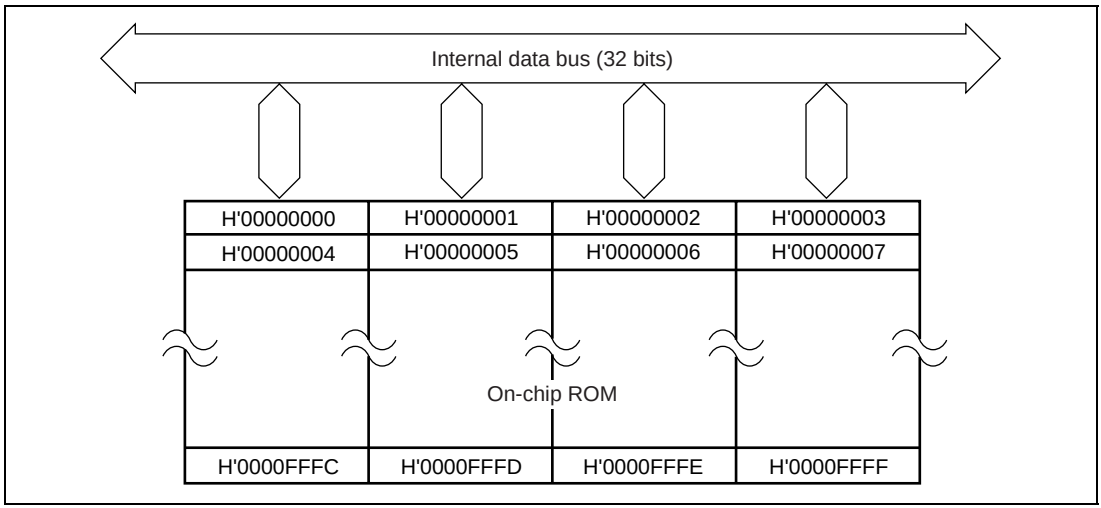


Figure 16.1 Masked ROM Block Diagram (SH7106/SH7107)

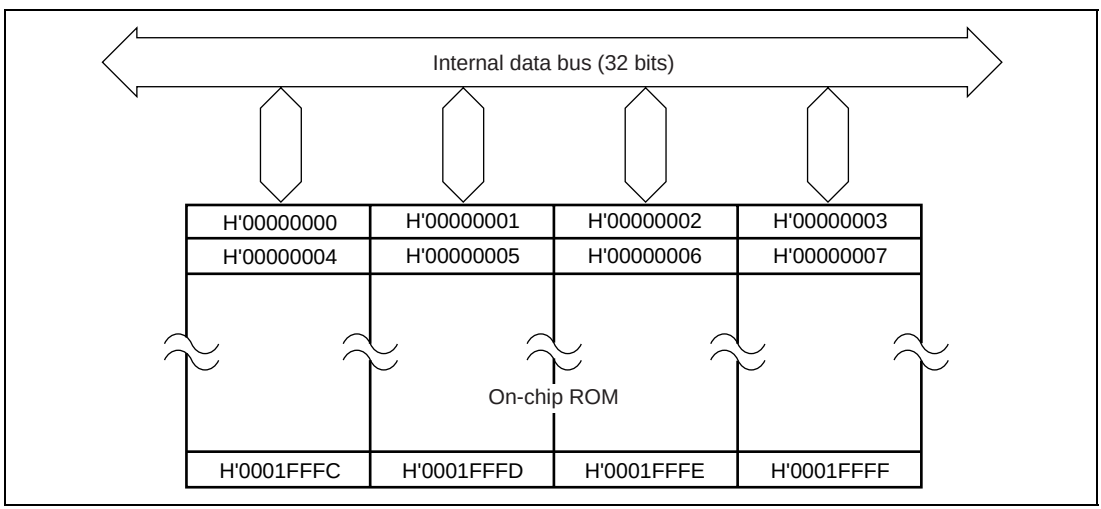


Figure 16.2 Masked ROM Block Diagram (SH7108/SH7109)

The operating mode determines whether the on-chip ROM is valid or not. The operating mode is selected using mode-setting pins FWP and MD3 to MD0 as shown in table 3.1. When the on-chip ROM is used, select mode 2 or mode 3; if not, select mode 0. The on-chip ROM is allocated to addresses H'00000000 to H'0000FFFF of memory area 0 (in the SH7106/SH7107) or H'00000000 to H'0001FFFF of memory area 0 (in the SH7108/SH7109).

16.1 Usage Note

- Setting module standby mode

  For masked ROM, this module can be disabled/enabled by the module standby control register. Masked ROM operation is enabled for the initial value. Accessing masked ROM is disabled by setting module standby mode. For details, refer to section 18, Power-Down Modes.

Section 17 RAM

This LSI has an on-chip high-speed static RAM. The on-chip RAM is connected to the CPU via a 32-bit data bus, enabling 8, 16, or 32-bit width access to data in the on-chip RAM. Data in the on-chip RAM can always be accessed in one cycle, providing high-speed access that makes this RAM ideal for use as a program area, stack area, or data area. The contents of the on-chip RAM are retained in both sleep and software standby modes.

The on-chip RAM can be enabled or disabled by means of the RAME bit in the system control register (SYSCR). For details on SYSCR, refer to section 18.2.2, System Control Register (SYSCR).

Product Type	Type of ROM	RAM Capacity	RAM Address
SH7108	Masked ROM	4 kbytes	H'FFFFF000 to H'FFFFFFFF

17.1 Usage Note

- Module Standby Mode Setting

  RAM can be enabled or disabled by the module standby control register. The initial value enables RAM operation. RAM access is disabled by setting module standby mode. For details, refer to section 18, Power-Down Modes.

Section 18 Power-Down Modes

In addition to the normal program execution state, this LSI has four power-down modes in which operation of the CPU and oscillator is halted and power consumption is reduced. Low-power operation can be achieved by individually controlling the CPU, on-chip peripheral functions, and so on.

This LSI's power-down modes are as follows:

- Sleep mode
- Software standby mode
- Hardware standby mode
- Module standby mode

Sleep mode indicates the state of the CPU, and module standby mode indicates the state of the on-chip peripheral function (including the bus master other than the CPU). Some of these states can be combined.

After a reset, this LSI is in normal operating mode.

Table 18.1 lists internal operation states in each mode.

Table 18.1 Internal Operating States in Each Mode

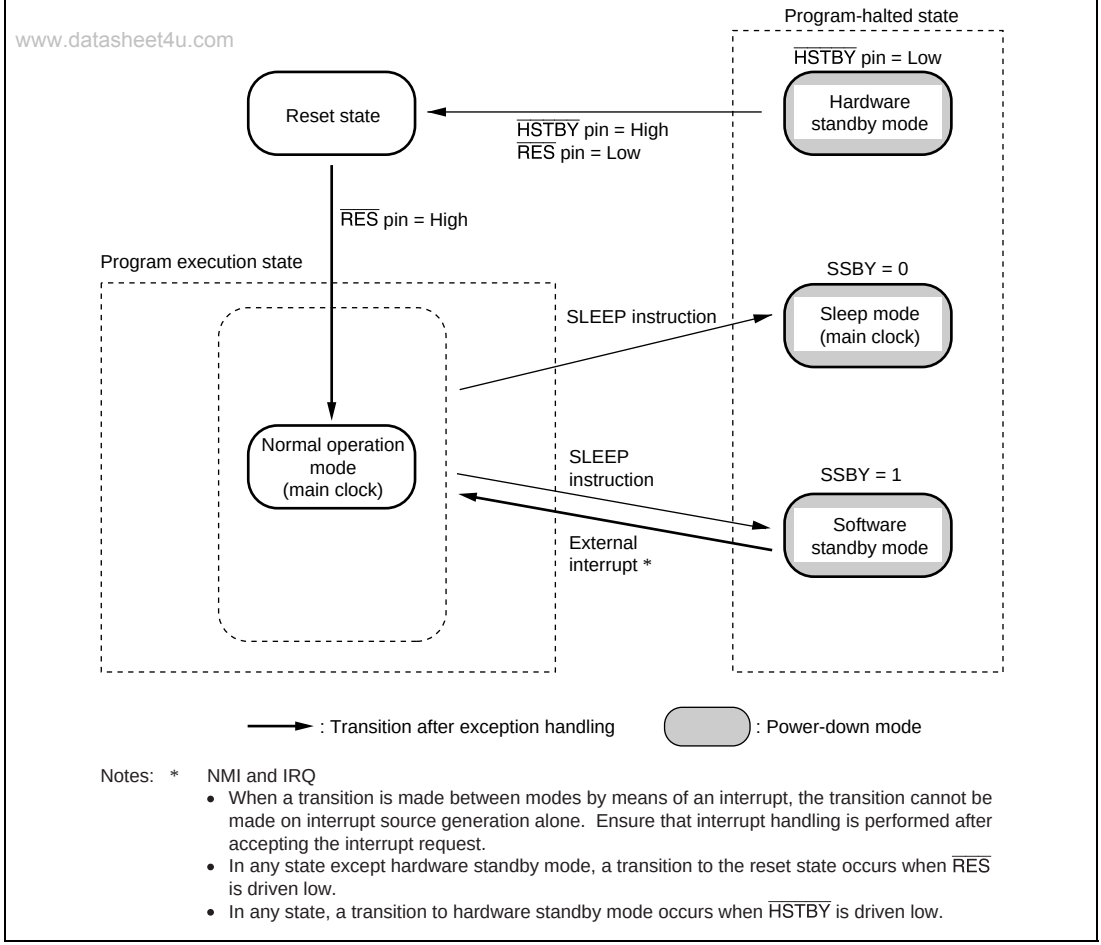
Function		Normal operation	Sleep	Module Standby	Software Standby	Hardware Standby
System clock pulse generator		Functioning	Functioning	Functioning	Halted	Halted
CPU	Instructions	Functioning	Halted (retained)	Functioning	Halted (retained)	Halted (undefined)
	Registers					
External interrupts	NMI	Functioning	Functioning	Functioning	Functioning	Halted
	$\overline{\text{IRQ3}}$ to $\overline{\text{IRQ0}}$					
Peripheral functions	I/O ports	Functioning	Functioning	Functioning	Retained	High impedance
	WDT	Functioning	Functioning	Functioning	Halted (retained)	Halted (reset)
	SCI	Functioning	Functioning	Halted (reset)	Halted (reset)	Halted (reset)
	A/D					
	MTU					
	CMT					
	MMT					
	ROM	Functioning	Functioning	Halted (reset)	Halted (reset)	Halted (reset)
	RAM	Functioning	Functioning	Retained	Retained	Retained

Notes: "Halted (retained)" means that the operation of the internal state is suspended, although internal register values are retained.

"Halted (reset)" means that internal register values and internal state are initialized.

In module standby mode, only modules for which a stop setting has been made are halted (reset or retained).

1. There are two types of on-chip peripheral module registers; ones which are initialized in software standby mode and module standby mode, and those not initialized in those modes. For details, refer to section 19.3, Register States in Each Operating Mode.
2. The port high-impedance bit (Hi-Z) in SBYCR sets the state of the I/O ports in software standby mode. For details on the setting, refer to section 18.2.1, Standby Control Register (SBYCR). For the state of pins, refer to appendix A, Pin States.



Notes: * NMI and IRQ

- When a transition is made between modes by means of an interrupt, the transition cannot be made on interrupt source generation alone. Ensure that interrupt handling is performed after accepting the interrupt request.
- In any state except hardware standby mode, a transition to the reset state occurs when $\overline{\text{RES}}$ is driven low.
- In any state, a transition to hardware standby mode occurs when $\overline{\text{HSTBY}}$ is driven low.

Figure 18.1 Mode Transition Diagram

18.1 Input/Output Pins

Table 18.2 lists the pins relating to power-down mode.

Table 18.2 Pin Configuration

Pin Name	I/O	Function
$\overline{\text{HSTBY}}$	Input	Hardware standby input pin
$\overline{\text{RES}}$	Input	Power-on reset input pin
$\overline{\text{MRES}}$	Input	Manual reset input pin

18.2 Register Descriptions

Registers related to power-down modes are shown below. For details on register addresses and register states during each process, refer to section 19, List of Registers.

- Standby control register (SBYCR)
- System control register (SYSCR)
- Module standby control register 1 (MSTCR1)
- Module standby control register 2 (MSTCR2)

18.2.1 Standby Control Register (SBYCR)

SBYCR is an 8-bit readable/writable register that performs software standby mode control.

Bit	Bit Name	Initial Value	R/W	Description
7	SSBY	0	R/W	Software Standby Specifies the transition mode after executing the SLEEP instruction. 0: Transition to sleep mode after the SLEEP instruction has been executed 1: Transition to software standby mode after the SLEEP instruction has been executed This bit cannot be set to 1 when the watchdog timer (WDT) is operating (when the TME bit in TCSR of the WDT is set to 1). When entering software standby mode, clear the TME bit to 0, stop the WDT, then set the SSBY bit to 1.
6	HIZ	0	R/W	Port High-Impedance In software standby mode, this bit selects whether the pin state of the I/O port is retained or changed to high-impedance. 0: In software standby mode, the pin state is retained. 1: In software standby mode, the pin state is changed to high-impedance. The HIZ bit cannot be set to 1 when the TEM bit in TCSR of the WDT is set to 1. When changing the pin state of the I/O port to high-impedance, clear the TEM bit to 0, then set the HIZ bit to 1.
5	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
4 to 1	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
0	IRQEL	1	R/W	IRQ3 to IRQ0 Enable Enables to clear software standby mode by IRQ interrupts. 0: Software standby mode is cleared. 1: Software standby mode is not cleared.

18.2.2 System Control Register (SYSCR)

SYSCR is an 8-bit readable/writable register that enables/disables the access to the on-chip RAM.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
5 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	RAME	1	R/W	RAM Enable Enables or disables the on-chip RAM. 0: On-chip RAM disabled 1: On-chip RAM enabled When this bit is cleared to 0, the access to the on-chip RAM is disabled. In this case, an undefined value is returned when reading or fetching the data or instruction from the on-chip RAM, and writing to the on-chip RAM is ignored. When RAME is cleared to 0 to disable the on-chip RAM, an instruction to access the on-chip RAM should not be set next to the instruction to write to SYSCR. If such an instruction is set, normal access is not guaranteed. When RAME is set to 1 to enable the on-chip RAM, an instruction to read SYSCR should be set next to the instruction to write to SYSCR. If an instruction to access the on-chip RAM is set next to the instruction to write to SYSCR, normal access is not guaranteed.

18.2.3 Module Standby Control Registers 1 and 2 (MSTCR1 and MSTCR2)

MSTCR is two 16-bit readable/writable registers that perform module standby mode control. Setting a bit to 1, the corresponding module enters module standby mode, while clearing the bit to 0 clears module standby mode.

- MSTCR1

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 1	R/W	Reserved These bits are always read as 1. The write value should always be 1.
11	MSTP27	0	R/W	On-chip RAM
10	MSTP26	0	R/W	On-chip ROM
9 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
3	MSTP19	1	R/W	Serial communication interface 3 (SCI_3)
2	MSTP18	1	R/W	Serial communication interface 2 (SCI_2)
1, 0	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

- MSTCR2

Bit	Bit Name	Initial Value	R/W	Description
15	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
14	MSTP14	1	R/W	Motor management timer (MMT)
13	MSTP13	1	R/W	Multifunction timer pulse unit (MTU)
12	MSTP12	1	R/W	Compare match timer (CMT)
11 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0
7	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
6	MSTP6	1	R/W	A/D converter (A/D2)
5	MSTP5	1	R/W	A/D converter (A/D1)
4	MSTP4	1	R/W	A/D converter (A/D0)
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

18.3 Operation

18.3.1 Sleep Mode

(1) Transition to Sleep Mode

If a SLEEP instruction is executed while the SSBY bit in SBYCR is cleared to 0, the CPU enters sleep mode. In sleep mode, CPU operation stops, however the contents of the CPU's internal registers are retained. Peripheral functions except the CPU do not stop.

(2) Clearing Sleep Mode

Sleep mode is cleared by the conditions below.

- Clearing by a power-on reset
  When the $\overline{\text{RES}}$ pin is driven low, the CPU enters the reset state. When the $\overline{\text{RES}}$ pin is driven high after the elapse of the specified reset input period, the CPU starts the reset exception handling.

When an internal power-on reset by the WDT occurs, sleep mode is also cleared.

- Clearing by a manual reset

  When the $\overline{\text{MRES}}$ pin is driven low while the $\overline{\text{RES}}$ pin goes high, the CPU shifts to the manual reset state and thus sleep mode is cleared.

  When an internal manual reset by the WDT occurs, sleep mode is also cleared.

18.3.2 Software Standby Mode

(1) Transition to Software Standby Mode

A transition is made to software standby mode if the SLEEP instruction is executed while the SSBY bit in SBYCR is set to 1. In this mode, the CPU, on-chip peripheral functions, and oscillator, all stop.

However, the contents of the CPU's internal registers and on-chip RAM data (when the RAME bit in SYSCR is 0) are retained as long as the specified voltage is supplied. There are two types of on-chip peripheral module registers; ones which are initialized by software standby mode, and those not initialized by that mode. For details, refer to section 19.3, Register States in Each Operating Mode. The port high-impedance bit (HIZ) in SBYCR sets the state of the I/O port either to "retained" or "high-impedance". For the state of pins, refer to appendix A, Pin States. In software standby mode, the oscillator stops and thus power consumption is significantly reduced.

(2) Clearing Software Standby Mode

Software standby mode is cleared by the condition below.

- Clearing by the NMI interrupt input

  When the falling edge or rising edge of the NMI pin (selected by the NMI edge select bit (NMIE) in ICR1 of the interrupt controller (INTC)) is detected, clock oscillation is started. This clock pulse is supplied only to the watchdog timer (WDT).

  After the elapse of the time set in the clock select bits (CKS2 to CKS0) in TCSR of the WDT before the transition to software standby mode, the WDT overflow occurs. Since this overflow indicates that the clock has been stabilized, clock pulse will be supplied to the entire chip after this overflow. Software standby mode is thus cleared and the NMI exception handling is started.

  When clearing software standby mode by the NMI interrupt, set the CKS2 to CKS0 bits so that the WDT overflow period will be longer than the oscillation stabilization time.

  When software standby mode is cleared by the falling edge of the NMI pin, the NMI pin should be high when the CPU enters software standby mode (when the clock pulse stops) and should be low when the CPU returns from standby mode (when the clock is initiated after the oscillation stabilization). When software standby mode is cleared by the rising edge of the NMI pin, the NMI pin should be low when the CPU enters software standby mode (when the clock pulse stops) and should be high when the CPU returns from software standby mode (when the clock is initiated after the oscillation stabilization).

- Clearing by the $\overline{\text{RES}}$ pin

  When the $\overline{\text{RES}}$ pin is driven low, clock oscillation is started. At the same time as clock oscillation is started, clock pulse is supplied to the entire chip. Ensure that the $\overline{\text{RES}}$ pin is held low until clock oscillation stabilizes. When the $\overline{\text{RES}}$ pin is driven high, the CPU starts the reset exception handling.

- Clearing by the IRQ interrupt input

  When the IRQEL bit in the standby control register (SBYCR) is set to 1 and when the falling edge or rising edge of the IRQ pin (selected by the IRQ3S to IRQ0S bits in ICR1 of the interrupt controller (INTC) and the IRQ3ES[1:0] to IRQ0ES[1:0] bits in ICR2) is detected, clock oscillation is started.* This clock pulse is supplied only to the watchdog timer (WDT). The IRQ interrupt priority level should be higher than the interrupt mask level set in the status register (SR) of the CPU before the transition to software standby mode.

After the elapse of the time set in the clock select bits (CKS2 to CKS0) in TCSR of the WDT before the transition to software standby mode, the WDT overflow occurs. Since this overflow indicates that the clock has been stabilized, clock pulse will be supplied to the entire chip after this overflow. Software standby mode is thus cleared and the IRQ exception handling is started.

When clearing software standby mode by the IRQ interrupt, set the CKS2 to CKS0 bits so that the WDT overflow period will be longer than the oscillation stabilization time.

When software standby mode is cleared by the falling edge or both edges of the $\overline{\text{IRQ}}$ pin, the $\overline{\text{IRQ}}$ pin should be high when the CPU enters software standby mode (when the clock pulse stops) and should be low when the CPU returns from software standby mode (when the clock is initiated after the oscillation stabilization). When software standby mode is cleared by the rising edge of the $\overline{\text{IRQ}}$ pin, the $\overline{\text{IRQ}}$ pin should be low when the CPU enters software standby mode (when the clock pulse stops) and should be high when the CPU returns from software standby mode (when the clock is initiated after the oscillation stabilization).

Note: * When the $\overline{\text{IRQ}}$ pin is set to falling-edge detection or both-edge detection, clock oscillation starts at falling-edge detection. When the $\overline{\text{IRQ}}$ pin is set to rising-edge detection, clock oscillation starts at rising-edge detection. Do not set the $\overline{\text{IRQ}}$ pin to low-level detection.

(3) Application Example of Software Standby Mode

Figure 18.2 shows an example in which a transition is made to software standby mode at the falling edge of the NMI pin, and software standby mode is cleared at a rising edge of the NMI pin.

In this example, when the NMI pin is driven from high to low while the NMI edge select bit (NMIE) in ICR1 is 0 (falling edge detection), an NMI interrupt is accepted. Then, when the NMIE bit is set to 1 (rising edge detection) in the NMI exception service routine, the SSBY bit in SBYCR is set to 1, and a SLEEP instruction is executed, a transition is made to software standby mode. Software standby mode is cleared by driving the NMI pin from low to high.

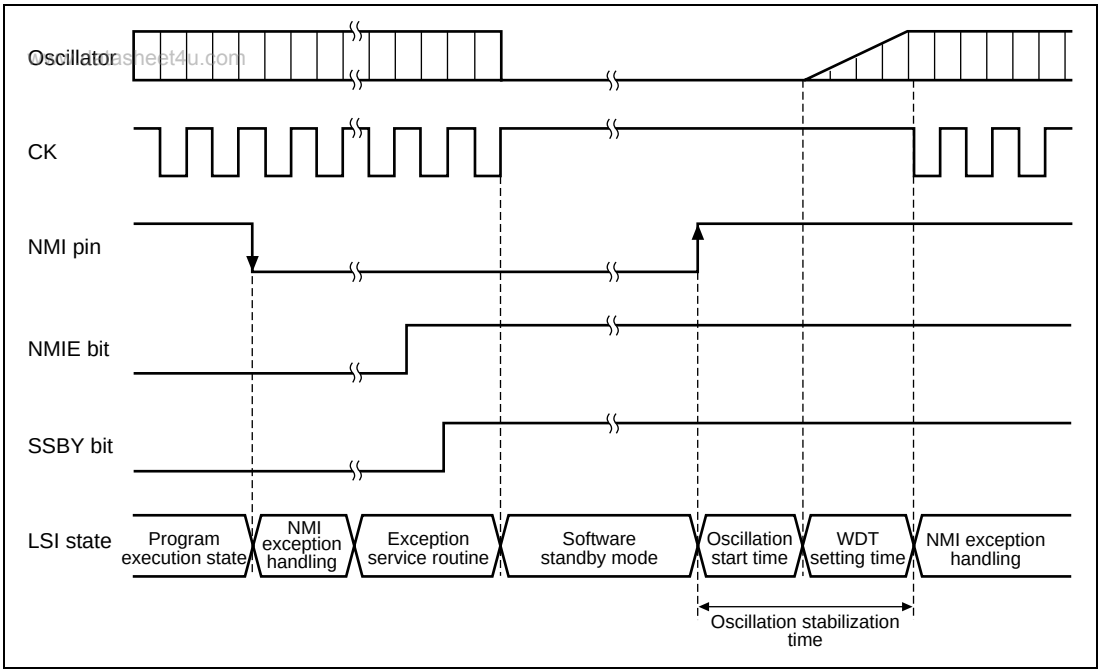


Figure 18.2 NMI Timing in Software Standby Mode

18.3.3 Hardware Standby Mode

(1) Transition to Hardware Standby Mode

When the $\overline{\text{HSTBY}}$ pin is driven low, a transition is made to hardware standby mode from any mode.

In hardware standby mode, all functions enter the reset state and stop operation, resulting in a significant reduction in power consumption. As long as the specified voltage is supplied, on-chip RAM data is retained.

In order to retain on-chip RAM data, the RAME bit in SYSCR should be cleared to 0 before driving the $\overline{\text{HSTBY}}$ pin low. Do not change the state of the mode pins (MD3 to MD0) while the CPU is in hardware standby mode.

(2) Clearing Hardware Standby Mode

Hardware standby mode is cleared by means of the $\overline{\text{HSTBY}}$ pin and $\overline{\text{RES}}$ pin. When the $\overline{\text{HSTBY}}$ pin is driven high while the $\overline{\text{RES}}$ pin is low, the reset state is set and clock oscillation is started. Ensure that the $\overline{\text{RES}}$ pin is held low until the clock oscillation stabilizes. When the $\overline{\text{RES}}$ pin is then driven high, a transition is made to the program execution state via the power-on reset exception handling state.

(3) Hardware Standby Mode Timing

Figure 18.3 shows a transition-timing example to hardware standby mode.

In this example, when the $\overline{\text{HSTBY}}$ pin is driven low, the transition to hardware standby mode is made. Hardware standby mode is cleared when the $\overline{\text{HSTBY}}$ pin is driven high and then the $\overline{\text{RES}}$ pin is driven high after the elapse of the oscillation stabilization time of the clock pulse.

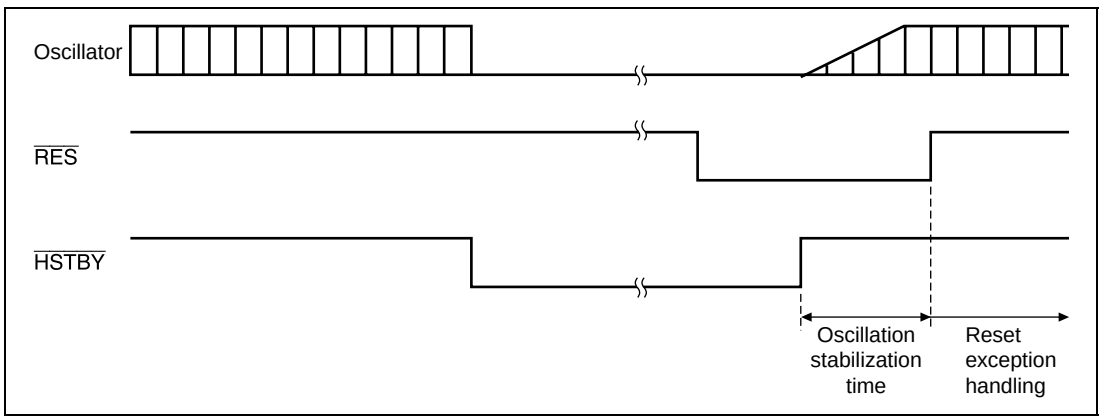


Figure 18.3 Transition Timing to Hardware Standby Mode

18.3.4 Module Standby Mode

Module standby mode can be set for individual on-chip peripheral functions.

When the corresponding MSTP bit in MSTCR is set to 1, module operation stops at the end of the bus cycle and a transition is made to module standby mode. The CPU continues operating independently.

When the corresponding MSTP bit is cleared to 0, module standby mode is cleared and the module starts operating at the end of the bus cycle. In module standby mode, the internal states of modules are initialized.

After reset clearing, the SCI, MTU, MMT, CMT, and A/D converter are in module standby mode.

When an on-chip peripheral module is in module standby mode, read/write access to its registers is disabled.

18.4 Usage Notes

18.4.1 I/O Port Status

When a transition is made to software standby mode while the port high-impedance bit (HIZ) in SBYCR is cleared to 0, I/O port states are retained. Therefore, there is no reduction in current consumption for the output current when a high-level signal is output.

18.4.2 Current Consumption during Oscillation Stabilization Wait Period

Current consumption increases during the oscillation stabilization wait period.

18.4.3 On-Chip Peripheral Module Interrupt

Relevant interrupt operations cannot be performed in module standby mode. Consequently, if the CPU enters module standby mode while an interrupt has been requested, it will not be possible to clear the CPU interrupt source.

Interrupts should therefore be disabled before entering module standby mode.

18.4.4 Writing to MSTCR1 and MSTCR2

MSTCR1 and MSTCR2 should only be written to by the CPU.

Section 19 List of Registers

The column “Access Size” shows the number of bits.

The column “Access States” shows the number of access states, in units of cycles, of the specified reference clock. B, W, and L in the column represent 8-bit, 16-bit, and 32-bit access, respectively.

19.1 Register Addresses (Address Order)

Register Name	Abbre-viation	Bits	Address	Module	Access Size	Access States
—	—	—	H'FFFF8000 to H'FFFF81BF	—	—	—
Serial mode register_2	SMR_2	8	H'FFFF81C0	SCI (channel 2)	8, 16	In Pϕ cycles B: 2 W: 4
Bit rate register_2	BRR_2	8	H'FFFF81C1		8	
Serial control register_2	SCR_2	8	H'FFFF81C2		8, 16	
Transmit data register_2	TDR_2	8	H'FFFF81C3		8	
Serial status register_2	SSR_2	8	H'FFFF81C4		8, 16	
Receive data register_2	RDR_2	8	H'FFFF81C5		8	
Serial direction control register_2	SDCR_2	8	H'FFFF81C6		8	
—	—	—	H'FFFF81C7 to H'FFFF81CF	—	—	
Serial mode register_3	SMR_3	8	H'FFFF81D0	SCI (channel 3)	8, 16	
Bit rate register_3	BRR_3	8	H'FFFF81D1		8	
Serial control register_3	SCR_3	8	H'FFFF81D2		8, 16	
Transmit data register_3	TDR_3	8	H'FFFF81D3		8	
Serial status register_3	SSR_3	8	H'FFFF81D4		8, 16	
Receive data register_3	RDR_3	8	H'FFFF81D5		8	
Serial direction control register_3	SDCR_3	8	H'FFFF81D6		8	
—	—	—	H'FFFF81D7 to H'FFFF81EF	—	—	
—	—	—	H'FFFF81F0 to H'FFFF81FF	—	—	—
Timer control register_3	TCR_3	8	H'FFFF8200	MTU (channels 3 and 4)	8, 16, 32	In Pϕ cycles B: 2 W: 2 L: 4
Timer control register_4	TCR_4	8	H'FFFF8201		8	
Timer mode register_3	TMDR_3	8	H'FFFF8202		8, 16	
Timer mode register_4	TMDR_4	8	H'FFFF8203		8	
Timer I/O control register H_3	TIORH_3	8	H'FFFF8204		8, 16, 32	
Timer I/O control register L_3	TIORL_3	8	H'FFFF8205		8	

Register Name	Abbre-viation	Bits	Address	Module	Access Size	Access States
Timer I/O control register H_4	TIORH_4	8	H'FFFF8206		8, 16	
Timer I/O control register L_4	TIORL_4	8	H'FFFF8207		8	
Timer interrupt enable register_3	TIER_3	8	H'FFFF8208		8, 16, 32	
Timer interrupt enable register_4	TIER_4	8	H'FFFF8209		8	
Timer output master enable register	TOER	8	H'FFFF820A		8, 16	
Timer output control register	TOCR	8	H'FFFF820B		8	
—	—	—	H'FFFF820C		—	
Timer gate control register	TGCR	8	H'FFFF820D		8	
—	—	—	H'FFFF820E		—	
—	—	—	H'FFFF820F		—	
Timer counter_3	TCNT_3	16	H'FFFF8210		16, 32	
Timer counter_4	TCNT_4	16	H'FFFF8212		16	
Timer period data register	TCDR	16	H'FFFF8214		16, 32	
Timer dead time data register	TDDR	16	H'FFFF8216		16	
Timer general register A_3	TGRA_3	16	H'FFFF8218		16, 32	
Timer general register B_3	TGRB_3	16	H'FFFF821A		16	
Timer general register A_4	TGRA_4	16	H'FFFF821C		16, 32	
Timer general register B_4	TGRB_4	16	H'FFFF821E		16	
Timer sub-counter	TCNTS	16	H'FFFF8220		16, 32	
Timer period buffer register	TCBR	16	H'FFFF8222		16	
Timer general register C_3	TGRC_3	16	H'FFFF8224		16, 32	
Timer general register D_3	TGRD_3	16	H'FFFF8226		16	
Timer general register C_4	TGRC_4	16	H'FFFF8228		16, 32	
Timer general register D_4	TGRD_4	16	H'FFFF822A		16	
Timer status register_3	TSR_3	8	H'FFFF822C		8, 16	
Timer status register_4	TSR_4	8	H'FFFF822D		8	
—	—	—	H'FFFF822E to H'FFFF823F		—	
Timer start register	TSTR	8	H'FFFF8240	MTU (common)	8, 16	In Pϕ cycles B: 2 W: 2
Timer synchro register	TSYR	8	H'FFFF8241		8	
—	—	—	H'FFFF8242 to H'FFFF825F		—	
Timer control register_0	TCR_0	8	H'FFFF8260	MTU (channel 0)	8, 16, 32	In Pϕ cycles B: 2 W: 2 L: 4
Timer mode register_0	TMDR_0	8	H'FFFF8261		8	
Timer I/O control register H_0	TIORH_0	8	H'FFFF8262		8, 16	

Register Name	Abbre-viation	Bits	Address	Module	Access Size	Access States
Timer I/O control register L_0	TIORL_0	8	H'FFFF8263		8	
Timer interrupt enable register_0	TIER_0	8	H'FFFF8264		8, 16, 32	
Timer status register_0	TSR_0	8	H'FFFF8265		8	
Timer counter_0	TCNT_0	16	H'FFFF8266		16	
Timer general register A_0	TGRA_0	16	H'FFFF8268		16, 32	
Timer general register B_0	TGRB_0	16	H'FFFF826A		16	
Timer general register C_0	TGRC_0	16	H'FFFF826C		16, 32	
Timer general register D_0	TGRD_0	16	H'FFFF826E		16	
—	—	—	H'FFFF8270 to H'FFFF827F		—	
Timer control register_1	TCR_1	8	H'FFFF8280	MTU (channel 1)	8, 16	
Timer mode register_1	TMDR_1	8	H'FFFF8281		8	
Timer I/O control register_1	TIOR_1	8	H'FFFF8282		8	
—	—	—	H'FFFF8283		—	
Timer interrupt enable register_1	TIER_1	8	H'FFFF8284		8, 16, 32	
Timer status register_1	TSR_1	8	H'FFFF8285		8	
Timer counter_1	TCNT_1	16	H'FFFF8286		16	
Timer general register A_1	TGRA_1	16	H'FFFF8288		16, 32	
Timer general register B_1	TGRB_1	16	H'FFFF828A		16	
—	—	—	H'FFFF828C to H'FFFF829F		—	
Timer control register_2	TCR_2	8	H'FFFF82A0	MTU (channel 2)	8, 16	
Timer mode register_2	TMDR_2	8	H'FFFF82A1		8	
Timer I/O control register_2	TIOR_2	8	H'FFFF82A2		8	
—	—	—	H'FFFF82A3		—	
Timer interrupt enable register_2	TIER_2	8	H'FFFF82A4		8, 16, 32	
Timer status register_2	TSR_2	8	H'FFFF82A5		8	
Timer counter_2	TCNT_2	16	H'FFFF82A6		16	
Timer general register A_2	TGRA_2	16	H'FFFF82A8		16, 32	
Timer general register B_2	TGRB_2	16	H'FFFF82AA		16	
—	—	—	H'FFFF82AC to H'FFFF833F	—	—	—
—	—	—	H'FFFF8340 to H'FFFF8347	INTC	—	In ϕ cycles B: 2 W: 2 L: 4
Interrupt priority register A	IPRA	16	H'FFFF8348		8, 16	
—	—	—	H'FFFF834A to H'FFFF834D		—	

Register Name	Abbre-viation	Bits	Address	Module	Access Size	Access States
Interrupt priority register D	IPRD	16	H'FFFF834E		8, 16	
Interrupt priority register E	IPRE	16	H'FFFF8350		8, 16, 32	
Interrupt priority register F	IPRF	16	H'FFFF8352		8, 16	
Interrupt priority register G	IPRG	16	H'FFFF8354		8, 16, 32	
Interrupt priority register H	IPRH	16	H'FFFF8356		8, 16	
Interrupt control register 1	ICR1	16	H'FFFF8358		8, 16, 32	
IRQ status register	ISR	16	H'FFFF835A		8, 16	
Interrupt priority register I	IPRI	16	H'FFFF835C		8, 16, 32	
Interrupt priority register J	IPRJ	16	H'FFFF835E		8, 16	
Interrupt priority register K	IPRK	16	H'FFFF8360		8, 16, 32	
—	—	—	H'FFFF8362 to H'FFFF8365		—	
Interrupt control register 2	ICR2	16	H'FFFF8366		8, 16	
—	—	—	H'FFFF8368 to H'FFFF837F		—	
—	—	—	H'FFFF8380 to H'FFFF8381	—	—	—
Port A data register L	PADRL	16	H'FFFF8382	I/O	8, 16	In ϕ cycles B: 2 W: 2 L: 4
—	—	—	H'FFFF8384 to H'FFFF8385	—	—	
Port A I/O register L	PAIORL	16	H'FFFF8386	PFC	8, 16	
—	—	—	H'FFFF8388 to H'FFFF8389	—	—	
Port A control register L3	PACRL3	16	H'FFFF838A	PFC	8, 16	
Port A control register L1	PACRL1	16	H'FFFF838C		8, 16, 32	
Port A control register L2	PACRL2	16	H'FFFF838E		8, 16	
Port B data register	PBDR	16	H'FFFF8390	I/O	8, 16	
—	—	—	H'FFFF8392 to H'FFFF8393	—	—	
Port B I/O register	PBIOR	16	H'FFFF8394	PFC	8, 16, 32	
—	—	—	H'FFFF8396 to H'FFFF8397	—	—	
Port B control register 1	PBCR1	16	H'FFFF8398	PFC	8, 16, 32	In ϕ cycles B: 2 W: 2 L: 4
Port B control register 2	PBCR2	16	H'FFFF839A		8, 16	
—	—	—	H'FFFF839C to H'FFFF83A1	—	—	
Port D data register L	PDDRL	16	H'FFFF83A2	I/O	8, 16	

Register Name	Abbre-viation	Bits	Address	Module	Access Size	Access States
—	—	—	H'FFFF83A4 to H'FFFF83A5	—	—	
Port D I/O register L	PDIORL	16	H'FFFF83A6	PFC	8, 16	
—	—	—	H'FFFF83A8 to H'FFFF83AB	—	—	
Port D control register L1	PDCRL1	16	H'FFFF83AC	PFC	8, 16, 32	
Port D control register L2	PDCRL2	16	H'FFFF83AE		8, 16	
Port E data register L	PEDRL	16	H'FFFF83B0	I/O	8, 16, 32	
Port F data register	PFDR	16	H'FFFF83B2		8, 16	
Port E I/O register L	PEIORL	16	H'FFFF83B4	PFC	8, 16, 32	
Port E I/O register H	PEIORH	16	H'FFFF83B6		8, 16	
Port E control register L1	PECRL1	16	H'FFFF83B8		8, 16, 32	
Port E control register L2	PECRL2	16	H'FFFF83BA		8, 16	
Port E control register H	PECRH	16	H'FFFF83BC		8, 16, 32	
Port E data register H	PEDRH	16	H'FFFF83BE	I/O	8, 16	
Input control/status register 1	ICSR1	16	H'FFFF83C0	MTU	8, 16, 32	In Pϕ cycles B: 2 W: 2 L: 4
Output control/status register	OCSR	16	H'FFFF83C2		8, 16	
Input control/status register 2	ICSR2	16	H'FFFF83C4	MMT	8, 16	
—	—	—	H'FFFF83C6 to H'FFFF83CC	—	—	—
Port G data register	PGDR	8	H'FFFF83CD	I/O	8	In ϕ cycles B: 2 W: 2 L: 4
—	—	—	H'FFFF83CE to H'FFFF83CF	—	—	—
Compare match timer start register	CMSTR	16	H'FFFF83D0	CMT	8, 16, 32	In Pϕ cycles B: 2 W: 2 L: 4
Compare match timer control/status register_0	CMCSR_0	16	H'FFFF83D2		8, 16	
Compare match timer counter_0	CMCNT_0	16	H'FFFF83D4		8, 16, 32	
Compare match timer constant register_0	CMCOR_0	16	H'FFFF83D6		8, 16	
Compare match timer control/status register_1	CMCSR_1	16	H'FFFF83D8		8, 16, 32	
Compare match timer counter_1	CMCNT_1	16	H'FFFF83DA		8, 16	
Compare match timer constant register_1	CMCOR_1	16	H'FFFF83DC		8, 16	
—	—	—	H'FFFF83DE		—	

Register Name	Abbre-viation	Bits	Address	Module	Access Size	Access States
—	—	—	H'FFFF83E0 to H'FFFF841F	—	—	—
A/D data register 0	ADDR0	16	H'FFFF8420	A/D (channel 0)	8, 16	In Pϕ cycles B: 3 W: 6
A/D data register 1	ADDR1	16	H'FFFF8422		8, 16	
A/D data register 2	ADDR2	16	H'FFFF8424		8, 16	
A/D data register 3	ADDR3	16	H'FFFF8426		8, 16	
A/D data register 4	ADDR4	16	H'FFFF8428	A/D (channel 1)	8, 16	
A/D data register 5	ADDR5	16	H'FFFF842A		8, 16	
A/D data register 6	ADDR6	16	H'FFFF842C		8, 16	
A/D data register 7	ADDR7	16	H'FFFF842E		8, 16	
A/D data register 8	ADDR8	16	H'FFFF8430	A/D (channel 0)	8, 16	
A/D data register 9	ADDR9	16	H'FFFF8432		8, 16	
A/D data register 10	ADDR10	16	H'FFFF8434		8, 16	
A/D data register 11	ADDR11	16	H'FFFF8436		8, 16	
A/D data register 12	ADDR12	16	H'FFFF8438	A/D (channel 1)	8, 16	
A/D data register 13	ADDR13	16	H'FFFF843A		8, 16	
A/D data register 14	ADDR14	16	H'FFFF843C		8, 16	
A/D data register 15	ADDR15	16	H'FFFF843E		8, 16	
A/D data register 16	ADDR16	16	H'FFFF8440	A/D (channel 2)	8, 16	
A/D data register 17	ADDR17	16	H'FFFF8442		8, 16	
A/D data register 18	ADDR18	16	H'FFFF8444		8, 16	
A/D data register 19	ADDR19	16	H'FFFF8446		8, 16	
—	—	—	H'FFFF8448 to H'FFFF847F	—	—	
A/D control/status register_0	ADCSR_0	8	H'FFFF8480	A/D	8, 16	
A/D control/status register_1	ADCSR_1	8	H'FFFF8481		8	
A/D control/status register_2	ADCSR_2	8	H'FFFF8482		8	
—	—	—	H'FFFF8483 to H'FFFF8487		—	
A/D control register_0	ADCR_0	8	H'FFFF8488		8, 16	
A/D control register_1	ADCR_1	8	H'FFFF8489		8	
A/D control register_2	ADCR_2	8	H'FFFF848A		8	
—	—	—	H'FFFF848B to H'FFFF860F		—	

Register Name	Abbreviation	Bits	Address	Module	Access Size	Access States
Timer control/status register	TCSR	8	H'FFFF8610	WDT	8*2/16*1	In φ cycles
Timer counter	TCNT*1	8	H'FFFF8610	*1: Write cycle	16	B: 3
Timer counter	TCNT*2	8	H'FFFF8611	*2: Read cycle	8	W: 3
Reset control/status register	RSTCSR*1	8	H'FFFF8612		16	
Reset control/status register	RSTCSR*2	8	H'FFFF8613		8	
Standby control register	SBYCR	8	H'FFFF8614	Power-down modes	8	In φ cycles B: 3
—	—	—	H'FFFF8615 to H'FFFF8617	—	—	—
System control register	SYSCR	8	H'FFFF8618	Power-down modes	8	In Pφ cycles B: 3 W: 3 L: 6
—	—	—	H'FFFF8619 to H'FFFF861B		—	
Module standby control register 1	MSTCR1	16	H'FFFF861C		8, 16, 32	
Module standby control register 2	MSTCR2	16	H'FFFF861E		8, 16	
Bus control register 1	BCR1	16	H'FFFF8620	BSC	8, 16, 32	In φ cycles B: 3 W: 3 L: 6
Bus control register 2	BCR2	16	H'FFFF8622		8, 16	
Wait control register 1	WCR1	16	H'FFFF8624		8, 16	
—	—	—	H'FFFF8626		—	
—	—	—	H'FFFF8628 to H'FFFF864F	—	—	—
—	—	—	H'FFFF8650 to H'FFFF87F3	—	—	—
A/D trigger select register	ADTSR	8	H'FFFF87F4	A/D	8	In Pφ cycles B: 3
—	—	—	H'FFFF87F5 to H'FFFF89FF		—	
Timer mode register	MMT_TMDR	8	H'FFFF8A00	MMT	8	In Pφ cycles B: 2 W: 2 L: 4
—	—	—	H'FFFF8A01		—	
Timer control register	TCNR	8	H'FFFF8A02		8	
—	—	—	H'FFFF8A03		—	
Timer status register	MMT_TSR	8	H'FFFF8A04		8	
—	—	—	H'FFFF8A05		—	
Timer counter	MMT_TCNT	16	H'FFFF8A06		16	
Timer period data register	TPDR	16	H'FFFF8A08		16, 32	
Timer period buffer register	TPBR	16	H'FFFF8A0A		16	
Timer dead time data register	MMT_TDDR	16	H'FFFF8A0C		16	

Register Name	Abbre-viation	Bits	Address	Module	Access Size	Access States
—	—	—	H'FFFF8A0E to H'FFFF8A0F		—	
Timer buffer register U_B	TBRU_B	16	H'FFFF8A10		16, 32	
Timer general register UU	TGRUU	16	H'FFFF8A12		16	
Timer general register U	TGRU	16	H'FFFF8A14		16, 32	
Timer general register UD	TGRUD	16	H'FFFF8A16		16	
Timer dead time counter 0	TDCNT0	16	H'FFFF8A18		16, 32	
Timer dead time counter 1	TDCNT1	16	H'FFFF8A1A		16	
Timer buffer register U_F	TBRU_F	16	H'FFFF8A1C		16	
—	—	—	H'FFFF8A1E to H'FFFF8A1F		—	
Timer buffer register V_B	TBRV_B	16	H'FFFF8A20		16, 32	
Timer general register VU	TGRVU	16	H'FFFF8A22		16	
Timer general register V	TGRV	16	H'FFFF8A24		16, 32	
Timer general register VD	TGRVD	16	H'FFFF8A26		16	
Timer dead time counter 2	TDCNT2	16	H'FFFF8A28		16, 32	
Timer dead time counter 3	TDCNT3	16	H'FFFF8A2A		16	
Timer buffer register V_F	TBRV_F	16	H'FFFF8A2C		16	
—	—	—	H'FFFF8A2E to H'FFFF8A2F		—	
Timer buffer register W_B	TBRW_B	16	H'FFFF8A30		16, 32	
Timer general register WU	TGRWU	16	H'FFFF8A32		16	
Timer general register W	TGRW	16	H'FFFF8A34		16, 32	
Timer general register WD	TGRWD	16	H'FFFF8A36		16	
Timer dead time counter 4	TDCNT4	16	H'FFFF8A38		16, 32	
Timer dead time counter 5	TDCNT5	16	H'FFFF8A3A		16	
Timer buffer register W_F	TBRW_F	16	H'FFFF8A3C		16	
—	—	—	H'FFFF8A3E to H'FFFF8A4F		—	

19.2 Register Bits

Addresses and bit names for on-chip peripheral module registers are shown in the following table.

16-bit and 32-bit registers are shown in two or four rows of 8 bits, respectively.

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
SMR_2	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI (channel 2)
BRR_2									
SCR_2	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
TDR_2									
SSR_2	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
RDR_2									
SDCR_2	—	—	—	—	DIR	—	—	—	
SMR_3	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI (channel 3)
BRR_3									
SCR_3	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
TDR_3									
SSR_3	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
RDR_3									
SDCR_3	—	—	—	—	DIR	—	—	—	
TCR_3	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	MTU (channels 3 and 4)
TCR_4	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	
TMDR_3	—	—	BFB	BFA	MD3	MD2	MD1	MD0	
TMDR_4	—	—	BFB	BFA	MD3	MD2	MD1	MD0	
TIORH_3	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIORL_3	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0	
TIORH_4	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIORL_4	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0	
TIER_3	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA	
TIER_4	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA	
TOER	—	—	OE4D	OE4C	OE3D	OE4B	OE4A	OE3B	
TOCR	—	PSYE	—	—	—	—	OLSN	OLSP	
TGCR	—	BDC	N	P	FB	WF	VF	UF	
TCNT_3									
TCNT_4									
TCDR									

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
TDDR									MTU (channels 3 and 4)
TGRA_3									
TGRB_3									
TGRA_4									
TGRB_4									
TCNTS									
TCBR									
TGRC_3									
TGRD_3									
TGRC_4									
TGRD_4									
TSR_3	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA	
TSR_4	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA	
TSTR	CST4	CST3	—	—	—	CST2	CST1	CST0	MTU (common)
TSYR	SYNC4	SYNC3	—	—	—	SYNC2	SYNC1	SYNC0	
TCR_0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	MTU (channel 0)
TMDR_0	—	—	BFB	BFA	MD3	MD2	MD1	MD0	
TIORH_0	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIORL_0	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0	
TIER_0	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA	
TSR_0	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA	
TCNT_0									
TGRA_0									
TGRB_0									

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
TGRC_0									MTU (channel 0)
TGRD_0									
TCR_1	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	MTU (channel 1)
TMDR_1	—	—	—	—	MD3	MD2	MD1	MD0	
TIOR_1	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIER_1	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA	
TSR_1	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA	
TCNT_1									
TGRA_1									
TGRB_1									
TCR_2	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	MTU (channel 2)
TMDR_2	—	—	—	—	MD3	MD2	MD1	MD0	
TIOR_2	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIER_2	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA	
TSR_2	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA	
TCNT_2									
TGRA_2									
TGRB_2									
IPRA	IRQ0	IRQ0	IRQ0	IRQ0	IRQ1	IRQ1	IRQ1	IRQ1	INTC
	IRQ2	IRQ2	IRQ2	IRQ2	IRQ3	IRQ3	IRQ3	IRQ3	
IPRD	MTU0	MTU0	MTU0	MTU0	MTU0	MTU0	MTU0	MTU0	
	MTU1	MTU1	MTU1	MTU1	MTU1	MTU1	MTU1	MTU1	
IPRE	MTU2	MTU2	MTU2	MTU2	MTU2	MTU2	MTU2	MTU2	
	MTU3	MTU3	MTU3	MTU3	MTU3	MTU3	MTU3	MTU3	
IPRF	MTU4	MTU4	MTU4	MTU4	MTU4	MTU4	MTU4	MTU4	
	—	—	—	—	—	—	—	—	
IPRG	A/D0,1	A/D0,1	A/D0,1	A/D0,1	—	—	—	—	
	CMT0	CMT0	CMT0	CMT0	CMT1	CMT1	CMT1	CMT1	
IPRH	WDT	WDT	WDT	WDT	I/O(MTU)	I/O(MTU)	I/O(MTU)	I/O(MTU)	
	—	—	—	—	—	—	—	—	

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
ICR1	NMIL	—	—	—	—	—	—	NMIE	INTC
	IRQ0S	IRQ1S	IRQ2S	IRQ3S	—	—	—	—	
ISR	—	—	—	—	—	—	—	—	
	IRQ0F	IRQ1F	IRQ2F	IRQ3F	—	—	—	—	
IPRI	SCI2	SCI2	SCI2	SCI2	SCI3	SCI3	SCI3	SCI3	
	—	—	—	—	MMT	MMT	MMT	MMT	
IPRJ	A/D2	A/D2	A/D2	A/D2	—	—	—	—	
	—	—	—	—	—	—	—	—	
IPRK	I/O(MMT)	I/O(MMT)	I/O(MMT)	I/O(MMT)	—	—	—	—	
	—	—	—	—	—	—	—	—	
ICR2	IRQ0ES1	IRQ0ES0	IRQ1ES1	IRQ1ES0	IRQ2ES1	IRQ2ES0	IRQ3ES1	IRQ3ES0	
	—	—	—	—	—	—	—	—	
PADRL	PA15DR	PA14DR	PA13DR	PA12DR	PA11DR	PA10DR	PA9DR	PA8DR	Port A
	PA7DR	PA6DR	PA5DR	PA4DR	PA3DR	PA2DR	PA1DR	PA0DR	
PAIORL	PA15IOR	PA14IOR	PA13IOR	PA12IOR	PA11IOR	PA10IOR	PA9IOR	PA8IOR	
	PA7IOR	PA6IOR	PA5IOR	PA4IOR	PA3IOR	PA2IOR	PA1IOR	PA0IOR	
PACRL3	PA15MD2	PA14MD2	PA13MD2	PA12MD2	PA11MD2	PA10MD2	PA9MD2	PA8MD2	
	PA7MD2	PA6MD2	PA5MD2	PA4MD2	PA3MD2	PA2MD2	PA1MD2	PA0MD2	
PACRL1	PA15MD1	PA15MD0	PA14MD1	PA14MD0	PA13MD1	PA13MD0	PA12MD1	PA12MD0	
	PA11MD1	PA11MD0	PA10MD1	PA10MD0	PA9MD1	PA9MD0	PA8MD1	PA8MD0	
PACRL2	PA7MD1	PA7MD0	PA6MD1	PA6MD0	PA5MD1	PA5MD0	PA4MD1	PA4MD0	
	PA3MD1	PA3MD0	PA2MD1	PA2MD0	PA1MD1	PA1MD0	PA0MD1	PA0MD0	
PBDR	—	—	—	—	—	—	—	—	Port B
	—	—	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR	
PBIOR	—	—	—	—	—	—	—	—	
	—	—	PB5IOR	PB4IOR	PB3IOR	PB2IOR	PB1IOR	PB0IOR	
PBCR1	—	—	PB5MD2	PB4MD2	PB3MD2	PB2MD2	PB1MD2	—	
	—	—	—	—	—	—	—	—	
PBCR2	—	—	—	—	PB5MD1	PB5MD0	PB4MD1	PB4MD0	
	PB3MD1	PB3MD0	PB2MD1	PB2MD0	PB1MD1	PB1MD0	PB0MD1	PB0MD0	
PDDRL	—	—	—	—	—	—	—	PD8DR	Port D
	PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR	
PDIORL	—	—	—	—	—	—	—	PD8IOR	
	PD7IOR	PD6IOR	PD5IOR	PD4IOR	PD3IOR	PD2IOR	PD1IOR	PD0IOR	
PDCRL1	—	—	—	—	—	—	—	PD8MD0	
	PD7MD0	PD6MD0	PD5MD0	PD4MD0	PD3MD0	PD2MD0	PD1MD0	PD0MD0	
PDCRL2	—	—	—	—	—	—	—	PD8MD1	
	PD7MD1	PD6MD1	PD5MD1	PD4MD1	PD3MD1	PD2MD1	PD1MD1	PD0MD1	

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
PEDRL	PE15DR	PE14DR	PE13DR	PE12DR	PE11DR	PE10DR	PE9DR	PE8DR	Port E
	PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR	
PFDR	PF15DR	PF14DR	PF13DR	PF12DR	PF11DR	PF10DR	PF9DR	PF8DR	Port F
	PF7DR	PF6DR	PF5DR	PF4DR	PF3DR	PF2DR	PF1DR	PF0DR	
PEIORL	PE15IOR	PE14IOR	PE13IOR	PE12IOR	PE11IOR	PE10IOR	PE9IOR	PE8IOR	Port E
	PE7IOR	PE6IOR	PE5IOR	PE4IOR	PE3IOR	PE2IOR	PE1IOR	PE0IOR	
PEIORH	—	—	—	—	—	—	—	—	
	—	—	PE21IOR	PE20IOR	PE19IOR	PE18IOR	PE17IOR	PE16IOR	
PECRL1	PE15MD1	PE15MD0	PE14MD1	PE14MD0	PE13MD1	PE13MD0	PE12MD1	PE12MD0	
	PE11MD1	PE11MD0	PE10MD1	PE10MD0	PE9MD1	PE9MD0	PE8MD1	PE8MD0	
PECRL2	PE7MD1	PE7MD0	PE6MD1	PE6MD0	PE5MD1	PE5MD0	PE4MD1	PE4MD0	
	PE3MD1	PE3MD0	PE2MD1	PE2MD0	PE1MD1	PE1MD0	PE0MD1	PE0MD0	
PECRH	—	—	—	—	PE21MD1	PE21MD0	PE20MD1	PE20MD0	
	PE19MD1	PE19MD0	PE18MD1	PE18MD0	PE17MD1	PE17MD0	PE16MD1	PE16MD0	
PEDRH	—	—	—	—	—	—	—	—	
	—	—	PE21DR	PE20DR	PE19DR	PE18DR	PE17DR	PE16DR	
ICSR1	POE3F	POE2F	POE1F	POE0F	—	—	—	PIE	MTU
	POE3M1	POE3M0	POE2M1	POE2M0	POE1M1	POE1M0	POE0M1	POE0M0	
OCSR	OSF	—	—	—	—	—	OCE	OIE	
	—	—	—	—	—	—	—	—	
ICSR2	—	POE6F	POE5F	POE4F	—	—	—	PIE	MMT
	—	—	POE6M1	POE6M0	POE5M1	POE5M0	POE4M1	POE4M0	
PGDR	—	—	—	—	PG3DR	PG2DR	PG1DR	PG0DR	Port G
CMSTR	—	—	—	—	—	—	—	—	CMT
	—	—	—	—	—	—	STR1	STR0	
CMCSR_0	—	—	—	—	—	—	—	—	
	CMF	CMIE	—	—	—	—	CKS1	CKS0	
CMCNT_0									
CMCOR_0									
CMCSR_1	—	—	—	—	—	—	—	—	
	CMF	CMIE	—	—	—	—	CKS1	CKS0	
CMCNT_1									
CMCOR_1									
ADDR0	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D
	AD1	AD0	—	—	—	—	—	—	

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
ADDR1	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D
	AD1	AD0	—	—	—	—	—	—	
ADDR2	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR3	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR4	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR5	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR6	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR7	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR8	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR9	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR11	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR12	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR13	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR14	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR15	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR16	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR17	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR18	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDR19	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
ADCSR_0	ADF	ADIE	ADM1	ADM0	—	CH2	CH1	CH0	A/D
ADCSR_1	ADF	ADIE	ADM1	ADM0	—	CH2	CH1	CH0	
ADCSR_2	ADF	ADIE	ADM1	ADM0	—	CH2	CH1	CH0	
ADCR_0	TRGE	CKS1	CKS0	ADST	ADCS	—	—	—	
ADCR_1	TRGE	CKS1	CKS0	ADST	ADCS	—	—	—	
ADCR_2	TRGE	CKS1	CKS0	ADST	ADCS	—	—	—	
TCSR	OVF	WT/IT	TME	—	—	CKS2	CKS1	CKS0	WDT
TCNT									
RSTCSR	WOVF	RSTE	RSTS	—	—	—	—	—	
SBYCR	SSBY	HIZ	—	—	—	—	—	IRQEL	Power-down modes
SYSCR	—	—	—	—	—	—	—	RAME	
MSTCR1	—	—	—	—	MSTP27	MSTP26	—	—	
	—	—	—	—	MSTP19	MSTP18	—	—	
MSTCR2	—	MSTP14	MSTP13	MSTP12	—	—	—	—	
	—	MSTP6	MSTP5	MSTP4	—	—	—	—	
—	—	—	—	—	—	—	—	—	—
BCR1	—	MMTRWE	MTURWE	—	—	—	—	—	BSC
	—	—	—	—	—	—	—	A0SZ	
BCR2	—	—	—	—	—	—	IW01	IW00	
	—	—	—	CW0	—	—	—	SW0	
WCR1	—	—	—	—	—	—	—	—	
	—	—	—	—	W03	W02	W01	W00	
ADTSR	—	—	TRG2S1	TRG2S0	TRG1S1	TRG1S0	TRG0S1	TRG0S0	A/D
MMT_TMDR	—	CKS2	CKS1	CKS0	OLSN	OLSP	MD1	MD0	MMT
TCNR	TTGE	CST	RPRO	—	—	—	TGIEN	TGIEM	
MMT_TSR	TCFD	—	—	—	—	—	TGFN	TGFM	
MMT_TCNT									
TPDR									
TPBR									
MMT_TDDR									
TBRU_B									
TGRUU									

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
TGRU									MMT
TGRUD									
TDCNT0									
TDCNT1									
TBRU_F									
TBRV_B									
TGRVU									
TGRV									
TGRVD									
TDCNT2									
TDCNT3									
TBRV_F									
TBRW_B									
TGRWU									
TGRW									
TGRWD									
TDCNT4									
TDCNT5									
TBRW_F									

19.3 Register States in Each Operating Mode

Register Abbreviation	Power-On Reset	Manual Reset	Hardware Standby	Software Standby	Module Standby	Sleep	Module
SMR_2	Initialized	Held	Initialized	Initialized	Initialized	Held	SCI (channel 2)
BRR_2	Initialized	Held	Initialized	Initialized	Initialized	Held	
SCR_2	Initialized	Held	Initialized	Initialized	Initialized	Held	
TDR_2	Initialized	Held	Initialized	Initialized	Initialized	Held	
SSR_2	Initialized	Held	Initialized	Initialized	Initialized	Held	
RDR_2	Initialized	Held	Initialized	Initialized	Initialized	Held	
SDCR_2	Initialized	Held	Initialized	Initialized	Initialized	Held	
SMR_3	Initialized	Held	Initialized	Initialized	Initialized	Held	SCI (channel 3)
BRR_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
SCR_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
TDR_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
SSR_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
RDR_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
SDCR_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
TCR_3	Initialized	Held	Initialized	Initialized	Initialized	Held	MTU (channels 3 and 4)
TCR_4	Initialized	Held	Initialized	Initialized	Initialized	Held	
TMDR_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
TMDR_4	Initialized	Held	Initialized	Initialized	Initialized	Held	
TIORH_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
TIORL_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
TIORH_4	Initialized	Held	Initialized	Initialized	Initialized	Held	
TIORL_4	Initialized	Held	Initialized	Initialized	Initialized	Held	
TIER_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
TIER_4	Initialized	Held	Initialized	Initialized	Initialized	Held	
TOER	Initialized	Held	Initialized	Initialized	Initialized	Held	
TOCR	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGCR	Initialized	Held	Initialized	Initialized	Initialized	Held	
TCNT_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
TCNT_4	Initialized	Held	Initialized	Initialized	Initialized	Held	
TCDR	Initialized	Held	Initialized	Initialized	Initialized	Held	
TDDR	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRA_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRB_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRA_4	Initialized	Held	Initialized	Initialized	Initialized	Held	

Register Abbreviation	Power-On Reset	Manual Reset	Hardware Standby	Software Standby	Module Standby	Sleep	Module
TGRB_4	Initialized	Held	Initialized	Initialized	Initialized	Held	MTU (channels 3 and 4)
TCNTS	Initialized	Held	Initialized	Initialized	Initialized	Held	
TCBR	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRC_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRD_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRC_4	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRD_4	Initialized	Held	Initialized	Initialized	Initialized	Held	
TSR_3	Initialized	Held	Initialized	Initialized	Initialized	Held	
TSR_4	Initialized	Held	Initialized	Initialized	Initialized	Held	
TSTR	Initialized	Held	Initialized	Initialized	Initialized	Held	MTU (common)
TSYR	Initialized	Held	Initialized	Initialized	Initialized	Held	
TCR_0	Initialized	Held	Initialized	Initialized	Initialized	Held	MTU (channel 0)
TMDR_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
TIORH_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
TIORL_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
TIER_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
TSR_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
TCNT_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRA_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRB_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRC_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRD_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
TCR_1	Initialized	Held	Initialized	Initialized	Initialized	Held	MTU (channel 1)
TMDR_1	Initialized	Held	Initialized	Initialized	Initialized	Held	
TIOR_1	Initialized	Held	Initialized	Initialized	Initialized	Held	
TIER_1	Initialized	Held	Initialized	Initialized	Initialized	Held	
TSR_1	Initialized	Held	Initialized	Initialized	Initialized	Held	
TCNT_1	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRA_1	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRB_1	Initialized	Held	Initialized	Initialized	Initialized	Held	
TCR_2	Initialized	Held	Initialized	Initialized	Initialized	Held	MTU (channel 2)
TMDR_2	Initialized	Held	Initialized	Initialized	Initialized	Held	
TIOR_2	Initialized	Held	Initialized	Initialized	Initialized	Held	
TIER_2	Initialized	Held	Initialized	Initialized	Initialized	Held	
TSR_2	Initialized	Held	Initialized	Initialized	Initialized	Held	

Register Abbreviation	Power-On Reset	Manual Reset	Hardware Standby	Software Standby	Module Standby	Sleep	Module
TCNT_2	Initialized	Held	Initialized	Initialized	Initialized	Held	MTU (channel 2)
TGRA_2	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRB_2	Initialized	Held	Initialized	Initialized	Initialized	Held	
IPRA	Initialized	Initialized	Initialized	Held	—	Held	INTC
IPRD	Initialized	Initialized	Initialized	Held	—	Held	
IPRE	Initialized	Initialized	Initialized	Held	—	Held	
IPRF	Initialized	Initialized	Initialized	Held	—	Held	
IPRG	Initialized	Initialized	Initialized	Held	—	Held	
IPRH	Initialized	Initialized	Initialized	Held	—	Held	
ICR1	Initialized	Initialized	Initialized	Held	—	Held	
ISR	Initialized	Initialized	Initialized	Held	—	Held	
IPRI	Initialized	Initialized	Initialized	Held	—	Held	
IPRJ	Initialized	Initialized	Initialized	Held	—	Held	
IPRK	Initialized	Initialized	Initialized	Held	—	Held	
ICR2	Initialized	Initialized	Initialized	Held	—	Held	
PADRL	Initialized	Held	Initialized	Held	—	Held	Port A
PAIORL	Initialized	Held	Initialized	Held	—	Held	
PACRL3	Initialized	Held	Initialized	Held	—	Held	
PACRL1	Initialized	Held	Initialized	Held	—	Held	
PACRL2	Initialized	Held	Initialized	Held	—	Held	
PBDR	Initialized	Held	Initialized	Held	—	Held	Port B
PBIOR	Initialized	Held	Initialized	Held	—	Held	
PBCR1	Initialized	Held	Initialized	Held	—	Held	
PBCR2	Initialized	Held	Initialized	Held	—	Held	
PDDRL	Initialized	Held	Initialized	Held	—	Held	Port D
PDIORL	Initialized	Held	Initialized	Held	—	Held	
PDCRL1	Initialized	Held	Initialized	Held	—	Held	
PDCRL2	Initialized	Held	Initialized	Held	—	Held	
PEDRL	Initialized	Held	Initialized	Held	—	Held	Port E
PFDR	Held	Held	Held	Held	—	Held	Port F
PEIORL	Initialized	Held	Initialized	Held	—	Held	Port E
PEIORH	Initialized	Held	Initialized	Held	—	Held	
PECRL1	Initialized	Held	Initialized	Held	—	Held	
PECRL2	Initialized	Held	Initialized	Held	—	Held	
PECRH	Initialized	Held	Initialized	Held	—	Held	

Register Abbreviation	Power-On Reset	Manual Reset	Hardware Standby	Software Standby	Module Standby	Sleep	Module
PEDRH	Initialized	Held	Initialized	Held	—	Held	Port E
ICSR1	Initialized	Held	Initialized	Held	Held	Held	MTU
OCSR	Initialized	Held	Initialized	Held	Held	Held	
ICSR2	Initialized	Held	Initialized	Held	Held	Held	MMT
PGDR	Held	Held	Held	Held	—	Held	Port G
CMSTR	Initialized	Held	Initialized	Initialized	Initialized	Held	CMT
CMCSR_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
CMCNT_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
CMCOR_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
CMCSR_1	Initialized	Held	Initialized	Initialized	Initialized	Held	
CMCNT_1	Initialized	Held	Initialized	Initialized	Initialized	Held	
CMCOR_1	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR0	Initialized	Held	Initialized	Initialized	Initialized	Held	A/D
ADDR1	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR2	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR3	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR4	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR5	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR6	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR7	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR8	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR9	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR10	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR11	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR12	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR13	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR14	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR15	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR16	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR17	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR18	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADDR19	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADCSR_0	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADCSR_1	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADCSR_2	Initialized	Held	Initialized	Initialized	Initialized	Held	

Register Abbreviation	Power-On Reset	Manual Reset	Hardware Standby	Software Standby	Module Standby	Sleep	Module
ADCR_0	Initialized	Held	Initialized	Initialized	Initialized	Held	A/D
ADCR_1	Initialized	Held	Initialized	Initialized	Initialized	Held	
ADCR_2	Initialized	Held	Initialized	Initialized	Initialized	Held	
TCSR	Initialized	Initialized	Initialized	Initialized/ held*[1]	—	Held	WDT
TCNT	Initialized	Initialized	Initialized	Initialized	—	Held	
RSTCSR	Initialized/ held*[2]	Held	Initialized	Initialized	—	Held	
SBYCR	Initialized	Initialized	Initialized	Held	—	Held	Power-down modes
SYSCR	Initialized	Held	Initialized	Held	—	Held	
MSTCR1	Initialized	Held	Initialized	Held	—	Held	
MSTCR2	Initialized	Held	Initialized	Held	—	Held	
BCR1	Initialized	Held	Initialized	Held	—	Held	BSC
BCR2	Initialized	Held	Initialized	Held	—	Held	
WCR1	Initialized	Held	Initialized	Held	—	Held	
ADTSR	Initialized	Held	Initialized	Held	—	Held	A/D
MMT_TMDR	Initialized	Held	Initialized	Initialized	Initialized	Held	MMT
TCNR	Initialized	Held	Initialized	Initialized	Initialized	Held	
MMT_TSR	Initialized	Held	Initialized	Initialized	Initialized	Held	
MMT_TCNT	Initialized	Held	Initialized	Initialized	Initialized	Held	
TPDR	Initialized	Held	Initialized	Initialized	Initialized	Held	
TPBR	Initialized	Held	Initialized	Initialized	Initialized	Held	
MMT_TDDR	Initialized	Held	Initialized	Initialized	Initialized	Held	
TBRU_B	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRUU	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRU	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRUD	Initialized	Held	Initialized	Initialized	Initialized	Held	
TDCNT0	Initialized	Held	Initialized	Initialized	Initialized	Held	
TDCNT1	Initialized	Held	Initialized	Initialized	Initialized	Held	
TBRU_F	Initialized	Held	Initialized	Initialized	Initialized	Held	
TBRV_B	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRVU	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRV	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRVD	Initialized	Held	Initialized	Initialized	Initialized	Held	
TDCNT2	Initialized	Held	Initialized	Initialized	Initialized	Held	
TDCNT3	Initialized	Held	Initialized	Initialized	Initialized	Held	

Register Abbreviation	Power-On Reset	Manual Reset	Hardware Standby	Software Standby	Module Standby	Sleep	Module
TBRV_F	Initialized	Held	Initialized	Initialized	Initialized	Held	MMT
TBRW_B	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRWU	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRW	Initialized	Held	Initialized	Initialized	Initialized	Held	
TGRWD	Initialized	Held	Initialized	Initialized	Initialized	Held	
TDCNT4	Initialized	Held	Initialized	Initialized	Initialized	Held	
TDCNT5	Initialized	Held	Initialized	Initialized	Initialized	Held	
TBRW_F	Initialized	Held	Initialized	Initialized	Initialized	Held	

Notes: 1. Bits 7 to 5 (OVF, WT/IT, and TME) in the TCSR register are initialized. The values of bits 2 to 0 (CKS2, CKS1, and CKS0) are retained.

2. The RSTC SR register value is retained on a power-on reset due to a watchdog timer overflow.

Section 20 Electrical Characteristics

20.1 Absolute Maximum Ratings

Table 20.1 shows the absolute maximum ratings.

Table 20.1 Absolute Maximum Ratings

Item		Symbol	Rating	Unit
Power supply voltage		V_{CC}	–0.3 to +7.0	V
Input voltage	EXTAL pin	Vin	–0.3 to V_{CC} +0.3	V
	All pins other than analog input and EXTAL pins	Vin	–0.3 to V_{CC} +0.3	V
Analog power supply voltage		AV_{CC}	–0.3 to +7.0	V
Analog input voltage		V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature (except programming or erasing flash memory)	Standard product*	T_{opr}	–20 to +75	°C
	Wide temperature-range product*		–40 to +85	
Storage temperature		T_{stg}	–55 to +125	°C

[Operating precautions]

Operating the LSI in excess of the absolute maximum ratings may result in permanent damage.

Note: * For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

20.2 DC Characteristics

Table 20.2 DC Characteristics (1)

Conditions: V_{CC} = 4.0 to 5.5 V, AV_{CC} = 4.0 to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*), T_a = –40°C to +85°C (wide temperature-range product*)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Conditions
Input high-level voltage (except Schmitt trigger input pin)	$\overline{RES}$, $\overline{MRES}$, $\overline{HSTBY}$, NMI, FWP, MD3 to MD0	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	EXTAL		V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	A/D port		2.2	—	AV_{CC} + 0.3	V	
	Other input pins		2.2	—	V_{CC} + 0.3	V	
Input low-level voltage (except Schmitt trigger input pin)	$\overline{RES}$, $\overline{MRES}$, $\overline{HSTBY}$, NMI, FWP, MD3 to MD0, EXTAL	V_{IL}	–0.3	—	0.5	V	
	Other input pins		–0.3	—	0.8	V	
Schmitt trigger input voltage	$\overline{IRQ3}$ to $\overline{IRQ0}$, $\overline{POE6}$ to $\overline{POE0}$, TCLKA to TCLKD, TIOC0A to TIOC0D, TIOC1A, TIOC1B, TIOC2A, TIOC2B, TIOC3A to TIOC3D, TIOC4A to TIOC4D	V_{T+} (VH)	V_{CC}–0.5	—	V_{CC} + 0.3	V	
		V_{T-} (VL)	–0.3	—	1.0	V	
		V_{T+}–V_{T-}	0.4	—	—	V	
Input leakage current	$\overline{RES}$, $\overline{MRES}$, NMI, $\overline{HSTBY}$, FWP, MD3 to MD0, $\overline{DBGMD}$	| I_{in} |	—	—	1.0	µA	Vin = 0.5 to V_{CC} –0.5 V
	Ports F, G		—	—	1.0	µA	Vin = 0.5 to AV_{CC} –0.5 V
	Other input pins		—	—	1.0	µA	Vin = 0.5 to V_{CC} –0.5 V

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Conditions
Three-state leakage current (while off)	Ports A, B, D, E	$\lvert I_{tsi} \rvert$	—	—	1.0	µA	Vin = 0.5 to V_{CC} –0.5 V
Output high-level voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low-level voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	PE9, PE11 to PE21		—	—	1.5	V	I_{OL} = 15 mA
Input capacitance	$\overline{RES}$	C_{in}	—	—	80	pF	Vin = 0 V
	NMI		—	—	50	pF	ϕ = 1 MHz
	All other input pins		—	—	20	pF	Ta = 25°C

Note: * For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

Table 20.2 DC Characteristics (2)

Conditions: V_{CC} = 4.0 to 5.5 V, AV_{CC} = 4.0 to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*[1]), T_a = –40°C to +85°C (wide temperature-range product*[1])

HD6437108, HD6437106

Item			Symbol	Min.	Typ.	Max.	Unit	Measurement Conditions
Current consumption*[2]	Normal operation	Clock 1:1	I_{CC}		110	140	mA	ϕ = 40 MHz
		Clock 1:1/2			115	145	mA	ϕ = 50 MHz
	Sleep	Clock 1:1			70	90	mA	ϕ = 40 MHz
		Clock 1:1/2			70	90	mA	ϕ = 50 MHz
	Standby				1	10	µA	$T_a \leq$ 50°C
						50	µA	50°C < T_a
Analog power supply current	During A/D conversion, A/D converter idle state		AI_{CC}		3.0	5.0	mA	—
	During standby					5.0	µA	
RAM standby voltage			V_{RAM}	2.0	—	—	V	V_{CC}

HD6437104

Item			Symbol	Min.	Typ.	Max.	Unit	Measurement Conditions
Current consumption*2	Normal operation	Clock 1:1	I_{CC}		120	150	mA	ϕ = 40 MHz
		Clock 1:1/2			125	155	mA	ϕ = 50 MHz
	Sleep	Clock 1:1			90	110	mA	ϕ = 40 MHz
		Clock 1:1/2			90	110	mA	ϕ = 50 MHz
	Standby				1	10	µA	$T_a \leq 50°C$
						50	µA	$50°C < T_a$
Analog power supply current	During A/D conversion, A/D converter idle state		AI_{CC}		3.0	5.0	mA	—
	During standby					5.0	µA	
RAM standby voltage			V_{RAM}	2.0	—	—	V	V_{CC}

HD6437101

Item			Symbol	Min.	Typ.	Max.	Unit	Measurement Conditions
Current consumption*2	Normal operation	Clock 1:1	I_{CC}		110	130	mA	ϕ = 40 MHz
		Clock 1:1/2			100	120	mA	ϕ = 40 MHz
		Clock 1:1/2			120	140	mA	ϕ = 50 MHz
	Sleep	Clock 1:1			70	90	mA	ϕ = 40 MHz
		Clock 1:1/2			60	80	mA	ϕ = 40 MHz
		Clock 1:1/2			70	90	mA	ϕ = 50 MHz
	Standby				1	10	µA	$T_a \leq 50°C$
						50	µA	$50°C < T_a$
Analog power supply current	During A/D conversion, A/D converter idle state		AI_{CC}		3.0	5.0	mA	—
	During standby					5.0	µA	
RAM standby voltage			V_{RAM}	2.0	—	—	V	V_{CC}

HD6437109, HD6437107

Item			Symbol	Min.	Typ.	Max.	Unit	Measurement Conditions
Current consumption*[2]	Normal operation	Clock 1:1	I_{CC}	—	110	140	mA	ϕ = 40 MHz
		Clock 1:1/2		—	115	145	mA	ϕ = 50 MHz
	Sleep	Clock 1:1		—	70	90	mA	ϕ = 40 MHz
		Clock 1:1/2		—	70	90	mA	ϕ = 50 MHz
	Standby			—	1	10	µA	$T_a \leq 50°C$
				—	—	50	µA	$50°C < T_a$
Analog power supply current	During A/D conversion, A/D converter idle state		AI_{CC}	—	2.0	5.0	mA	—
	During standby			—	—	5.0	µA	
RAM standby voltage			V_{RAM}	2.0	—	—	V	V_{CC}

HD6437105

Item			Symbol	Min.	Typ.	Max.	Unit	Measurement Conditions
Current consumption*[2]	Normal operation	Clock 1:1	I_{CC}	—	120	150	mA	ϕ = 40 MHz
		Clock 1:1/2		—	125	155	mA	ϕ = 50 MHz
	Sleep	Clock 1:1		—	90	110	mA	ϕ = 40 MHz
		Clock 1:1/2		—	90	110	mA	ϕ = 50 MHz
	Standby			—	1	10	µA	$T_a \leq 50°C$
				—	—	50	µA	$50°C < T_a$
Analog power supply current	During A/D conversion, A/D converter idle state		AI_{CC}	—	2.0	5.0	mA	—
	During standby			—	—	5.0	µA	
RAM standby voltage			V_{RAM}	2.0	—	—	V	V_{CC}

[Operating precautions]

When the A/D converter is not used, do not leave the AV_{CC} and AV_{SS} pins open.

Notes: 1. For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

2. The current consumption is measured when V_{IH}min. = V_{CC} – 0.5 V, V_{IL} = 0.5 V, with all output pins unloaded.

Table 20.3 Permitted Output Current Values

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*[1]), T_a = –40°C to +85°C (wide temperature-range product*[1])

Item	Symbol	Min.	Typ.	Max.	Unit
Output low-level permissible current (per pin)	I_{OL}	—	—	2.0*[2]	mA
Output low-level permissible current (total)	ΣI_{OL}	—	—	110	mA
Output high-level permissible current (per pin)	$-I_{OH}$	—	—	2.0	mA
Output high-level permissible current (total)	$\Sigma -I_{OH}$	—	—	25	mA

[Operating precautions]

To assure LSI reliability, do not exceed the output values listed in this table.

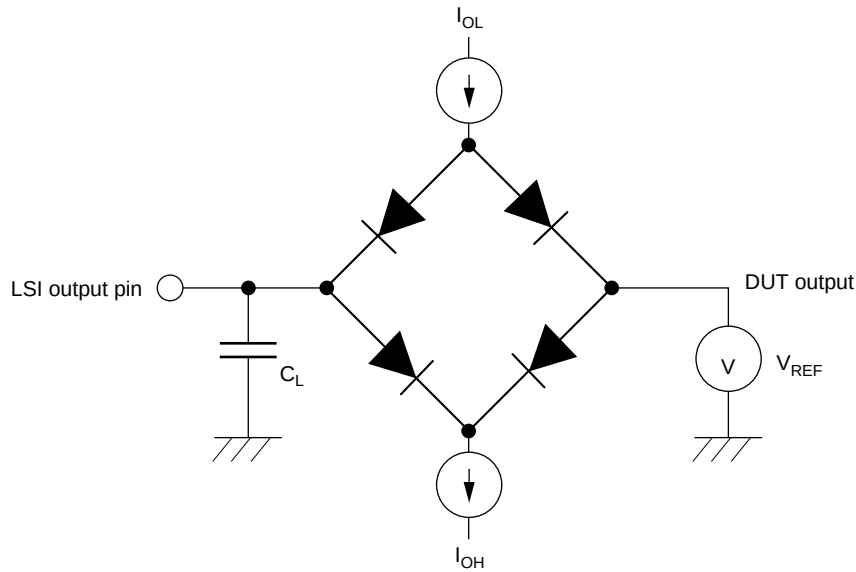
Notes: 1. For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

2. I_{OL}= 15 mA (max.) about the pins PE9 and PE11 to PE21. However, six pins at most are permitted to have simultaneously I_{OL} > 2.0 mA among these pins.

20.3 AC Characteristics

20.3.1 Test Conditions for AC Characteristics

Input reference levels	high level: V_{IH} minimum value, low level: V_{IL} maximum value
Output reference levels	high level: 2.0 V, low level: 0.8 V



CL is a total value that includes the capacitance of measurement equipment, and is set as follows:
30 pF: CK, $\overline{CS0}$, $\overline{BACK}$, $\overline{IRQOUT}$
50 pF: A17 to A0, D7 to D0, $\overline{RD}$, $\overline{WRL}$
30 pF: Port output pins and peripheral module output pins other than the above
It is assumed that I_{OL} = 1.6 mA, I_{OH} = 200 µA in the test conditions.

Figure 20.1 Output Load Circuit

20.3.2 Clock Timing

Table 20.4 shows the clock timing.

Table 20.4 Clock Timing

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*), T_a = –40°C to +85°C (wide temperature-range product*)

Item		Symbol	Min.	Max.	Unit	Figures
Operating frequency	50-MHz operation*	f_{op}	10	50	MHz	Figure 20.2
	40-MHz operation*		10	40		
Clock cycle time	50-MHz operation*	t_{cyc}	20	100	ns	
	40-MHz operation*		25	100		
Clock low-level pulse width		t_{CL}	4	—	ns	
Clock high-level pulse width		t_{CH}	4	—	ns	
Clock rise time		t_{CR}	—	5	ns	
Clock fall time		t_{CF}	—	5	ns	
EXTAL clock input frequency	50-MHz operation*	f_{EX}	4	12.5	MHz	Figure 20.3
	40-MHz operation*		4	10.0		
EXTAL clock input cycle time	50-MHz operation*	t_{EXcyc}	80	250	ns	
	40-MHz operation*		100	250		
EXTAL clock input low-level pulse width	50-MHz operation*	t_{EXL}	35	—	ns	
	40-MHz operation*		45			
EXTAL clock input high-level pulse width	50-MHz operation*	t_{EXH}	35	—	ns	
	40-MHz operation*		45			
EXTAL clock input rise time		t_{EXR}	—	5	ns	
EXTAL clock input fall time		t_{EXF}	—	5	ns	
Reset oscillation settling time		t_{OSC1}	10	—	ms	Figure 20.4
Standby return oscillation settling time		t_{OSC2}	10	—	ms	
Clock cycle time for peripheral modules		t_{pcyc}	25	100	ns	—

Note: * For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

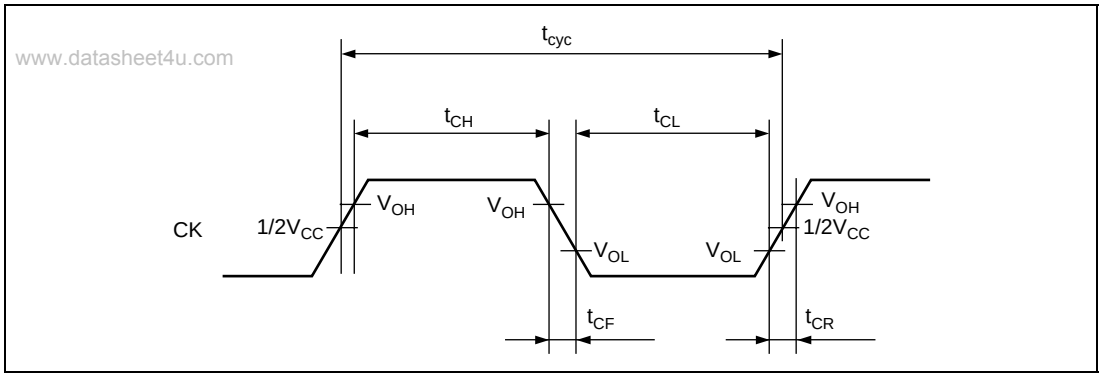


Figure 20.2 System Clock Timing

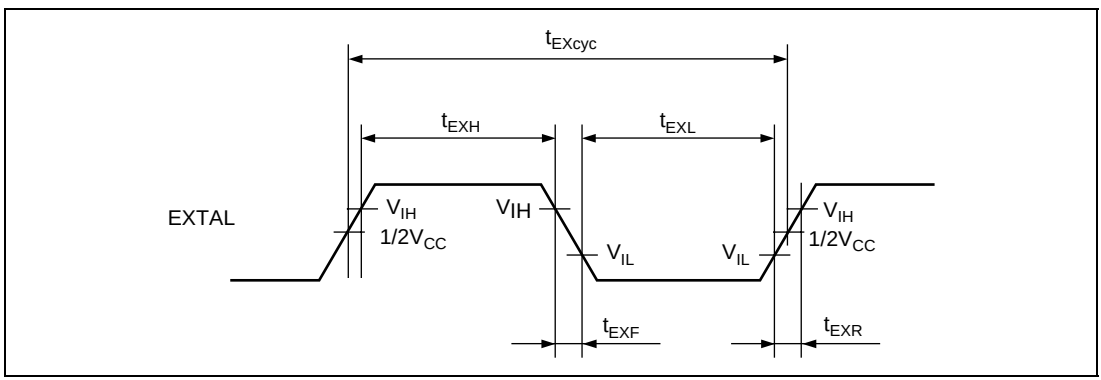


Figure 20.3 EXTAL Clock Input Timing

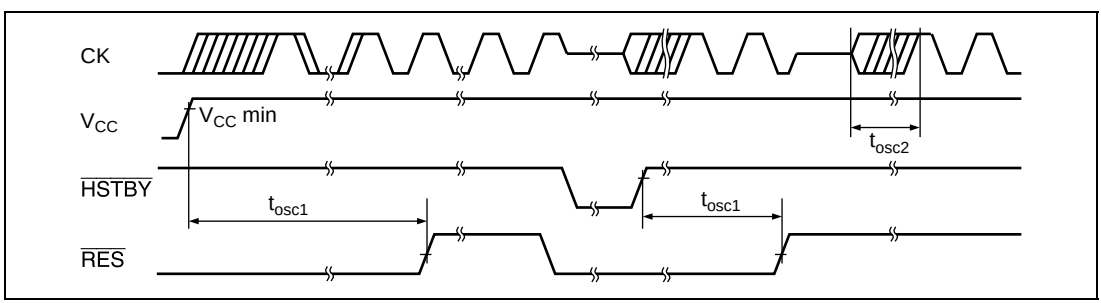


Figure 20.4 Oscillation Settling Time

20.3.3 Control Signal Timing

Table 20.5 shows the control signal timing.

Table 20.5 Control Signal Timing

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*[1]), T_a = –40°C to +85°C (wide temperature-range product*[1])

Item	Symbol	Min.	Max.	Unit	Figures
$\overline{RES}$ rise time, fall time	t_{RESr}, t_{RESf}	—	200	ns	Figure 20.5, Figure 20.6
$\overline{RES}$ pulse width	t_{RESW}	25	—	t_{cyc}	
$\overline{RES}$ setup time	t_{RESS}	25	—	ns	
$\overline{MRES}$ pulse width	t_{MRESW}	25	—	t_{cyc}	
$\overline{MRES}$ setup time	t_{MRESS}	19	—	ns	
MD3 to MD0, FWP setup time	t_{MDS}	20	—	t_{cyc}	
NMI rise time, fall time	t_{NMIr}, t_{NMIIf}	—	200	ns	
NMI setup time	t_{NMIS}	19	—	ns	Figure 20.7
$\overline{IRQ3}$ to $\overline{IRQ0}$ setup time*[2] (edge detection)	t_{IRQES}	19	—	ns	
$\overline{IRQ3}$ to $\overline{IRQ0}$ setup time*[2] (level detection)	t_{IRQLS}	19	—	ns	
NMI hold time	t_{NMIH}	19	—	ns	
$\overline{IRQ3}$ to $\overline{IRQ0}$ hold time	t_{IRQEH}	19	—	ns	
$\overline{IRQOUT}$ output delay time	t_{IRQOD}	—	100	ns	Figure 20.8
Bus request setup time	t_{BRQS}	19	—	ns	Figure 20.9
Bus acknowledge delay time 1	t_{BACKD1}	—	30	ns	
Bus acknowledge delay time 2	t_{BACKD2}	—	30	ns	
Bus three-state delay time	t_{BZD}	—	30	ns	

Notes: 1. For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

2. The $\overline{RES}$, $\overline{MRES}$, NMI, $\overline{BREQ}$, and $\overline{IRQ3}$ to $\overline{IRQ0}$ signals are asynchronous inputs, but when the setup times shown here are observed, the signals are considered to have been changed at clock rise ($\overline{RES}$, $\overline{MRES}$, and $\overline{BREQ}$) or fall (NMI and $\overline{IRQ3}$ to $\overline{IRQ0}$). If the setup times are not observed, the recognition of these signals may be delayed until the next clock rise or fall.

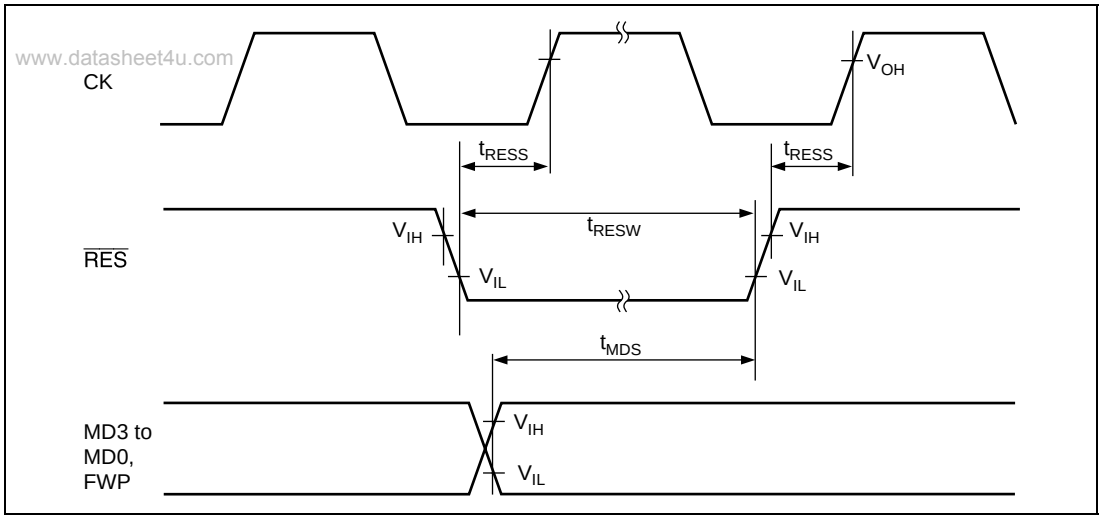


Figure 20.5 Reset Input Timing

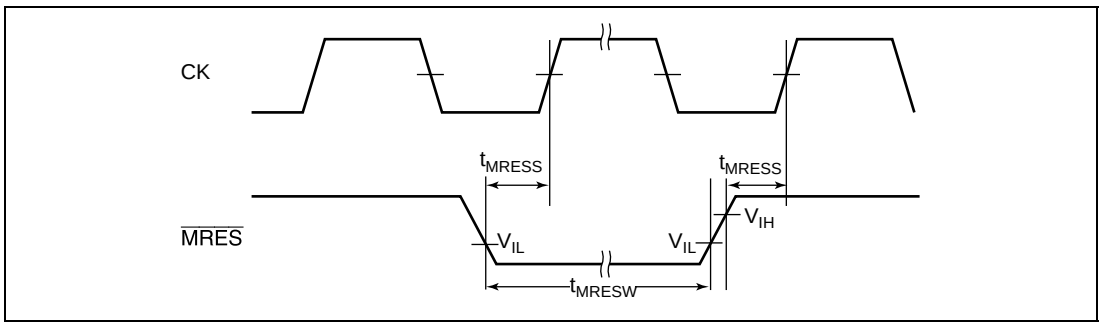


Figure 20.6 Reset Input Timing

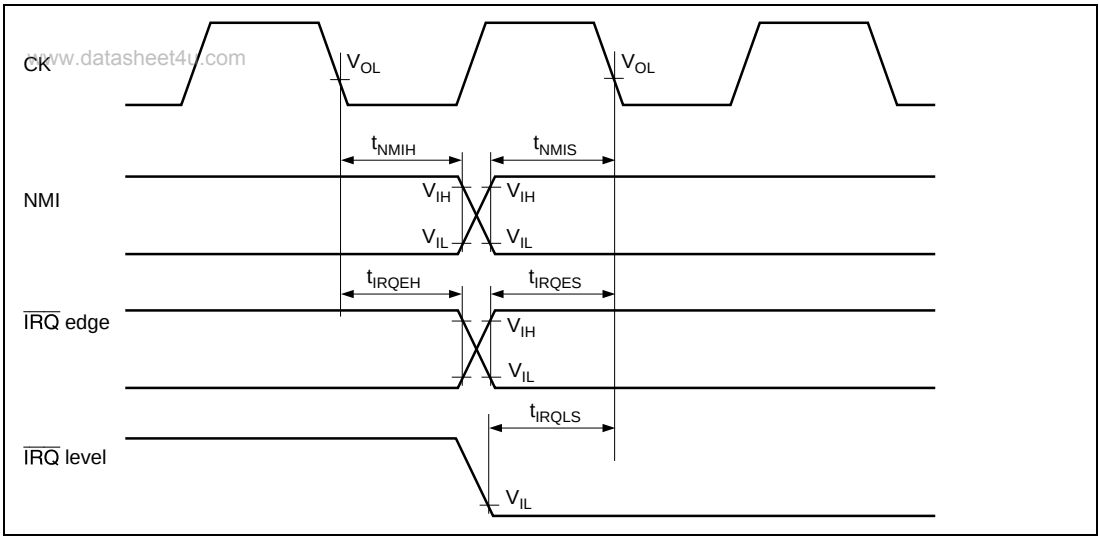


Figure 20.7 Interrupt Signal Input Timing

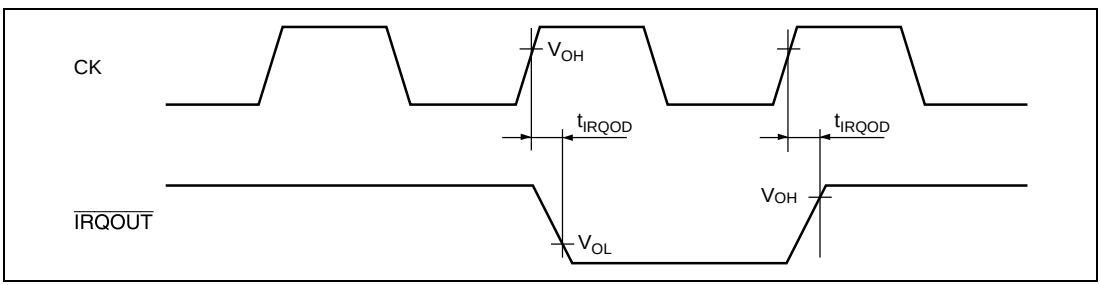


Figure 20.8 Interrupt Signal Output Timing

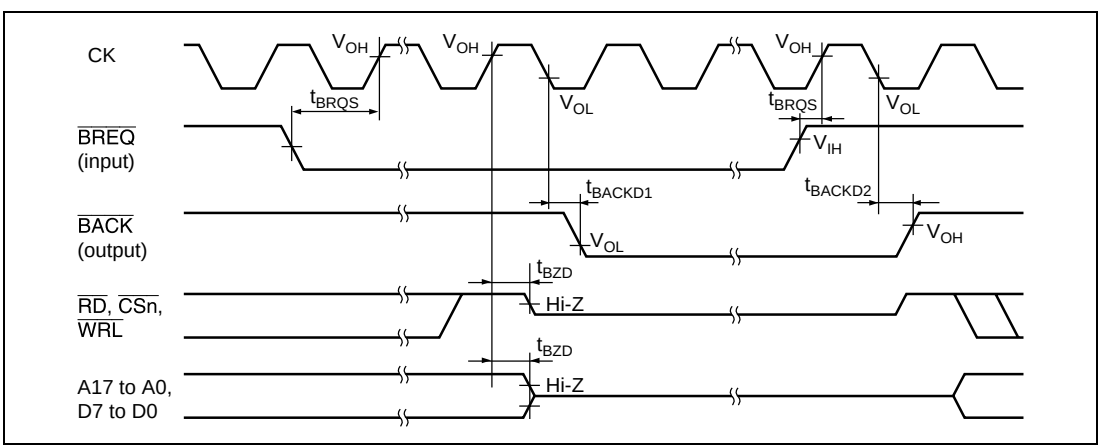


Figure 20.9 Bus Release Timing

20.3.4 Bus Timing

Table 20.6 shows the bus timing.

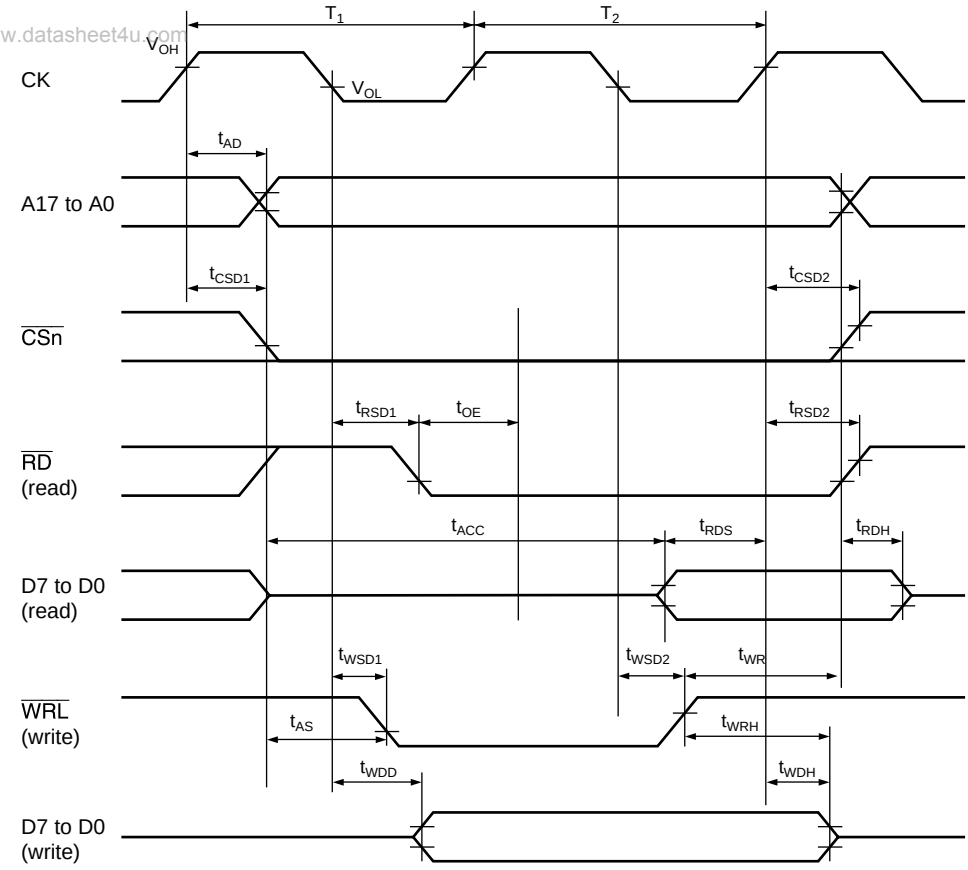
Table 20.6 Bus Timing

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*[1]), T_a = –40°C to +85°C (wide temperature-range product*[1])

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Address delay time	t_{AD}	—	22	30	ns	Figure 20.10, Figure 20.11
CS delay time 1	t_{CSD1}	—	22	35	ns	
CS delay time 2	t_{CSD2}	—	15	35	ns	
Read strobe delay time 1	t_{RSD1}	—	20	35	ns	
Read strobe delay time 2	t_{RSD2}	—	15	35	ns	
Read data setup time	t_{RDS}	15	—	—	ns	
Read data hold time	t_{RDH}	0	—	—	ns	
Write strobe delay time 1	t_{WSD1}	—	20	30	ns	
Write strobe delay time 2	t_{WSD2}	—	15	30	ns	
Write data delay time	t_{WDD}	—	—	30	ns	
Write data hold time	t_{WDH}	0	—	—	ns	
WAIT setup time	t_{WTS}	15	—	—	ns	Figure 20.12
WAIT hold time	t_{WTH}	0	—	—	ns	
Read data access time	t_{ACC}	$t_{CYC} \times (2 + n) - 35$*[2]	—	—	ns	Figure 20.10, Figure 20.11
Access time from read strobe	t_{OE}	$t_{CYC} \times (1.5 + n) - 33$*[2]	—	—	ns	
Write address setup time	t_{AS}	0	—	—	ns	
Write address hold time	t_{WR}	5	—	—	ns	
Write data hold time	t_{WRH}	0	—	—	ns	

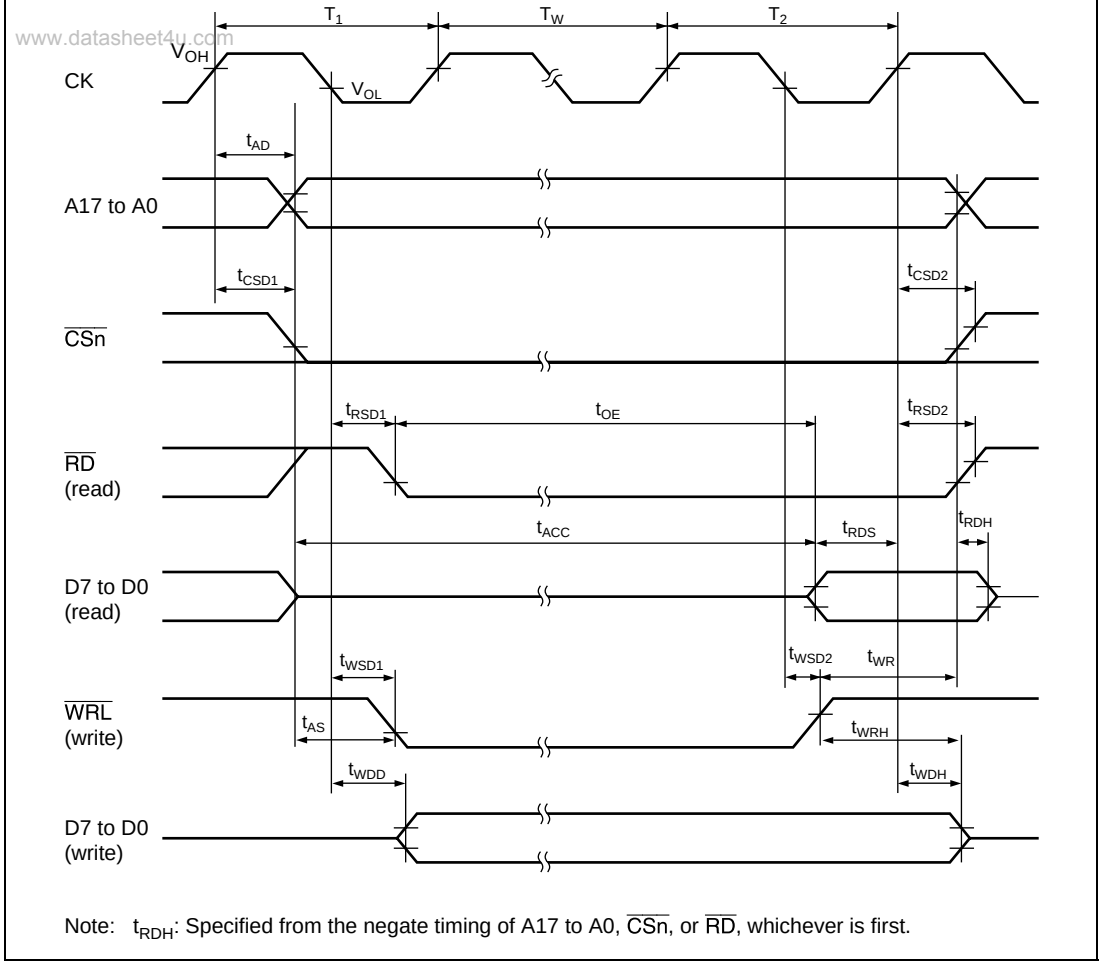
Notes: 1. For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

2. n is the number of wait cycles.



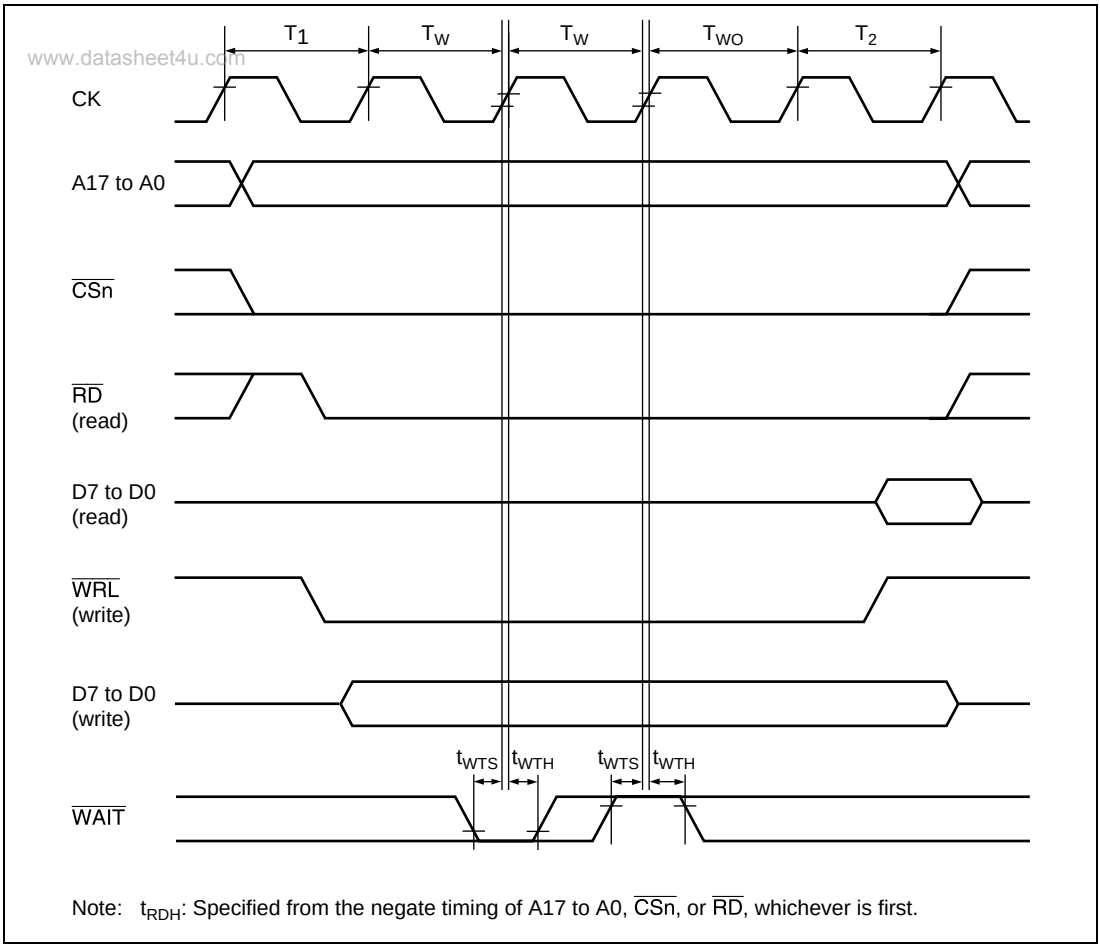
Note: t_{RDH}: Specified from the negate timing of A17 to A0, $\overline{CSn}$, or $\overline{RD}$, whichever is first.

Figure 20.10 Basic Cycle (No Waits)



Note: t_{RDH}: Specified from the negate timing of A17 to A0, $\overline{CSn}$, or $\overline{RD}$, whichever is first.

Figure 20.11 Basic Cycle (One Software Wait)



Note: t_{RDH}: Specified from the negate timing of A17 to A0, $\overline{CSn}$, or $\overline{RD}$, whichever is first.

Figure 20.12 Basic Cycle (Two Software Waits + Waits by WAIT Signal)

20.3.5 Multifunction Timer Pulse Unit (MTU) Timing

Table 20.7 shows the multifunction timer pulse unit timing.

Table 20.7 Multifunction Timer Pulse Unit (MTU) Timing

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*), T_a = –40°C to +85°C (wide temperature-range product*)

Item	Symbol	Min.	Max.	Unit	Figures
Output compare output delay time	t_{TOCD}	—	100	ns	Figure 20.13
Input capture input setup time	t_{TICS}	19	—	ns	
Timer input setup time	t_{TCKS}	35	—	ns	Figure 20.14
Timer clock pulse width (single edge specified)	$t_{TCKWH/L}$	1.5	—	t_{pcyc}	
Timer clock pulse width (both edges specified)	$t_{TCKWH/L}$	2.5	—	t_{pcyc}	
Timer clock pulse width (phase count mode)	$t_{TCKWH/L}$	2.5	—	t_{pcyc}	

Note: * For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

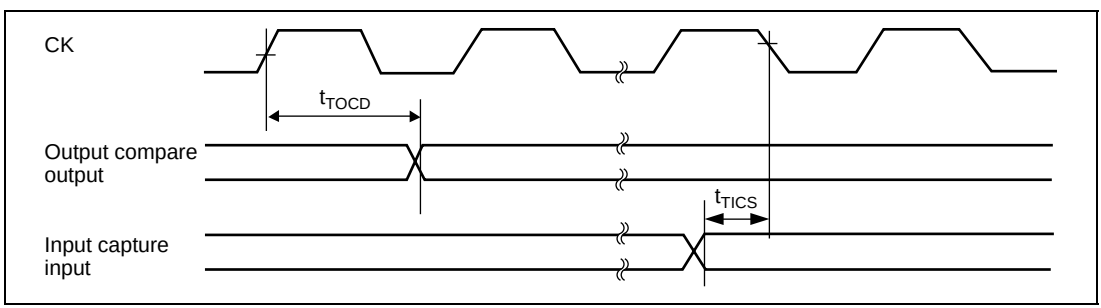


Figure 20.13 MTU Input/Output Timing

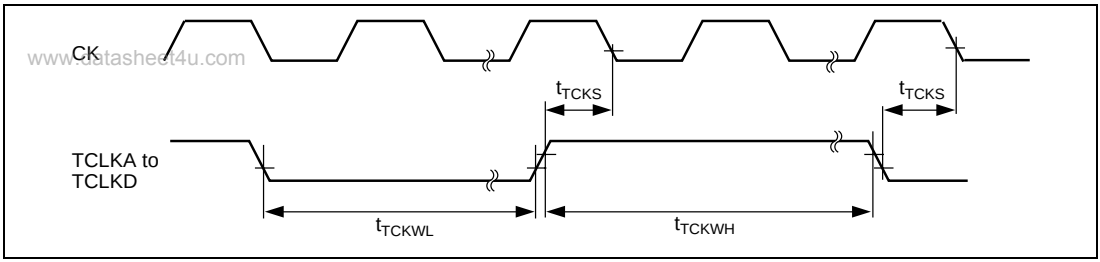


Figure 20.14 MTU Clock Input Timing

20.3.6 I/O Port Timing

Table 20.8 shows the I/O port timing.

Table 20.8 I/O Port Timing

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*), T_a = –40°C to +85°C (wide temperature-range product*)

Item	Symbol	Min.	Max.	Unit	Figure
Port output data delay time	t_{PWD}	—	100	ns	Figure 20.15
Port input hold time	t_{PRH}	19	—	ns	
Port input setup time	t_{PRS}	19	—	ns	

[Operating precautions]

The port input signals are asynchronous. They are, however, considered to have been changed at CK clock falling edge with two-state intervals shown in figure 20.15. If the setup times shown here are not observed, recognition may be delayed until the clock falling two states after that timing.

Note: * For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

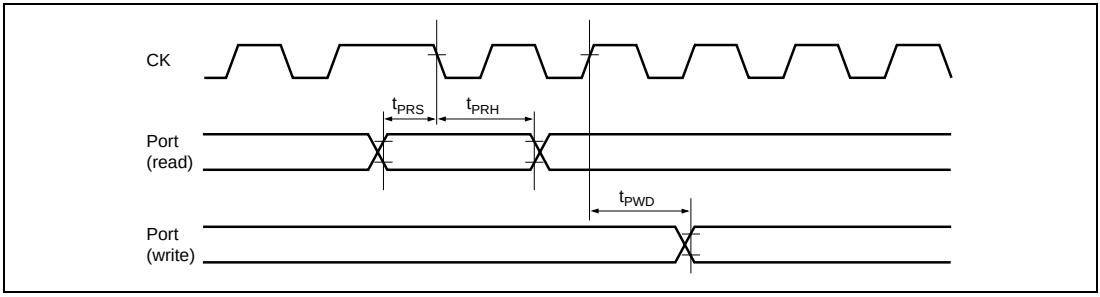


Figure 20.15 I/O Port Input/Output Timing

20.3.7 Watchdog Timer (WDT) Timing

Table 20.9 shows the watchdog timer timing.

Table 20.9 Watchdog Timer (WDT) Timing

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*), T_a = –40°C to +85°C (wide temperature-range product*)

Item	Symbol	Min.	Max.	Unit	Figure
$\overline{\text{WDTOVF}}$ delay time	t_{WOVD}	—	100	ns	Figure 20.16

Note: * For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

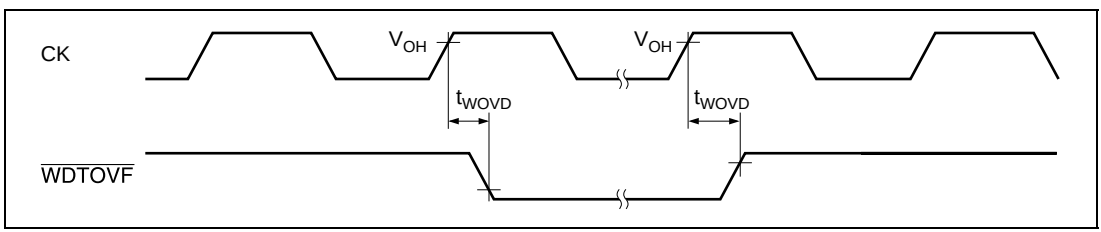


Figure 20.16 Watchdog Timer Timing

20.3.8 Serial Communication Interface (SCI) Timing

Table 20.10 shows the serial communication interface timing.

Table 20.10 Serial Communication Interface (SCI) Timing

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*), T_a = –40°C to +85°C (wide temperature-range product*)

Item		Symbol	Min.	Max.	Unit	Figures
Input clock cycle (asynchronous)		t_{scyc}	4	—	t_{pcyc}	Figure 20.17
Input clock cycle (clocked synchronous)		t_{scyc}	6	—	t_{pcyc}	
Input clock pulse width		t_{sckw}	0.4	0.6	t_{scyc}	
Input clock rise time		t_{sckr}	—	1.5	t_{pcyc}	
Input clock fall time		t_{sckf}	—	1.5	t_{pcyc}	
Transmit data delay time	Asynchronous	t_{TxD}	—	100	ns	Figure 20.18
Receive data setup time		t_{RxS}	100	—	ns	
Receive data hold time		t_{RxH}	100	—	ns	
Transmit data delay time	Clocked synchronous	t_{TxD}	—	t_{spcyc} + 70	ns	
Receive data setup time	(SCK input)	t_{RxS}	t_{pcyc} + 25	—	ns	
Receive data hold time		t_{RxH}	t_{pcyc} + 25	—	ns	
Transmit data delay time	Clocked synchronous	t_{TxD}	—	65	ns	
Receive data setup time	(SCK output)	t_{RxS}	0.5 t_{pcyc} + 50	—	ns	
Receive data hold time		t_{RxH}	1.5 t_{pcyc}	—	ns	

[Operating precautions]

The inputs and outputs are asynchronous in asynchronous mode, but as shown in figure 20.18, the receive data is considered to have been changed at CK clock rise (two-clock intervals). The transmit signals change with a reference of CK clock rise (two-clock intervals).

Note: t_{pcyc} (ns) = 1/(Pϕ (MHz) supplied to the module)

* For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

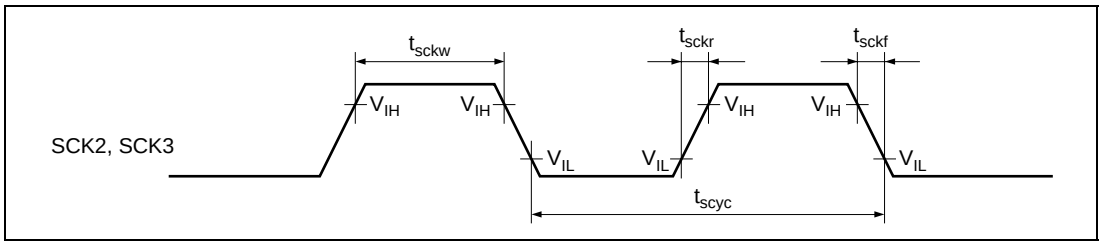


Figure 20.17 Input Clock Timing

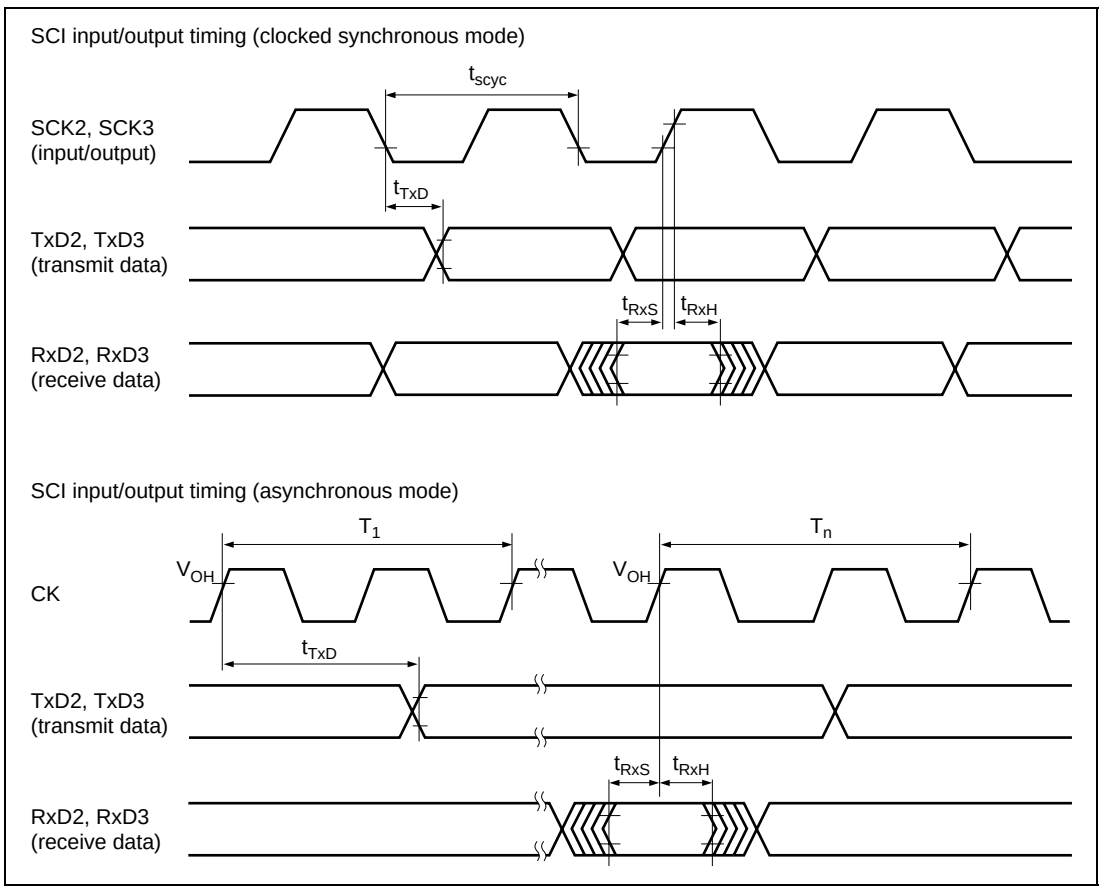


Figure 20.18 SCI Input/Output Timing

20.3.9 Motor Management Timer (MMT) Timing

Table 20.11 Motor Management Timer (MMT) Timing

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*), T_a = –40°C to +85°C (wide temperature-range product*)

Item	Symbol	Min.	Max.	Unit	Figure
MMT output delay time	t_{MTOD}	—	100	ns	Figure 20.19
PCI input setup time	t_{PCIS}	35	—	ns	
PCI input pulse time	t_{PCIW}	1.5	—	t_{pcyc}	

Note: * For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

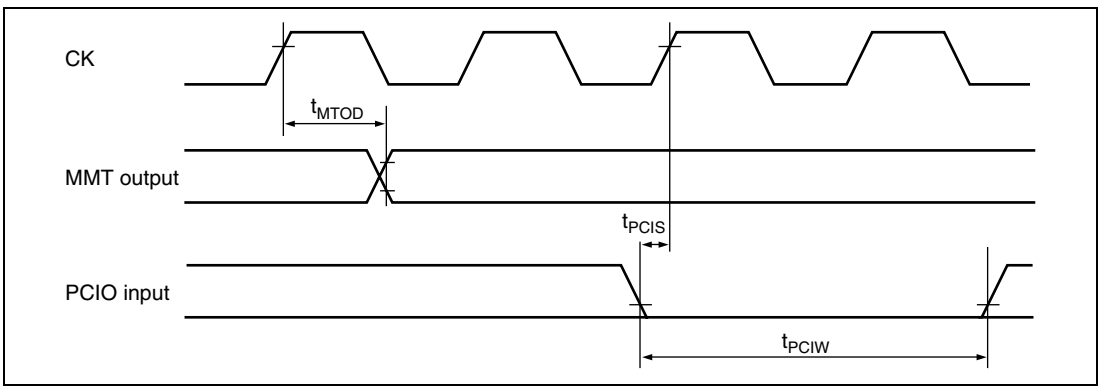


Figure 20.19 MMT Input/Output Timing

20.3.10 Output Enable (POE) Timing

Table 20.12 Output Enable (POE) Timing

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*), T_a = –40°C to +85°C (wide temperature-range product*)

Item	Symbol	Min.	Max.	Unit	Figure
POE input setup time	t_{POES}	100	—	ns	Figure 20.20
POE input pulse width	t_{POEW}	1.5	—	t_{pcyc}	

Note: * For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

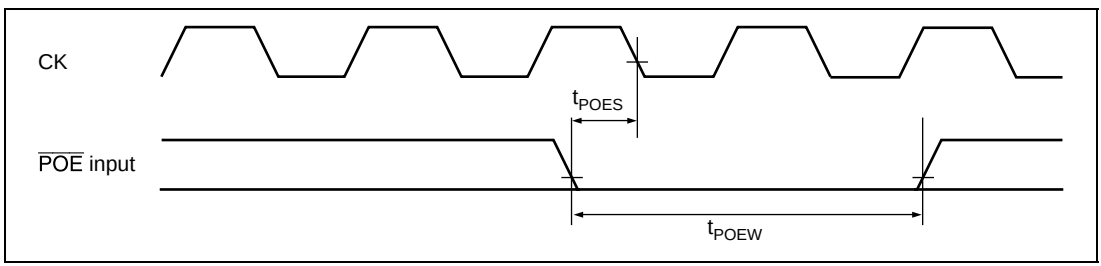


Figure 20.20 POE Input/Output Timing

20.3.11 A/D Converter Timing

Table 20.13 shows the A/D converter timing.

Table 20.13 A/D Converter Timing

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*), T_a = –40°C to +85°C (wide temperature-range product*)

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
External trigger input start delay time	t_{TRGS}	50	—	—	ns	Figure 20.22

Note: * For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

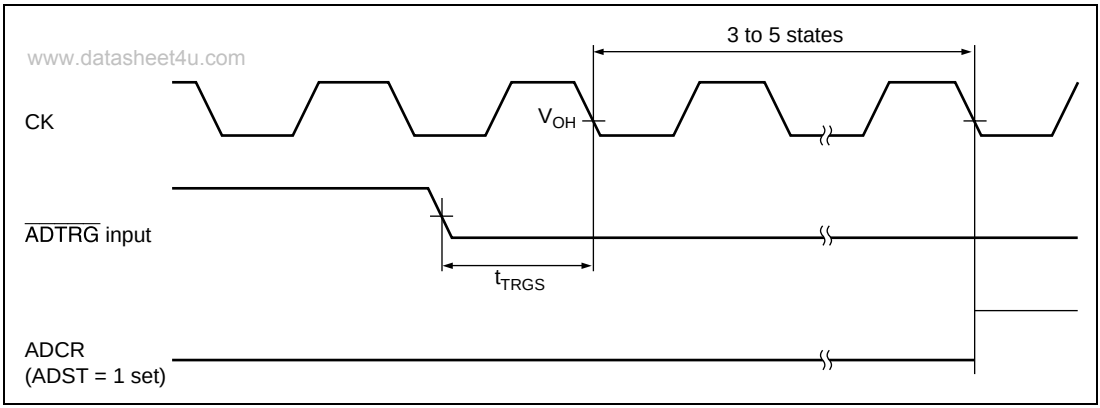


Figure 20.21 External Trigger Input Timing

20.4 A/D Converter Characteristics

Table 20.14 shows the A/D converter characteristics.

Table 20.14 A/D Converter Characteristics

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (standard product*[3]), T_a = –40°C to +85°C (wide temperature-range product*[3])

Item	Min.	Typ.	Max.	Unit
Resolution	10	10	10	bit
A/D conversion time	—	—	6.7*[1]/5.4*[2]	µs
Analog input capacitance	—	—	20	pF
Permitted analog signal source impedance	—	—	3*[1]/1*[2]	kΩ
Nonlinearlity error (Value provided for reference purposes.)	—	—	±3.0*[1]/ ±5.0*[2]	LSB
Offset error (Value provided for reference purposes.)	—	—	±3.0*[1]/ ±5.0*[2]	LSB
Full-scale error (Value provided for reference purposes.)	—	—	±3.0*[1]/ ±5.0*[2]	LSB
Quantization error	—	—	±0.5	LSB
Absolute error	—	—	±4.0*[1]/ ±6.0*[2]	LSB

Notes: 1. Value when (CKS1, CKS0) = (11) and t_{pcyc} = 50 ns
2. Value when (CKS1, CKS0) = (11) and t_{pcyc} = 40 ns
3. For details on correspondence of the standard product, wide temperature-range product, and product model name, refer to description of maximum operating frequency and operating temperature range in section 1.1, Features.

Appendix A Pin States

The initial values differ in each MCU operating mode. For details, refer to section 14, Pin Function Controller (PFC).

Table A.1 Pin States

Pin Function		Pin State								
		Reset State			Power-Down Mode					
		Power-On								
Type	Pin Name	Extended without ROM	Extended with ROM	Single-Chip	Manual	Hardware Standby	Software Standby	Sleep	Bus Release State	Software Standby in Bus Release State
Clock	CK	O		Z	O	Z	O	O	O	O
	XTAL	O			O	L	L	O	O	L
	EXTAL	I			I	Z	I	I	I	I
	PLLCAP	I			I	I	I	I	I	I
System control	$\overline{RES}$	I			I	I	I	I	I	I
	$\overline{MRES}$	Z			I	Z	Z*2	I	I	Z*2
	$\overline{WDTOVF}$	O*3			O	O	O	O	O	O
	$\overline{BREQ}$	Z			I	Z	Z	I	I	I
	$\overline{BACK}$	Z			O	Z	Z	O	O	L
Operating mode control	MD0 to MD3	I			I	I	I	I	I	I
	FWP	I			I	I	I	I	I	I
Interrupts	NMI	I			I	Z	I	I	I	I
	$\overline{IRQ0}$ to $\overline{IRQ3}$	Z			I	Z	Z*4	I	I	Z*4
	$\overline{IRQOUT}$	Z			O	Z	K*1	O	O	K*1
Address bus	A0 to A17	O	Z		O	Z	Z	O	Z	Z
Data bus	D0 to D7	Z			I/O	Z	Z	I/O	I/O	Z
Bus control	$\overline{WAIT}$	Z			I	Z	Z	I	I	Z
	$\overline{CS0}$	H	Z		O	Z	O	O	Z	Z
	$\overline{RD}$	H	Z		O	Z	O	O	Z	Z
	$\overline{WRL}$	H	Z		O	Z	O	O	Z	Z
MTU	TCLKA to TCLKD	Z			I	Z	Z	I	I	Z
	TIOC0A to TIOC0D	Z			I/O	Z	K*1	I/O	I/O	K*1
	TIOC1A, TIOC1B									
	TIOC2A, TIOC2B									
	TIOC3A, TIOC3C									
	$\overline{TIOC3B}$, TIOC3D	Z			I/O	Z	Z*2	I/O	I/O	Z*2
	TIOC4A to TIOC4D									

Pin Function		Pin State								
		Reset State			Power-Down Mode					
		Power-On								
Type	Pin Name	Extended without ROM	Extended with ROM	Single-Chip	Manual	Hardware Standby	Software Standby	Sleep	Bus Release State	Software Standby in Bus Release State
MMT	PCIO	Z			I/O	Z	K*1	I/O	I/O	K*1
	PUOA, PUOB PVOA, PVOB PWOA, PWOB	Z			O	Z	Z*2	O	O	Z*2
Port control	$\overline{POE0}$ to $\overline{POE6}$	Z			I	Z	Z	I	I	Z
SCI	SCK2, SCK3	Z			I/O	Z	Z	I/O	I/O	Z
	RxD2, RxD3	Z			I	Z	Z	I	I	Z
	TxD2, TxD3	Z			O	Z	O*1	O	O	O*1
A/D converter	AN0 to AN19	Z			I	Z	Z	I	I	Z
	$\overline{ADTRG}$	Z			I	Z	Z	I	I	Z
I/O ports	PA0 to PA15	Z			I/O	Z	K*1	I/O	I/O	K*1
	PB0 to PB5									
	PD0 to PD8									
	PE0 to PE8, PE10									
	PE9, PE11 to PE21	Z			I/O	Z	Z*2	I/O	I/O	Z*2
	PF0 to PF15	Z			I	Z	Z	I	I	Z
	PG0 to PG3									

Legend:

I: Input

O: Output

H: High-level output

L: Low-level output

Z: High impedance

K: Input pins become high-impedance, and output pins retain their state.

Notes: 1. When the HIZ bit in SBYCR is set to 1, the output pins enter the high-impedance state.

2. Those pins multiplexed with large-current pins (PE9 and PE11 to PE15) unconditionally enter the high-impedance state.

3. This pin operates as an input pin during a power-on reset. This pin should be pulled up to avoid malfunction.

4. This pin operates as an input pin when the IRQEL bit in SBYCR is cleared to 0.

Table A.2 Pin States (1)

Pin Name		On-Chip ROM Space	On-Chip RAM Space	On-Chip Peripheral Module			
				8-Bit Space	16-Bit Space		
					Upper Byte	Lower Byte	Word/Longword
$\overline{CS0}$		H	H	H	H	H	H
$\overline{RD}$	R	H	H	H	H	H	H
	W	—	H	H	H	H	H
$\overline{WRL}$	R	H	H	H	H	H	H
	W	—	H	H	H	H	H
A17 to A0		Address	Address	Address	Address	Address	Address
D7 to D0		Z	Z	Z	Z	Z	Z

Legend:

R: Read

W: Write

Z: High impedance

Table A.2 Pin States (2)

Pin Name		External Normal Space
		8-Bit Space
$\overline{CS0}$		L
$\overline{RD}$	R	L
	W	H
$\overline{WRL}$	R	H
	W	L
A17 to A0		Address
D7 to D0		Data

Legend:

R: Read

W: Write

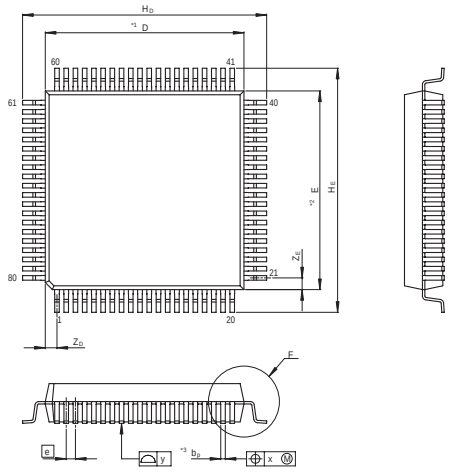
Appendix B Product Code Lineup

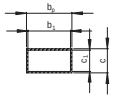
Product Type			Part No.	Package (Package Code)
SH7108	Masked ROM version	Standard product	HD6437108	QFP-80 (FP-80Q)
			HD6437106	
			HD6437104	
			HD6437101	
SH7109	Masked ROM version	Standard product	HD6437109	QFP-100 (FP-100M)
			HD6437107	
			HD6437105	

Appendix C Package Dimensions

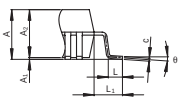
The package dimension that is shown in the Renesas Semiconductor Package Data Book has priority.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP80-14x14-0.65	PRQP0080JD-A	FP-80Q/FP-80QV	1.2g





Terminal cross section



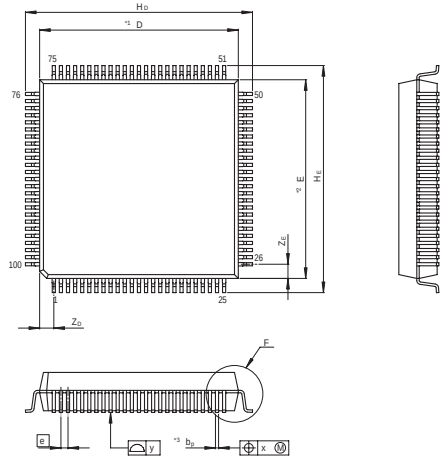
Detail F

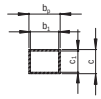
NOTE)
1. DIMENSIONS"*1"AND"*2" DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	14	—
E	—	14	—
A_2	—	2.70	—
H_D	17.0	17.2	17.4
H_E	17.0	17.2	17.4
A	—	—	3.05
A_1	0.00	0.10	0.25
b_p	0.24	0.32	0.40
b_1	—	0.30	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.12
y	—	—	0.10
Z_D	—	0.83	—
Z_E	—	0.83	—
L	0.6	0.8	1.0
L_1	—	1.6	—

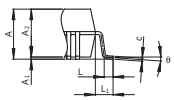
Figure C.1 FP-80Q

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x14-0.50	PRQP0100KB-A	FP-100M/FP-100MV	1.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS"*1"AND"*2" DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	14	—
E	—	14	—
A_2	—	2.70	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	3.05
A_1	0.00	0.12	0.25
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.4	0.5	0.6
L_1	—	1.0	—

Figure C.2 FP-100M

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Renesas 32-Bit RISC Microcomputer
Hardware Manual
SH7108, SH7109 Group

Publication Date: Rev.1.00, September 18, 2008
Published by: Sales Strategic Planning Div.
Renesas Technology Corp.
Edited by: Customer Support Department
Global Strategic Communication Div.
Renesas Solutions Corp.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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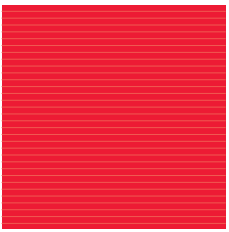

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