

### High Density FLASH Memory Card 32, 64, 96, 128, 160, 192 MEGABYTE

#### General Description

WEDC's Flash memory cards - FLF10 Series - offer high density linear Flash memory for code and data storage, high performance disk emulation, mobile PC and embedded applications.

The WEDC FLF10 series is based on Intel's Multi Level Cell (MLC) Flash memory technology, providing high density Flash components at a significantly lower cost per megabyte. MLC technology allows for two bits of information to be stored in a single cell. This leads to reduced die size and reduced cost per megabyte.

WEDC's FLF10 series cards are built with Intel's 128Mb memory component, 28F128J3A, with a manufacturer/device ID of 89/18H. The FLF10 series is available in densities of 32, 64, 96, 128, 160, and 192MB.

WEDC's FLF10 series provides densities from 32MB to 192MB, in 32MB increments. The cards up to the 64MB density operate in the regular PCMCIA mode. The densities beyond the 64MB density are implemented using a "paging scheme", which is also supported by the PCMCIA standard. By writing a page address to the Configuration Option Register (address 4000H), an additional page of memory can be accessed. The current FLF10 series supports densities to 192MB: total of 3 pages: page 0 := 64MB, page 1 := 64MB, and page 2 := 64MB.

The FLF10 series card operates in a wide, universal voltage range, from 3V to 5V, allowing full "plug and play" functionality and upgrade solutions in all mobile, battery powered applications.

Each memory component in the card also has a 128-bit Protection Register, containing 64 bits of User Programmable OTP (One Time Programmable) Cells. These cells can be programmed with a numeric security measure, such as an electronic signature.

To provide a 16 bit word wide access supported by the PCMCIA standard, devices are paired on the card. Therefore, the Flash array is structured in 128K word (256kB) blocks. Write, read and block erase operations can be performed as either a word or byte wide operation.

The FLF10 series cards conform to the PC Card 95 Standard supported by PCMCIA and JEIDA, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

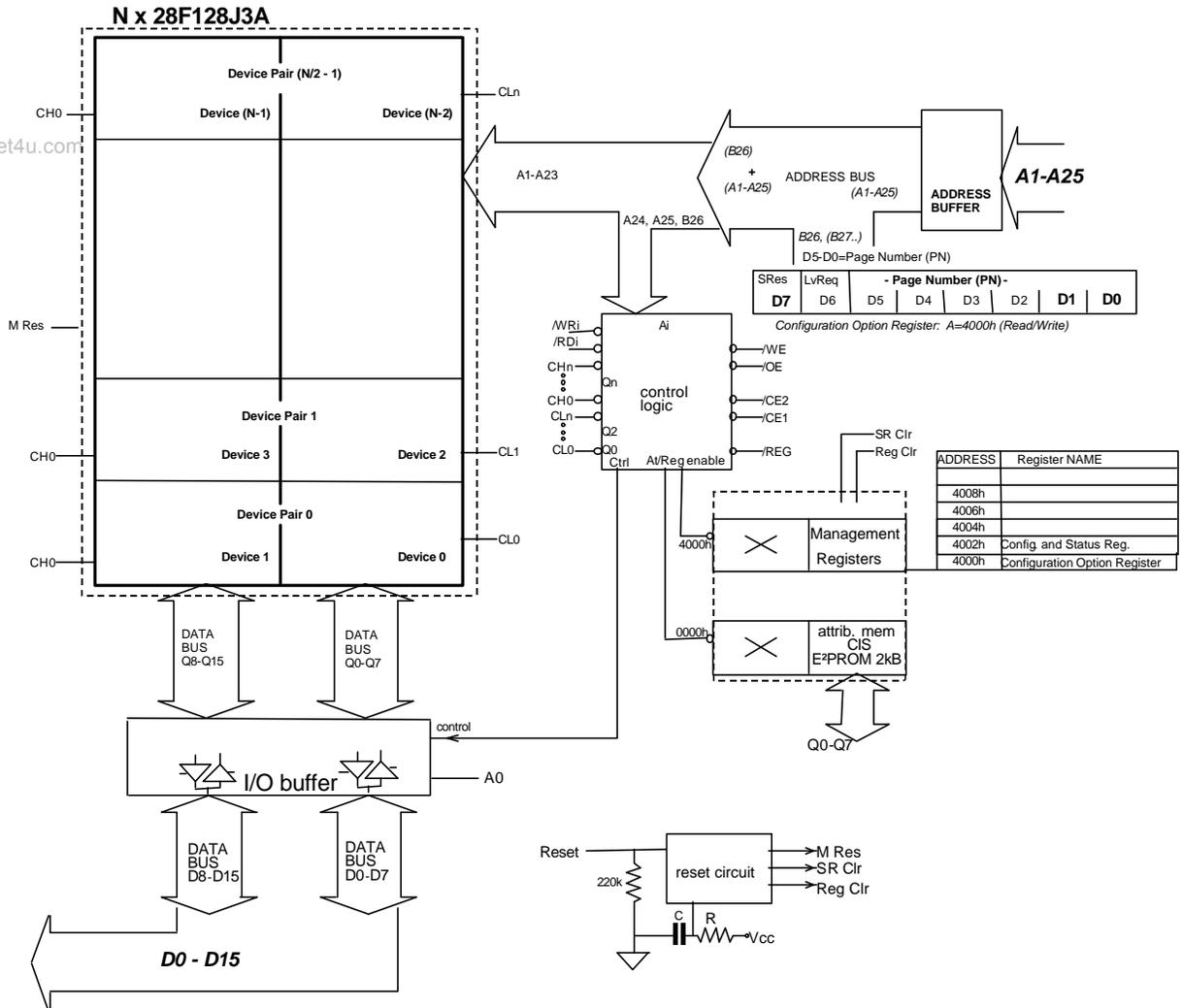
WEDC's standard cards are shipped with WEDC's Flash Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both, a recessed (for label) or flat housing. Please contact your WEDC sales representative for further information on Custom artwork.

#### Features

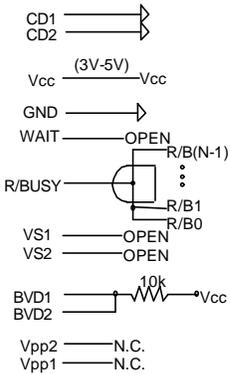
- Low cost, high density Linear Flash Card
- Universal 3V to 5V operating range providing full "plug and play" exchangeability between different systems
- Based on Intel 28F128J3A (MLC) Components
- Fast Read Performance
  - 250ns Maximum Access Time
  - (200ns optional)
- PCMCIA compatible
  - x8/ x16 Data Interface
- 32-Byte Write Buffer (per Memory Device)
  - 6µs per Byte Effective Write Time
- 128-bit Protection Register (per Memory Device)
  - 64-bit Unique Device Identifier
  - 64-bit User Programmable OTP Cells
- Cross-Compatible Command Support
  - Common Flash Interface (CFI)
  - Intel Basic Command Set
  - Scaleable Command Set
- Power-Down Mode
  - Reset, Power Down Registers
- 100,000 Erase Cycles per Block
- 128K word symmetrical Block Architecture
- PC Card Standard Type I Form Factor



**Block Diagram**



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$\overline{CE1}$ ,  $\overline{CE2}$ ,  $\overline{OE}$ ,  $\overline{WE}$ ,  $\overline{REG}$ : pull up typ 100k  
 A0: pull down typ 100k  
 Reset: pull down typ 220k  
 R/Busy - Open Drain output pull up typ 100k

**Configuration Option Register: ADR=4000h**

Read/Write							
SRes	LvReq	- Page Number (PN) -				D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 Soft Reset, active High  
 1=Reset State  
 0=End Reset State  
 D6 LevelReq (not supported)  
 D5-D0 Configuration index  
 D5-D2 reserved  
 D0:D1 Page Number Config. (PN) Power On default=0

**Configuration Status Register: ADR=4002h**

Read/Write							
reserved		reserved		PwrDwn	reserved		
D7	D6	D5	D4	D3	D2	D1	D0

D2 Power Down; active High  
 1 = Place all memory devices in power down mode  
 0 = normal operation Power On default=0

Manufacturer ID	Intel	89 <sub>H</sub>
Device ID	28F128J3A	18 <sub>H</sub>

**FLF10 Flash Card**  
 based on Strata Flash 28F128J3A



### FLF10 Series

#### Pinout

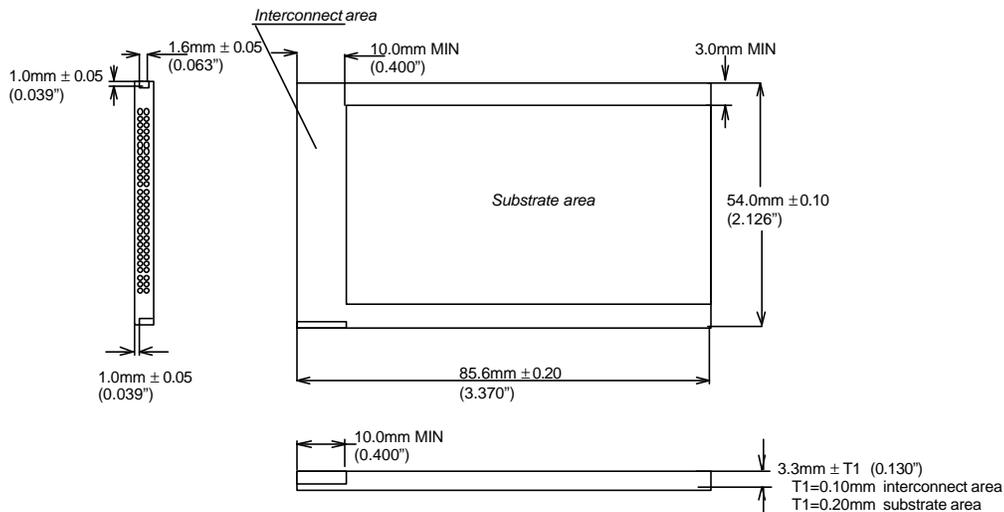
Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#	I	Card enable 1	LOW
8	A10	I	Address bit 10	
9	OE#	I	Output enable	LOW
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY #	O	Ready/Busy	LOW(1)
17	Vcc		Supply Voltage	
18	Vpp1		Prog. Voltage	N.C.
19	A16	I	Address bit 16	
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	CD1#	O	Card Detect 1	LOW
37	DQ11	I/O	Data bit 11	
38	DQ12	I/O	Data bit 12	
39	DQ13	I/O	Data bit 13	
40	DQ14	I/O	Data bit 14	
41	DQ15	I	Data bit 15	
42	CE2#	I	Card Enable 2	LOW
43	VS1	O	Voltage Sense 1	NC (2)
44	RFU		Reserved	
45	RFU		Reserved	
46	A17	I	Address bit 17	
47	A18	I	Address bit 18	
48	A19	I	Address bit 19	
49	A20	I	Address bit 20	
50	A21	I	Address bit 21	
51	Vcc		Supply Voltage	
52	Vpp2		Prog. Voltage	N.C.
53	A22	I	Address bit 22	
54	A23	I	Address bit 23	
55	A24	I	Address bit 24	
56	A25	I	Address bit 25	
57	VS2	O	Voltage Sense 2	N.C.
58	RST	I	Card Reset	HIGH
59	Wait#	O	Extended Bus cycle	LOW(3)
60	RFU		Reserved	
61	REG#	I	Attrib Mem Select	
62	BVD2	O	Bat. Volt. Detect 2	(3)
63	BVD1	O	Bat. Volt. Detect 1	(3)
64	DQ8	I/O	Data bit 8	
65	DQ9	I/O	Data bit 9	
66	DQ10	O	Data bit 10	
67	CD2#	O	Card Detect 2	LOW
68	GND		Ground	

#### Notes:

1. RDY/BSY signal is an open drain type output, pull-up resistors are required on the host side.
2. VS1 is connected to GND.
3. Wait#, BVD1 and BVD2 are internally connected to Vcc by resistors for compatibility.

#### Mechanical





**Card Signal Description**

Symbol	Type	Name and Function
A0 - A25	INPUT	<b>ADDRESS INPUTS:</b> A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not used in word access mode. A25 is the most significant bit
DQ0 - DQ15	INPUT/OUTPUT	<b>DATA INPUT/OUTPUT:</b> DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ15 is the MSB.
CE1#, CE2#	INPUT	<b>CARD ENABLE 1 AND 2:</b> CE1# enables even byte accesses, CE2# enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows 8-bit hosts to access all data on DQ0 - DQ7 (see truth table).
OE#	INPUT	<b>OUTPUT ENABLE:</b> Active low signal gating read data from the memory card.
WE#	INPUT	<b>WRITE ENABLE:</b> Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	<b>READY/BUSY OUTPUT:</b> Indicates status of internally timed erase or program algorithms. A high output indicates that the card is ready to accept accesses. A low output indicates that one or more devices in the memory card are busy with internally timed erase or write activities.
CD1#, CD2#	OUTPUT	<b>CARD DETECT 1 and 2:</b> Provide card insertion detection. These signals are internally connected to ground on the card. The host shall monitor these signals to detect card insertion. Pulled up on host side.
WP	OUTPUT	<b>WRITE PROTECT:</b> Write protect reflects the status of the Write Protect switch on the memory card WP set to high = write protected, providing internal hardware write lockout to the Flash array. If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = "off".
VPP1, VPP2	N.C.	<b>PROGRAMMING VOLTAGES:</b> Not connected
VCC		<b>CARD POWER SUPPLY:</b> Universal 3V to 5V Supply
GND		<b>CARD GROUND</b>
REG#	INPUT	<b>ATTRIBUTE MEMORY SELECT:</b> Active low signal, enables access to attribute memory space, occupied by the Card Information Structure (CIS) and Card Registers.
RST	INPUT	<b>RESET:</b> Active high signal for placing card in Power-on default state. Reset can be used as a Power-Down control for the memory array.
WAIT#	OUTPUT	<b>WAIT:</b> This signal is pulled high internally for compatibility. No wait states are generated.
BVD1, BVD2	OUTPUT	<b>BATTERY VOLTAGE DETECT:</b> These signals are pulled high to maintain SRAM card compatibility.
VS1, VS2	OUTPUT	<b>VOLTAGE SENSE:</b> Notifies the host socket of the card's VCC requirements. VS1 grounded and VS2 is open to indicate a 3/5V card.
RFU N.C.		<b>RESERVED FOR FUTURE USE</b> <b>NO INTERNAL CONNECTION TO CARD:</b> pin may be driven or left floating.

**Functional Truth Table**

READ function						Common Memory			Attribute Memory		
Function Mode	/CE2	/CE1	A0	/OE	/WE	/REG	D15-D8	D7-D0	/REG	D15-D8	D7-D0
Standby Mode	H	H	X	X	X	X	High-Z	High-Z	X	High-Z	High-Z
Byte Access (8 bits)	H	L	L	L	H	H	High-Z	Even-Byte	L	High-Z	Even-Byte
	H	L	H	L	H	H	High-Z	Odd-Byte	L	High-Z	Not Valid
Word Access (16 bits)	L	L	X	L	H	H	Odd-Byte	Even-Byte	L	Not Valid	Even-Byte
Odd-Byte Only Access	L	H	X	L	H	H	Odd-Byte	High-Z	L	Not Valid	High-Z
WRITE function											
Standby Mode	H	H	X	X	X	X	X	X	X	X	X
Byte Access (8 bits)	H	L	L	H	L	H	X	Even-Byte	L	X	Even-Byte
	H	L	H	H	L	H	X	Odd-Byte	L	X	X
Word Access (16 bits)	L	L	X	H	L	H	Odd-Byte	Even-Byte	L	X	Even-Byte
Odd-Byte Only Access	L	H	X	H	L	H	Odd-Byte	X	L	X	X



## FLF10 Series

### Card Interface

The FLF10 series flash card complies with PC Card standard (PCMCIA, March 1997). While maintaining PCMCIA compatibility, the FLF10 series card has integrated special features to extend functionality.

The card has built-in 2 control registers:

- Configuration Option Register (COR)      Address = 4000<sub>h</sub>
- Configuration and Status Register (CSR)      Address = 4002<sub>h</sub>

**COR register:** provides a soft reset function (bit D7) and additional page bits (bits D0 and D1) to extend card capacity beyond 64MB.

#### SReset

As defined by PCMCIA, setting the SReset bit to 1, places the card in the reset state. During this state all memory devices are placed in power down mode, minimizing power consumption. Returning this bit to 0 leaves the reset cycle and places the card in the same condition as following a power up or hardware reset. This bit must be cleared to 0, to access any device on the card.

Complete soft reset cycle must consist of a 2 step write sequence to the SReset bit:

1. Initialization: write 1 to SReset
  - reset cycle begin
  - memory devices enters Power-Down mode aborting all operations and clearing all registers.
2. Write 0 to SReset
  - Reset cycle ends
  - memory devices and registers enter power on default state

The card can also be placed in Power Down mode by activating the Reset signal (pin58) or by controlling the bit D2 (PwrDwn) in the CSR register.

#### LevlRequest

Not supported

#### Configuration Index

Configuration Index bits (D0 - D5) are defined to provide address extension bits -page address, to extend card capacity beyond 64MB.

Only bits D0 and D1 are supported:

- D1D0 set to 00<sub>bin</sub> (0<sub>H</sub>) selects      **page 0**
- D1D0 set to 01<sub>bin</sub> (1<sub>H</sub>) selects:      **page 1**
- D1D0 set to 10<sub>bin</sub> (2<sub>H</sub>) selects:      **page 2**
- D1D0 set to 11<sub>bin</sub> (3<sub>H</sub>) selects:      **page 3 (No Memory Access)**

D1D0 is set to the value of 00<sub>bin</sub> (0<sub>H</sub>) during any reset cycle (Power on Reset, Hardware Reset, and SReset). Attempting to access page 3 will not result in the writing or reading of data.

**CSR register:** provides a power control of the memory array. Only bit D2 is supported; all other bits are "don't care"

#### PwrDwn

Writing 1 to PwrDwn bit (D2) forces each memory device on the card into a reset/power down mode by asserting all the devices RP# pins. Writing 0 to the bit returns the array to stand by mode.



## FLF10 Series

The Card Information Structure (CIS) contains information about Register addressing and Memory structure.

Cards with memory capacity up to 64MB do not support Configuration Index bits.

### Notes:

1. Reading from undefined address location or unsupported bits will return random data.
2. Writing to undefined address location may result in card malfunctioning due to limited address decoding.
3. See block diagram for more details about control registers.

Writing commands to the CUI enables reading of device data, query, identifier codes, inspection and clearing of the status register, and, when  $V_{PEN} = V_{PENH}$ , block erasure, program, and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Byte/Word Program command requires the command and address of the location to be written. Set Block Lock-Bit commands require the command and block within the device to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when the device is enabled and  $WE\#$  is active. The address and data needed to execute a command are latched on the rising edge of  $WE\#$  or the first edge of  $CE_0$ ,  $CE_1$ , or  $CE_2$  that disables the device. Standard microprocessor write timings are used.

**For information regarding modes of operation, commands, and programming details for the memory components, please consult the Intel 28F128J3A data sheet.**



### FLF10 Series

#### Absolute Maximum Ratings <sup>(2)</sup>

Operating Temperature TA (ambient)	
Commercial	0°C to +60 °C
Storage Temperature	-10°C to +70 °C
Voltage on any pin relative to VSS	-0.5V to VCC+0.5V
VCC supply Voltage relative to VSS	-0.5V to +7.0V

#### Note:

Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### Recommended Supply Voltage

VCC	Tolerance
3.3V	± 0.3V
5.0V	± 0.5V

**Note:** The FLF10 Series Card will function at either 3.3V or 5.0V

#### DC Characteristics <sup>(1)</sup>

Symbol	Parameter	Density (Mbytes)	Notes	Typ <sup>(3)</sup>	Max	Units	Test Conditions
ICCR	VCC Read Current	32,64,96,128,160,192		70	110	mA	VCC = VCCmax tcycle = 200ns
ICCW	VCC Program Current	32,64,96,128,160,192		70	120	mA	2 memory devices
ICCE	VCC Erase Current	32,64,96,128,160,192		70	140	mA	2 memory devices
ICCD	VCC Power-down Current	32	2	100	200	µA	VCC = VCCmax Control Signals = VCC Reset = VCC (active)
		64		200	400		
		96		300	600		
		128		400	800		
		160		500	1000		
		192		600	1200		
ICCS (CMOS)	VCC Standby Current	32	2	0.1	0.2	mA	VCC = VCCmax Control Signals = VCC  Reset = 0V (not active)
		64		0.2	0.4		
		96		0.3	0.6		
		128		0.4	0.8		
		160		0.5	1.0		
		192		0.6	1.2		

CMOS Test Conditions: VCC = 5V ± 5%, VIL = VSS ± 0.2V, VIH = VCC ± 0.2V

#### Notes:

- All currents are RMS values unless otherwise specified. ICCR, ICCW and ICCE are based on Word wide operations (2 memory devices activated).
- Control Signals: CE<sub>1</sub>#, CE<sub>2</sub>#, OE#, WE#.
- Typical: VCC = 5V or VCC = 3V, T = +25°C.



## FLF10 Series

VCC = 3.3V or 5V

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
ILI	Input Leakage Current	1, 2		±20	µA	VCC = VCCMAX Vin = VCC or GND
ILO	Output Leakage Current	1		±20	µA	VCC = VCCMAX Vin = VCC or GND
VIL	Input Low Voltage	1	0	0.8	V	
VIH	Input High Voltage	1	2.0V	VCC+0.5	V	
VOL	Output Low Voltage	1		0.4	V	IOL = 3.2mA
VOH	Output High Voltage	1	2.4V		V	IOH = -2.0mA
VLKO	VCC Erase/Program Lock Voltage	1	2.0		V	

**Notes:**

1. Values are the same for byte and word wide modes for all card densities.
2. Exception: Leakage current on control signals with internal pull up resistors (see block diag) will be < 500µA when VIN=GND.



**AC Characteristics**

Read Timing Parameters

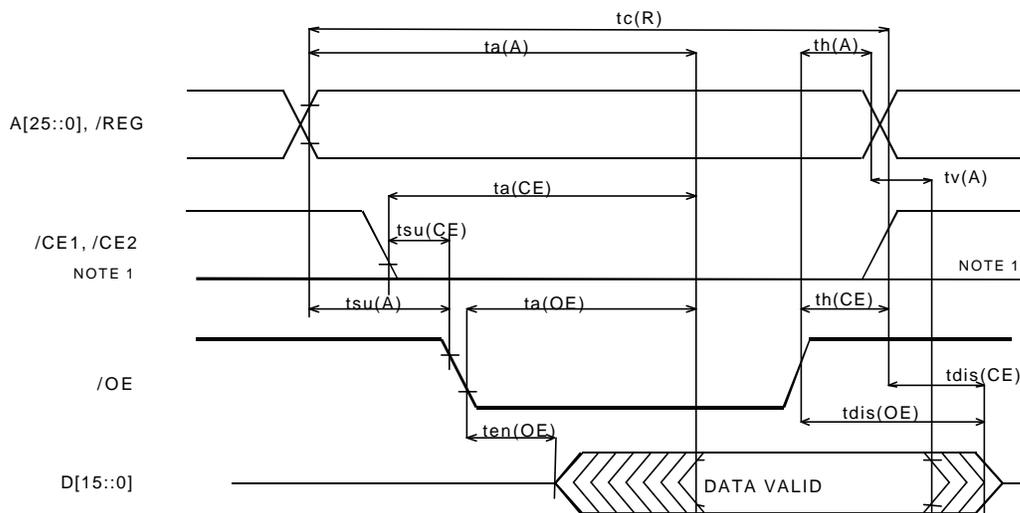
VCC = 3.3V or 5V

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SYMBOL (PCMCIA)	Parameter	200ns		250ns		Unit
		Min	Max	Min	Max	
$t_c(R)$	Read Cycle Time	200		250		ns
$t_a(A)$	Address Access Time		200		250	ns
$t_a(CE)$	Card Enable Access Time		200		250	ns
$t_a(OE)$	Output Enable Access Time		90		100	ns
$t_{su}(A)$	Address Setup Time		20		30	ns
$t_{su}(CE)$	Card Enable Setup Time		0		0	ns
$t_h(A)$	Address Hold Time		20		20	ns
$t_h(CE)$	Card Enable Hold Time		20		20	ns
$t_v(A)$	Output Hold from Address Change		0		0	ns
$t_{dis}(CE)$	Output Disable Time from CE#		90		100	ns
$t_{dis}(OE)$	Output Disable Time from OE#		90		100	ns
$t_{en}(CE)$	Output Enable Time from CE#	5		5		ns
$t_{en}(OE)$	Output Enable Time from OE#	5		5		ns
$t_{rec}(RST)$	Power Down recovery to Output Delay. VCC = 5V		500		500	ns

**Note:** AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Read Timing Diagram





FLF10 Series

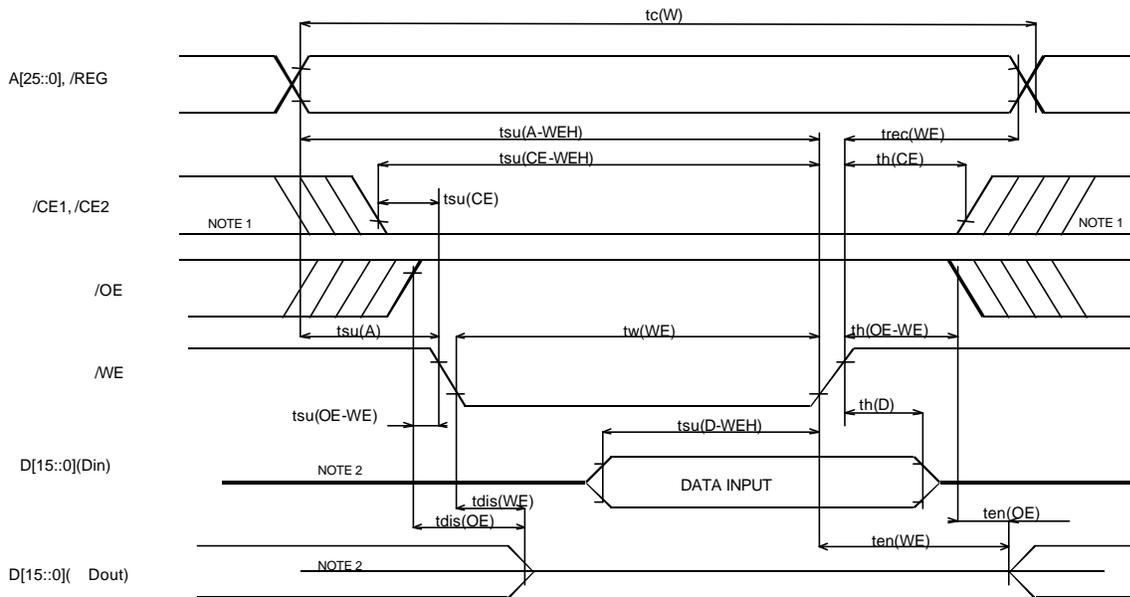
Write Timing Parameters

VCC = 3.3V or 5V

SYMBOL (PCMCIA)	Parameter	200ns		250ns		Unit
		Min	Max	Min	Max	
$t_{cW}$	Write Cycle Time	200		250		ns
$t_w(WE)$	Write Pulse Width	120		150		ns
$t_{su}(A)$	Address Setup Time	20		30		ns
$t_{su}(A-WEH)$	Address Setup Time for WE#	140		180		ns
$t_{su}(CE-WEH)$	Card Enable Setup Time for WE#	140		180		ns
$t_{su}(D-WEH)$	Data Setup Time for WE#	60		80		ns
$t_h(D)$	Data Hold Time	30		30		ns
$t_{rec}(WE)$	Write Recover Time/Address hold	30		30		ns
$t_{dis}(WE)$	Output Disable Time from WE#		90		100	ns
$t_{dis}(OE)$	Output Disable Time from OE#		90		100	ns
$t_{en}(WE)$	Output Enable Time from WE#	5		5		ns
$t_{en}(OE)$	Output Enable Time from OE#	5		5		ns
$t_{su}(OE-WE)$	Output Enable Setup from WE#	10		10		ns
$t_h(OE-WE)$	Output Enable Hold from WE#	50		50		ns
$t_{su}(CE)$	Card Enable Setup Time from OE#	0		0		ns
$t_h(CE)$	Card Enable Hold Time	20		20		ns
$t_{rec}(WEL)$	Reset recovery to WE going low	1		1		$\mu$ s

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Write Timing Diagram





**Data Write and Erase Performance** <sup>(1,3)</sup>

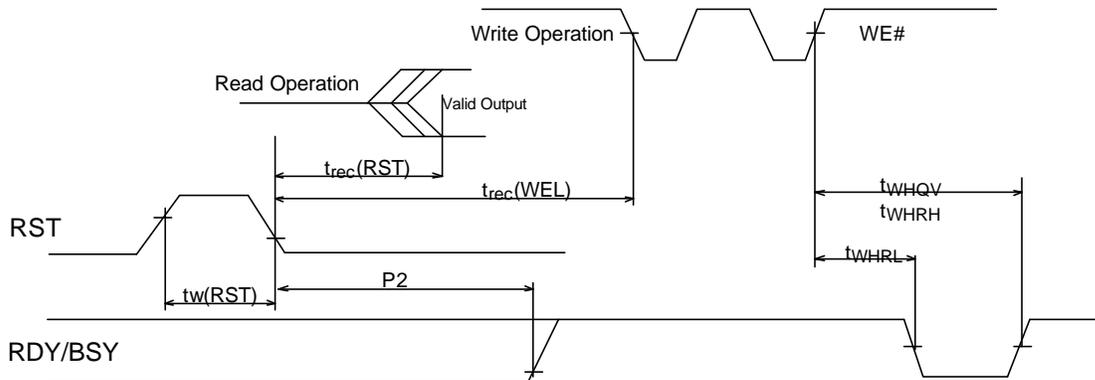
VCC = 5V ± 5%, T<sub>A</sub> = 0C to + 70C

SYM	Parameter	Notes	Min	Typ <sup>(1)</sup>	Max	Units	Test Conditions
t <sub>WHQV1</sub>	Word/Byte Program time	2,4		6.3		µs	Effective time per Byte (using Write Buffer)
t <sub>WHQV3</sub>	Byte Program Time (using Byte program command)			180		µs	
	Block Program Time (using write to buffer command)	2		0.8		sec	Word Program Mode
t <sub>WHQV4</sub>	Block Erase Time	2		0.7		sec	
t <sub>WHRH</sub>	Erase Suspend Latency Time to Read			26	35	µs	

**Notes:**

1. Typical: Nominal voltages and T<sub>A</sub> = 25C.
2. Excludes system overhead.
3. Valid for all speed options.
4. To maximize system performance RDY/BSY# signal should be polled.

**Waveforms for Reset Operation**



SYMBOL	Parameter	Min	Max	Unit
t <sub>w</sub> (RST)	Reset pulse High time	35		µs
P2	RST Low to reset during Erase/Program/Lock-bit		100	ns
t <sub>rec</sub> (RST)	Reset Low to output delay		500	ns
t <sub>rec</sub> (WEL)	Reset Recovery to WE going Low	1		µs
t <sub>WHRL</sub>	WE High to Rdy/Bsy going low		100	ns



**CIS DATA FOR FLF10 32MB & 64 MB CARDS BASED ON INTEL 28F128J3A**

Address	Value	Description	Address	Value	Description
00H	01H	CISTPL_DEVICE	48H	05H	TPL_LINK(05H)
02H	03H	TPL_LINK	4AH	F6H	EDI TPLMID_MANF: LSB
04H	51H	FLASH = 250ns (device writable)	4CH	01H	EDI TPLMID_MANF: MSB
06H	7EH	CARD SIZE: 32MB	4EH	00H	LSB: Number Not Assigned
	FEH	64MB	50H	00H	MSB: Number Not Assigned
08H	FFH	END OF DEVICE	52H	FFH	END OF TUPLE
0AH	1CH	CISTPL_DEVICE_OC	54H	1AH	CISTPL_CONF
0CH	04H	TPL_LINK	56H	06H	TPL_LINK
0EH	02H	3 VOLT OPERATION	58H	01H	TPCC_SZ
10H	51H	FLASH = 250ns (device writable)	5AH	00H	TPCC_LAST
12H	7EH	CARD SIZE:32MB	5CH	00H	TPCC_RADR
	FEH	64MB	5EH	40H	TPCC_RADR
14H	FFH	END OF DEVICE	60H	00H	TPCC RMSK
16H	18H	CISTPL_JEDEC_C	62H	FFH	END OF TUPLE
18H	03H	TPL_LINK	64H	1BH	CISTPL_CFTABLE_ENTRY
1AH	89H	Manufacturer ID -INTEL	66H	03H	TPL_LINK
1CH	18H	Device ID - 28F0128J3A	68H	00H	TPCE_INDEX
1EH	FFH	END OF DEVICE	6AH	00H	TPCE_FS (no selection)
20H	17H	CISTPL_DEVICE A	6CH	FFH	END OF TUPLE
22H	03H	TPL_LINK	6EH	15H	CISTPL_VERS1
24H	42H	EEPROM - 200ns	70H	7FH	TPL_LINK
26H	01H	Device Size = 2KBytes	72H	04H	TPLL1_MAJOR
28H	FFH	END OF TUPLE	74H	01H	TPLL1_MINOR
2AH	1DH	CISTPL_DEVICE OA	76H	37H	7
2CH	03H	TPL_LINK	78H	50H	P
2EH	02H	3 VOLT OPERATION	7AH	30H	0
30H	11H	ROM - 250ns	7CH	33H	3
32H	FFH	END OF DEVICE	7EH	32H	2
34H	1EH	CISTPL_DEVICEGEO	80H	46H	F
36H	07H	TPL_LINK	82H	4CH	L
38H	02H	DGTPL_BUS	84H	46H	F
3AH	12H	DGTPL_EBS	86H	31H	1
3CH	01H	DGTPL_RBS	88H	32H	2
3EH	01H	DGTPL_WBS	8AH	2DH	-
40H	01H	DGTPL_PART	8CH	2DH	-
42H	01H	FLASH DEVICE NON-INTERLEAVED	8EH	2DH	-
44H	FFH	END OF TUPLE	90H	32H	2
46H	20H	CISTPL_MANFID	92H	35H	5
			94H	20H	SPACE



**CIS DATA FOR FLF10 32MB & 64 MB CARDS BASED ON INTEL 28F128J3A (CONT.)**

Address	Value	Description
96H	00H	END TEXT
98H	43H	C
9AH	4FH	O
9CH	50H	P
9EH	59H	Y
A0H	52H	R
A2H	49H	I
A4H	47H	G
A6H	48H	H
A8H	54H	T
AAH	20H	SPACE
ACH	57H	W
AEH	48H	H
B0H	49H	I
B2H	54H	T
B4H	45H	E
B6H	20H	SPACE
B8H	45H	E
BAH	4CH	L
BCH	45H	E
BEH	43H	C
COH	54H	T
C2H	52H	R
C4H	4FH	O
C6H	4EH	N
C8H	49H	I
CAH	43H	C
CCH	20H	SPACE
CEH	44H	D
DOH	45H	E
D2H	53H	S
D4H	49H	I
D6H	47H	G
D8H	4EH	N
DAH	53H	S
DCH	20H	SPACE
DEH	43H	C
EOH	4FH	O
E2H	52H	R
E4H	50H	P
E6H	4FH	O
E8H	52H	R

Address	Value	Description
EAH	41H	A
ECH	54H	T
EEH	49H	I
F0H	4FH	O
F2H	4EH	N
F4H	20H	SPACE
F6H	00H	END TEXT
F8H	31H	1
FAH	39H	9
FCH	39H	9
FEH	39H	9
100H	00H	END TEXT
102H	00H	NULL
104H	FFH	END OF LIST

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**CIS DATA FOR FLF10 96MB - 192MB CARDS BASED ON INTEL 28F128J3A**

Address	Value	Description	Address	Value	Description
00H	01H	CISTPL_DEVICE	48H	02H	DGTPL_BUS
02H	03H	TPL_LINK	4AH	12H	DGTPL_EBS
04H	51H	FLASH = 250ns (device writable)	4CH	01H	DGTPL_RBS
06H	FEH	CARD SIZE: 64MB (1 <sup>st</sup> page)	4EH	01H	DGTPL_WBS
08H	FFH	END OF DEVICE	50H	01H	DGTPL_PART
0AH	1CH	CISTPL_DEVICE_OC	52H	01H	FLASH DEVICE NON-INTERLEAVED
0CH	04H	TPL_LINK	54H	FFH	END OF TUPLE
0EH	02H	3 VOLT OPERATION	56H	20H	CISTPL_MANFID
10H	51H	FLASH = 250ns (device writable)	58H	05H	TPL_LINK(05H)
12H	FEH	CARD SIZE:64MB (1 <sup>st</sup> page)	5AH	F6H	EDI TPLMID_MANF: LSB
14H	FFH	END OF DEVICE	5CH	01H	EDI TPLMID_MANF: MSB
16H	09H	CISTPL_EXTDEVICE	5EH	00H	LSB: Number Not Assigned
18H	06H	TPL_LINK	60H	00H	MSB: Number Not Assigned
1AH	0CH	Mem Paging Info:2bit/COR/64MB	62H	FFH	END OF TUPLE
1CH	51H	Flash = 250 ns	64H	1AH	CISTPL_CONF
1EH	07H	Device Size Extender	66H	06H	TPL_LINK
20H	01H	1x64MB (for 96MB and 128MB)	68H	01H	TPCC_SZ
	02H	2x64MB (for 160MB and 192MB)	6AH	00H	TPCC_LAST
22H	7DH	+32MB (for 96MB and 160MB)	6CH	00H	TPCC_RADR
	FEH	+64MB (for 128MB and 192 MB)	6EH	40H	TPCC_RADR
24H	FFH	END OF TUPLE	70H	03H	TPCC_RMSK
26H	18H	CISTPL JEDEC C	72H	FFH	END OF TUPLE
28H	03H	TPL LINK	74H	15H	CISTPL_VERS1
2AH	89H	Manufacturer ID - INTEL	76H	7FH	TPL_LINK
2CH	18H	Device ID - 28F0128J3A	78H	04H	TPLL1_MAJOR
2EH	FFH	END OF DEVICE	7AH	01H	TPLL1_MINOR
30H	17H	CISTPL_DEVICE A	7CH	37H	7
32H	03H	TPL_LINK	7EH	50H	P
34H	42H	EEPROM - 200ns	80H	30H	0
36H	01H	Device Size = 2Kbytes	82H	39H	9
38H	FFH	END OF TUPLE	84H	36H	6
3AH	1DH	CISTPL_DEVICE_OA	86H	46H	F
3CH	03H	TPL_LINK	88H	4CH	L
3EH	02H	3 VOLT OPERATION	8AH	46H	F
40H	11H	ROM - 250ns	8CH	31H	1
42H	FFH	END OF DEVICE	8EH	32H	2
44H	1EH	CISTPL_DEVICEGEO	90H	2DH	-
46H	07H	TPL_LINK	92H	2DH	-

**CIS DATA FOR FLF10 96MB - 192MB CARDS BASED ON INTEL 28F128J3A (CONT.)**

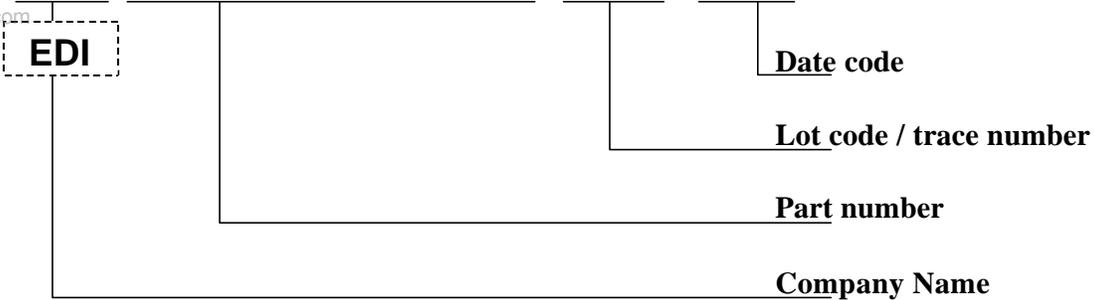
Address	Value	Description
94H	2DH	-
96H	32H	2
98H	35H	5
9AH	20H	SPACE
9CH	00H	END TEXT
9EH	43H	C
A0H	4FH	O
A2H	50H	P
A4H	59H	Y
A6H	52H	R
A8H	49H	I
AAH	47H	G
ACH	48H	H
AEH	54H	T
B0H	20H	SPACE
B2H	57H	W
B4H	48H	H
B6H	49H	I
B8H	54H	T
BAH	45H	E
BCH	20H	SPACE
BEH	45H	E
C0H	4CH	L
C2H	45H	E
C4H	43H	C
C6H	54H	T
C8H	52H	R
CAH	4FH	O
CCH	4EH	N
CEH	49H	I
D0H	43H	C
D2H	20H	SPACE
D4H	44H	D
D6H	45H	E
D8H	53H	S
DAH	49H	I
DCH	47H	G
DEH	4EH	N
E0H	53H	S
E2H	20H	SPACE
E4H	43H	C
E6H	4FH	O

Address	Value	Description
E8H	52H	R
EAH	50H	P
ECH	4FH	O
EEH	52H	R
F0H	41H	A
F2H	54H	T
F4H	49H	I
F6H	4FH	O
F8H	4EH	N
FAH	20H	SPACE
FCH	00H	END TEXT
FEH	31H	1
100H	39H	9
102H	39H	9
104H	39H	9
106H	00H	END TEXT
108H	00H	NULL
10AH	FFH	END OF LIST



**PRODUCT MARKING**

**WED 7P032FLF1200C15 C995 9915**

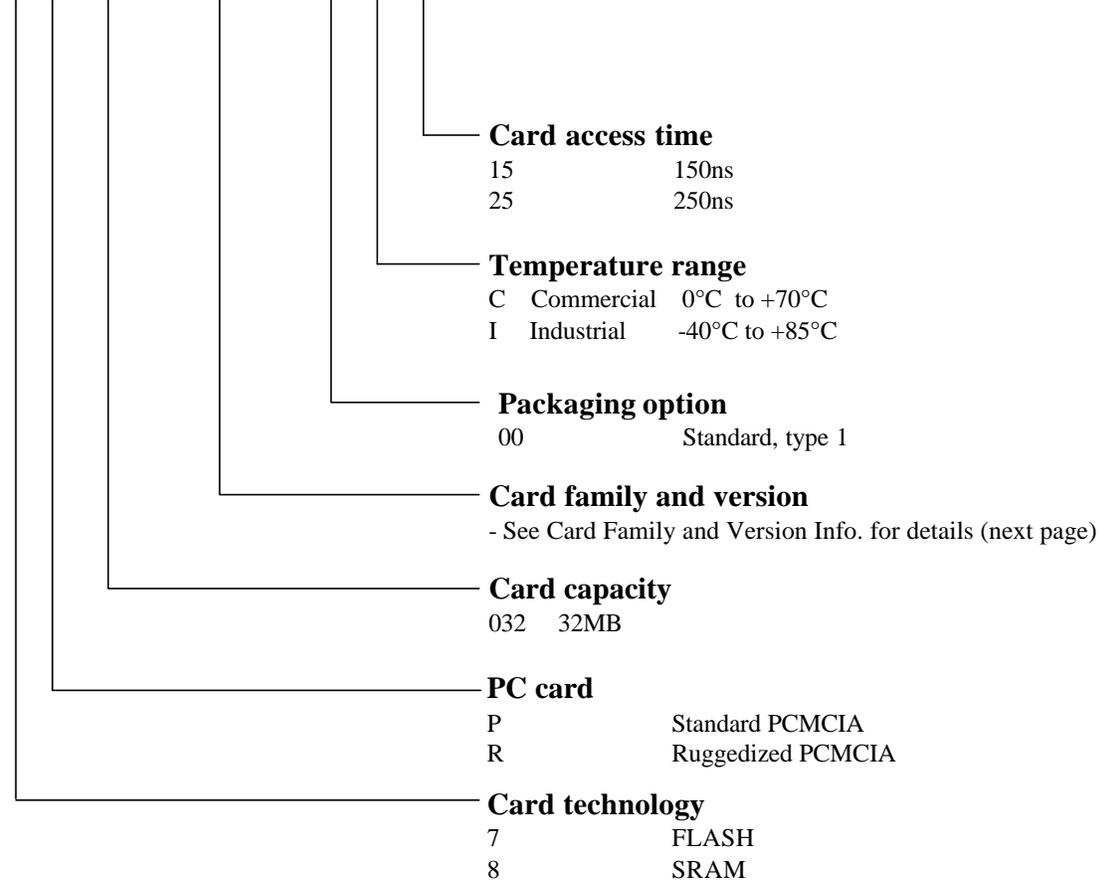


**Note:**

Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2001 all PCMCIA products will be marked only with the WED prefix.

**PART NUMBERING**

**7 P 032 FLF12 00 C 15**





**Ordering Information**

**7P XXX FLF YY SS T ZZ**

where

**XXX:**      **032**      **32MB**  
               **064**      **64MB**  
               **096**      **96MB**  
               **128**      **128MB**  
               **160**      **160MB**  
               **192**      **192MB**

**YY:**        **12**            **based on 28F128J3A**  
    **With Attribute Memory**  
               **14**            **based on 28F128J3A**  
    **With Attribute Memory and**  
    **Write Protect Switch (optional)**

**SS:**        **00**            **WEDC Logo**  
    **01**            **Blank Housing Type 1**  
    **02**            **Blank Housing T 1 (Recessed)**

**T:**            **C**            **Commercial**

**ZZ:**        **20**            **200ns**  
    **25**            **250ns**

REVISION HISTORY		
Date of revision	Version	Description
22-Jul-99	-000	Initial release
03-May-01	-001	Added page 16
01-Aug-00	-002	Corrected Timing Errors, Pgs. 9&10
17-Oct-00	-003	Corrected CIS Errors, Pg. 14
		Added Memory Chip Info, Pg. 6
3/18/01	-004	Corrected VIH, VOH Pg 8
		CIS for 96-192MB, in Adr 12h: 7E->FE

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