



5V 1Mb (128K x 8) FAST Asynchronous SRAM

**Revision History AS7C1024B**

Revision	Details	Date
Rev 1.0	Preliminary datasheet	prior to 2004
Rev 1.1	Die Revision A to B	March 2004
Rev 2.0	PCN issued yield issues with industrial temperature TJ = SOJ 300 mil-10/12ns	May 2015
Rev 3.0	Re-introduced 12ns, 15ns and 20ns Industrial Grade parts for 32p SOJ 300mils. Corrections done in ordering codes to keep only Green Part numbers.	March 2022

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 Fax: 425-896-8628 Alliance Memory Inc. reserves the right to change products or specification without notice

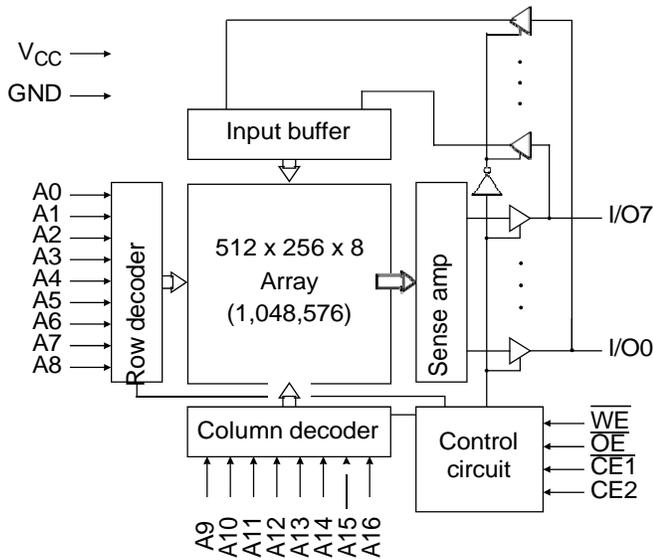


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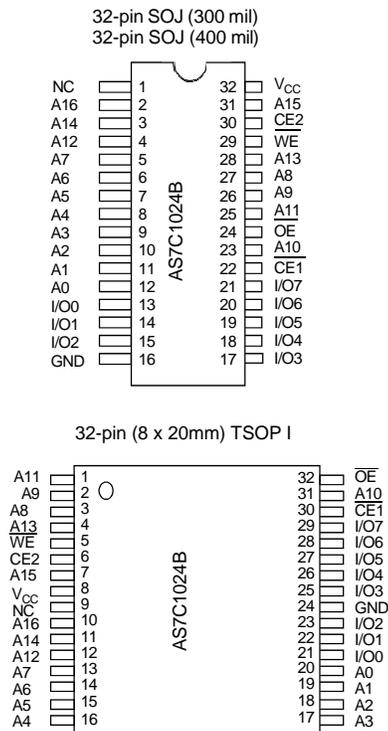
**Features**

- Industrial and commercial temperatures
- Organization: 131,072 words x 8 bits
- High speed
  - 10/12/15/20 ns address access time
  - 5/6/7/8 ns output enable access time
- Low power consumption: ACTIVE
  - 605 mW / max @ 10 ns
- Low power consumption: STANDBY
  - 55 mW / max CMOS
- Easy memory expansion with  $\overline{CE1}$ ,  $\overline{CE2}$ ,  $\overline{OE}$  inputs
- TTL/LVTTL-compatible, three-state I/O
- 32-pin JEDEC standard packages
  - 300 mil SOJ
  - 400 mil SOJ
  - 8 x 20mm TSOP I
- ESD protection  $\geq 2000$  volts
- Latch-up current  $\geq 200$  mA

**Logic block diagram**



**Pin arrangement**



**Selection guide**

	-10	-12	-15	-20	Unit
Maximum address access time	10	12	15	20	ns
Maximum output enable access time	5	6	7	8	ns
Maximum Operating Current	110	100	90	80	mA
Maximum CMOS standby Current	10	10	10	10	mA



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## Functional description

The AS7C1024B is a high performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) device organized as 131,072 words x 8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times ( $t_{AA}$ ,  $t_{RC}$ ,  $t_{WC}$ ) of 10/12/15/20 ns with output enable access times ( $t_{OE}$ ) of 5/6/7/8 ns are ideal for high performance applications. Active high and low chip enables ( $\overline{CE1}$ , CE2) permit easy memory expansion with multiple-bank systems.

When  $\overline{CE1}$  is high or CE2 is low, the devices enter standby mode. If inputs are still toggling, the device will consume  $I_{SB}$  power. If the bus is static, then full standby power is reached ( $I_{SB1}$ ). For example, the AS7C1024B is guaranteed not to exceed 55 mW under nominal full standby conditions.

A write cycle is accomplished by asserting write enable ( $\overline{WE}$ ) and both chip enables ( $\overline{CE1}$ , CE2). Data on the input pins I/O0 through I/O7 is written on the rising edge of  $\overline{WE}$  (write cycle 1) or the active-to-inactive edge of  $\overline{CE1}$  or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ( $\overline{OE}$ ) or write enable ( $\overline{WE}$ ).

A read cycle is accomplished by asserting output enable ( $\overline{OE}$ ) and both chip enables ( $\overline{CE1}$ , CE2), with write enable ( $\overline{WE}$ ) high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable is inactive, output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

## Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on $V_{CC}$ relative to GND	$V_{t1}$	-0.50	+7.0	V
Voltage on any pin relative to GND	$V_{t2}$	-0.50	$V_{CC} + 0.50$	V
Power dissipation	$P_D$	–	1.0	W
Storage temperature (plastic)	$T_{stg}$	-65	+150	°C
Ambient temperature with $V_{CC}$ applied	$T_{bias}$	-55	+125	°C
DC current into outputs (low)	$I_{OUT}$	–	20	mA

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Truth table

CE1	CE2	WE	OE	Data	Mode
H	X	X	X	High Z	Standby ( $I_{SB}$ , $I_{SB1}$ )
X	L	X	X	High Z	Standby ( $I_{SB}$ , $I_{SB1}$ )
L	H	H	H	High Z	Output disable ( $I_{CC}$ )
L	H	H	L	$D_{OUT}$	Read ( $I_{CC}$ )
L	H	L	X	$D_{IN}$	Write ( $I_{CC}$ )

Key: X = don't care, L = low, H = high



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**Recommended operating conditions**

Parameter		Symbol	Min	Nominal	Max	Unit
Supply Voltage		$V_{CC}$	4.5	5.0	5.5	V
Input Voltage		$V_{IH}$	2.2	-	$V_{CC} + 0.5$	V
		$V_{IL}$	-0.5	-	0.8	V
Ambient operating temperature	commercial	$T_A$	0	-	70	°C
	industrial	$T_A$	-40	-	85	°C

$V_{IL}$  min = -1.0V for pulse width less than 5ns

$V_{IH}$  max =  $V_{CC} + 2.0V$  for pulse width less than 5ns.

**DC operating characteristics (over the operating range)<sup>1</sup>**

Parameter	Sym	Test conditions	-10		-12		-15		-20		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	$ I_{LI} $	$V_{CC} = \text{Max}, V_{IN} = \text{GND to } V_{CC}$	-	1	-	1	-	1	-	1	$\mu\text{A}$
Output leakage current	$ I_{LO} $	$V_{CC} = \text{Max}, \overline{CE1} = V_{IH}$ or $CE2 = V_{IL}, V_{OUT} = \text{GND to } V_{CC}$	-	1	-	1	-	1	-	1	$\mu\text{A}$
Operating power supply current	$I_{CC}$	$V_{CC} = \text{Max}, CE1 \leq V_{IL}, CE2 \geq V_{IH}, f = f_{\text{Max}}, I_{OUT} = 0 \text{ mA}$	-	110	-	100	-	90	-	80	mA
Standby power supply current	$I_{SB}$	$V_{CC} = \text{Max}, CE1 \geq V_{IH}$ and/or $CE2 \leq V_{IL}, f = f_{\text{Max}}$	-	50	-	45	-	45	-	40	mA
	$I_{SB1}$	$V_{CC} = \text{Max}, CE1 \geq V_{CC} - 0.2V$ and/or $CE2 \leq 0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V, f = 0$	-	10	-	10	-	10	-	10	
Output voltage	$V_{OL}$	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$	-	0.4	-	0.4	-	0.4	-	0.4	V
	$V_{OH}$	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	2.4	-	2.4	-	2.4	-	2.4	-	

**Capacitance (f = 1 MHz,  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = \text{NOMINAL}$ )<sup>2</sup>**

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	$C_{IN}$	A, $\overline{CE1}$ , $\overline{CE2}$ , $\overline{WE}$ , $\overline{OE}$	$V_{IN} = 0V$	5	pF
I/O capacitance	$C_{IO}$	I/O	$V_{IN} = V_{OUT} = 0V$	7	pF



5V 1Mb (128K x 8) FAST Asynchronous SRAM

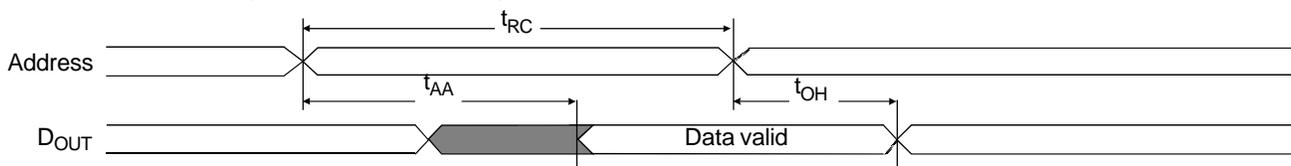
Read cycle (over the operating range)<sup>3,9,12</sup>

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	$t_{RC}$	10	-	12	-	15	-	20	-	ns	
Address access time	$t_{AA}$	-	10	-	12	-	15	-	20	ns	3
Chip enable ( $\overline{CE1}$ ) access time	$t_{ACE1}$	-	10	-	12	-	15	-	20	ns	3, 12
Chip enable ( $\overline{CE2}$ ) access time	$t_{ACE2}$	-	10	-	12	-	15	-	20	ns	3, 12
Output enable ( $\overline{OE}$ ) access time	$t_{OE}$	-	5	-	6	-	7	-	8	ns	
Output hold from address change	$t_{OH}$	3	-	3	-	3	-	3	-	ns	5
$\overline{CE1}$ Low to output in low Z	$t_{CLZ1}$	3	-	3	-	3	-	3	-	ns	4, 5, 12
$\overline{CE2}$ High to output in low Z	$t_{CLZ2}$	3	-	3	-	3	-	3	-	ns	4, 5, 12
$\overline{CE1}$ Low to output in high Z	$t_{CHZ1}$	-	4	-	5	-	6	-	7	ns	4, 5, 12
$\overline{CE2}$ Low to output in high Z	$t_{CHZ2}$	-	4	-	5	-	6	-	7	ns	4, 5, 12
$\overline{OE}$ Low to output in low Z	$t_{OLZ}$	0	-	0	-	0	-	0	-	ns	4, 5
$\overline{OE}$ High to output in high Z	$t_{OHZ}$	-	4	-	5	-	6	-	7	ns	4, 5
Power up time	$t_{PU}$	0	-	0	-	0	-	0	-	ns	4, 5, 12
Power down time	$t_{PD}$	-	10	-	12	-	15	-	20	ns	4, 5, 12

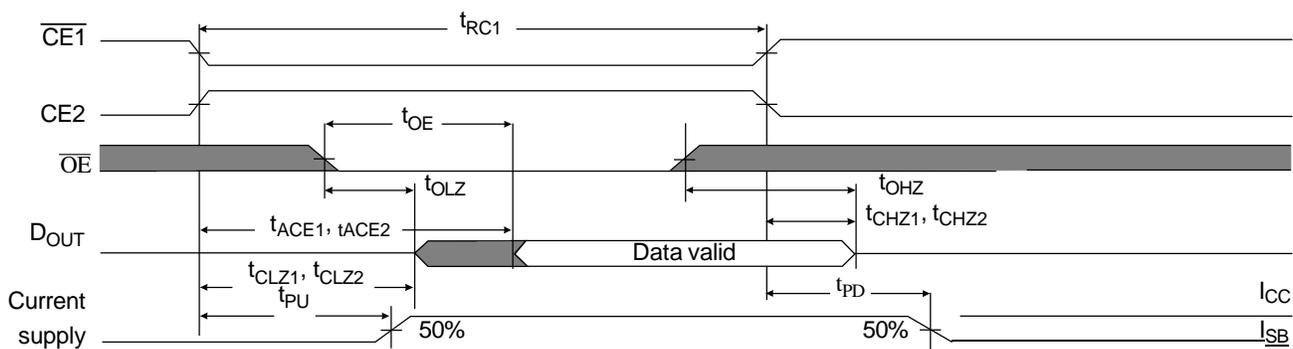
Key to switching waveforms



Read waveform 1 (address controlled)<sup>3,6,7,9,12</sup>



Read waveform 2 ( $\overline{CE1}$ ,  $\overline{CE2}$ , and  $\overline{OE}$  controlled)<sup>3,6,8,9,12</sup>



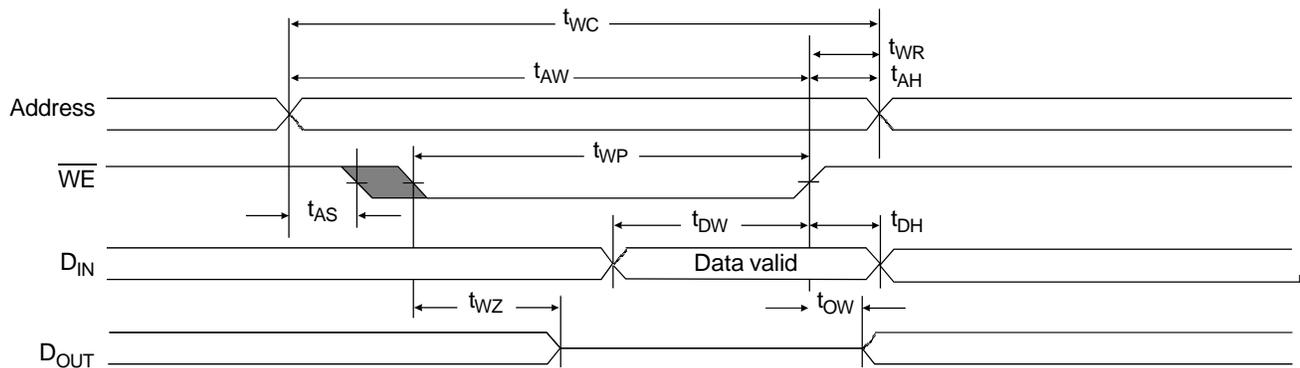


5V 1Mb (128K x 8) FAST Asynchronous SRAM

Write cycle (over the operating range)<sup>11, 12</sup>

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	$t_{WC}$	10	-	12	-	15	-	20	-	ns	
Chip enable (CE1) to write end	$t_{CW1}$	8	-	9	-	10	-	12	-	ns	12
Chip enable (CE2) to write end	$t_{CW2}$	8	-	9	-	10	-	12	-	ns	12
Address setup to write end	$t_{AW}$	8	-	9	-	10	-	12	-	ns	
Address setup time	$t_{AS}$	0		0	-	0	-	0	-	ns	12
Write pulse width	$t_{WP}$	7		8	-	9	-	12	-	ns	
Write recovery time	$t_{WR}$	0	-	0	-	0	-	0	-	ns	
Address hold from end of write	$t_{AH}$	0	-	0	-	0	-	0	-	ns	
Data valid to write end	$t_{DW}$	5		6	-	8	-	10	-	ns	
Data hold time	$t_{DH}$	0		0	-	0	-	0	-	ns	4, 5
Write enable to output in high Z	$t_{WZ}$	-	5	-	6	-	7	-	8	ns	4, 5
Output active from write end	$t_{OW}$	1	-	1	-	1	-	2	-	ns	4, 5

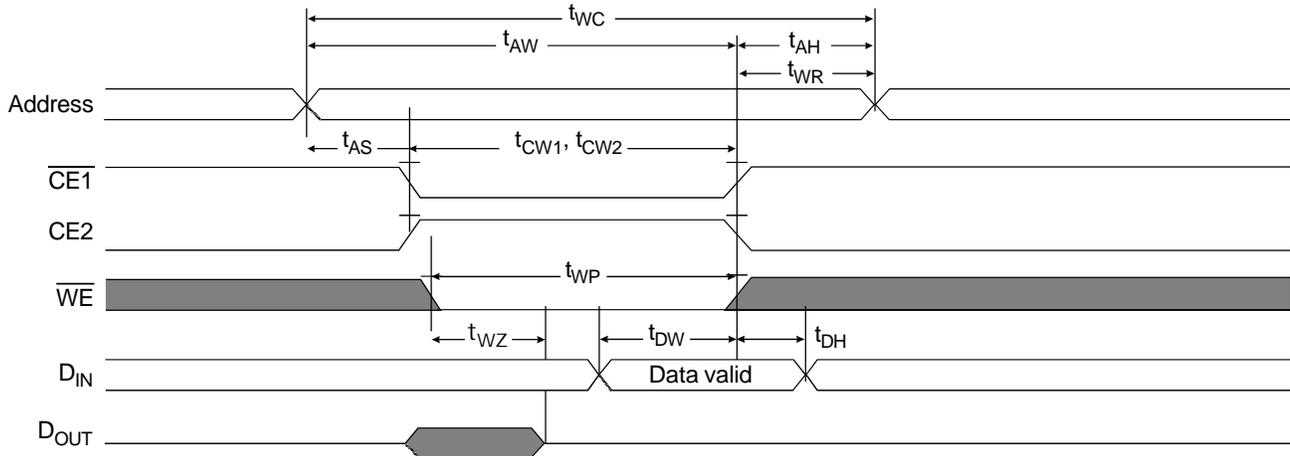
Write waveform 1 ( $\overline{WE}$  controlled)<sup>10,11,12</sup>





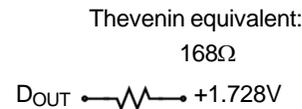
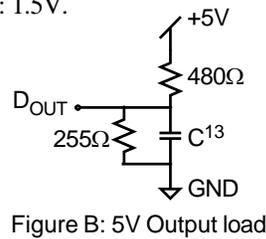
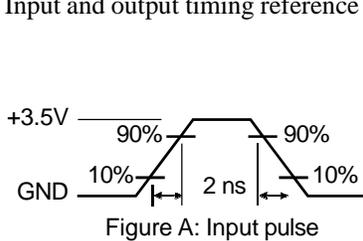
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Write waveform 2 ( $\overline{CE1}$  and CE2 controlled)<sup>10,11,12</sup>



AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.5V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.



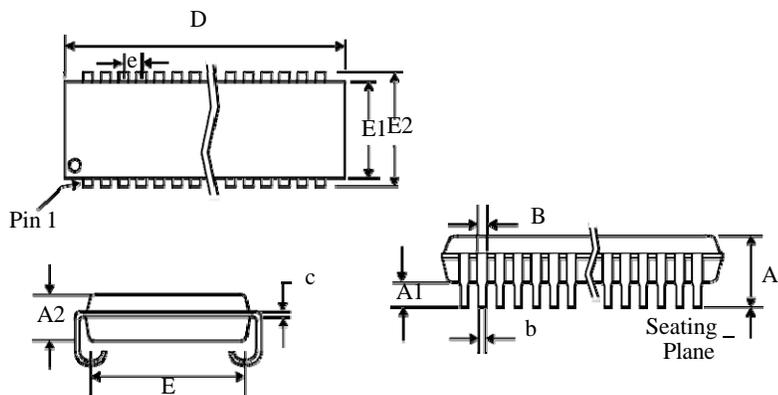
Notes

- 1 During  $V_{CC}$  power-up, a pull-up resistor to  $V_{CC}$  on  $\overline{CE1}$  is required to meet  $I_{SB}$  specification.
- 2 This parameter is sampled and not 100% tested.
- 3 For test conditions, see *AC Test Conditions*, Figures A and B.
- 4  $t_{CLZ}$  and  $t_{CHZ}$  are specified with  $CL = 5pF$ , as in Figure C. Transition is measured  $\pm 500$  mV from steady-state voltage.
- 5 This parameter is guaranteed, but not 100% tested.
- 6  $\overline{WE}$  is high for read cycle.
- 7  $\overline{CE1}$  and  $\overline{OE}$  are low and CE2 is high for read cycle.
- 8 Address valid prior to or coincident with  $\overline{CE1}$  transition Low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 N/A
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 CE1 and CE2 have identical timing.
- 13 C = 30 pF, except all high Z and low Z parameters where C = 5 pF.

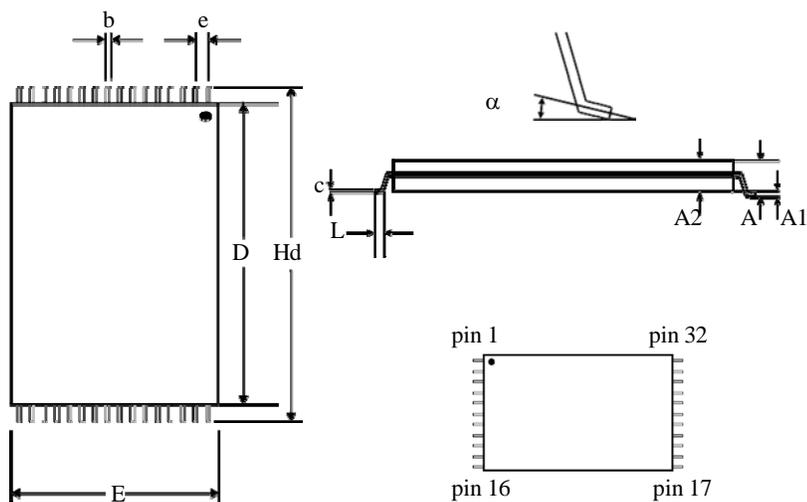


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Package dimensions



	32-pin SOJ 300 mil		32-pin SOJ 400 mil	
	Min	Max	Min	Max
A	0.128	0.145	0.132	0.146
A1	0.025	-	0.025	-
A2	0.095	0.105	0.105	0.115
B	0.026	0.032	0.026	0.032
b	0.016	0.020	0.015	0.020
c	0.007	0.010	0.007	0.013
D	0.820	0.830	0.820	0.830
E	0.255	0.275	0.354	0.378
E1	0.295	0.305	0.395	0.405
E2	0.330	0.340	0.435	0.445
e	0.050 BSC		0.050 BSC	



	32-pin TSOP 8x20 mm	
	Min	Max
A	-	1.20
A1	0.05	0.15
A2	0.95	1.05
b	0.17	0.27
c	0.10	0.21
D	18.30	18.50
e	0.50 nominal	
E	7.90	8.10
Hd	19.80	20.20
L	0.50	0.70
alpha	0°	5°



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**Ordering codes**

**Access times**

Package	Temp	10 ns	12 ns	15 ns	20 ns
Plastic SOJ, 300 mil	Commercial	-	AS7C1024B-12TJCN	AS7C1024B-15TJCN	AS7C1024B-20TJCN
	Industrial	-	AS7C1024B-12TJIN	AS7C1024B-15TJIN	AS7C1024B-20TJIN
Plastic SOJ, 400 mil	Commercial	-	AS7C1024B-12JCN	AS7C1024B-15JCN	AS7C1024B-20JCN
	Industrial	-	AS7C1024B-12JIN	-	-
TSOP1 8x20 mm	Commercial	-	AS7C1024B-12TCN	AS7C1024B-15TCN	AS7C1024B-20TCN
	Industrial	-	-	-	-

**Part numbering system**

AS7C	1024B	-XX	X	X	X	XX
SRAM prefix	Device number 1024: 1Mb (x8) B : revision B	Access time -10 = 10ns -12 = 12ns -15 = 15ns -20 = 20ns	Package: J = SOJ 400 mils T = TSOP1 TJ = SOJ 300mils	Temperature range: C = Commercial I = Industrial	N=Lead Free and Halogen Free Part	Packing Type None: Tray TR: Reel



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