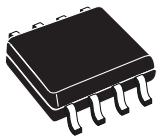
STS5N15F3

N-channel 150 V, 0.045 Ω, 5 A, SO-8 STripFET™ III Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STS5N15F3	150 V	< 0.057 Ω	5 A

- Low on-resistance
- Low input capacitance and gate charge
- Low gate input resistance



SO-8

Application

- Switching applications

Description

This product utilizes the latest advanced design rules of ST's proprietary STripFET™ technology which is suitable for the most demanding DC-DC converter applications where high efficiency is required.

Figure 1. Internal schematic diagram

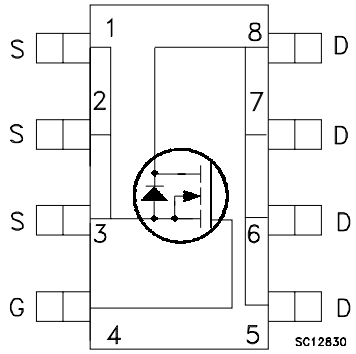


Table 1. Device summary

Order code	Marking	Package	Packaging
STS5N15F3	5R15-	SO-8	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	150	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	5	A
I_D	Drain current (continuous) at T_C=100 °C	3.2	A
I_{DM} (1)	Drain current (pulsed)	20	A
P_{TOT}	Total dissipation at T_C = 25 °C	2.5	W
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Operating junction temperature		

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	50	°C/W

1. When mounted on FR-4 board of 1 inch², 2 oz Cu, t < 10 sec

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2.5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AS}, V_{DD} = 140 V)	300	mJ

2 Electrical characteristics

(T_J = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	150			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 150 V, V_{DS} = 150 V, @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 2.5 A		0.045	0.057	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f = 1 MHz, V_{GS} = 0		1300 140 20.5		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 75 V, I_D = 5 A V_{GS} =10 V *Figure 14 on page 8*		29 3.6 14.6		nC nC nC
R_g	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level=20 mV open drain		3.7		Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}= 75 V, I_D= 2.5 A, R_G=4.7 Ω, V_{GS}=10 V *Figure 13 on page 8*		9 13 46 20		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				5	A
I_{SDM}(1)	Source-drain current (pulsed)				20	A
V_{SD}(2)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5 A, di/dt = 100 A/µs, V_R = 40 V, T_J = 150 °C *Figure 15 on page 8*		110 498 9.1		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

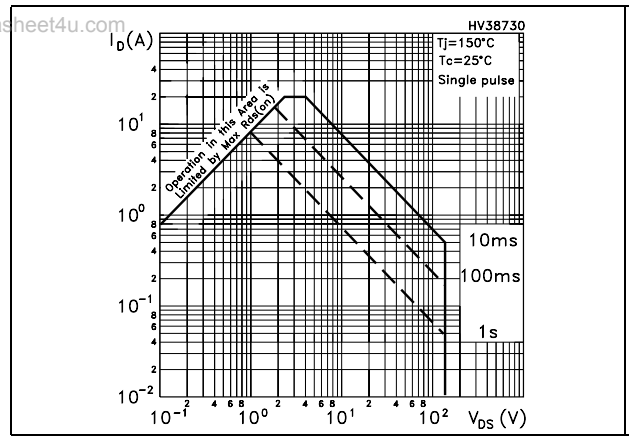


Figure 3. Thermal impedance

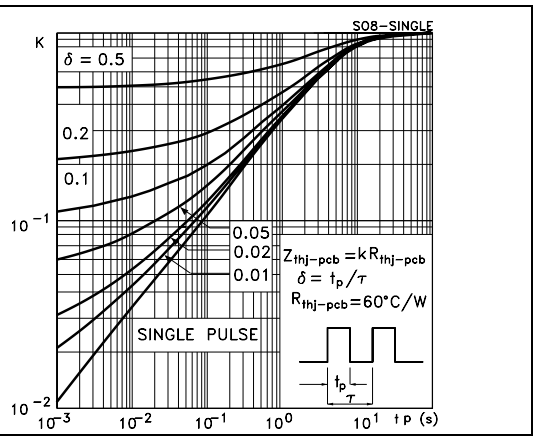


Figure 4. Output characteristics

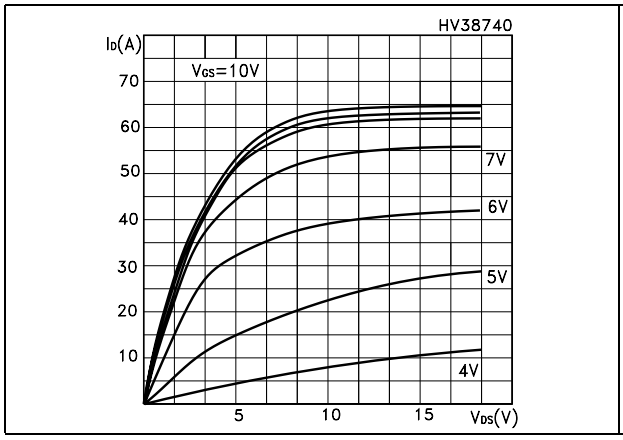


Figure 5. Transfer characteristics

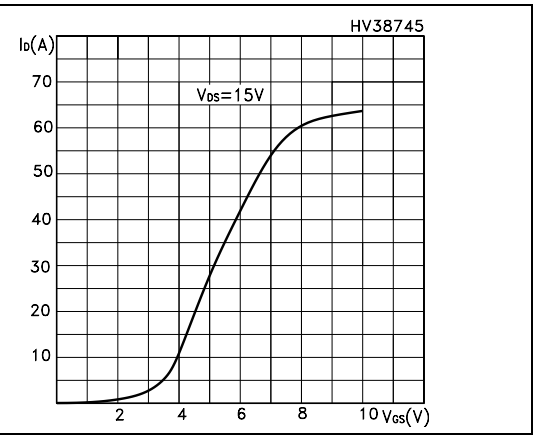


Figure 6. Normalized BV_{DSS} vs temperature

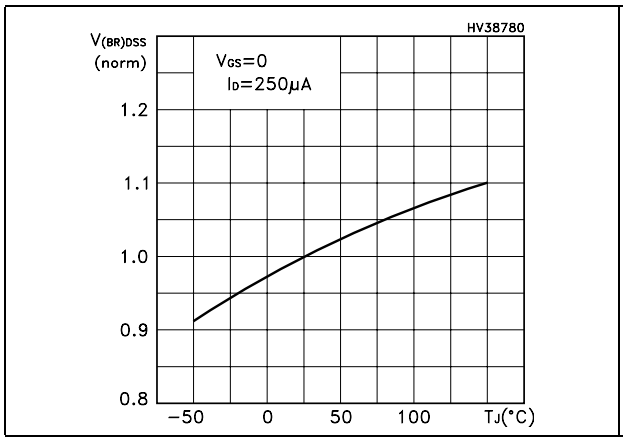


Figure 7. Static drain-source on resistance

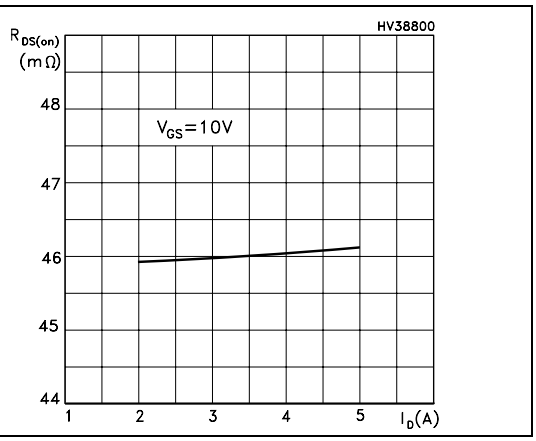


Figure 8. Capacitance variations

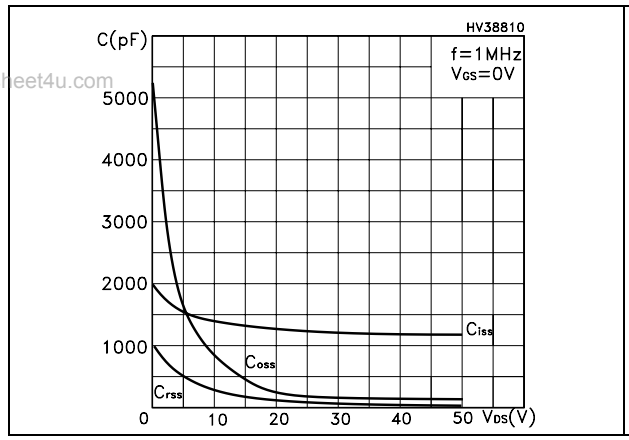


Figure 9. Gate charge vs gate-source voltage

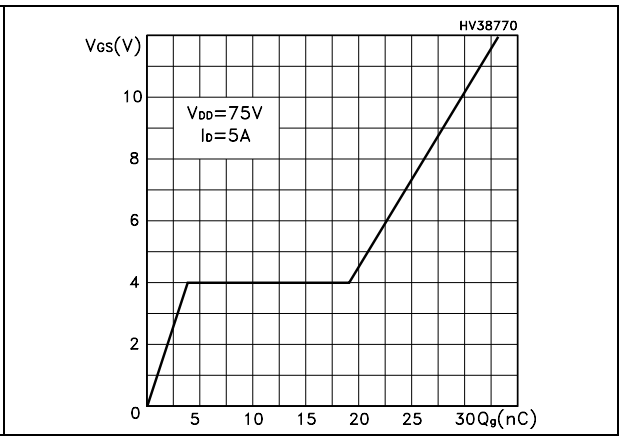


Figure 10. Normalized gate threshold voltage vs temperature

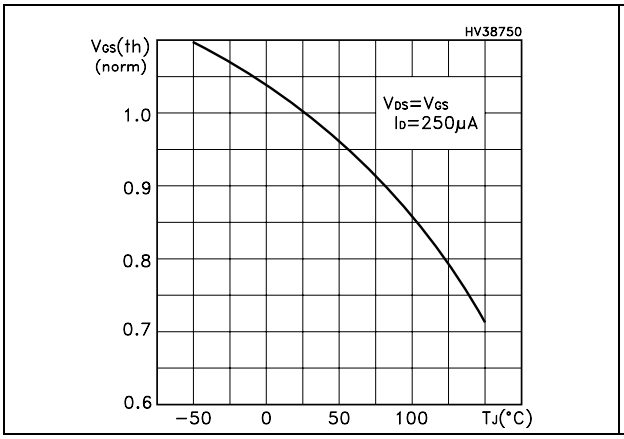


Figure 11. Normalized on resistance vs temperature

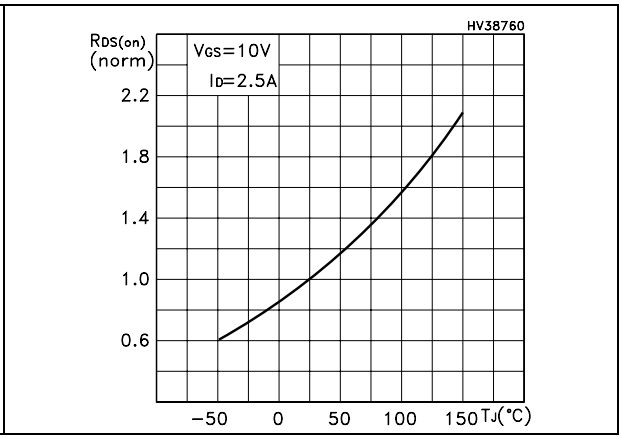
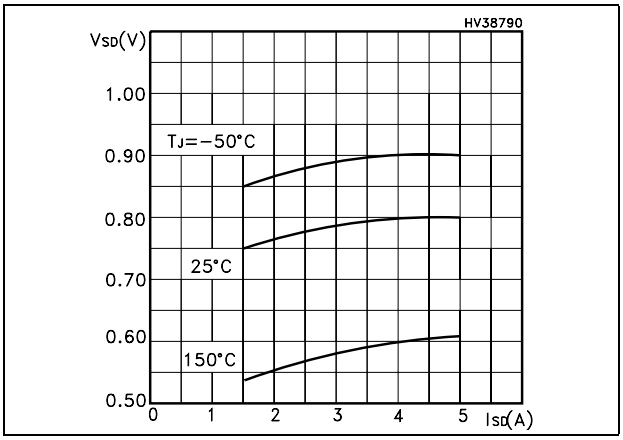


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Switching times test circuit for resistive load

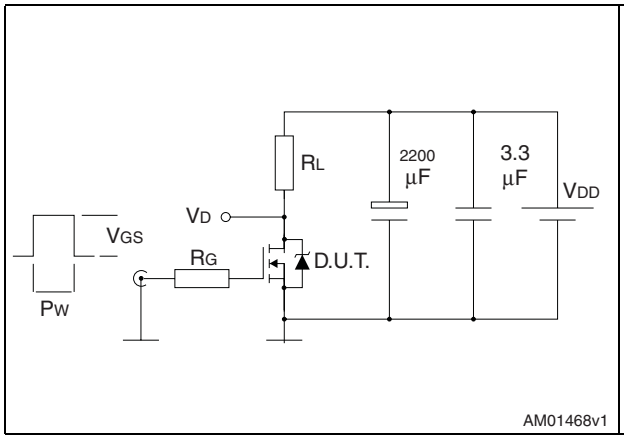


Figure 14. Gate charge test circuit

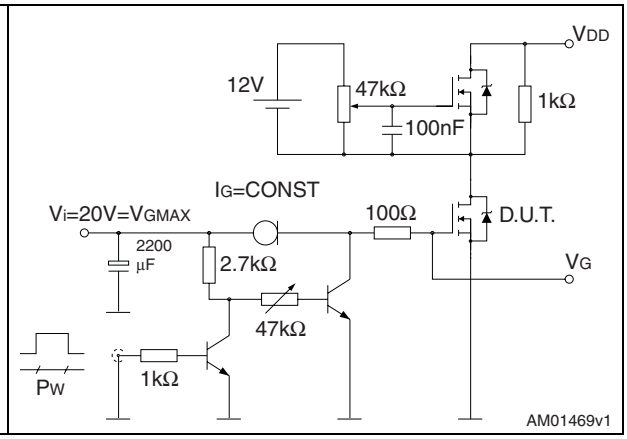


Figure 15. Test circuit for inductive load switching and diode recovery times

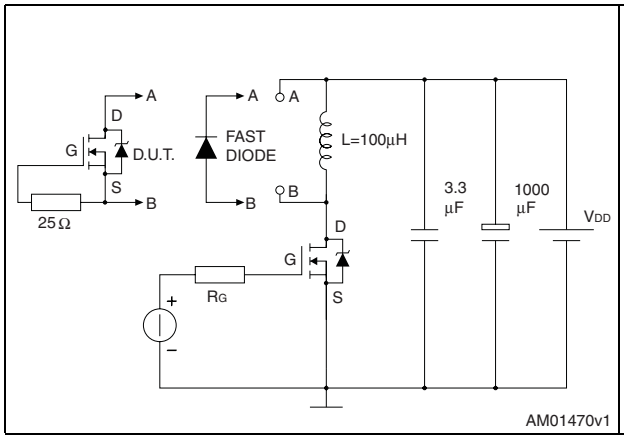


Figure 16. Unclamped inductive load test circuit

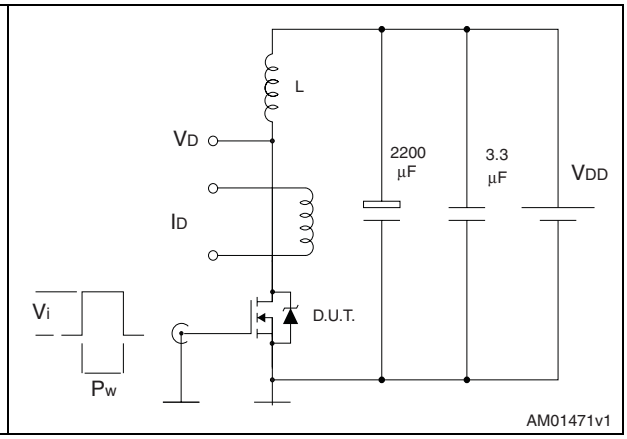


Figure 17. Unclamped inductive waveform

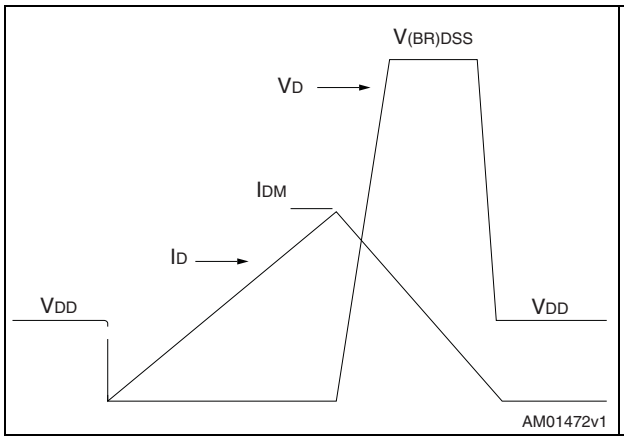
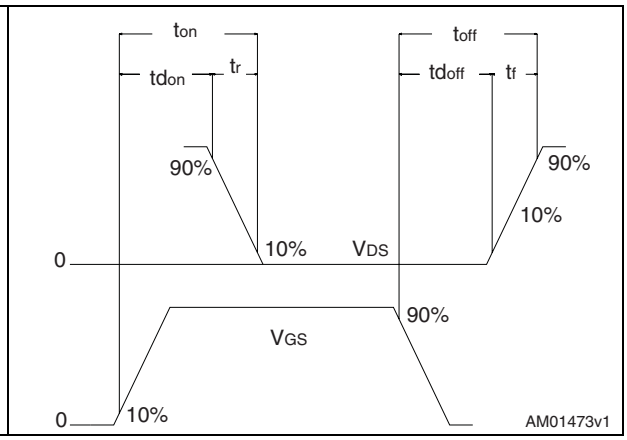


Figure 18. Switching time waveform

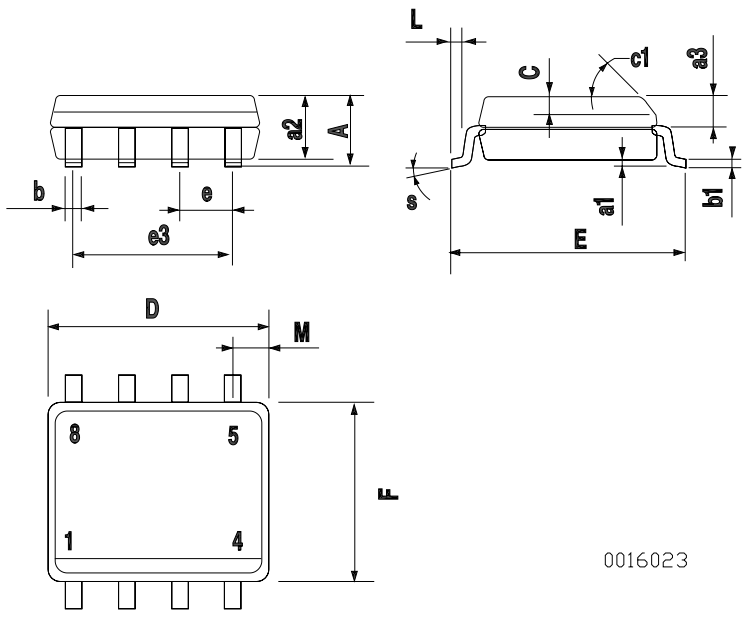


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Mar-2009	1	First release

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